



The Silicon Micro-strip Upstream Tracker for the LHCb Upgrade



Carlos Abellan on behalf of the UT collaboration

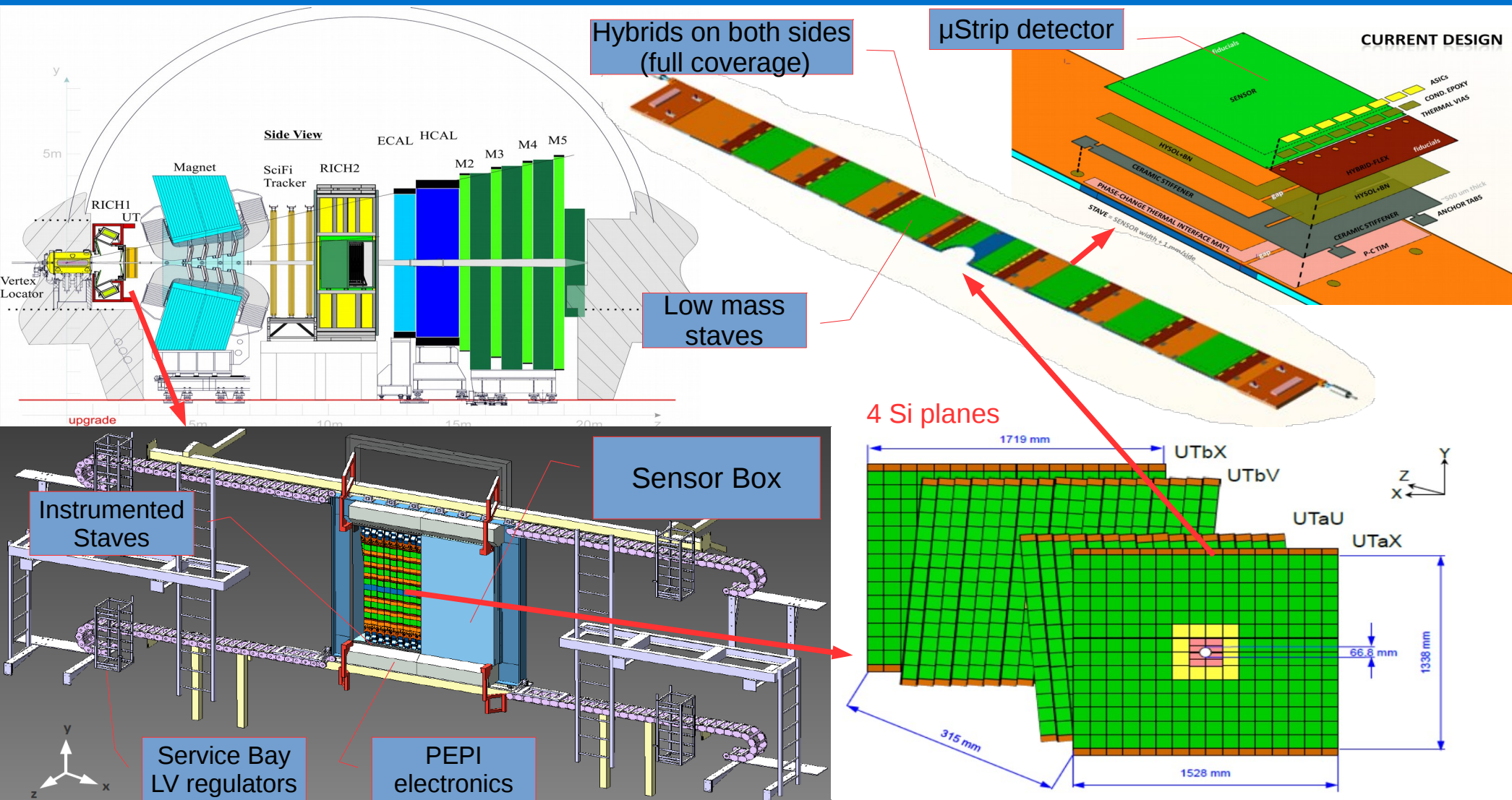


Beijing, 23th May 2017

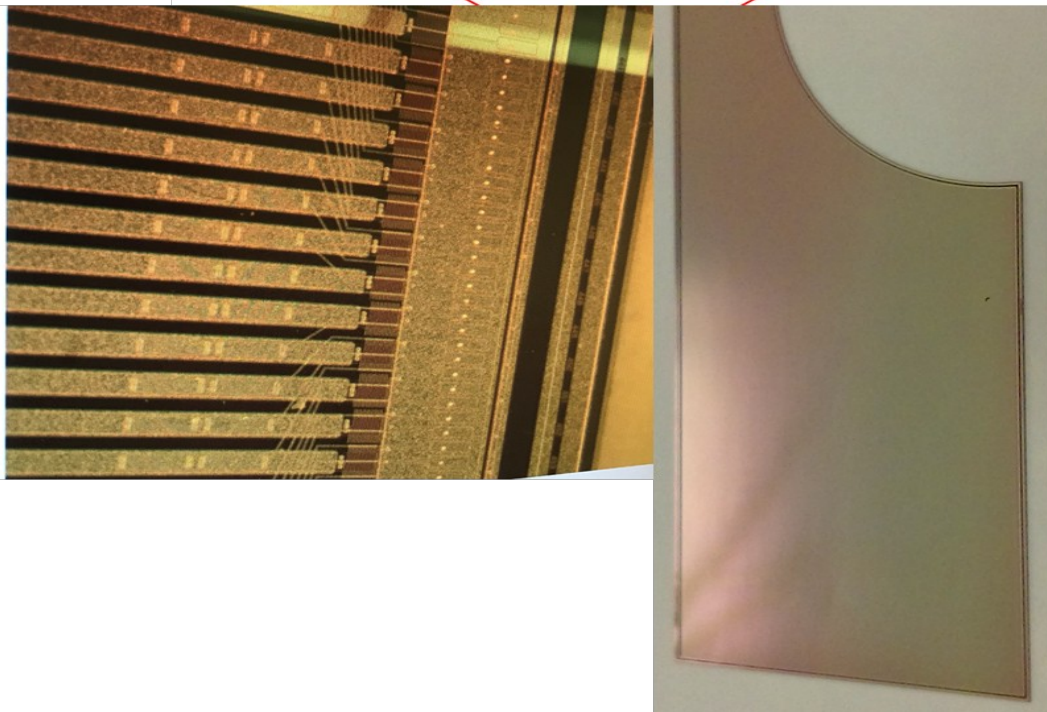
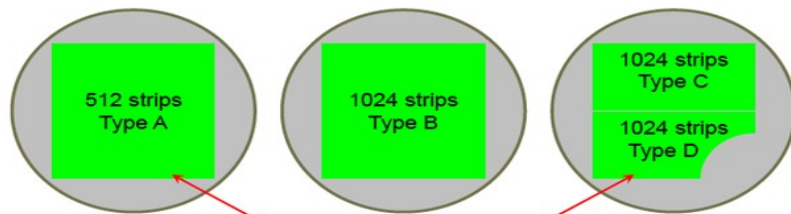


- The UT detector
- SALT ASIC
- Flex cables
- Infrastructure
- Conclusions

The UT detector



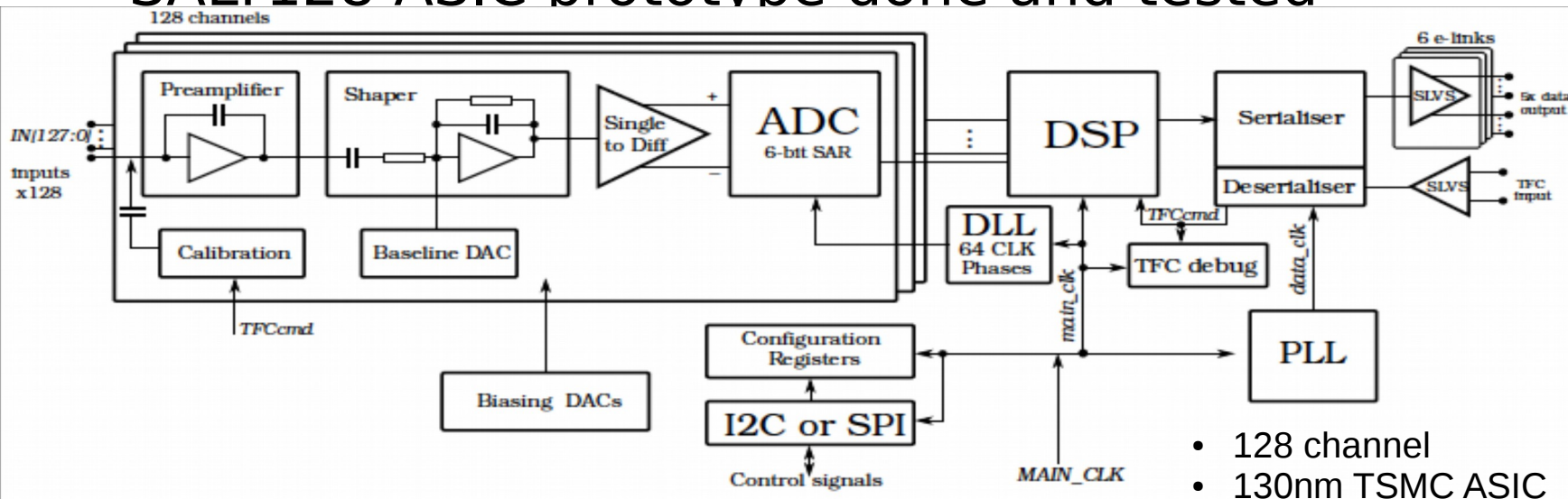
• Silicon Sensors



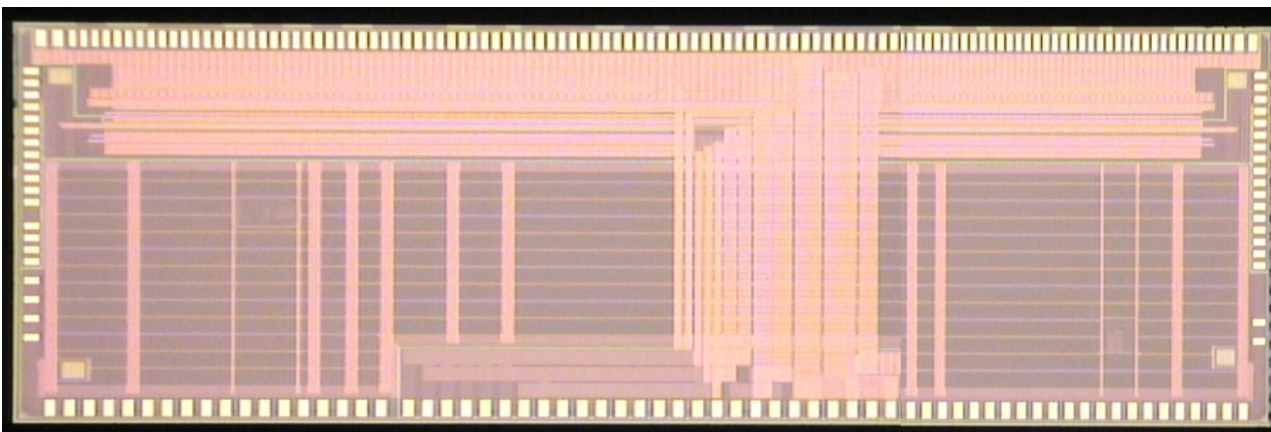
Key technical aspects:

- D type sensors:
 - Circular cut-out to maximize acceptance next to beam pipe
- A type sensors:
 - Built-in pitch adapters (190um to 80um)
- Top-side biasing via wire bonds rather than conductive glue to backplane

- SALT128 ASIC prototype done and tested

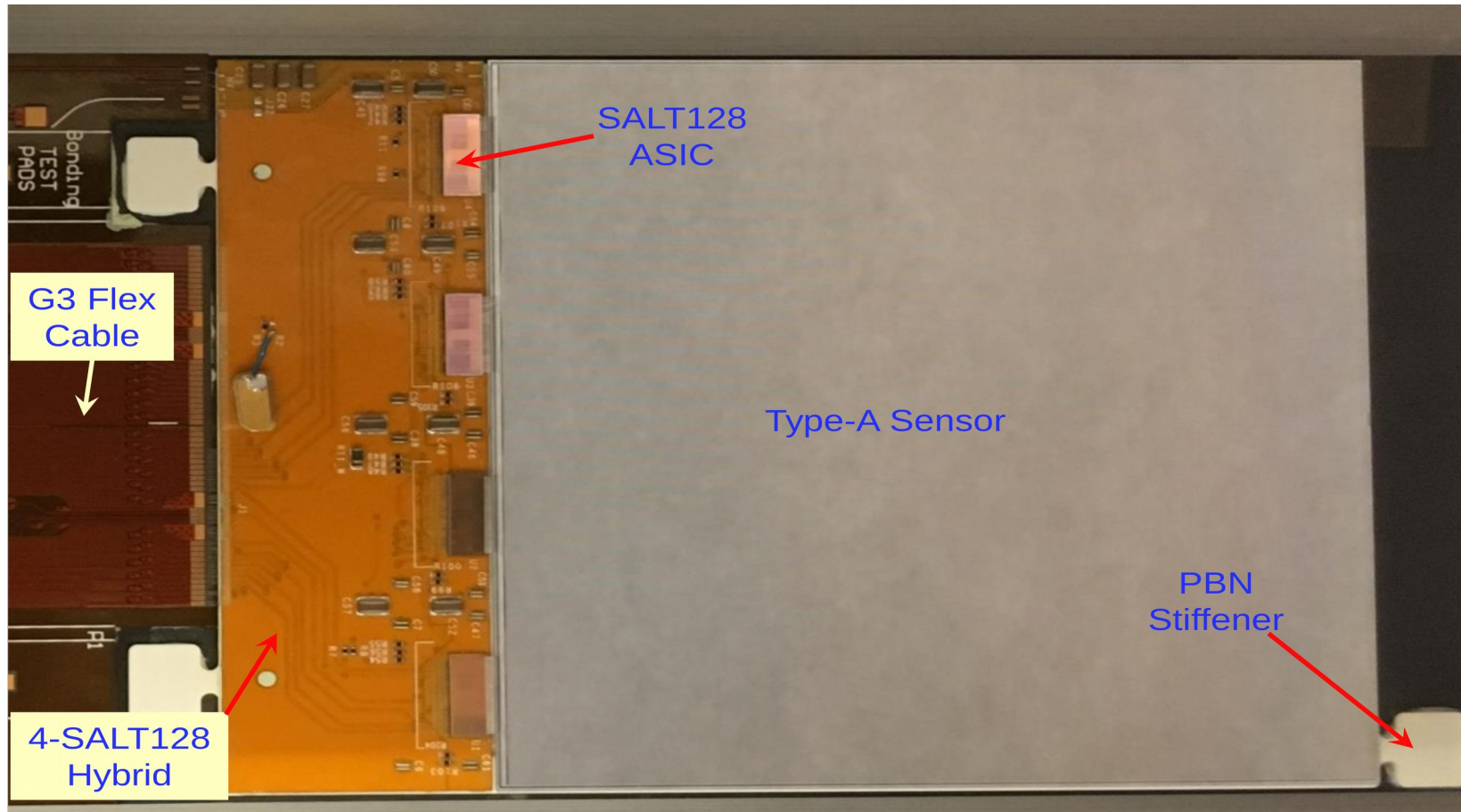


- 128 channel
- 130nm TSMC ASIC
- Fast shaping time/return to baseline
- 6 bit embedded ADC
- DSP:
 - Pedestal subtraction
 - Zero suppression
 - e-link data forming
- On-chip memory
- SLVS e-links (up to 6, typically 3 active)

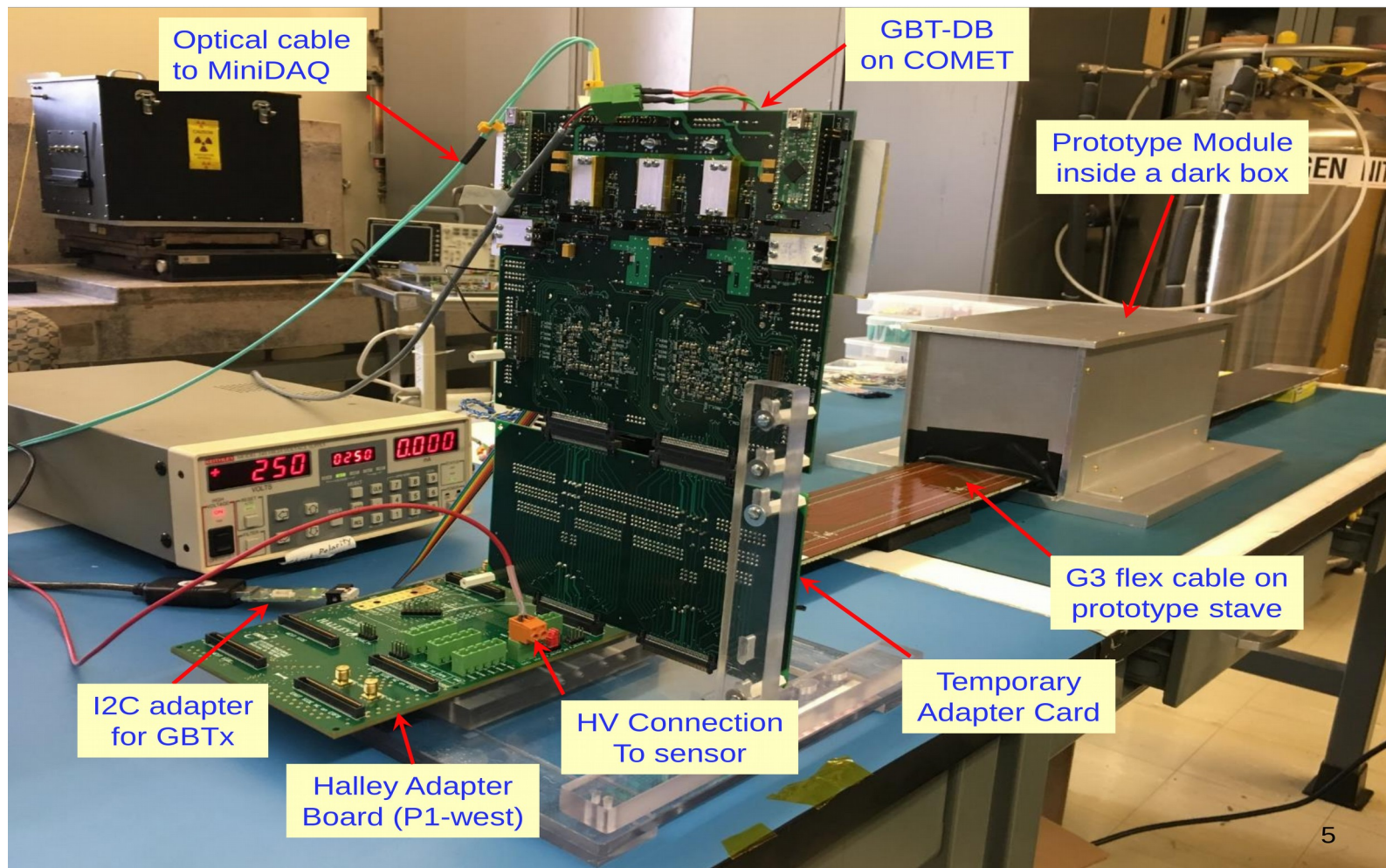


The first UT Module

- First Hybrid produced with current prototype version
- This allows us to make a slice test

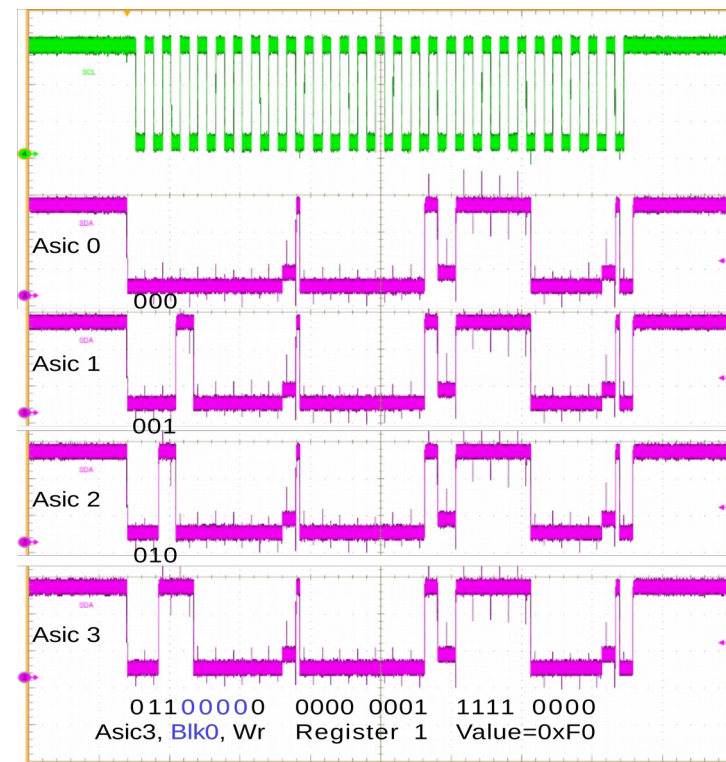
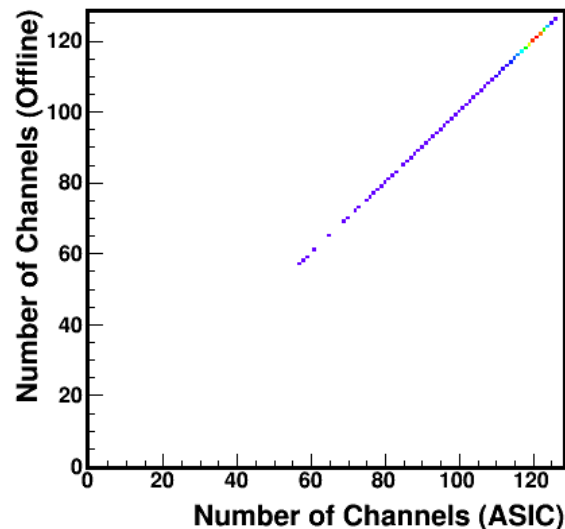
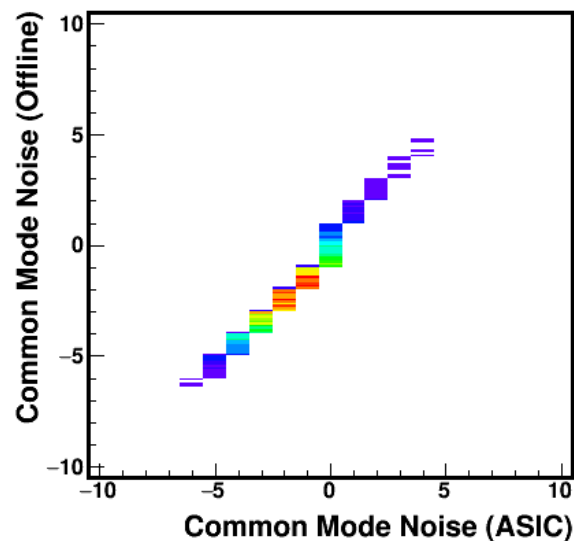


- Slice test



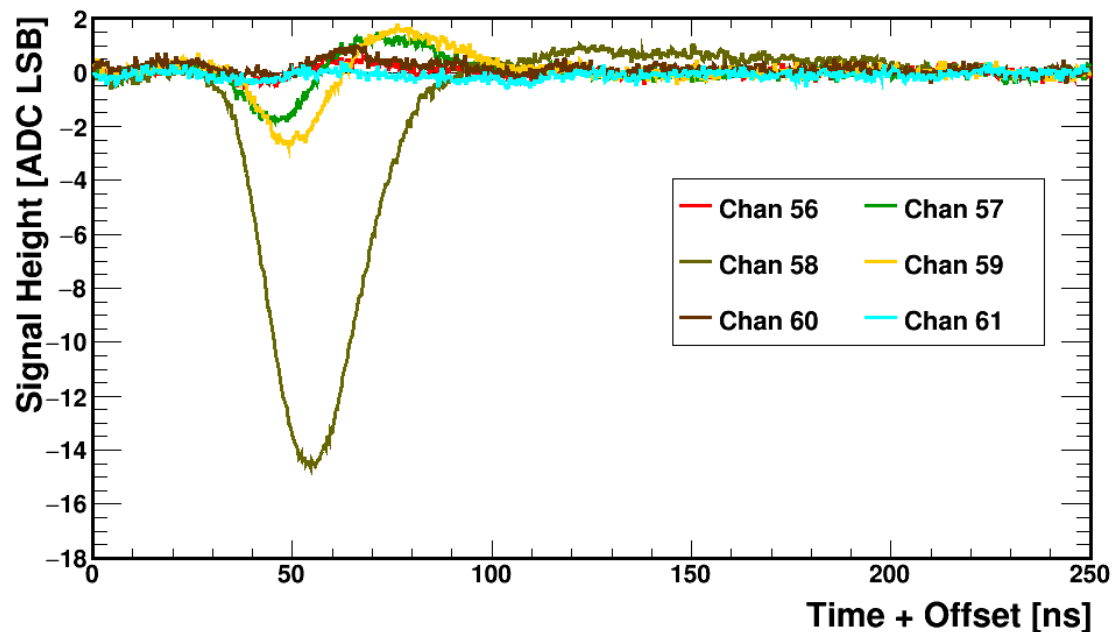
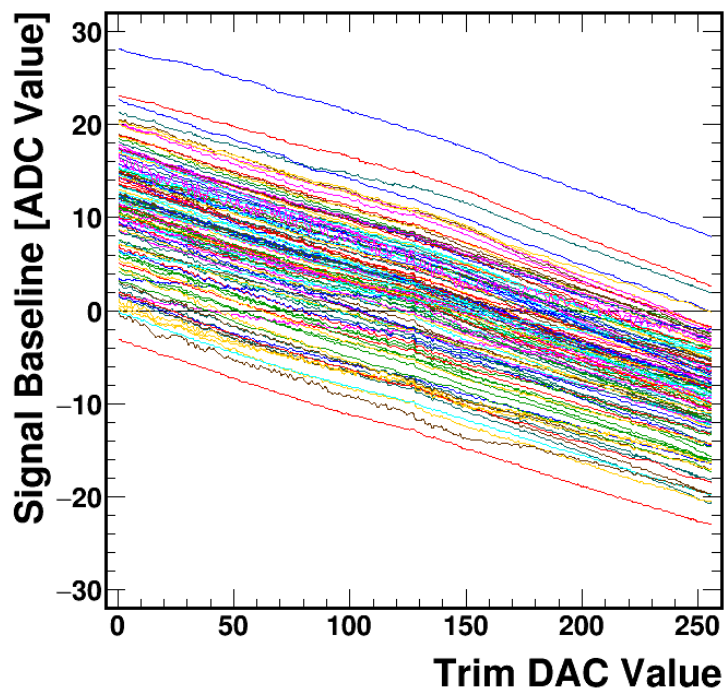
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- Digital functions mostly tested to work as intended (PLL, DLL, I2C, ser, TFC, data packaging,...)
- Pedestal and CM subtraction work exactly as offline simulated
- A new prototype is being designed:
 - Small issue with the ADC sync. with the readout
 - Improvement: saturating logic for computations

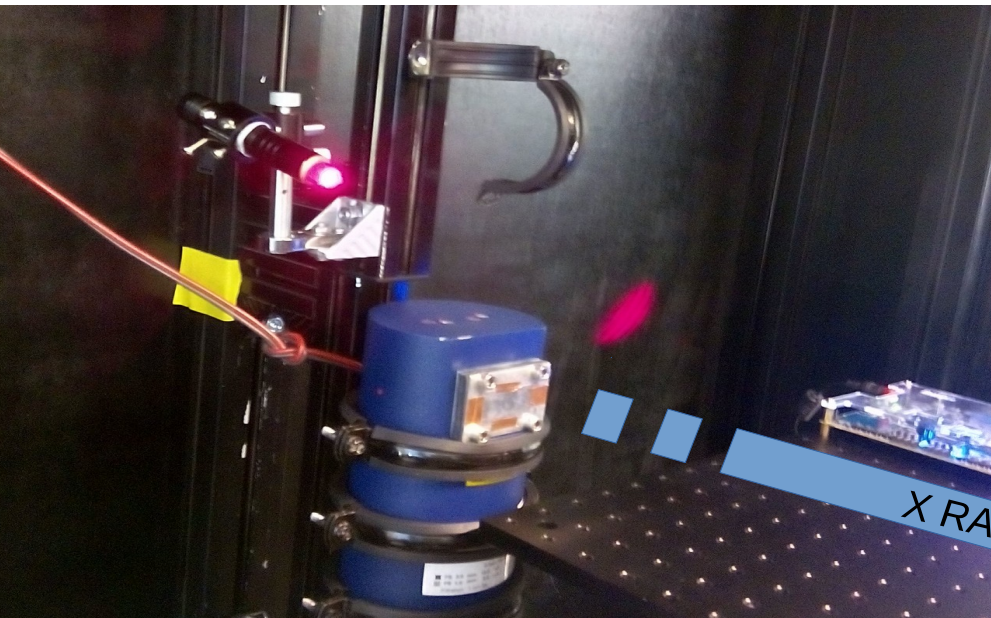


• Analog results

- Version 1 SALT128 works generally as designed. A calibration DAC can be used to align the baseline of all channels. In a test with a laser beam the pulse shapes are as expected in the channel that receives signal and its adjacent channels. Note the fast baseline return with our novel shaper stage.
- However, there are issues in this version that will be fixed in a newer prototype.



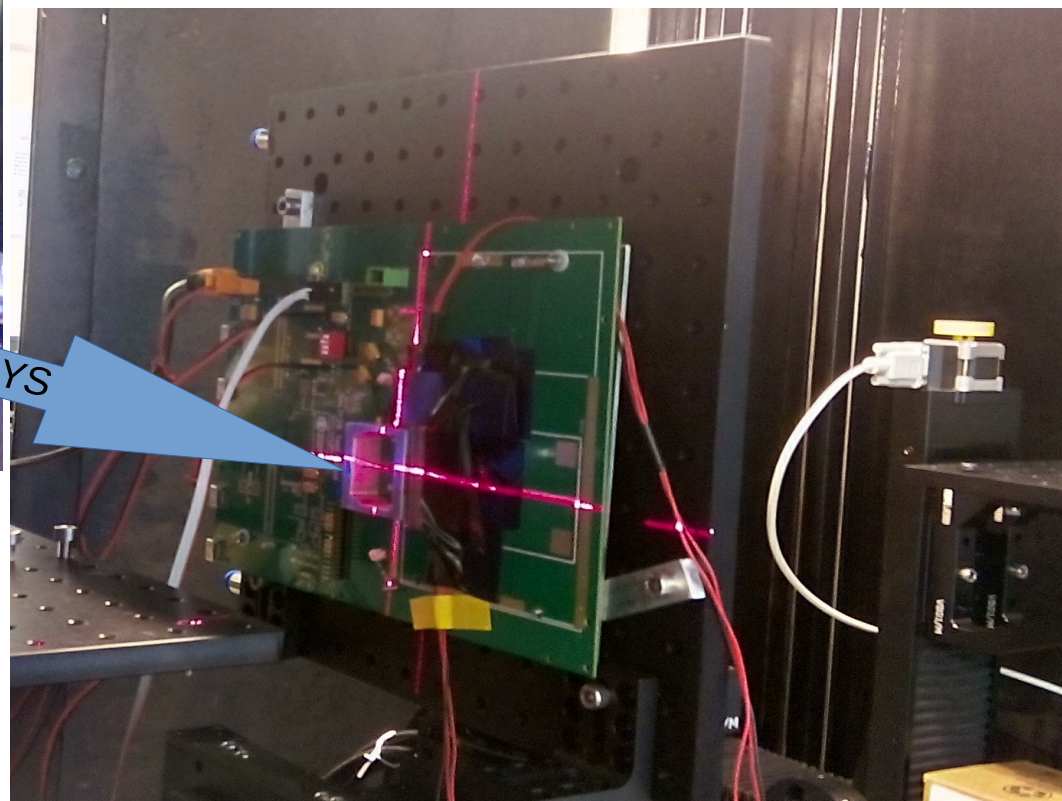
- TID test also performed to see current consumption variation



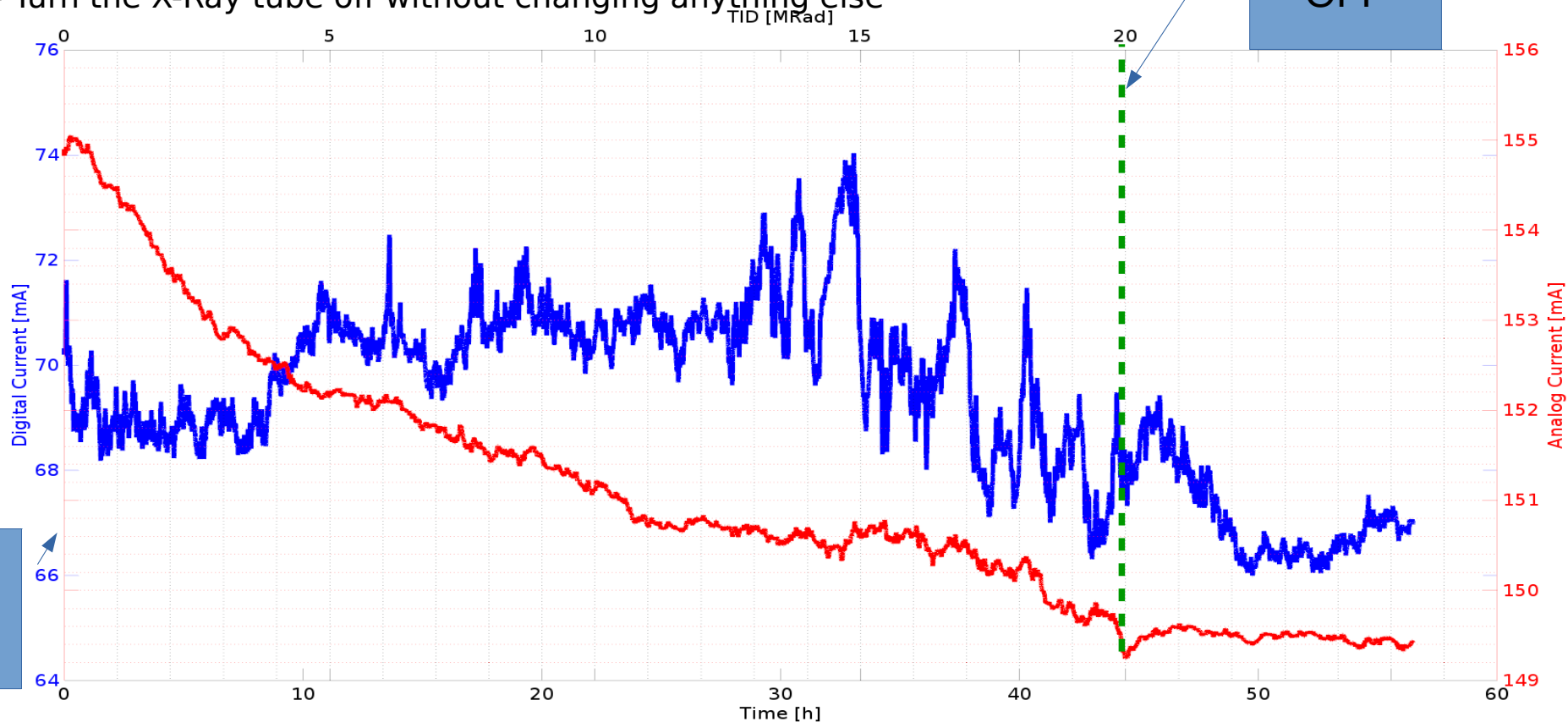
X-Rays
Tested up to 20Mrad

Rate: 0.45Mrad/h
Annealing monitor: 12h

Thanks to Glasgow colleagues for their help!



- 0.- Warm up for 12h
- 1.- Turn the X-Ray tube on without changing anything else
- 2.- Wait 44.4h (0.45Mrad/h → 20Mrad total)
- 3.- Turn the X-Ray tube off without changing anything else

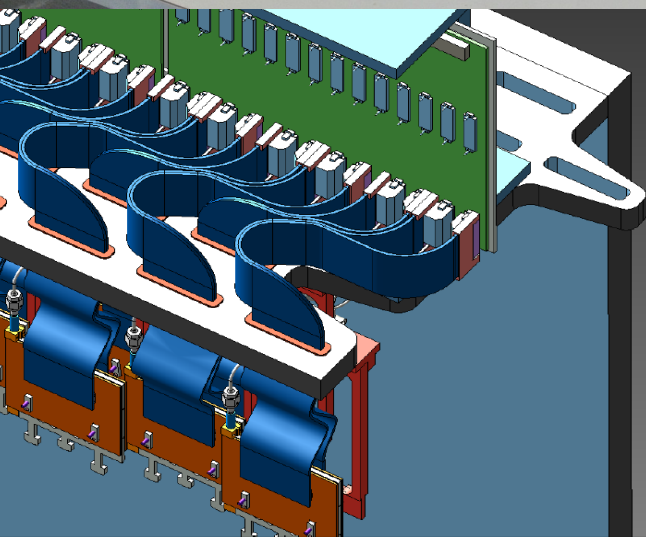
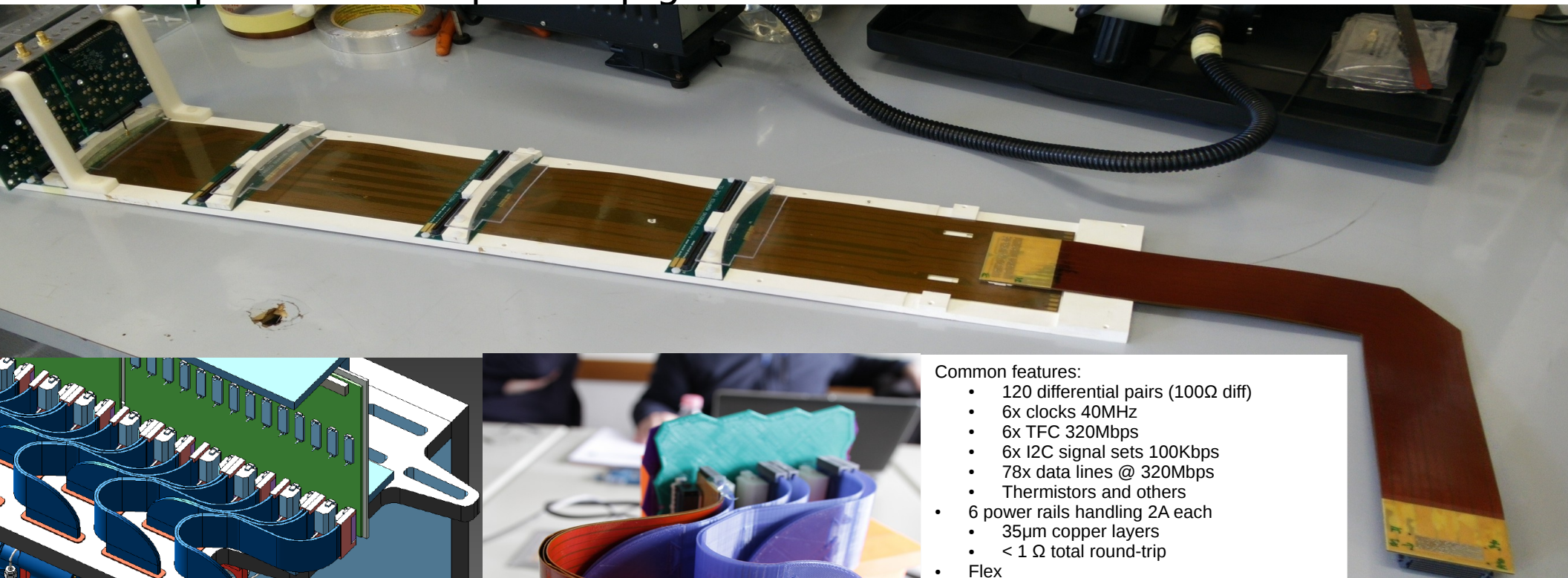


X Rays
ON

X Rays
OFF

The flex cables

- Two pieces: flex tape and pigtails

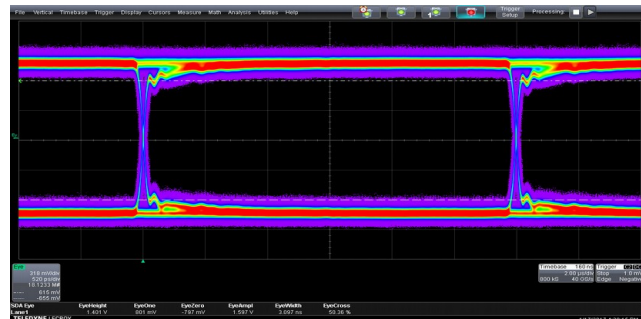


Common features:

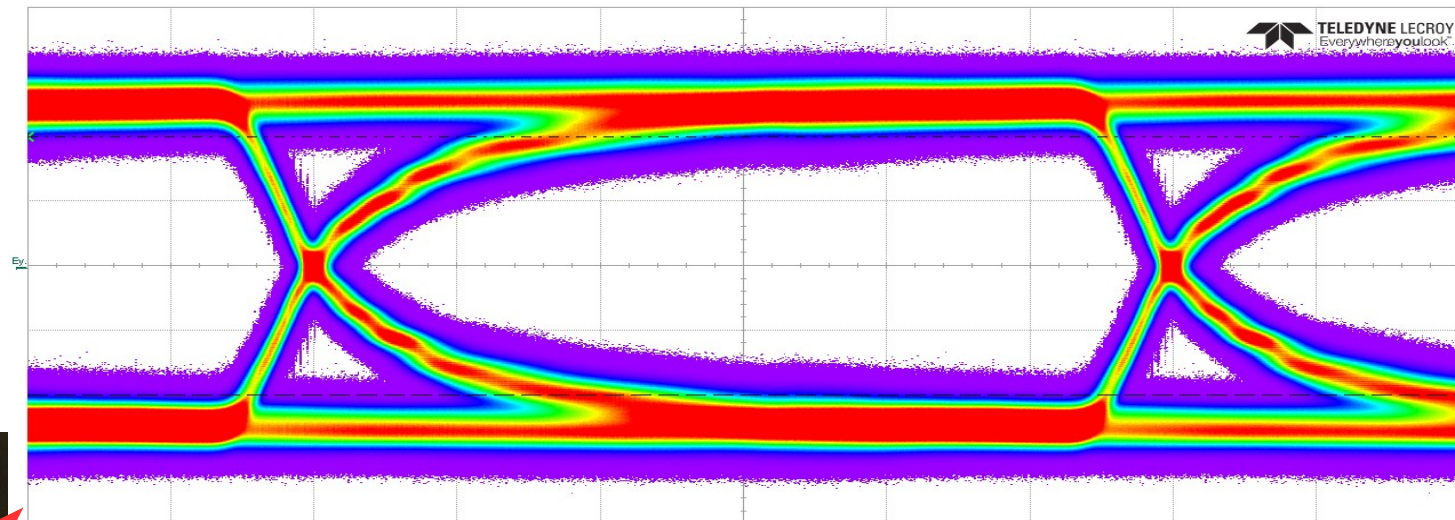
- 120 differential pairs (100Ω diff)
- 6x clocks 40MHz
- 6x TFC 320Mbps
- 6x I2C signal sets 100Kbps
- 78x data lines @ 320Mbps
- Thermistors and others
- 6 power rails handling 2A each
 - 35μm copper layers
 - < 1 Ω total round-trip
- Flex
 - 4 High voltage power lanes
 - Sensor biasing <500V
 - Minimal material budget
 - 80 cm total length
- Pigtail
 - Narrower by almost 50%
 - 23 mm bending radius
 - 55 cm total length

The flex cables

- Tested as a single piece



320Mbps PRBS Generator



Eye
267 mV/div
520 ps/div
21.3899 M#
543 mV
521 mV

SDA Eye
Lane1
SDA Jitter
Lane1

EyeHeight
926 mV
Tj(1e-12)

EyeOne
663 mV
Rj(sp)

EyeZero
-633 mV
Dj(sp)

EyeAmpl
1.296 V

EyeWidth
2.932 ns

EyeCross
49.60 %

EyeBER
44.7538182e-27

Timebase 800 ns
10.0 ps/div
2.00 MS
Trigger Stop
Edge Positiv



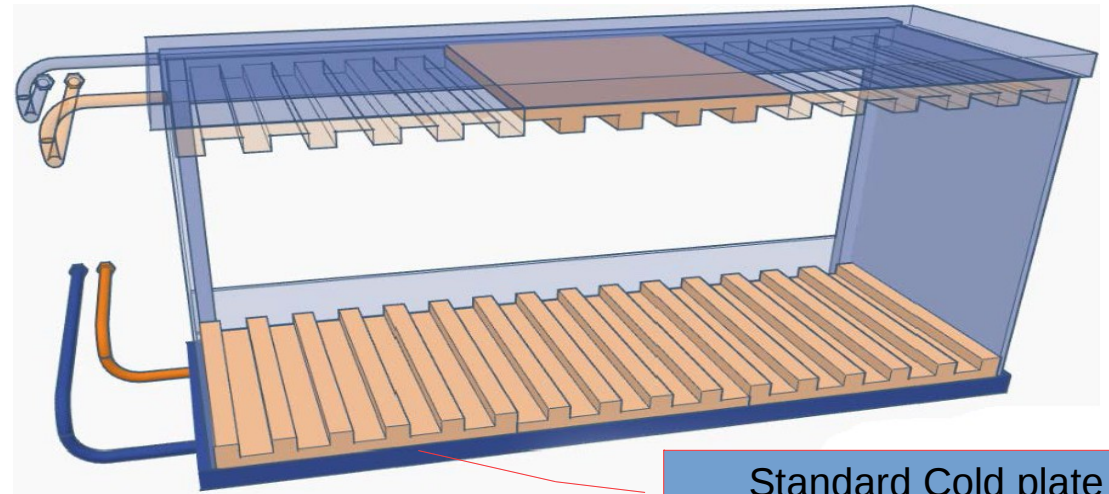
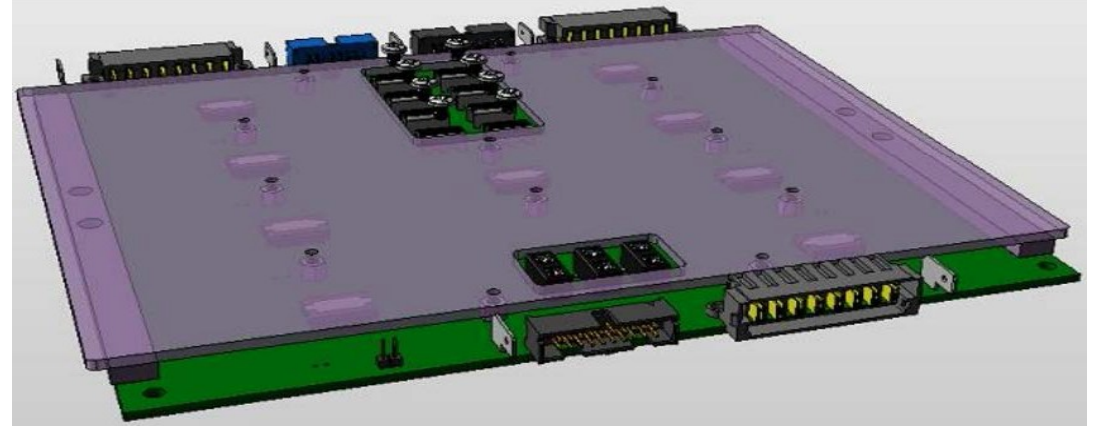
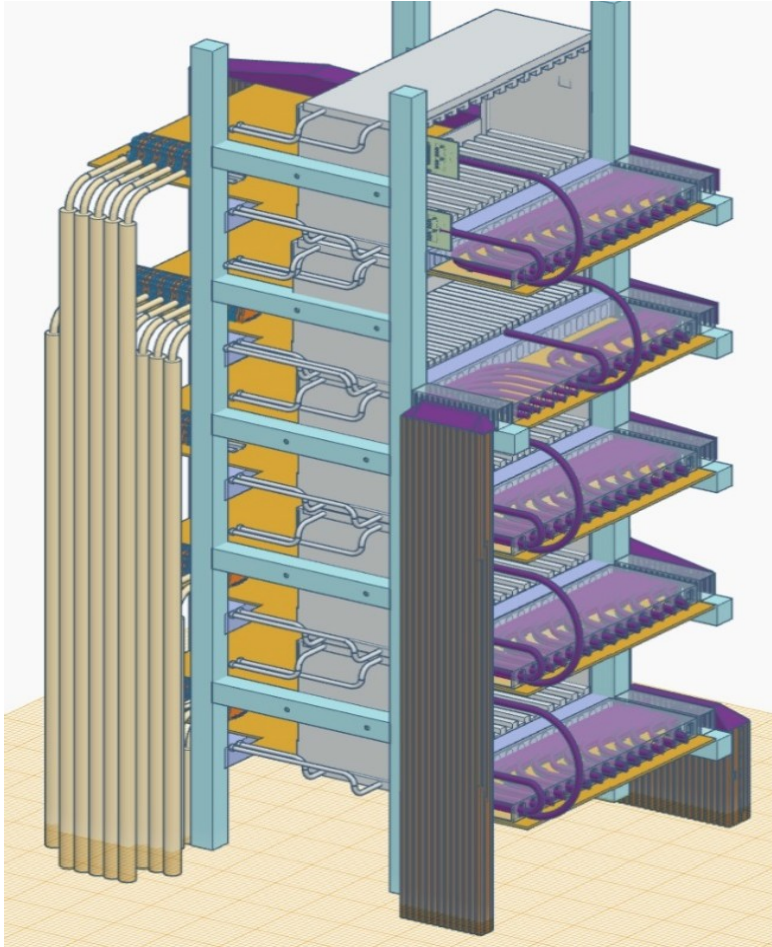
Signal DC resistance:

Measured: 22 Ω roundtrip

Target: 10 Ω roundtrip

Over-etching!
We get signal attenuation...

- Low voltage power regulation
 - Cable management very relevant! 490x 25mm diameter cables



Standard Cold plate

- SALT ASIC:
 - The digital communication works even when using the flex cable. Single ended I2C works even with common mode.
 - Digital performance has minor synchronization issues. Analog performance needs some improvements
 - We see no crosstalk between ASICs even when using a flex cable
 - The ASIC reacts well to the total ionization dose: there is around 3% power consumption variation only
 - A new version of the ASIC is ongoing. It should solve the issues we measured.
- Flex Cables
 - Prototypes are produced and perform well
 - Digital transmission lines have some more resistance than planned. Slice tests prove we can live with it. We are trying to improve it anyway.
 - Now facing production and testing procedures: discussion about pricing, manufacturability improvement , test procedure, etc...
- Infrastructure
 - The design of the low voltage infrastructure is quite advanced
 - We need to see how to manage all the cables we have: they have a big cross section that we have to see how to input to the PEPI area
 - We plan to produce some prototypes to have real tests
 - Summarizing: the project progresses in all aspects. The ASIC requires some extra refinements in its performance, but our team is working on it.