Contribution ID: **151** Type: **oral**

The Silicon Micro-strip Upstream Tracker for the LHCb Upgrade

Tuesday, May 23, 2017 12:12 PM (18 minutes)

A comprehensive upgrade of the LHCb detector is foreseen for the long shutdown of the LHC in 2019/20 (LSII). The upgrade has two main goals: enabling the experiment to operate at an up to five times higher instantaneous luminosity and increasing trigger efficiencies by substituting the current hardware trigger by a software one. As part of the upgrade, the existing TT tracking station in front of the LHCb dipole magnet will be replaced by a new silicon micro-strip detector, the Upstream Tracker (UT).

Similar to the TT, the UT will consist of four planar detection layers covering the full acceptance of the experiment. In total, the detector will use about 1000 silicon sensors and 5000 ASICs.

Sensor R&D concentrates on three advanced features that are being considered: a quadrantile cut-out for the innermost sensors to optimize the detector coverage around the LHC beam pipe, an embedded pitch adapter implemented as a double metal layer, and strip-side contacts for connecting the bias voltage through the silicon bulk to the backplane.

A new radiation-hard front end readout chip for the UT is being developed in 130 nm TSCM technology. It incorporates 128 input channels with the complete DAQ chain integrated: preamplifier, shaper and a 6-bit ADC, pedestal and common-mode subtraction, and zero-suppression as well as data serialization.

Measurements on a full-featured prototype chip are well advanced and results from these tests will be shown.

Detector modules host 4 or 8 ASICs and are mounted onto the front and back of 130 cm long staves that cover the full height of the detector acceptance. The staves consist of light-weight foam embedded between two sheets of carbon fibre. The cooling of the silicon sensors and the front-end chips is done via embedded titanium cooling pipes, through which innovative bi-phase C02 is circulated as coolant. The progress of this system will also be discussed.

Output signals and control signals, low-voltage power for the front-end chips and bias voltage for the silicon sensors are transported along the staves via kapton flex cables that are glued onto both at sides of the stave. Each of these cables carry up to 120 high speed differential pairs with a total of 38.4Gbps and 8A of current to power up to 24 ASICs while maintaining a minimal material budget and being easy to manufacture. The design solutions and results of prototype iterations will be presented.

The detector design presents several practical challenges. These include a retractable detector frame, a light-weight detector box that will seal directly around the LHC beam pipe, and custom-made electronics for signal processing and detector control that are mounted against the detector frame as well as practical implementation issues. These will be discussed too.

Primary author: ABELLAN, Carlos (U)

Co-author: Dr SCHMIDT, Burkhard (CERN)

Presenter: ABELLAN, Carlos (U)

Session Classification: R4-Semiconductor detectors(2)

Track Classification: Semiconductor detectors