The Intelligent FPGA Data Acquisition

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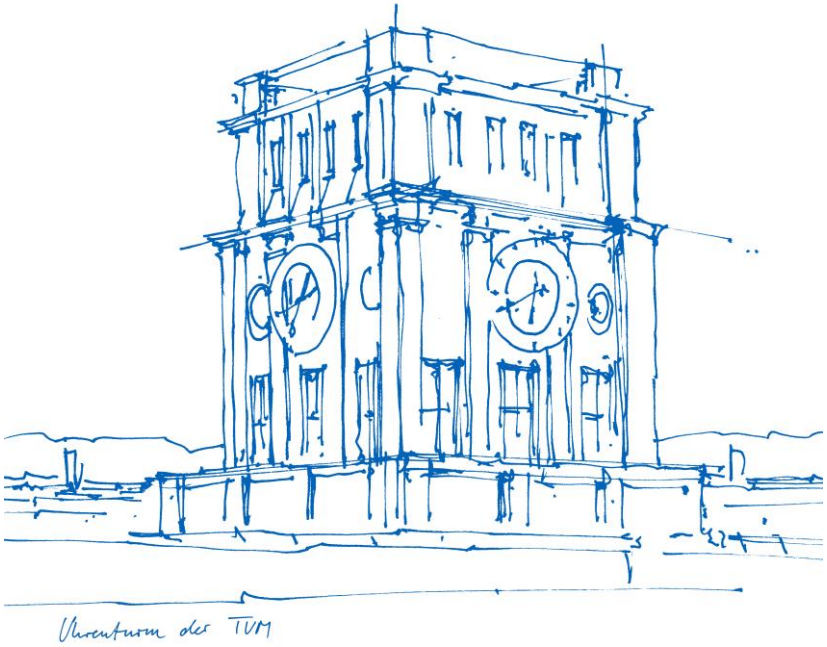
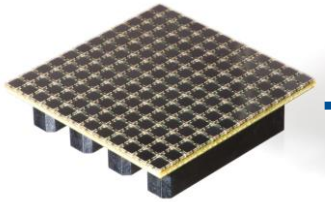


Cooking recipe for a modern data acquisition system



1. Detector/Sensor

2. Front-End

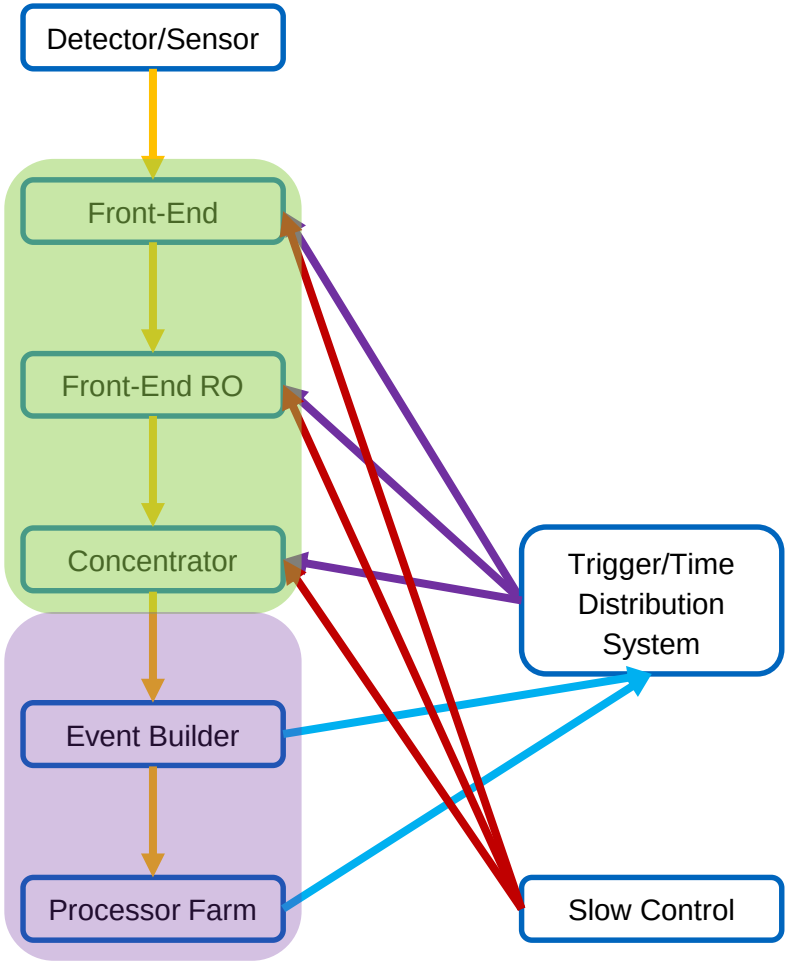
3. Front-End read-out

4. Data concentrator

5. Event builder

6. PC processing

Cooking recipe for a modern data acquisition system – status quo

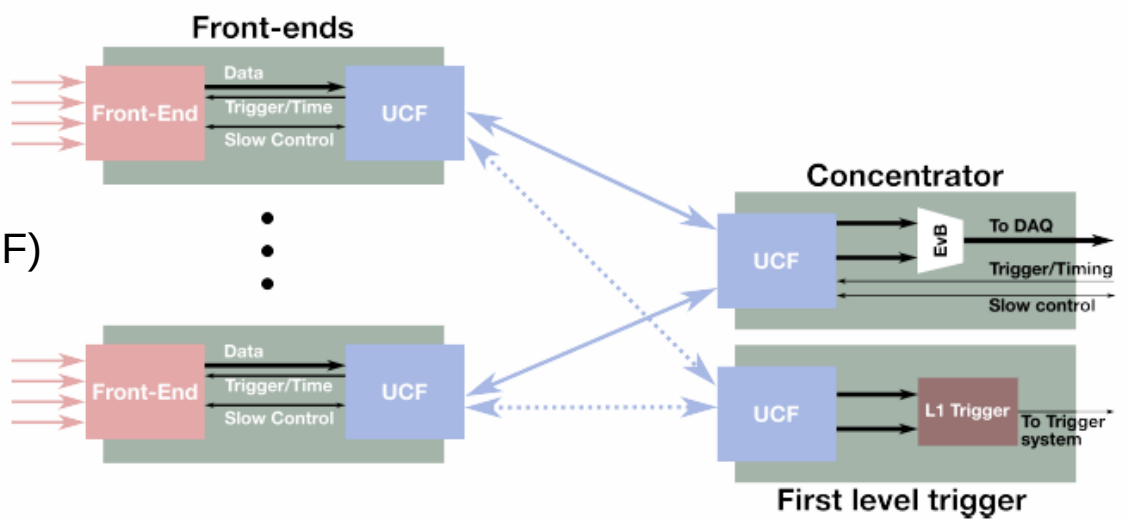


- Separate links for trigger, data and slow control communication
- Event builder implemented on CPUs
- Different communication interfaces between the different modules
- This kind of structure is used in many experiments like COMPASS, ATLAS or CMS

→ Why unify communication channels?
→ Why not using generic hardware?
→ Why not taking advantage of FPGAs on more stages than Front-End read-out, Front-End and concentrator?

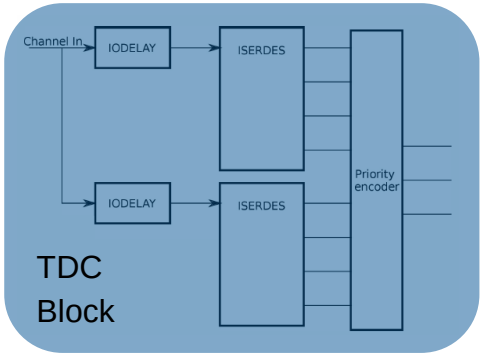
Intelligent FPGA Data Acquisition (IFDAQ)

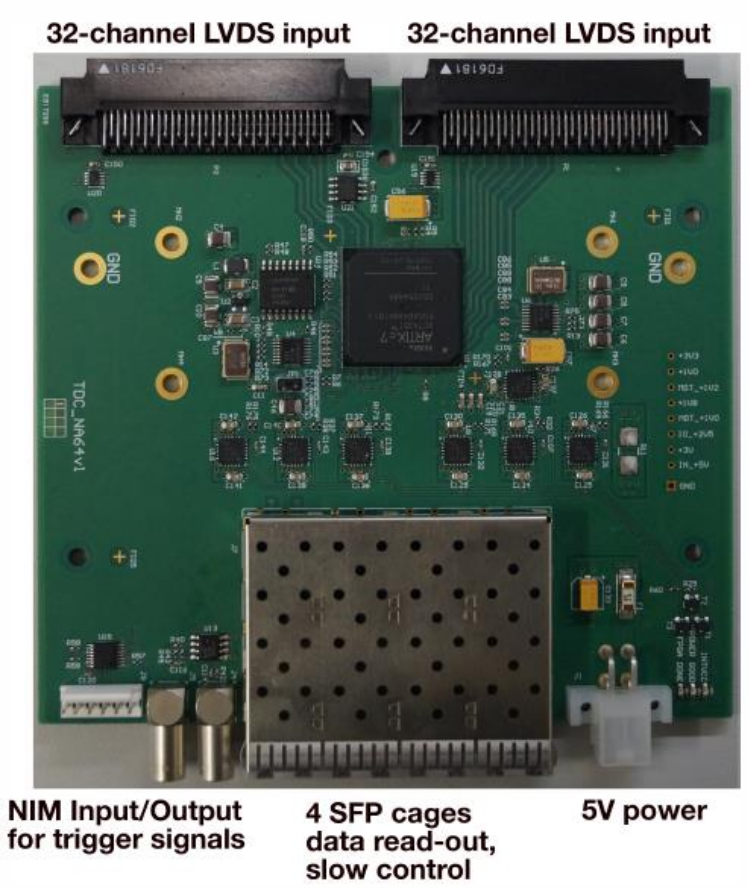
- Three generic modules:
  - Front-End
  - Data Concentrator
  - Trigger Distribution
- Front-End can communicate to an external ADC or can be used as a TDC system
- Front-Ends can be either used to digitize data or receive already digitized data
- All internal and optionally all external communication is handled by the unified communication framework (UCF)
- Error tolerant
- Self-recoverable



IFDAQ – Time-to-Digital Converter (TDC)

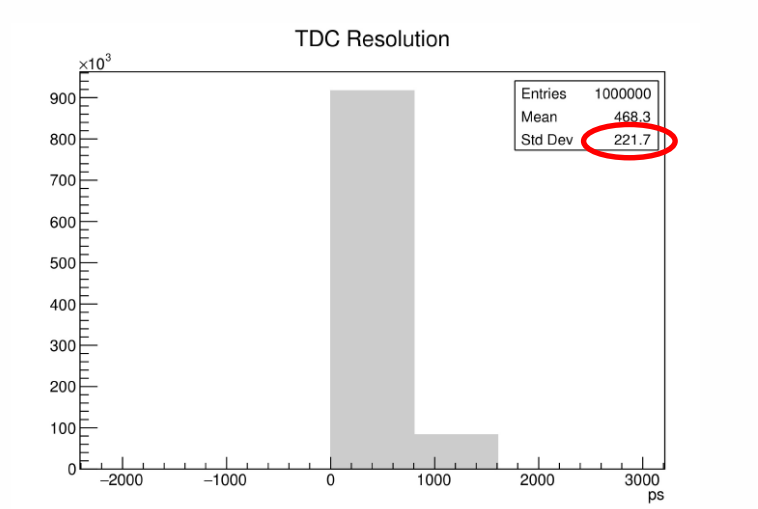
- Utilizes hardware components available within the FPGA
  - Serial-to-parallel converter ISERDES
  - Programmable temperature stabilized IODELAY
- TDC can either be used with 2 or 4 ISERDES/ IODELAY pairs per channel depending on the resolution
- Time-over-Threshold measurements are possible
- Consumes 42 FF and 30 LUT on Xilinx Artix-7
- Usable as lab set-up with direct UDP and Ethernet connection or in a bigger set-up with UCF

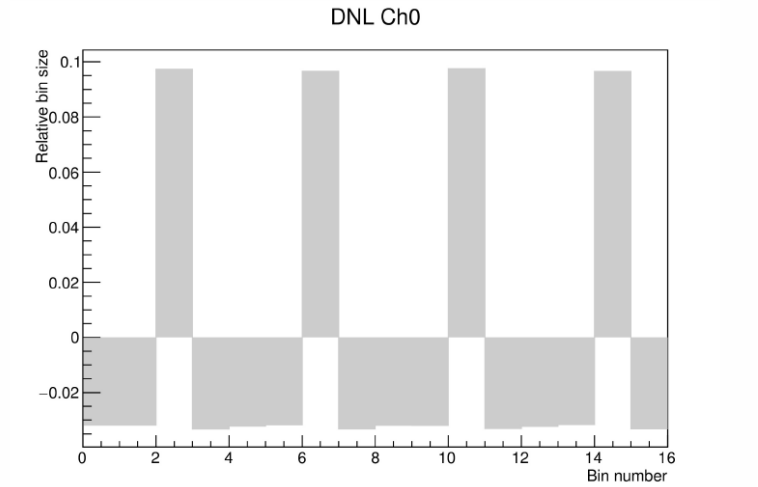




IFDAQ – TDC Measurements

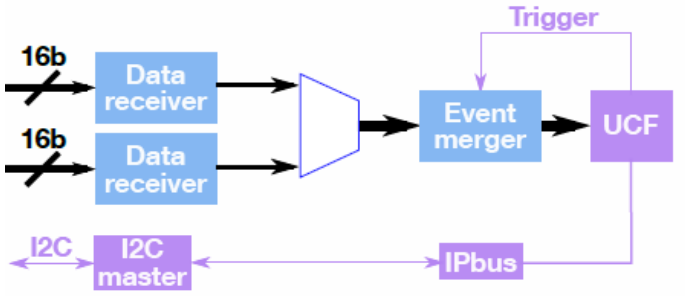
- Artix-7 **xc7a35t-1** FPGA
- TDC resolution measurement:
  - 2 ISERDES/channel
  - Time difference between two channels with random signal
  - Bin size of 803 ps (311 MHz at 4 bit/ISERDES)
  - Resolution: stddev/sqrt(2) = 156 ps
  - Standar deviation of 221.7 ps
- TDC differential non-linearity (DNL):
  - Represent deviation of the real bin width with respect to the mean bin width
  - DNL range of 4.9 %
  - DNL minimal value is 4.85 % for this set-up
- Higher Resolution possible by just changing the speedgrade or type of FPGA:
  - Virtex 6 -2 speedgrade: 100 ps



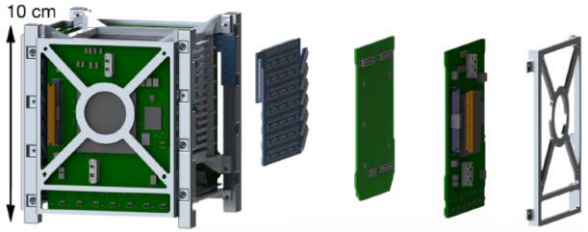


IFDAQ – Analog-to-Digital Converter (ADC) Interface

- 16 bit SPI parallel readout of the ADS527x ADC
- Sampling rate of 1 MS/s
- Interleaved mode: 2 ADCs/channel
- Configuration via I2C interface



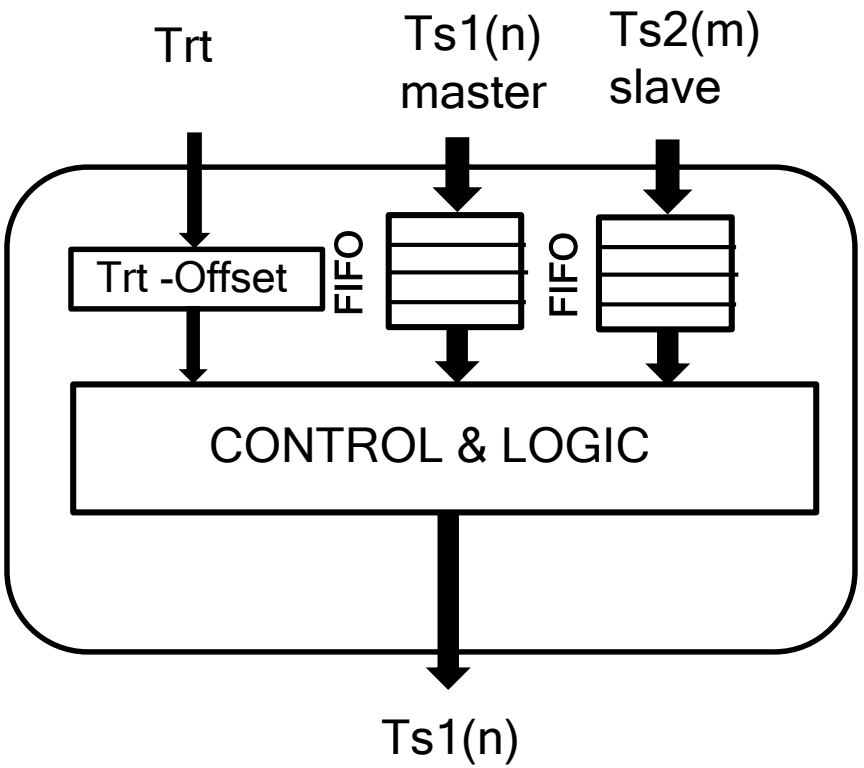
- Example:
  - Read out of 16 SiPM for a novel particle detector MAPT developed at the TUM



IFDAQ – Level 1 Trigger Logic

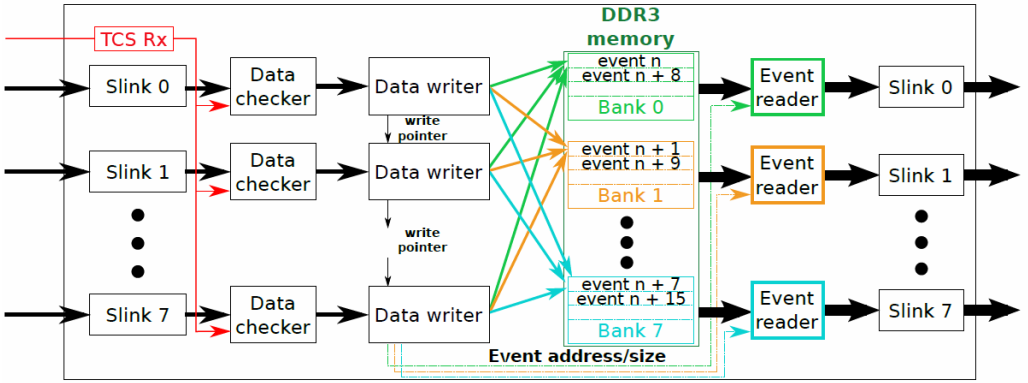
- Generation of the first level trigger based on the data from the front-ends
- Application of the logical operators (AND, OR, NOT) on the digitized signals with time reference
- Graphic representation of the trigger condition → automatic VHDL generation from the graphical model

- Example:
  Trt → real time
  Ts1(n) < Trt - OFFSET
  Ts2(m) < Trt - OFFSET
  Coincidence condition:
  (Ts2(m) – GATE)< Ts1(n) < Ts2(m)



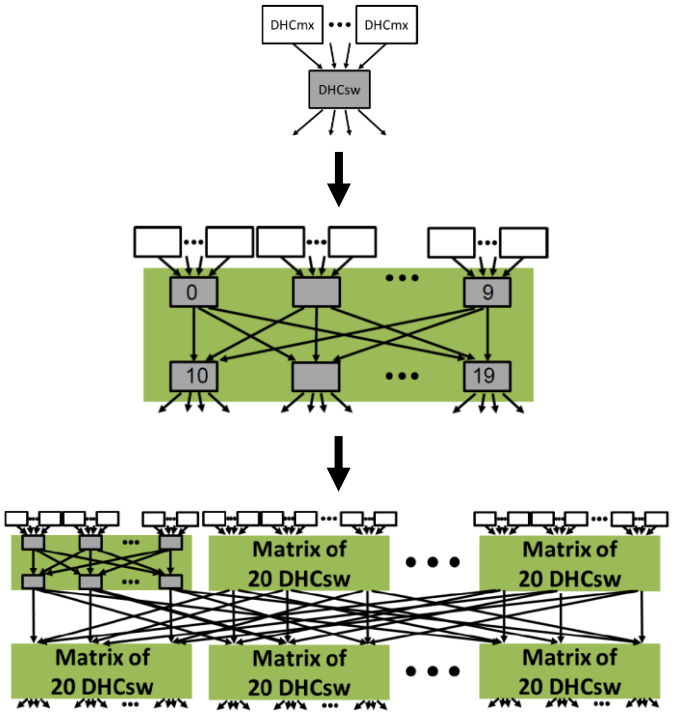
IFDAQ – Hardware Event Builder

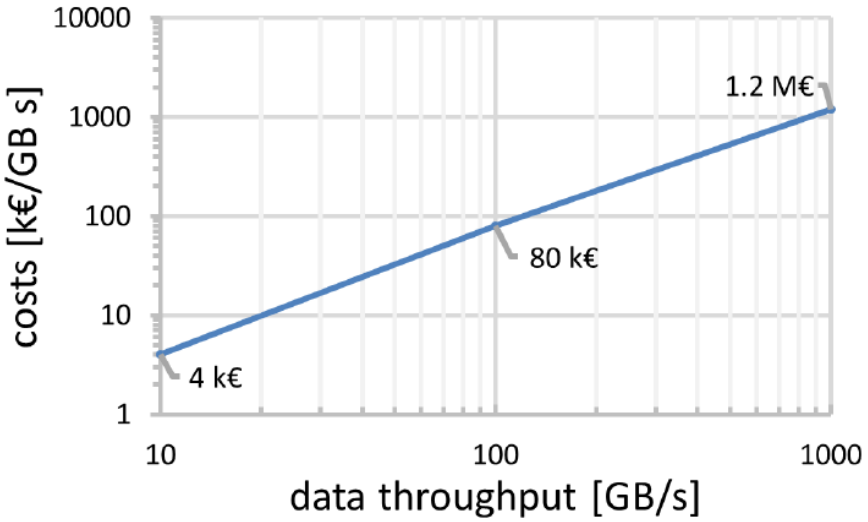
- Xilinx MIG memory core
- Memory divided into banks depending on the number of outgoing links
- Data synchronization and consistency check at the receiver
- Memory throughput: 3 GB/s and up to 4 GB of memory
- Fixed size event blocks in memory:
  - Event block accessed by a single writer
  - Requires back-pressure support in the data link



IFDAQ – Hardware Event Builder

- Event Builder theoretically scalable from 10 GB/s over 100 GB/s to up to 1 TB/s
- Low-cost solution for high data rates and stable operation
- Calculated with Kintex 7 and DDR4 memory



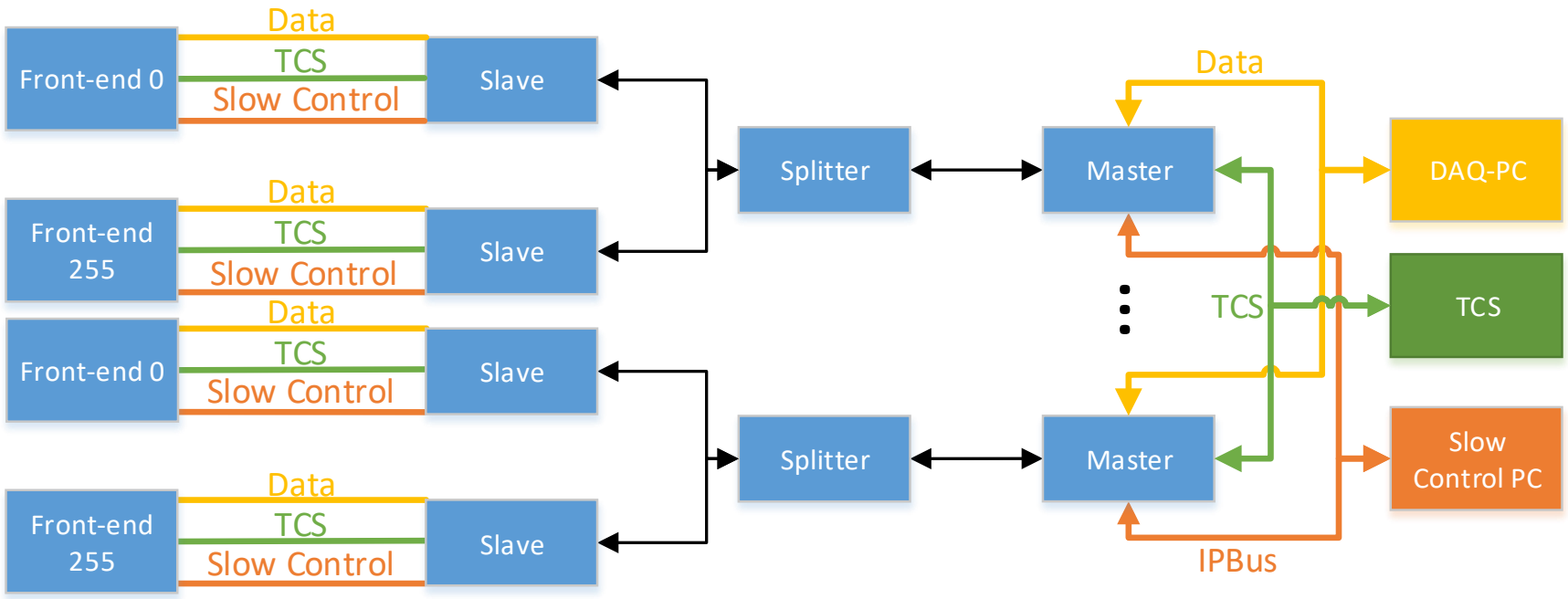


IFDAQ – Unified Communication Framework (UCF)

- Originates from the SODA time distribution system developed for the PANDA experiment
- Single high-speed serial link for data, slow control, trigger, and timing information implemented on FPGAs
- Up to 64 different communication channels (e.g. timing, slow control, Data, JTAG, I2C, SPI, TCP, UDP…)
- Fixed latency for one channel
- Priority handling for all channels
- Independent from physical layer
- All channels are addressed via the standardized ARM AMBA AXI4 Stream interface
- Leads to easy interfacing with other IP-Cores
- Configuration of all parameters with a generic directly in the top module instantiation:
  - Link speed
  - Topology
  - Device type (Spartan6, Virtex6, Artix7)

IFDAQ – Unified Communication Framework (UCF)

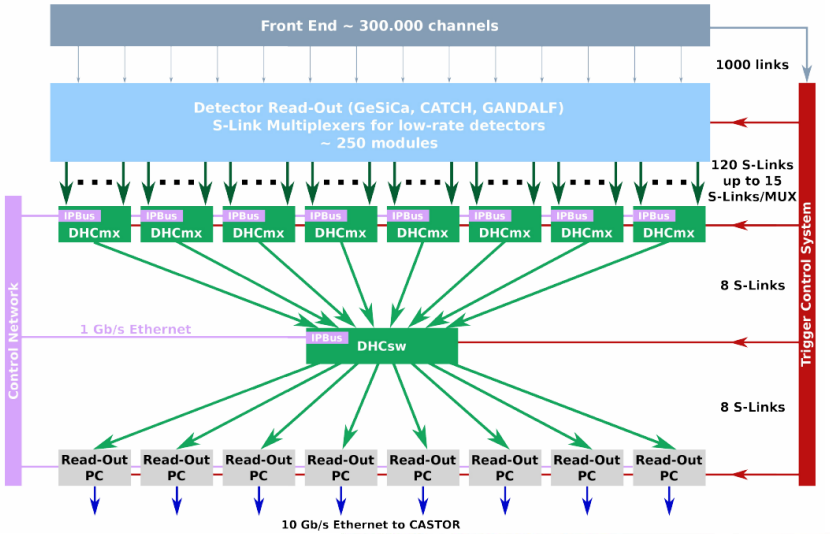
- Hybrid topology:
  - Combination of point-to-point and star-like topologies
  - Bidirectional on all channels



IFDAQ – COMPASS

- Fixed target experiment at SPS, CERN
- 300.000 channels
- Trigger rate: 30 kHz
- Event size: 50 kB
- On-spill data rate: 1.5 GB/s
- Sustained data rate: 500 MB/s
- Peak data rate: 8 GB/s

- Data acquisition system:
  - 8 S-Link Multiplexer 15:1 in FPGA
  - 1 FPGA-based event builder
  - Commercial FPGA boards for data receiving on PC
  - Synchronization by the TCS
  - Same hardware for multiplexers and event builder
  - Slow control over Ethernet using IPbus



IFDAQ – COMPASS

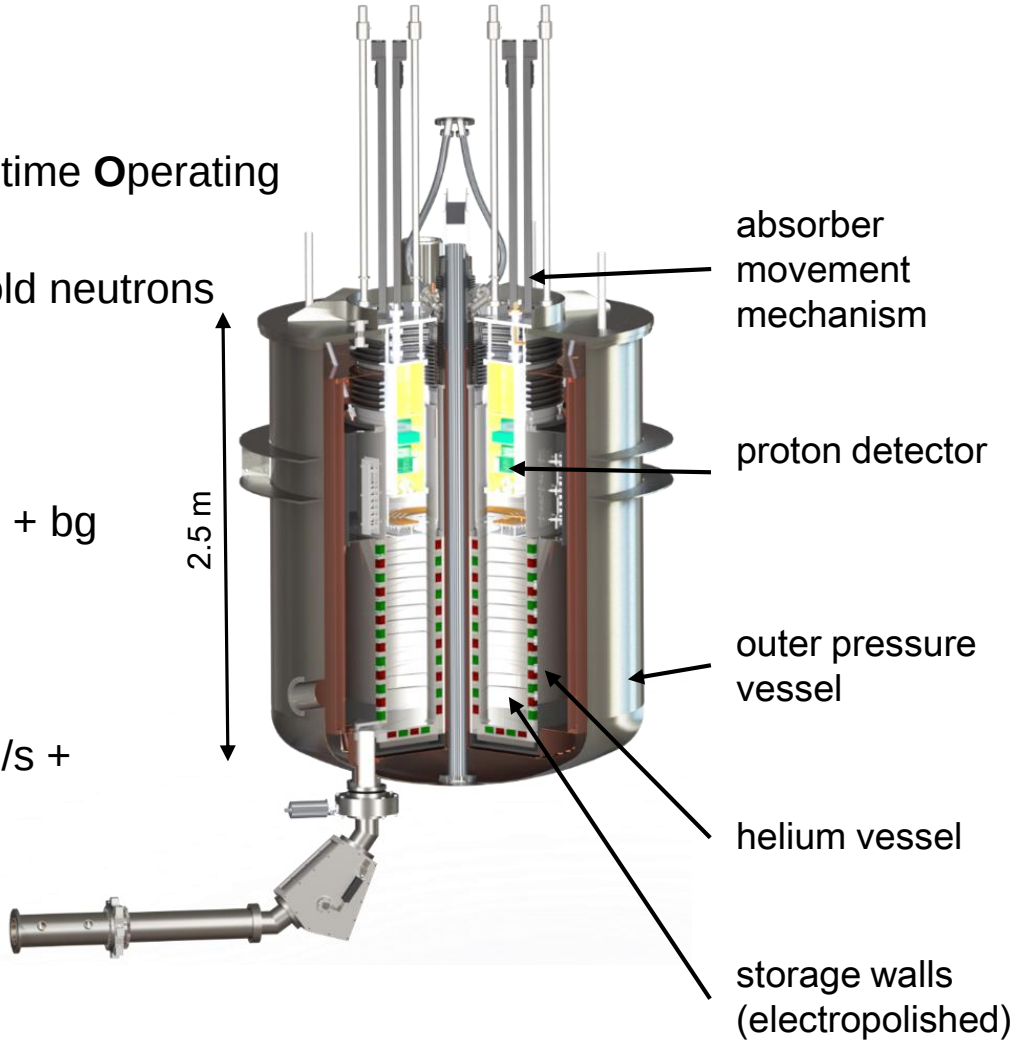
- Further upgrade of the COMPASS MWPC and ECAL with the new TDC card
- MWPC
  - 26000 channels
  - Low cost module with FPGA-based TDC
  - Artix-7 FPGA
  - Approx. 400 modules
  - Required resolution: 600 ps/bin

- Electromagnetic calorimeter
  - 7000 channels
  - Low cost FPGA modules with the 4-channel ADC
  - Sampling rate: up to 200 MS/s
  - JESD204B ADC interface
  - Artix-7 FPGA

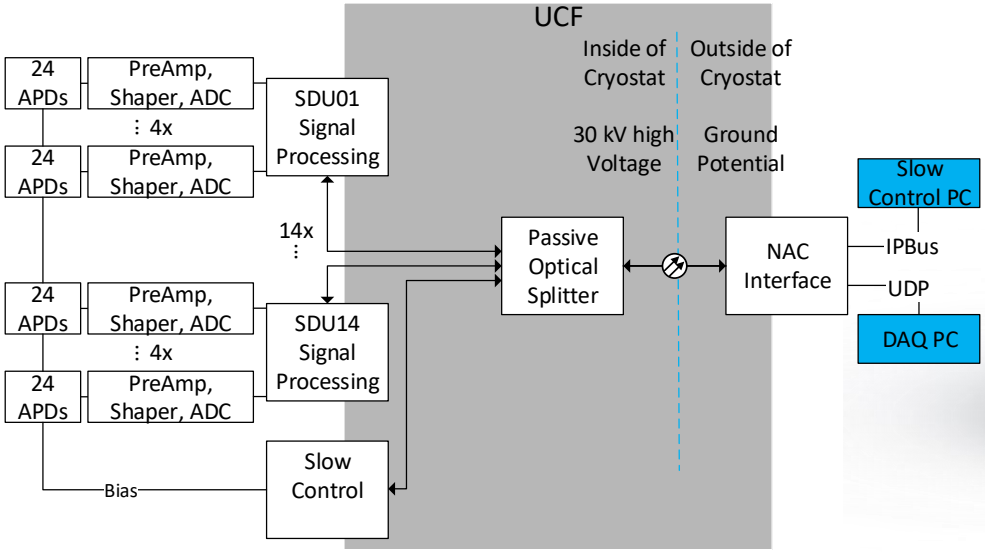
IFDAQ – PENeLOPE

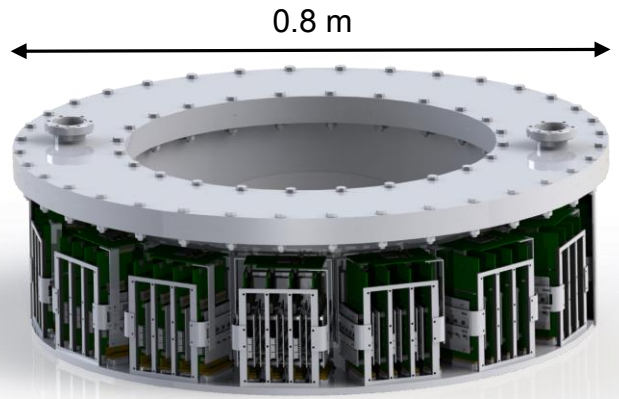
- **P**recision **E**xperiment on **Ne**utron **L**ifetime **O**perating with **P**roton **E**xtraction
- Magneto-gravitational trap for ultra-cold neutrons
- Aiming for a precision of ± 0.1 s
- Measuring protons and neutrons

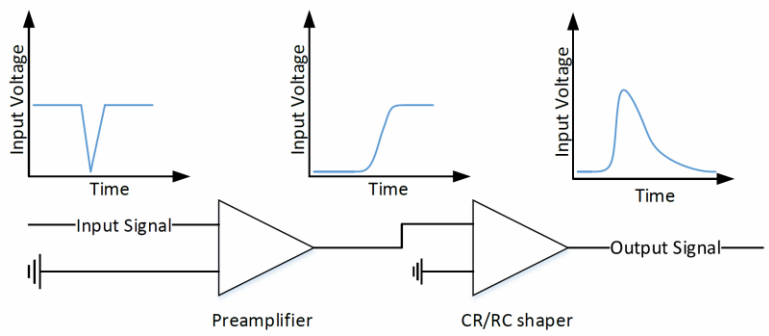
- Average event rate: 130.000 events/s + bg
  ≈ data rate: 500 Mbit/s
- Active area of 0.23 m^2
- 1300 detector channels
- Peak event rate per channel: ca. 70 p/s + 35 e^-/s + γ = 105 events/s + bg
- Avalanche Photodiodes used as a proton detector

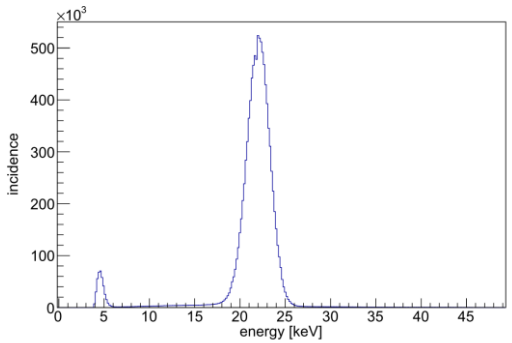


IFDAQ – PENeLOPE



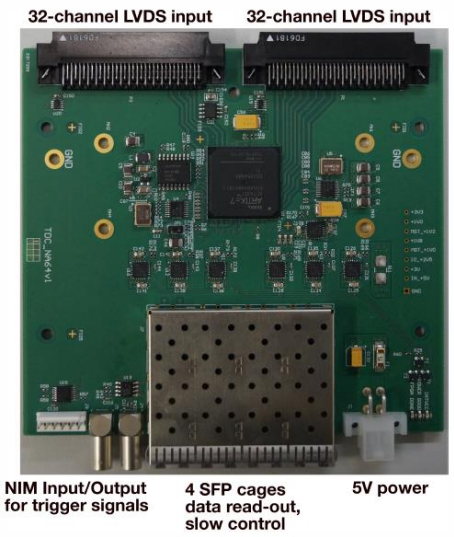


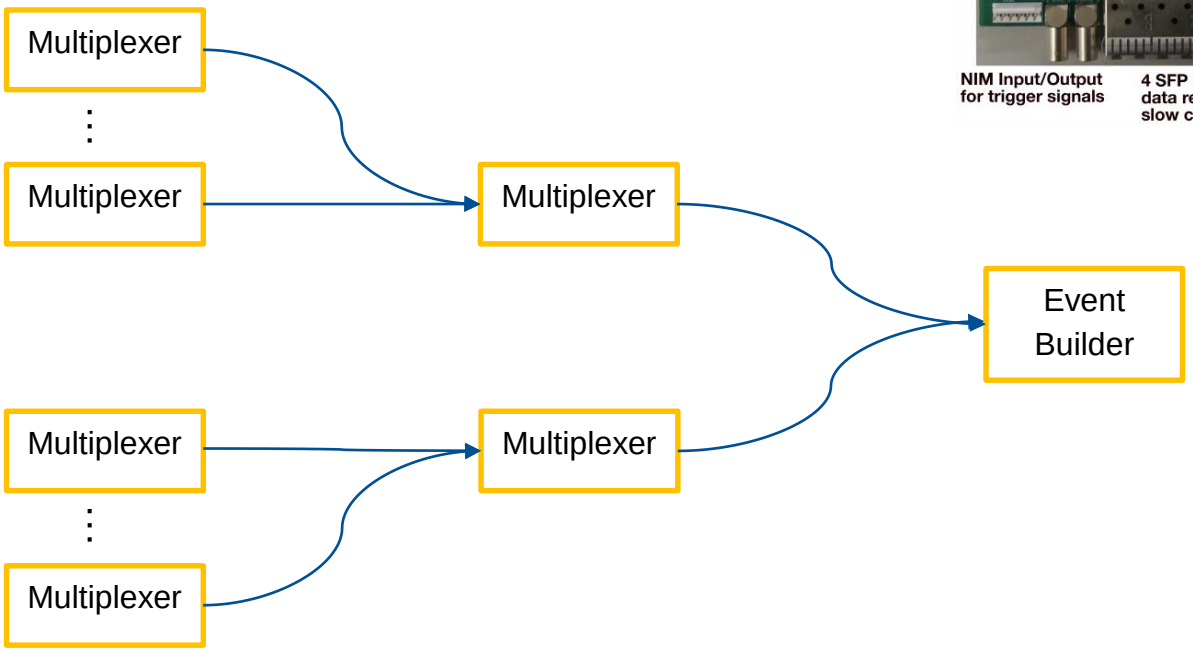




IFDAQ – NA64

- Clean, mono-energ. 100 GeV e- beam
- Read out of the STRAW detector
- 16 modules with 64 channels each
- 2 multiplexer cards





IFDAQ – Summary and Outlook

- IFDAQ framework simplifies the designing of DAQ systems
- As generic as possible through standard communication interfaces
- The framework includes:
  - Front-end cores
  - L1 trigger generation
  - Unified communication framework (UCF)
  - Hardware event builder

- Different aspects of the framework have been tested in the COMPASS Belle II and the PENeLOPE experiment
- A IFDAQ TDC system is currently being integrated into the NA64 experiment

Thank you for your attention