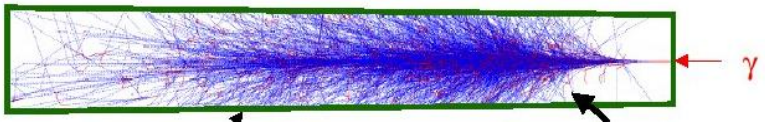
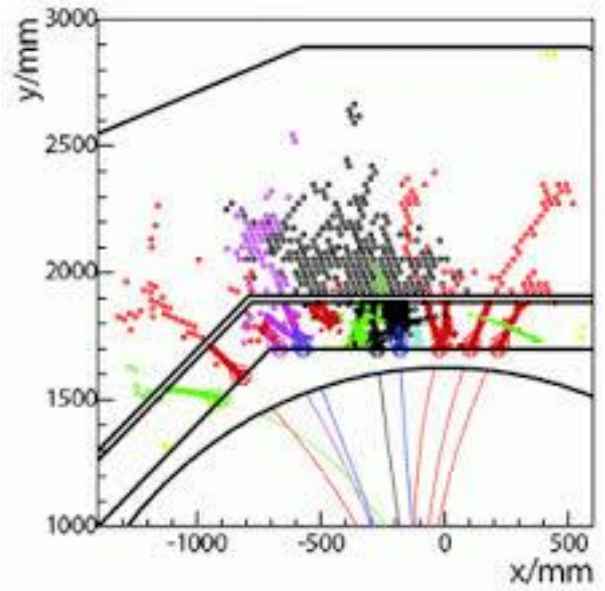
FRONT-END ELECTRONICS for IMAGING/TIMING CALORIMETRY

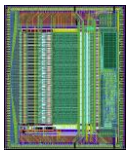
Christophe de LA TAILLE TIPP 2017 Beijing

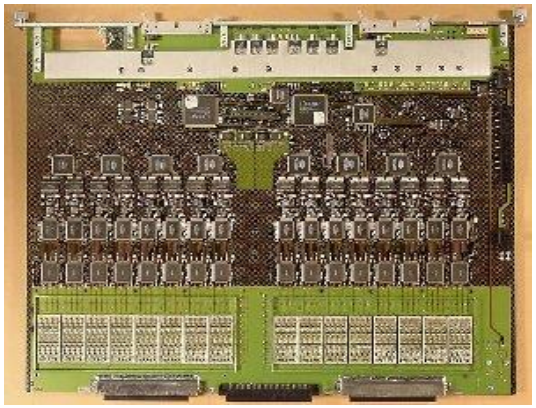
Evolution of calorimetry





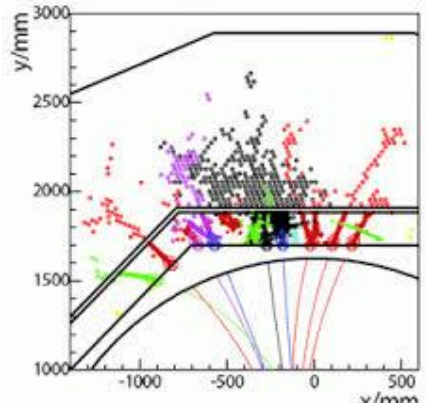
- 3D calorimetry : eta, phi, Energy
- 4D calorimetry : x,y,z,E
- 5D calorimetry : x,y,z,E,t
  - High granularity=> Millions of channels = > Low power !
    - Power pulsing ~1% for ILC
    - Low power + C02 cooling for HL-LHC
  - Energy measurement : Large dynamic range
    - MIP sensitivity => low noise (~0.1 fC)
    - Up to thousands of MIPs (~10 pC)
  - Timing information
    - Nice addition for ILC for PID : few ns is enough
    - Crucial for HL-LHC : pileup mitigation, need few tens of ps
  - Embedded electronics vs data out
    - Daisy chain and low power busses for ILC
    - High speed e/optical links for HL-LHC
  - Radiation levels
    - Negligible at an ILC
    - Daunting at HL-LHC : >100 Mrad $1^{E}16N$
- *See talk by Eva Sicklng and referred talks*



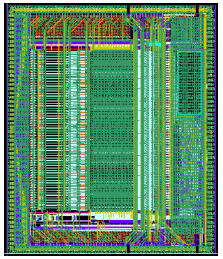


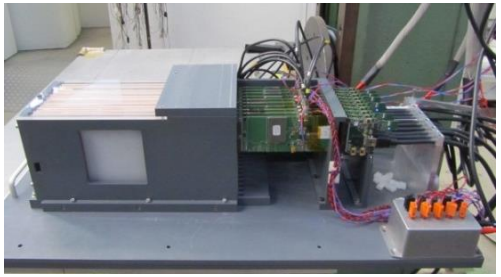
CALICE technological prototypes

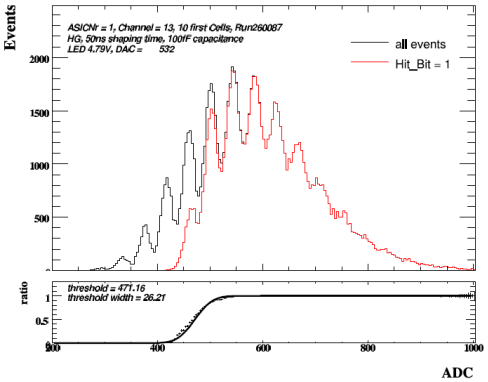
- R&D on imaging calorimetry
  - Particle Flow Algorithms [
  - Electronics crucial (low noise, low power, fully integrated)
  - Several innovative features (power pulsing, SiPM…)
  - Validation of technological prototypes
  - Common R/O features
  - Worldwide collaboration



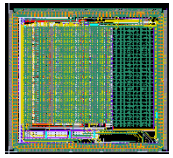
SKIROC2



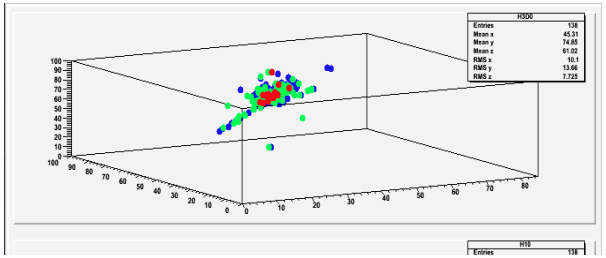




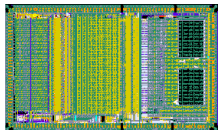
SPIROC2



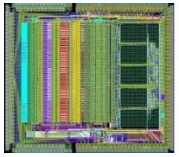
AIDA



HARDROC2



MICROROC



SiW ECAL

- 25 mm² Si pads 300 µm thick
- 4 wafers per ASU 18x18 cm
- Readout 16 SKIROC2 chips 64ch
- Chip on board or BGA package
- Daisy-chain readout
- MIP/noise ~18

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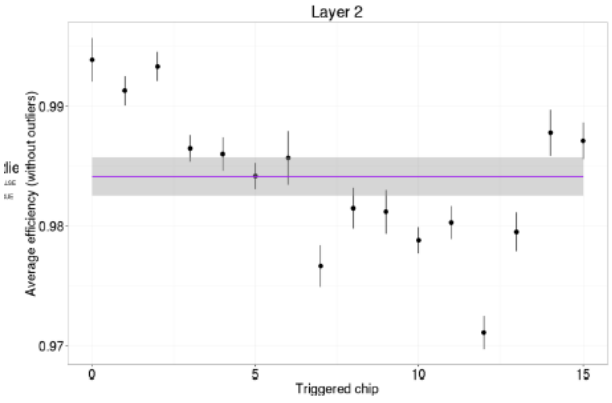
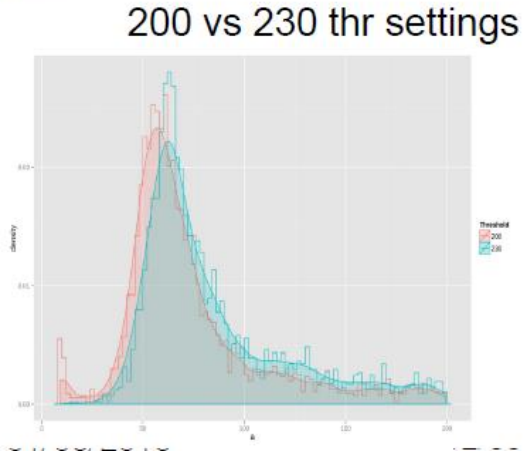
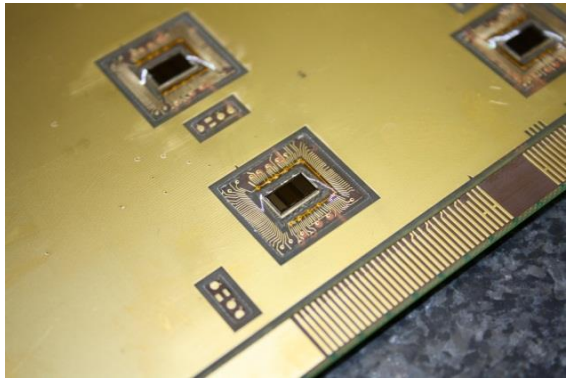
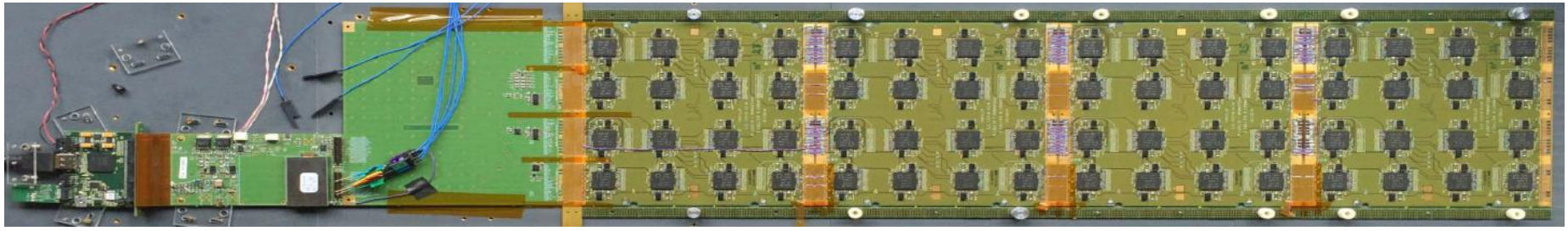
https://agenda.linearcollider.org/event/7014/contributions/34685/

$\langle\varepsilon\rangle_{CHIP} > 97\%$; $\langle\varepsilon\rangle_{LAYER} \geq 98.3\ \%$



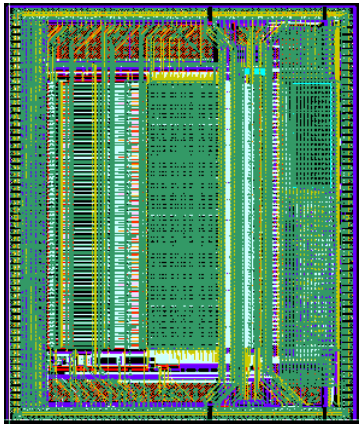


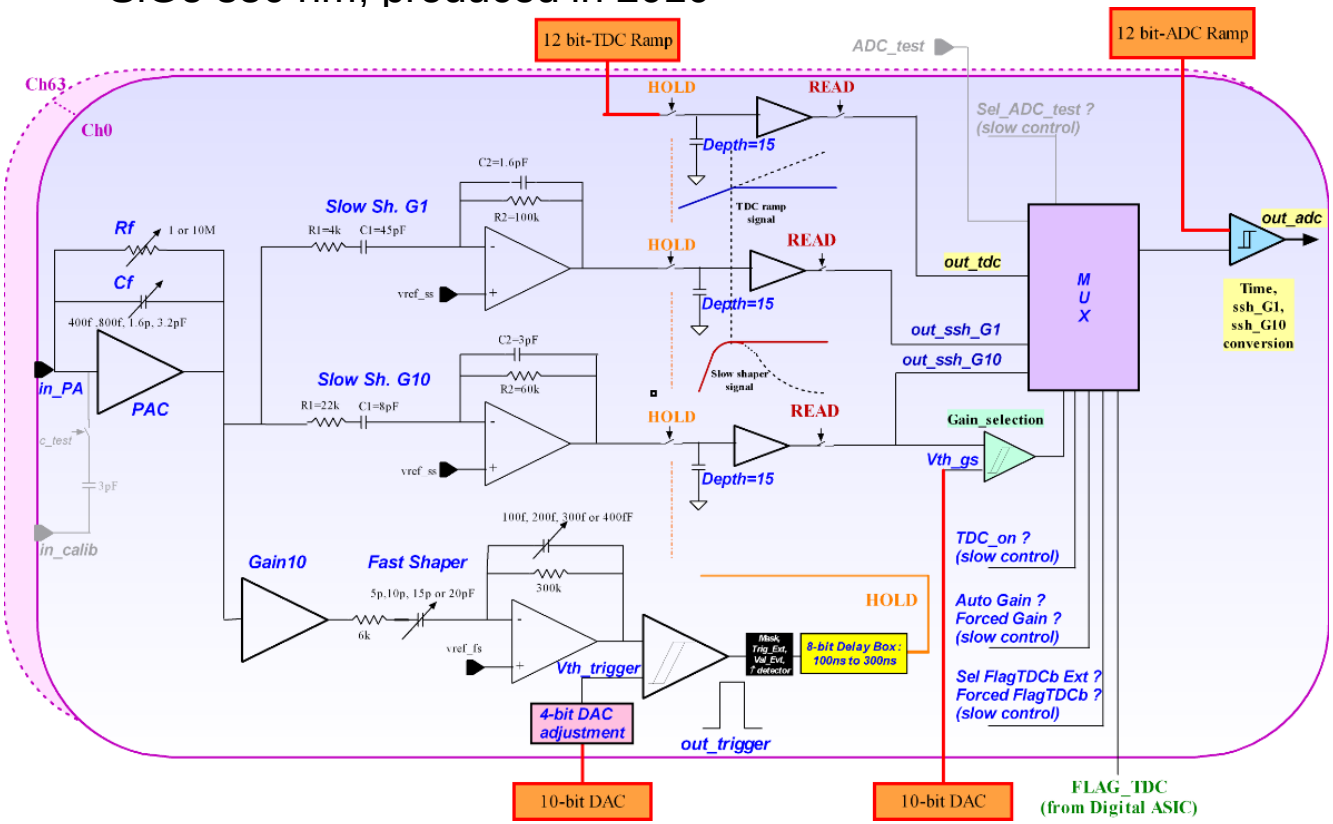


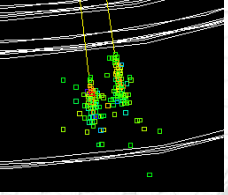


SKIROC2 readout ASIC

- 64-channel Silicon Kalorimeter Integrated Read-Out Chip
  - Autotrigger @ ½ MIP = 2 fC
  - Charge measurement 15 bits in two gains
  - 16-deep Analog memory
  - Low power 25µW/Ch with power pulsing
  - Embedded readout (see SPIROC)
  - SiGe 350 nm, produced in 2010



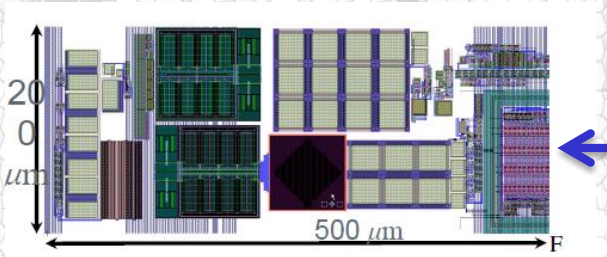




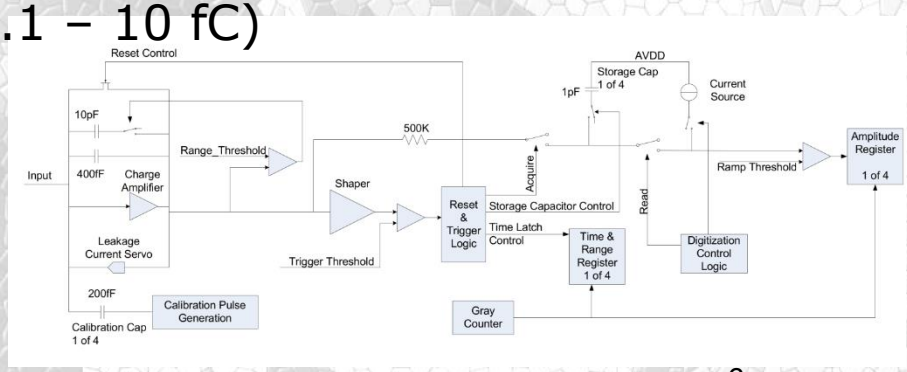
KPiX – System on a Chip

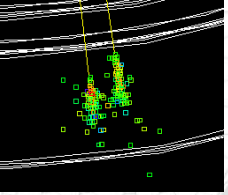
KPiX is a 1024 channel ASIC to bump bond to Si detectors, optimized for the ILC (1 ms trains, 5 Hz rate):

- Low noise dual range charge amplifier w/ 17 bit dynamic range.
- Power modulation w/ average power <20 μW/channel (ILC mode).
- Up to 4 measurements during ILC train; each measurement is amplitude and bunch number.
- Digitization and readout during the inter-train period.
- Internal calibration system
- Noise Floor: 0.15 fC (1000 e^-)
- Peak signal (Auto-ranging) 10 pC
- Trigger Threshold Selectable (0.1 – 10 fC)



One pixel,
200 x 500 μm^2

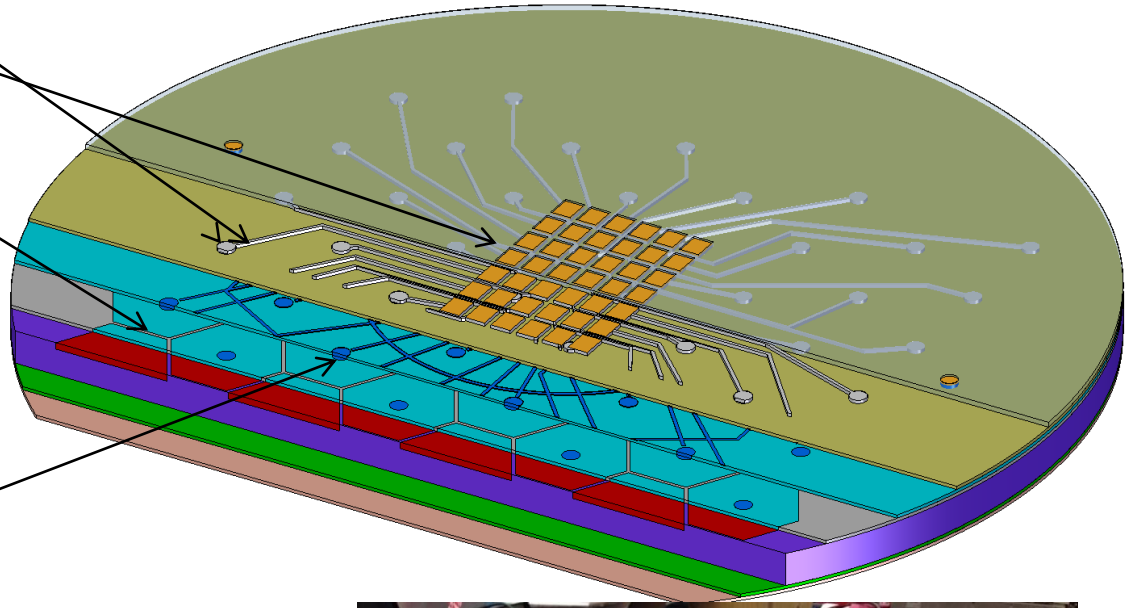


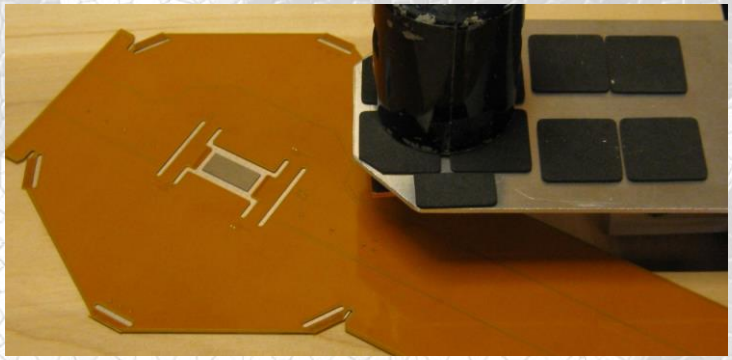


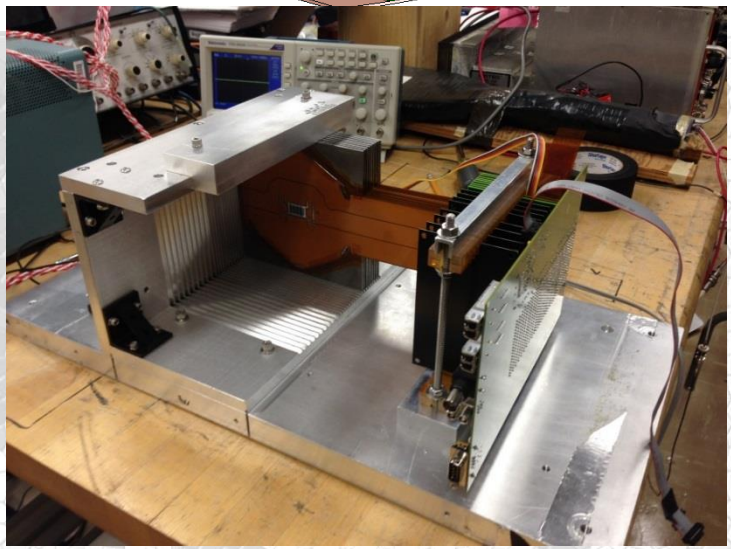
Sensor Traces

In present design, metal 2 traces from pixels to pad array run over other pixels: parasitic capacitances cause crosstalk.

New scheme has "same" metal 2 traces, but a fixed potential metal 1 trace shields the signal traces from the pixels.

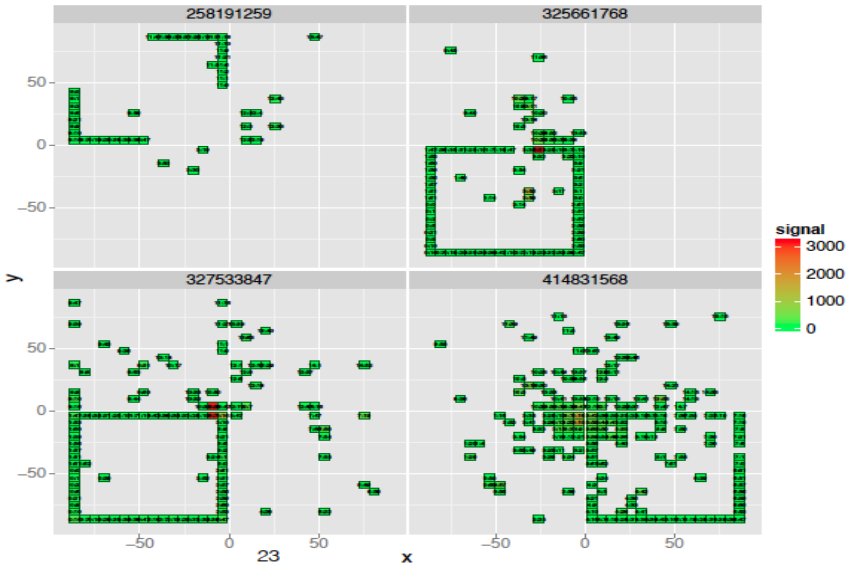


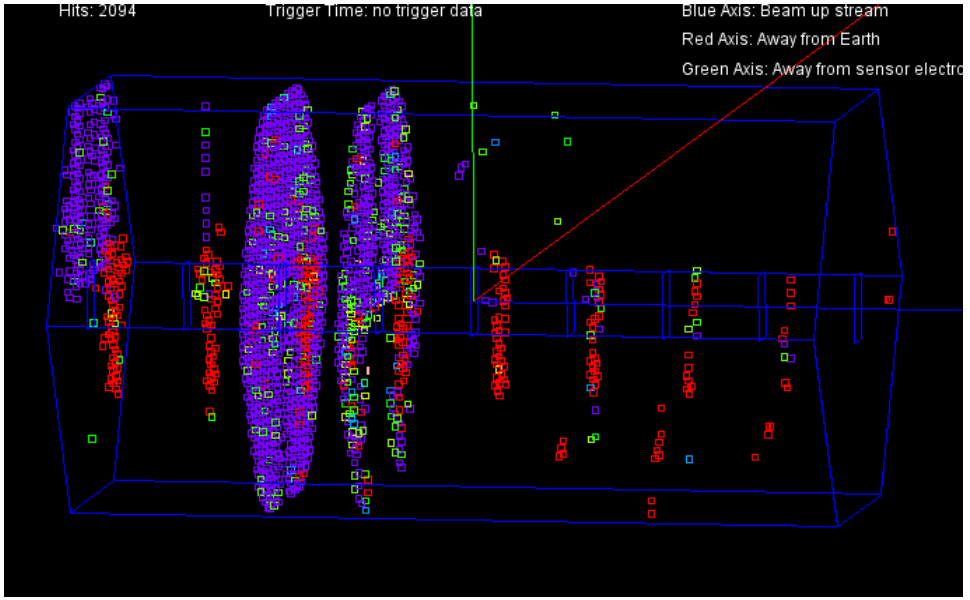


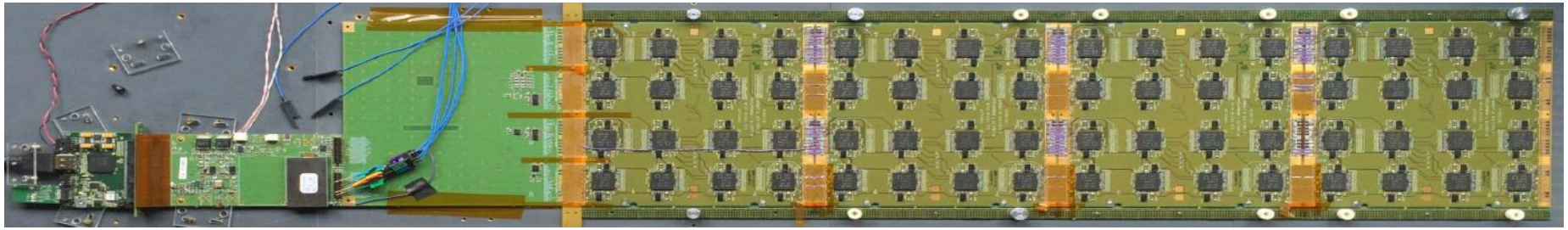


Issues (both)

- Noise, crosstalk, « square events » « monster events »
- Retriggering, digital noise
- Connectors and power supplies





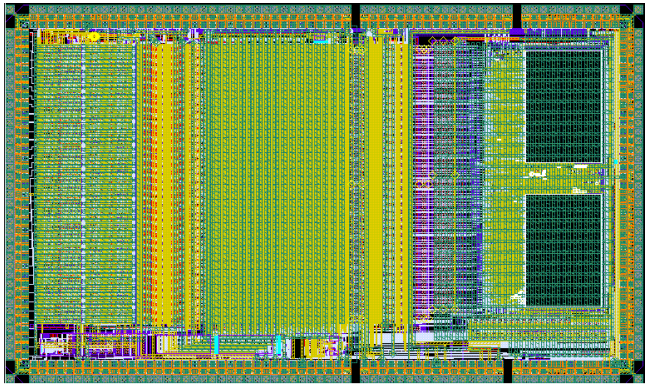


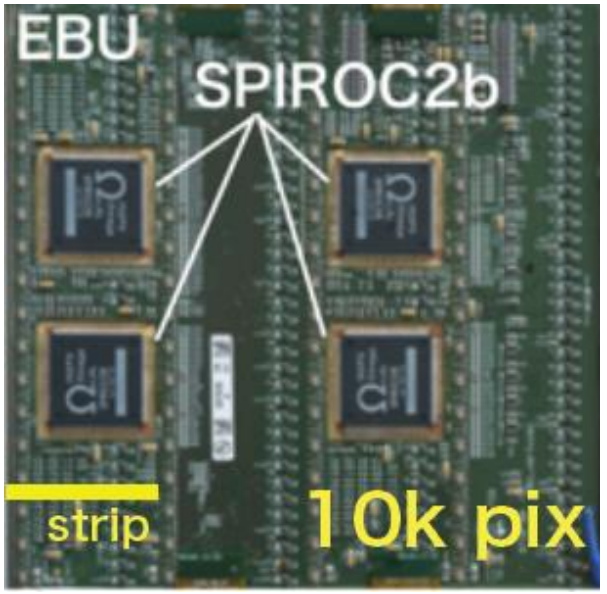
AHCAL/ScECAL : SiPM readout

- Scintillating tiles and SiPM
  - Pioneered by DESY (EUDET/AIDA)
  - Chip embedded in detector : low power !

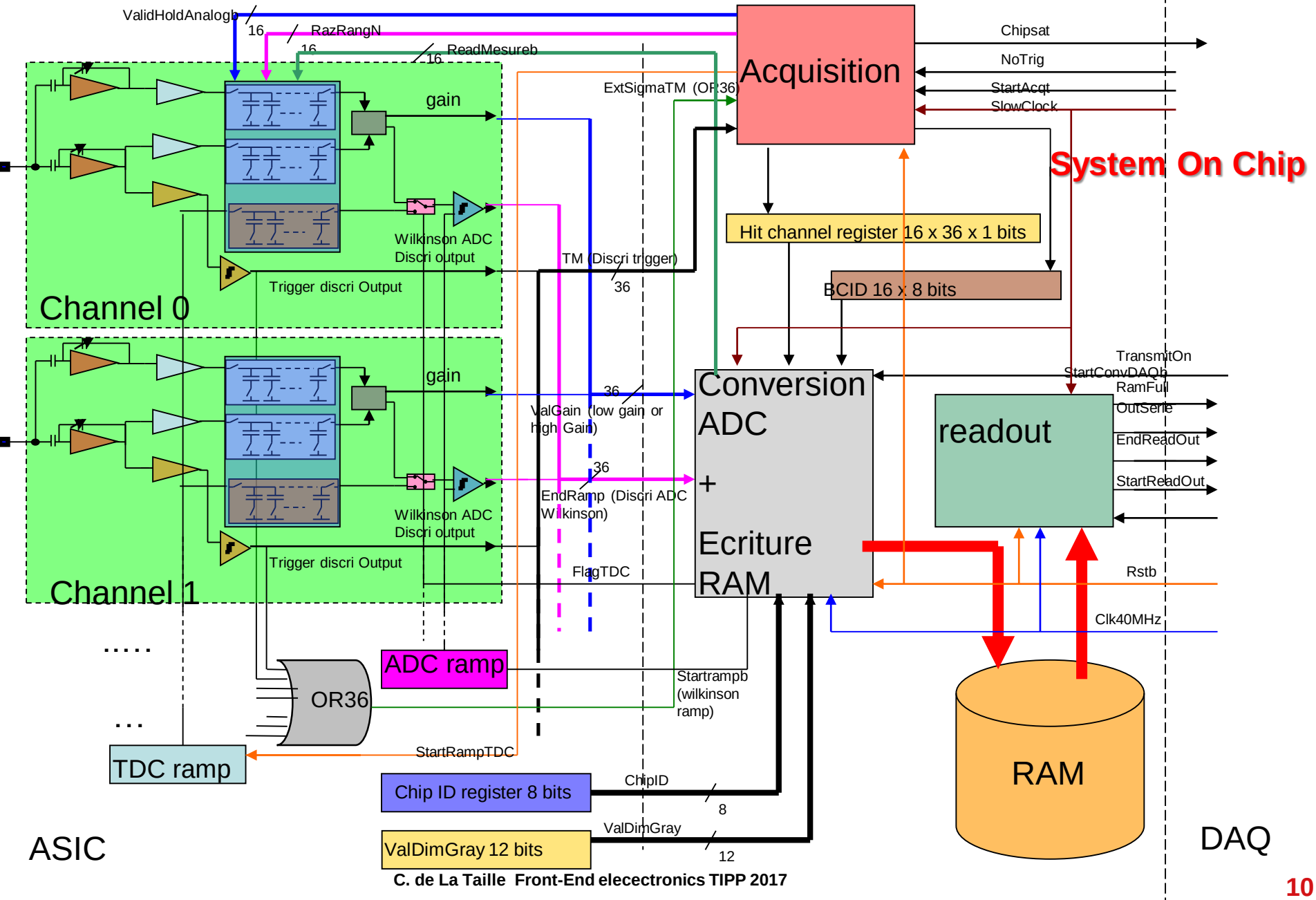
- SPIROC : Silicon Photomultiplier Integrated Readout Chip
  - Variant of skiroc
  - 36 channels autotrigger 15bit readout
  - Energy measurement : 15 bits in 2 gains
  - Autotrigger down to ½ p.e. (80 fC)
  - Time measurement to ~1 ns
  - Power dissipation : 25µW/ch (power pulsed)

$(0.36m)^2$ Tiles + SiPM + SPIROC (144ch)



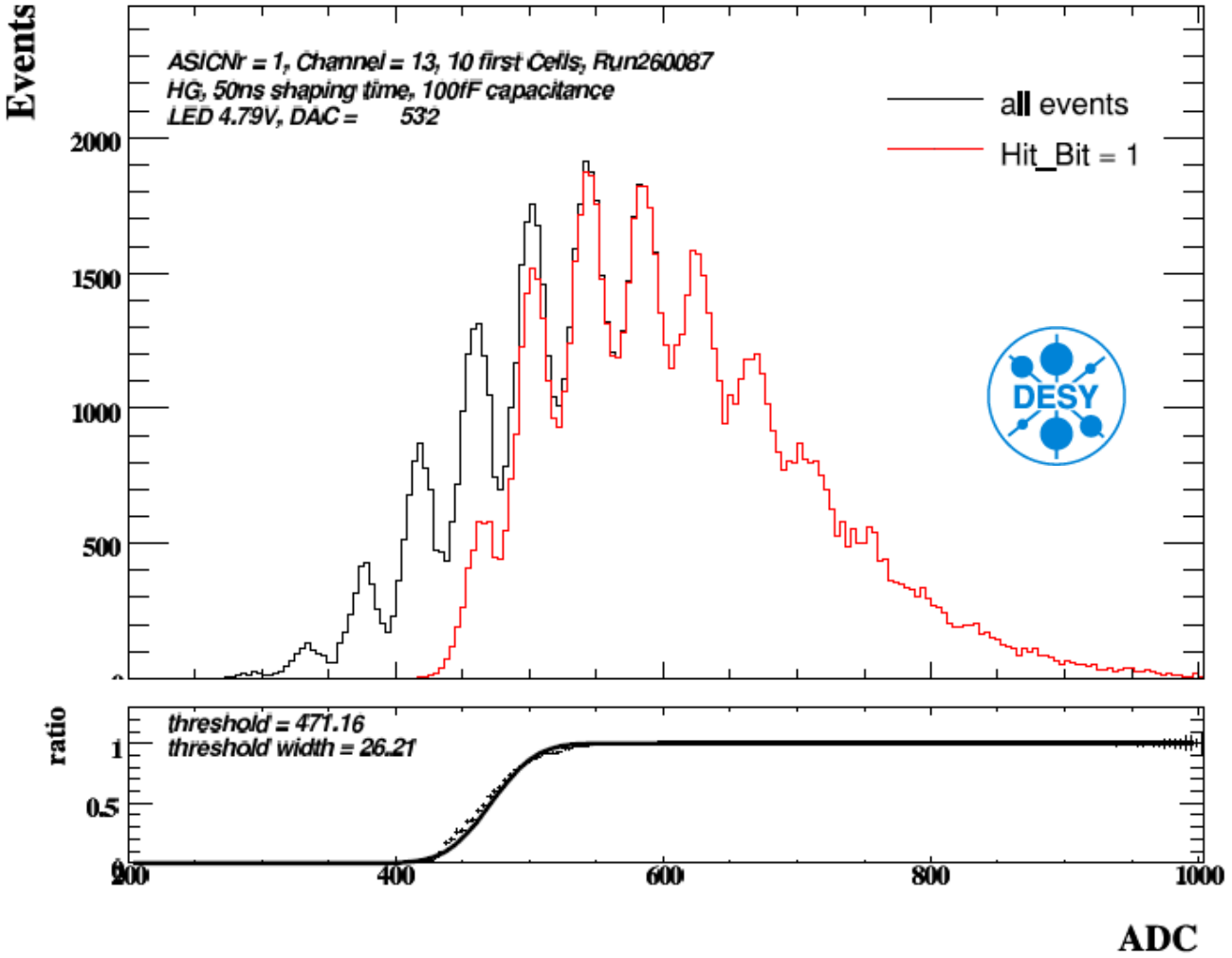


SPIROC : System On Chip



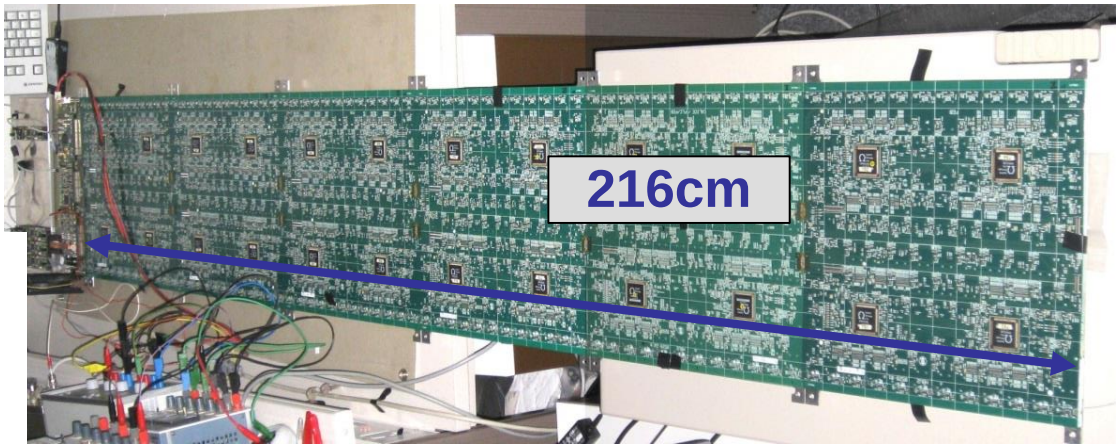
SPIROC2 performance

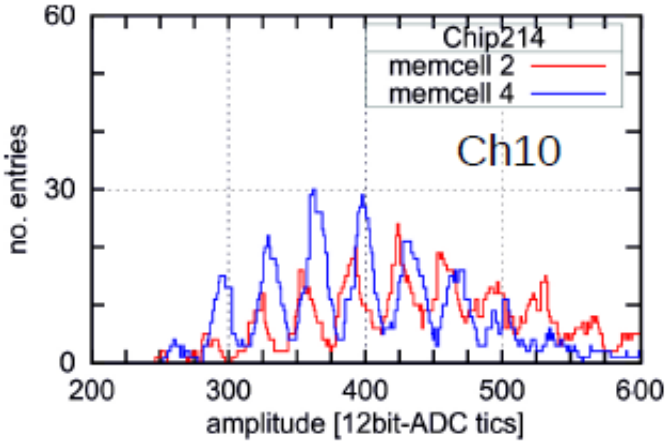
SiPM SPECTRUM with Autotrigger

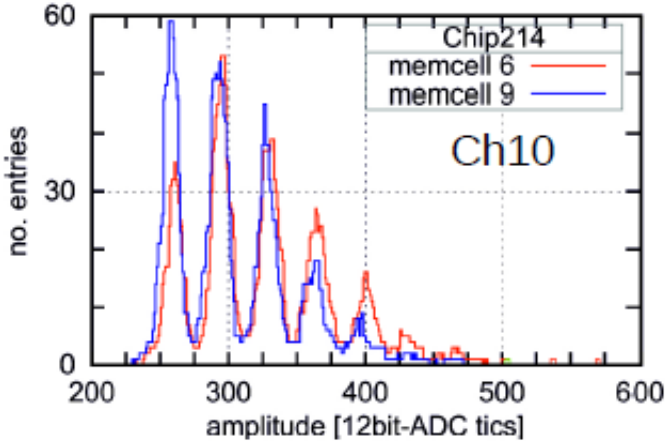


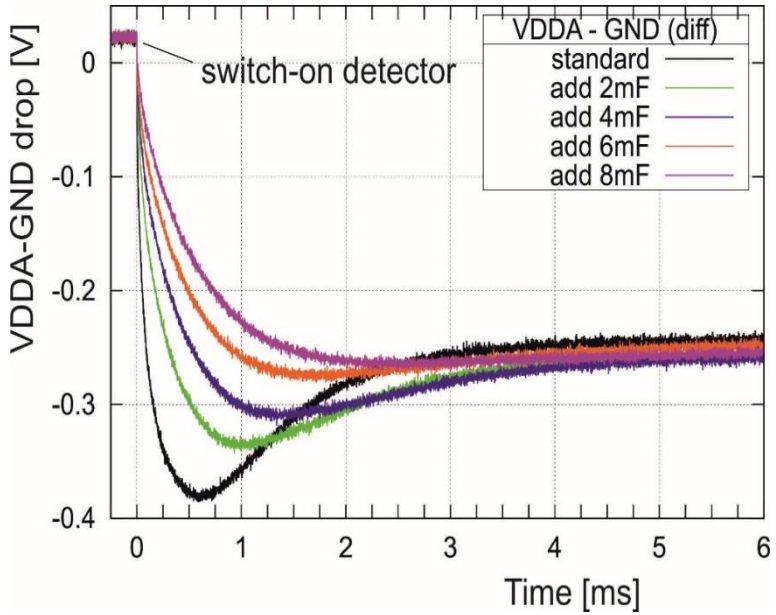
Power pulsing studies

- 2.5 A switched at 5 Hz
- 150 µs settling time



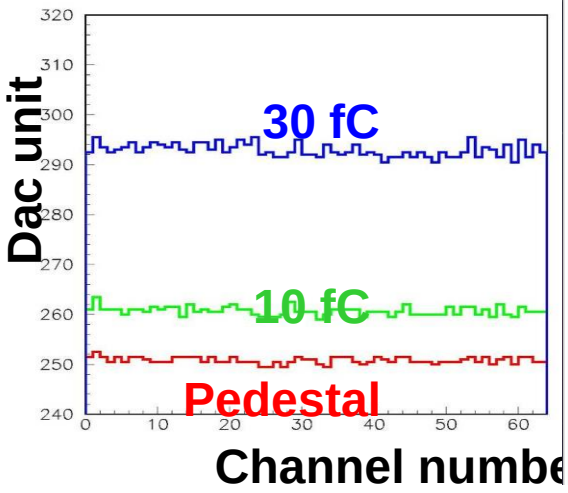


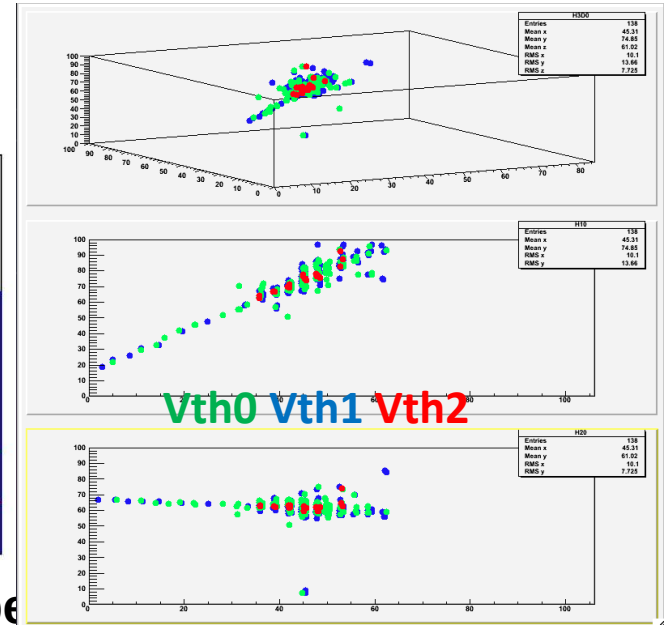




SDHCAL RPC calorimeter

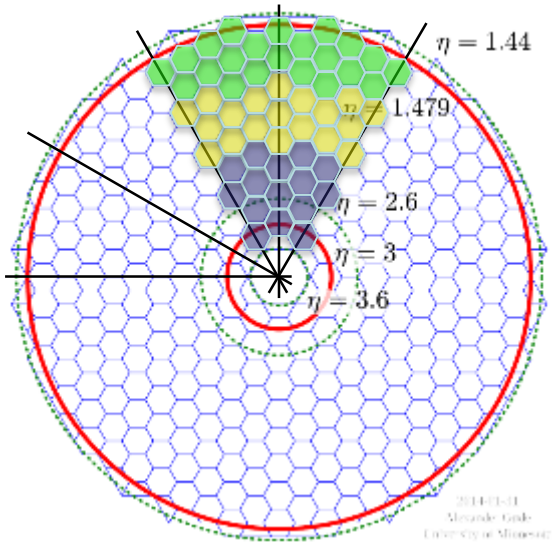
- Semi-digital Hadronic calorimeter (SDHCAL) technological proto with up to **50 layers** built in 2010-2011.
- Scalable readout scheme successfully tested
- 10 fC threshold on 1 m² (1 fC with micromegas)
- Complete system in TB with **460 000 channels**, **AUTOTRIGGER** mode and **power pulsing (5%)**

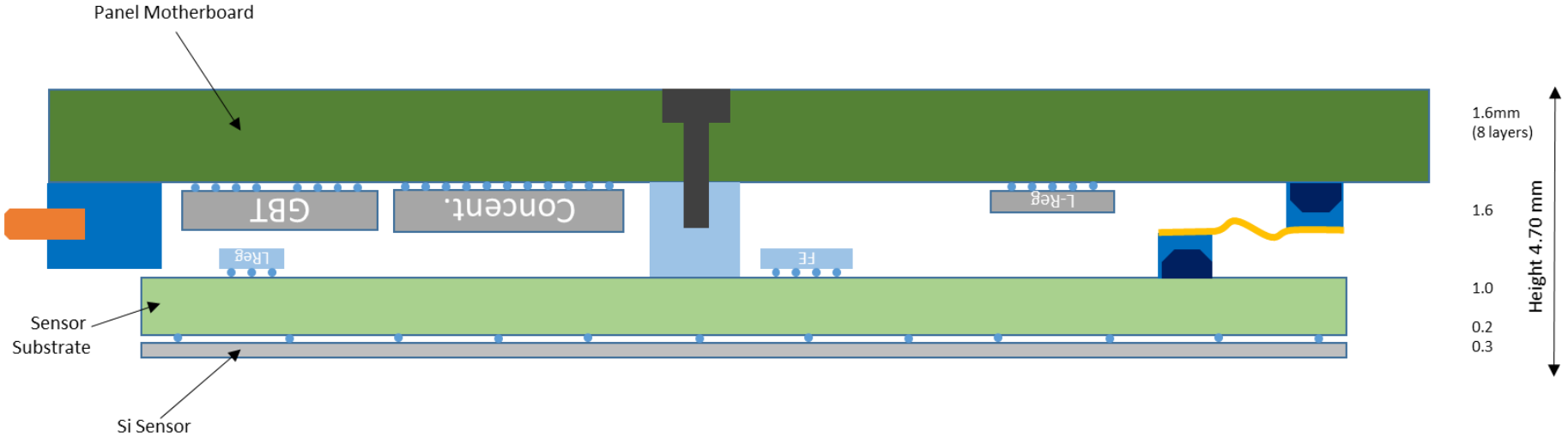




CMS HGCAL Detector overview

- Stringent requirements for Front-End Electronics
  - Low power (< 10 mW),
  - low noise (< 2000 e-) MIP ~ 1-4 fC
  - High radiation (200 Mrad, 10^E16 N)
  - System on chip (digitization, processing…)
  - High speed readout (5-10 Gb/s)
  - ~ 10 million channels

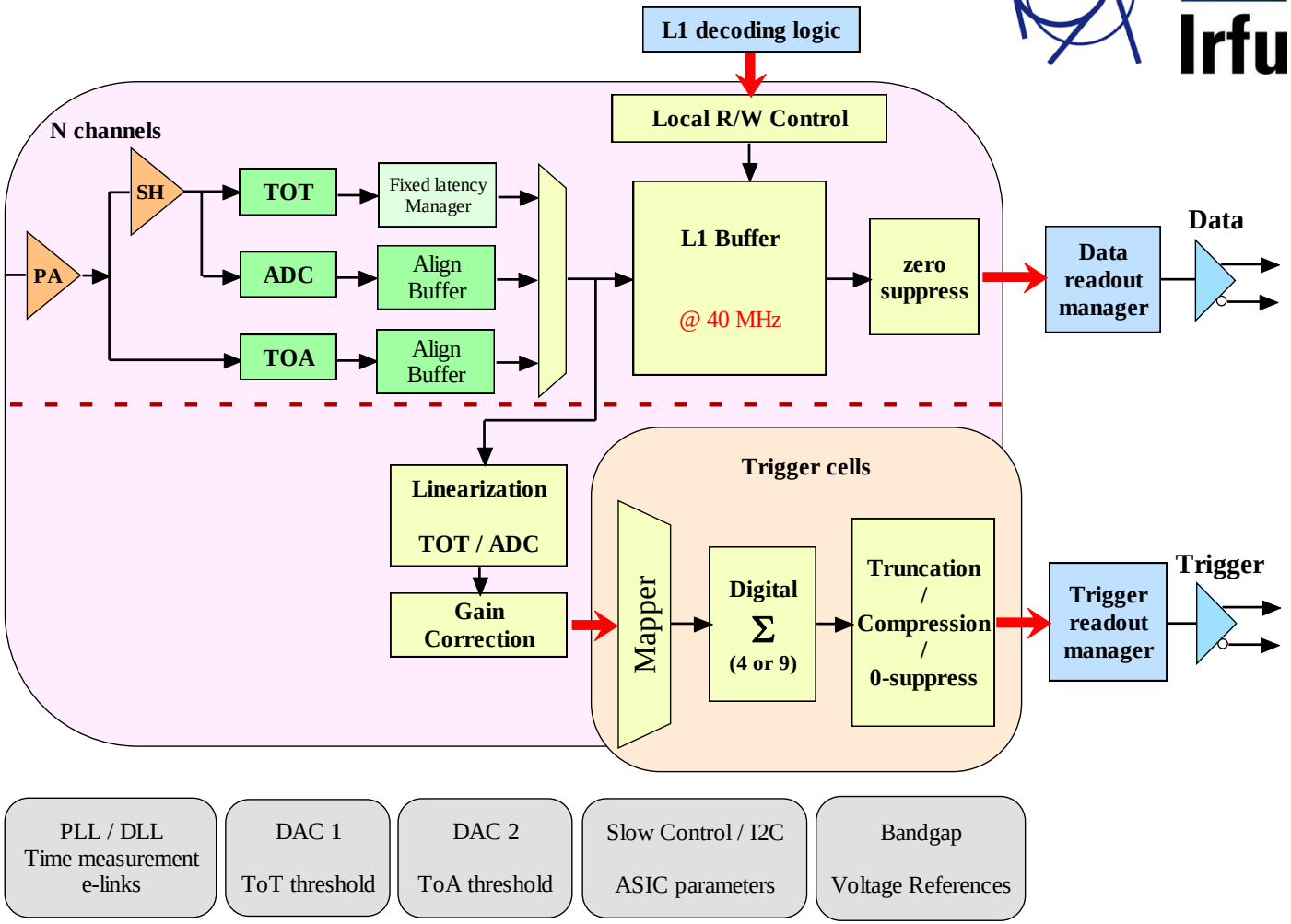




HGCAL readout ASIC

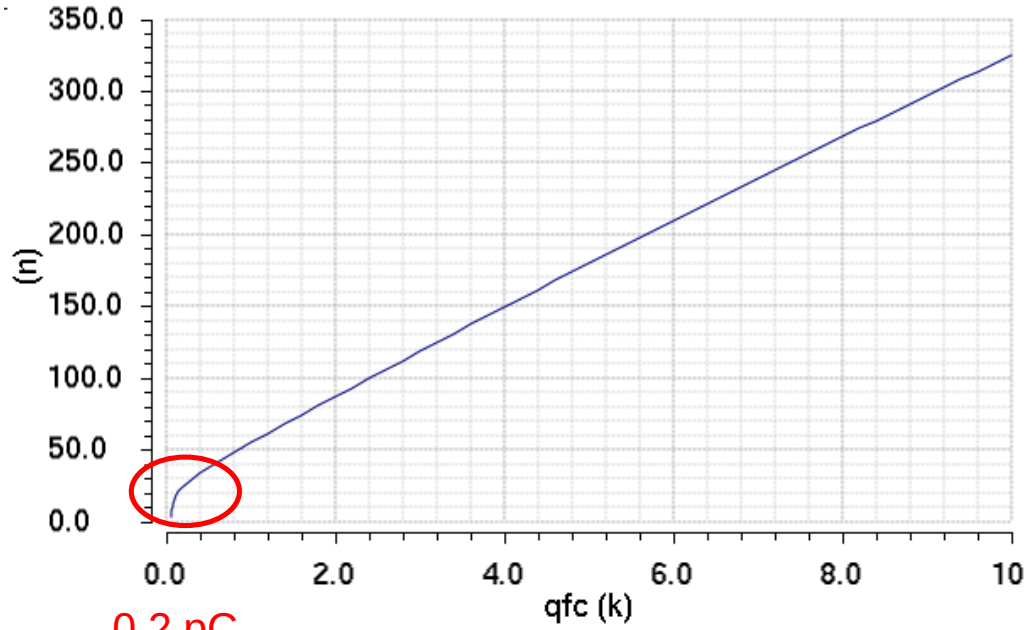
HGROCv1 features:

- 32 channels
- Dual polarity
- TOT with 2 variants:
  - Low power @ Imperial
  - DLL @ OMEGA (CERN based)
- TOA (CEA)
- 11-bit SAR ADC (OMEGA)
- Simplified Trigger path
  - Only sum by 4
  - No 0-suppress (4+4 log)
- Data readout to be defined
- SC with triple voting (shift register like SK2-CMS)
- Many digital block with simplified architecture
- Services
  - Bandgap from CERN
  - PLL from CEA-IRFU
  - 10b DAC from TV2

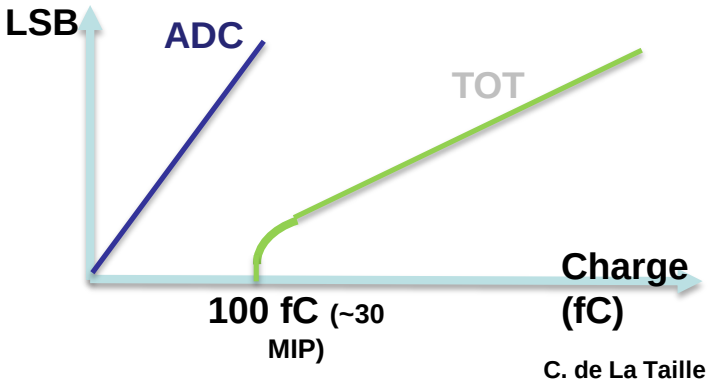


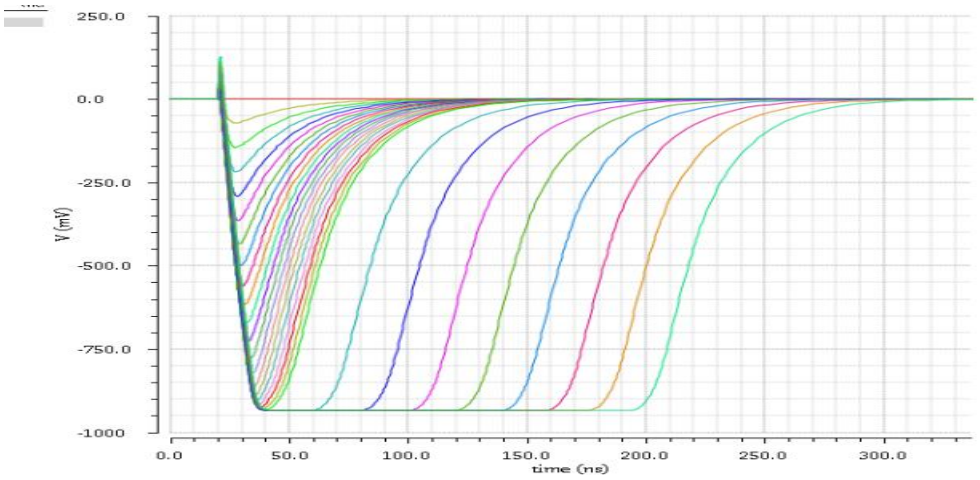
VFE architectural issues

- key issues to be studied :
  - Noise
  - Resolution
  - Stability
  - Linearity
  - Accuracy
  - Calibration
  - crosstalk
  - Radiation
  - Timing
  - Systematic effects



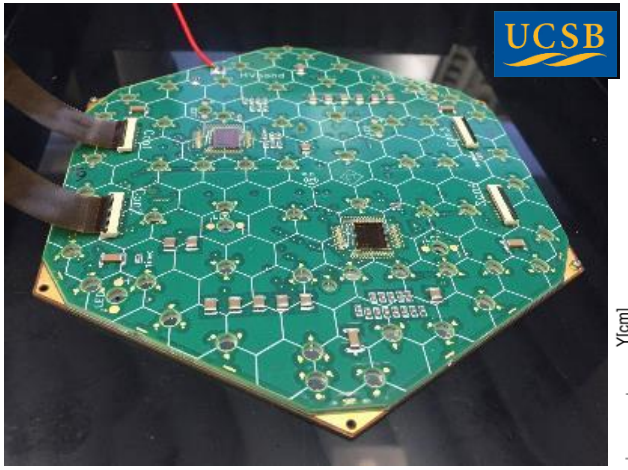
0.2 pC
~100 MIPS

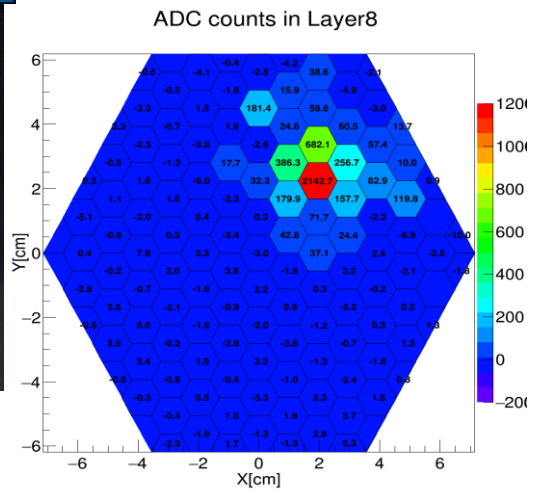


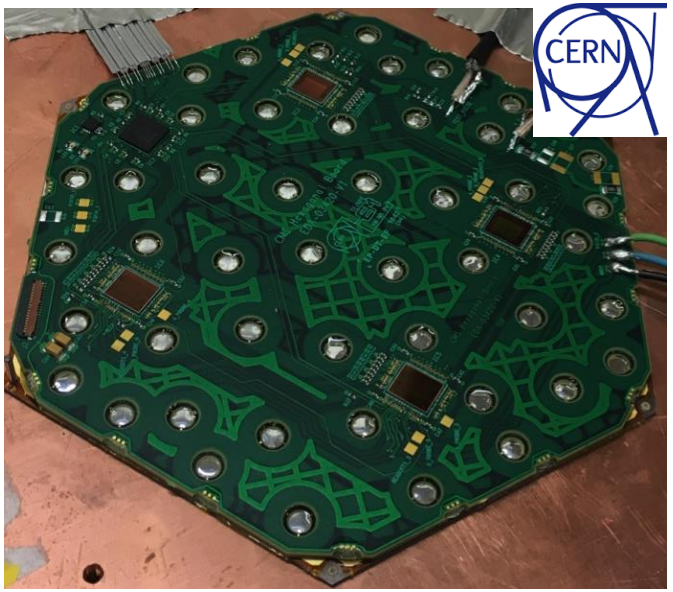


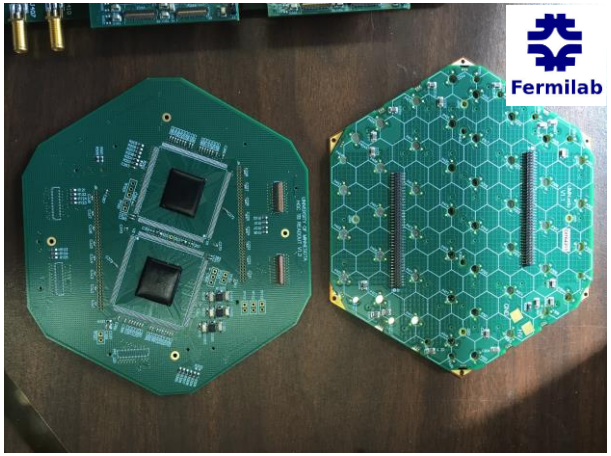
Testbeam setup(s)

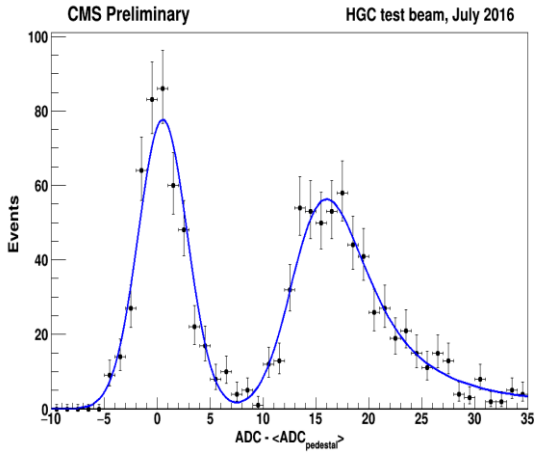
- Boards with SKIROC2 used in 2016 [UCSB, FNAL,UM]
- Hexaboards with SK2_CMS in 2017 [CERN]





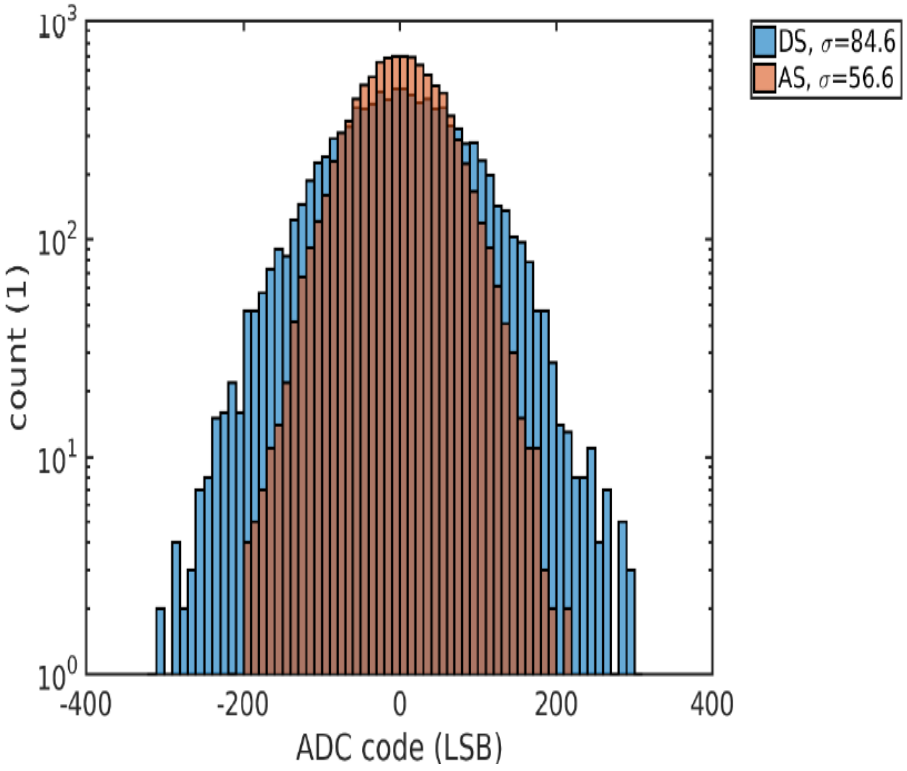


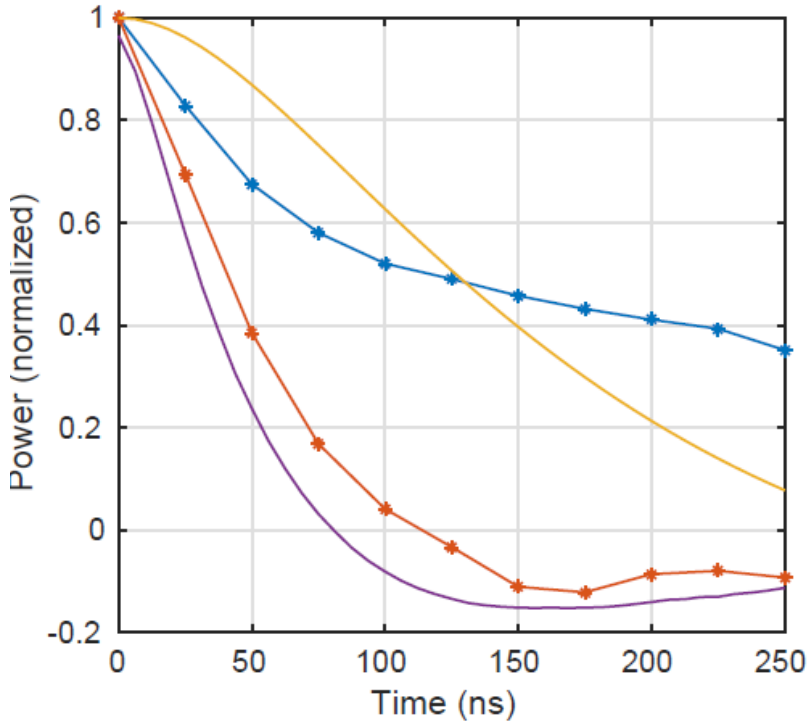




Coherent and incoherent noise

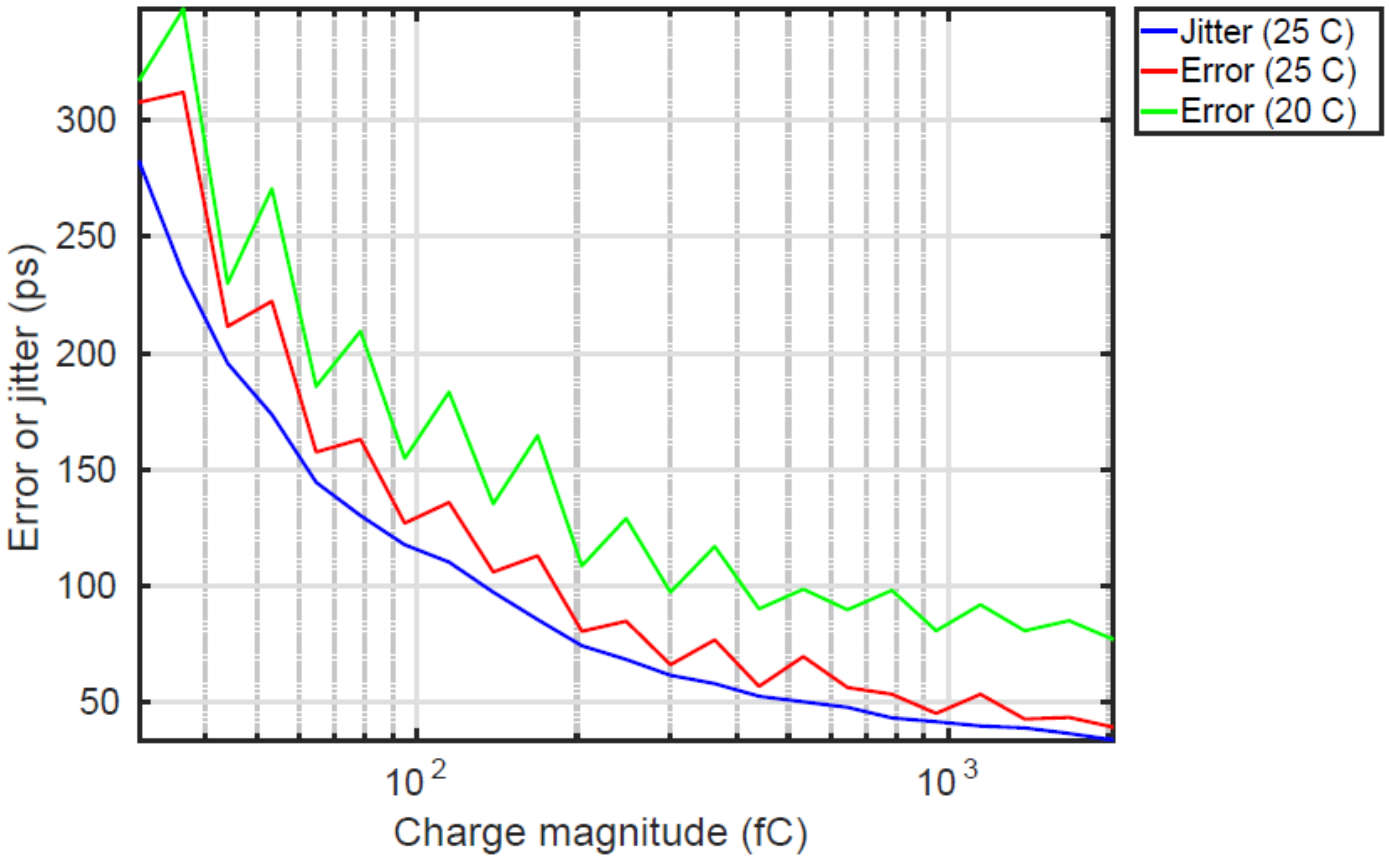
- A constant concern in calorimetry
  - Coherent noise extracted by comparing direct and alternate sums on n channels (n=64) : DS = ∑ ped[i] ; AS = ∑ $(-1)^i$ ped[i]
  - Incoherent noise IN = rms(AS) / √n
  - Coherent noise : CN = $\sqrt{var(DS) - var(AS)}$ / n
- Need to show that CN / IN ~ 10% can be obtained at system level





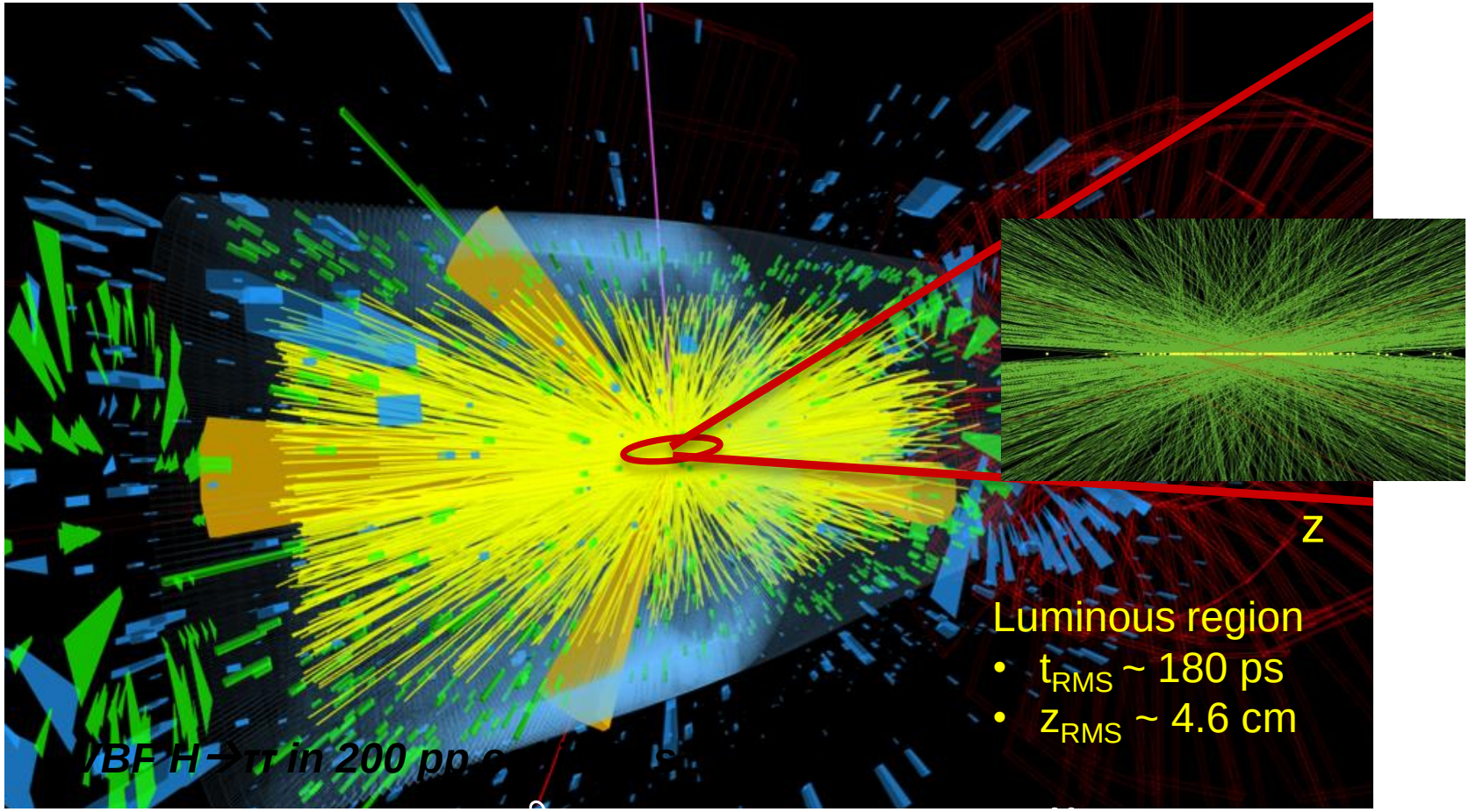
Time of arrival (ToA)

- TOA measured with internal TDC and corrected for time walk
- Constant term = 50 ps
- Noise term = 10 ns / Q(fC) (~4 ns/Q expected)
- What can be obtained at system level ?



Timing at High-Luminosity LHC

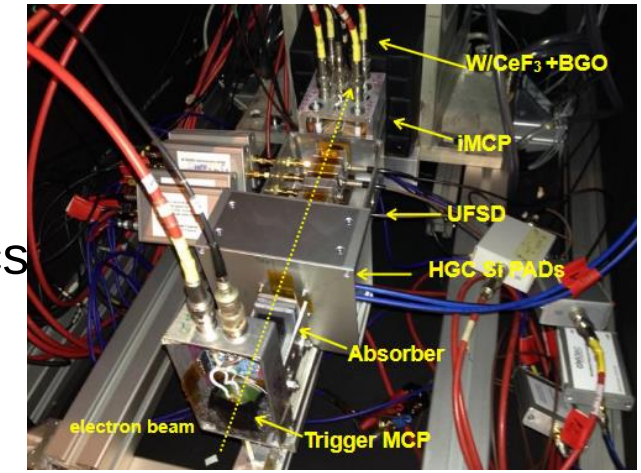
- Pileup mitigation with fine time information (~25 ps)

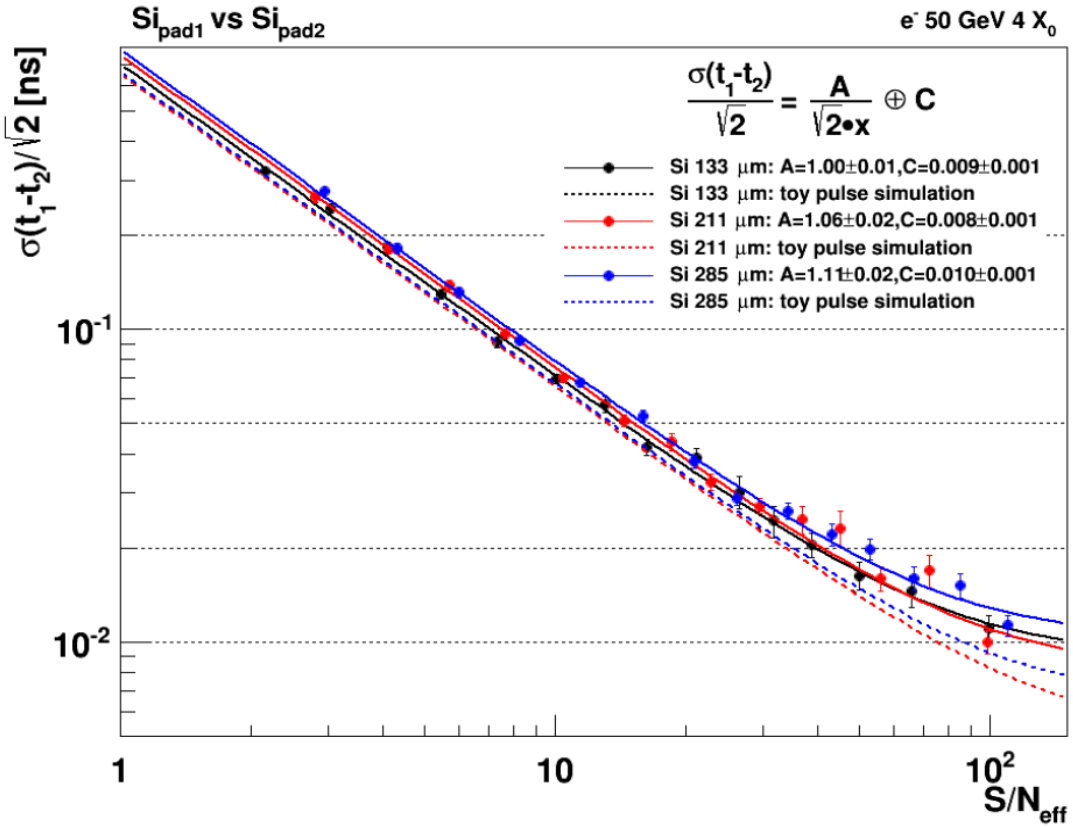


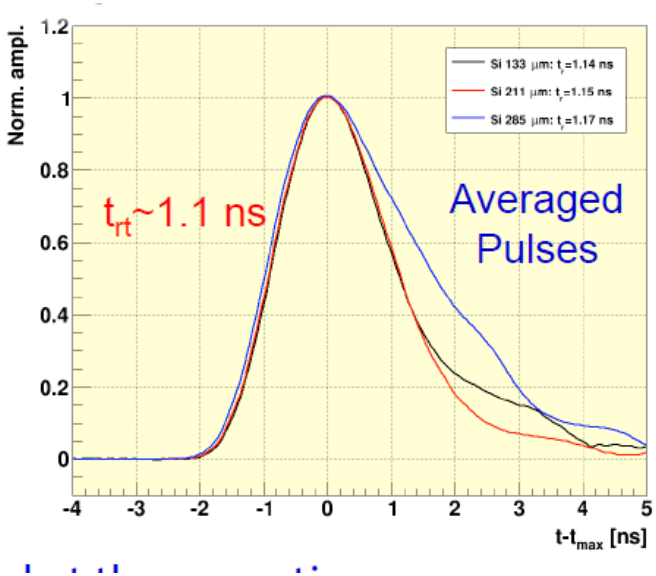
© G. tully CERN seminar on timing
/https://indico.cern.ch/event/633341/

HGCAL timing performance

- CMS HGCAL testbeam measurements
- Jitter : j ~1 ns / S/N
  - But S and N depend on BW…
  - Parts come from detector and from electronics





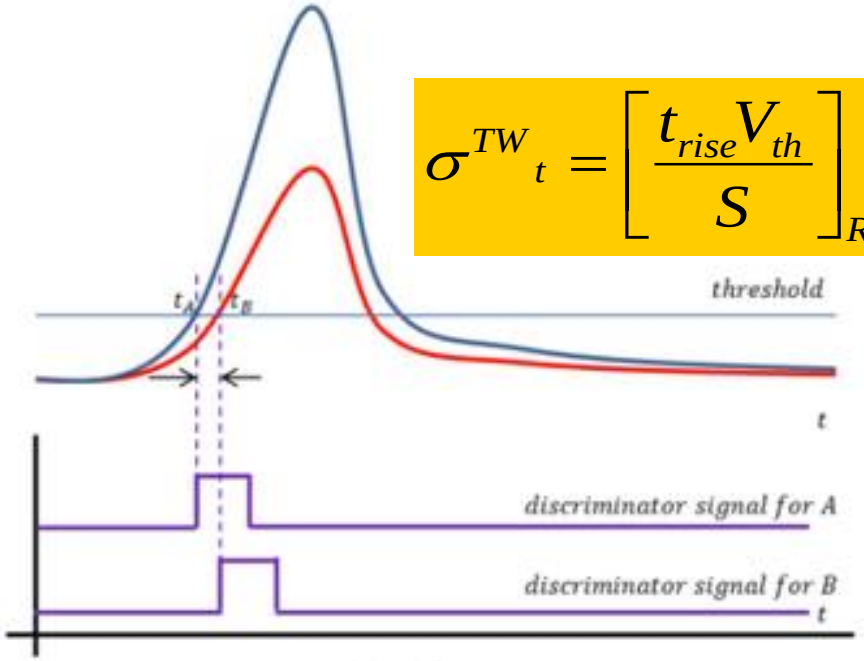


© *M. Mannelli et al. ACES 2016*
https://indico.cern.ch/event/468486

Time walk and Time jitter

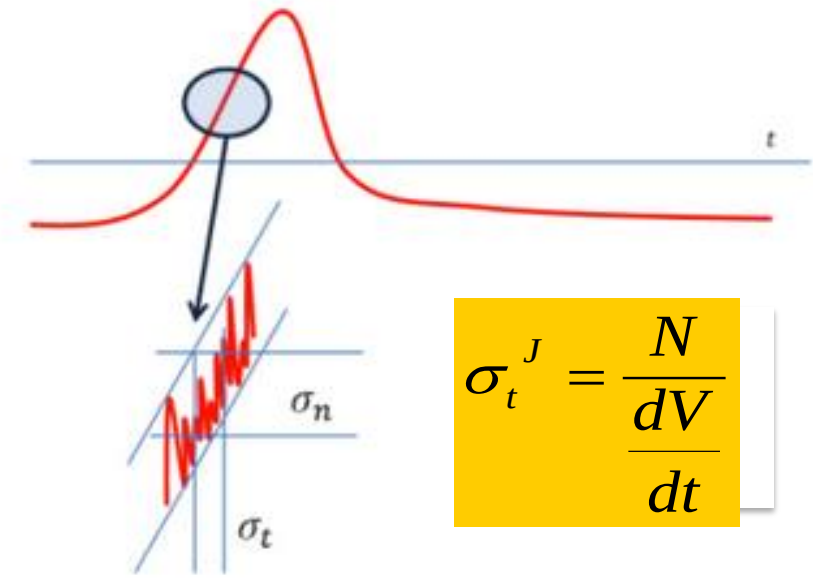
Time walk: the voltage value Vo is reached at different time for signal of different amplitudes

Jitter: the noise is summed to the signal, causing amplitude variations



Time walk effect

$$\sigma^{TW}{}_t = \left[\frac{t_{rise} V_{th}}{S}\right]_{RMS}$$



Jitter effect

$$\sigma_t{}^{J} = \frac{N}{\frac{dV}{dt}}$$

Due to the physics of signal formation

Mostly due to electronic noise

$$\sigma_t^{\,2} = \left(\frac{t_{rise}}{S/N}\right)^2 + \left(\left[\frac{t_{rise} V_{th}}{S}\right]_{RMS}\right)^2 + \left(\frac{TDC_{bin}}{\sqrt{12}}\right)^2$$

Jitter

Time Walk

TDC

Timing optimization : common view

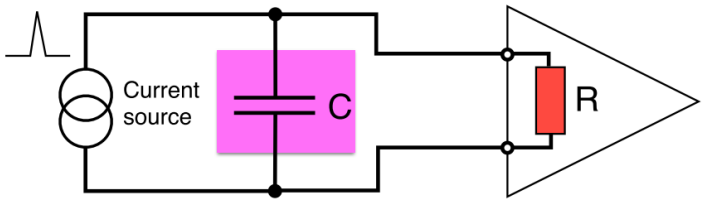
- Jitter due to electronics noise:

$$\sigma_t^J = \frac{N}{\frac{dV}{dt}}$$

- also presented as j = tr / (S/N)
- dV/dt prop to BW, N prop to √ BW => jitter prop to 1/√BW

⇒ « the faster the amplifier the better the jitter ? »

⇒ « High speed preamps need to be low impedance (50 Ω or less) »



NB : tr = $t_{10\text{-}90\%}$ = 2.2 tau.

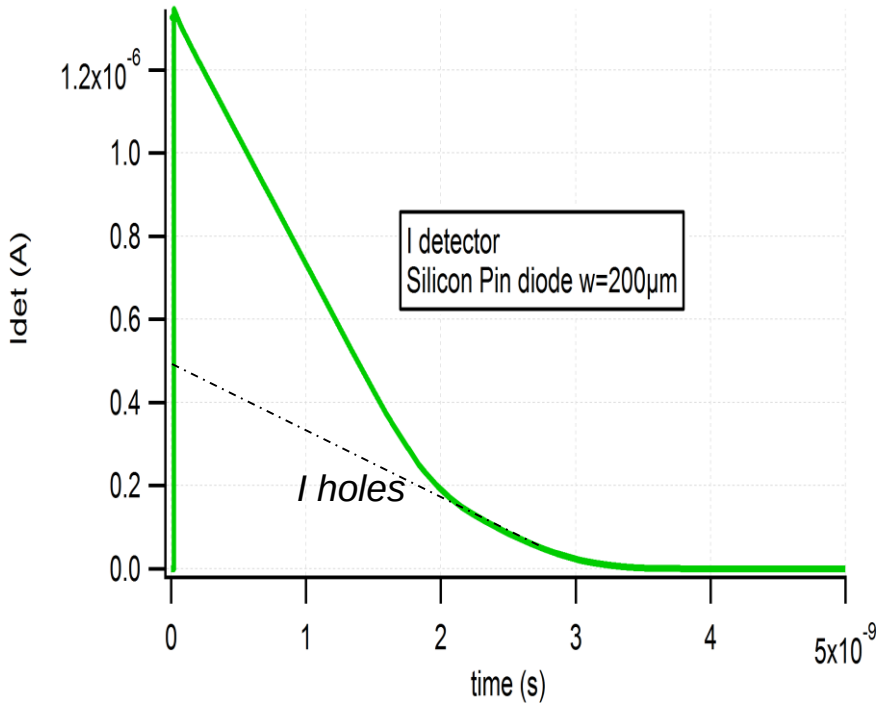
f_{-3dB} = 1/2πtau = 0. 35 / $t_{10\text{-}90}$

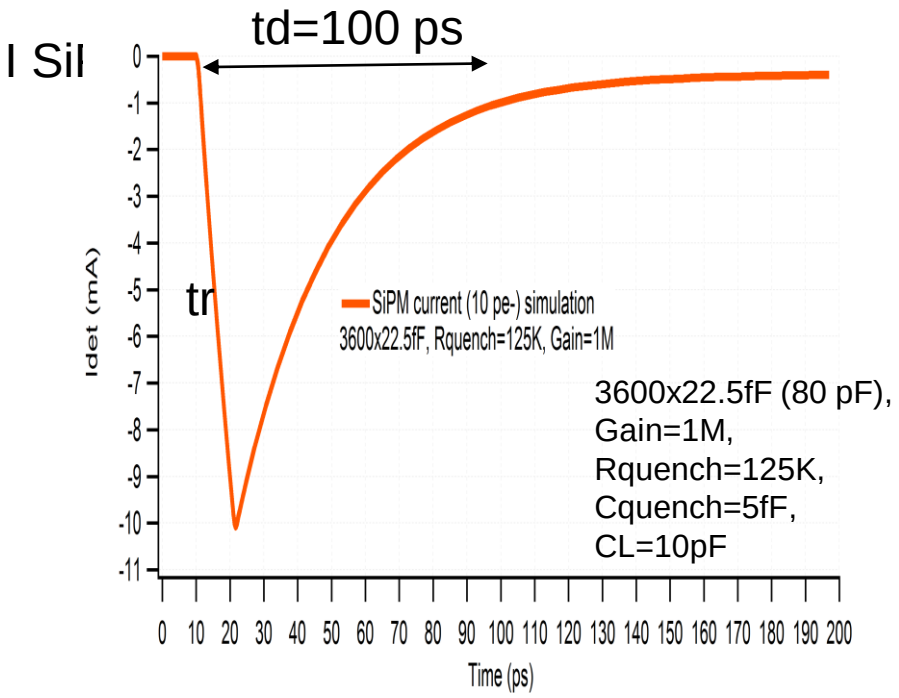
f_{-3dB} = 1 GHz <-> $t_{10\text{-}90\%}$ = 300 ps

Signal : detector current

- PN diode w =200µm
- Very short rise time : tr~10ps
- Relatively long «drift time» : td~2ns

- SiPM detector (10pe-)
- very short rise time : tr~10 ps
- Short duration : td~100ps),

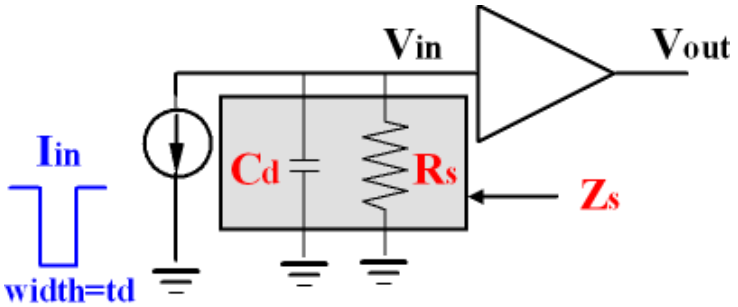


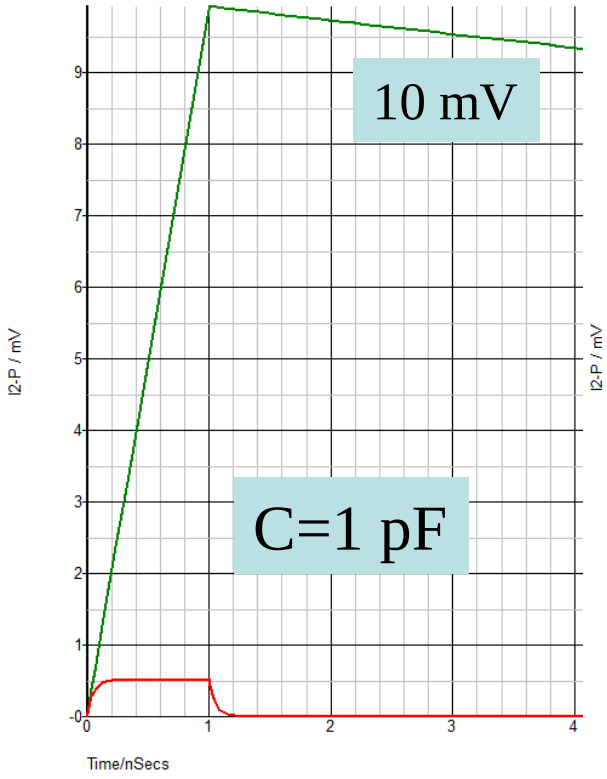


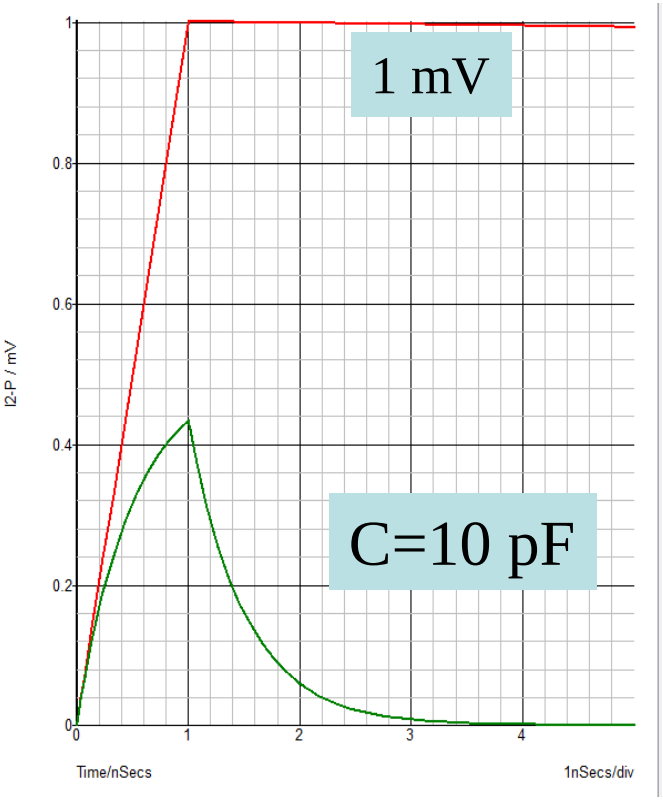
© Harmut Sadrozinski (Santa Cruz) "the beautiful risetime of the detector is spoilt by the electronics"

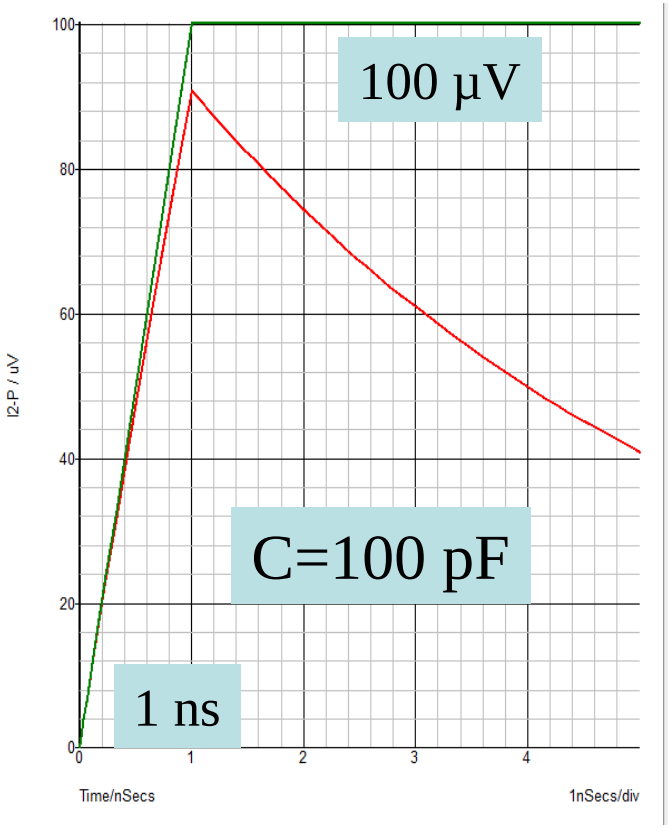
voltage vs current sensitive

- *Example* : 10 fC – 1 ns signal from 1-10-100 pF sensors into 50 Ω (current) or 50k (voltage) preamp



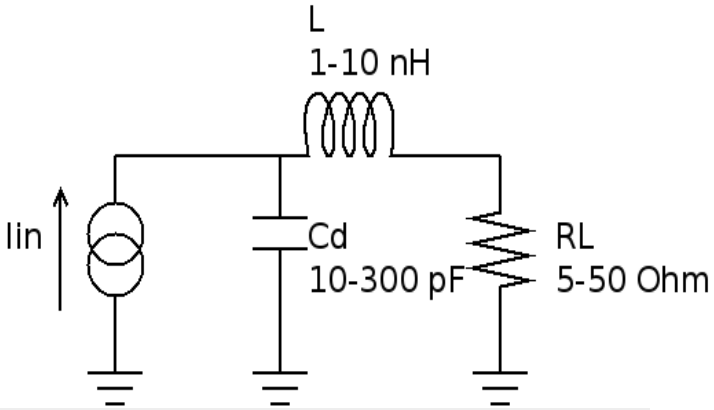


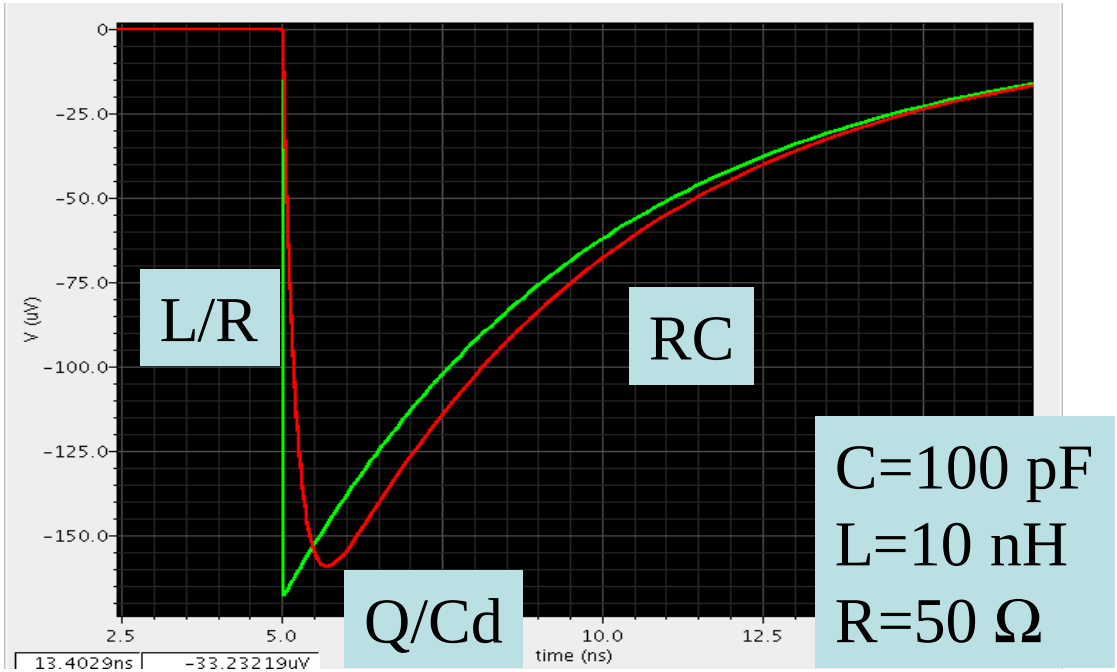


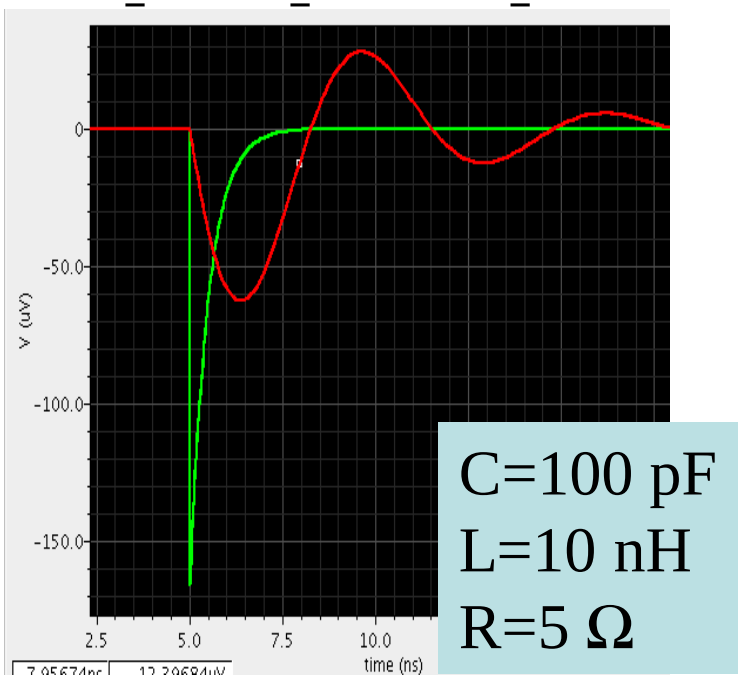


Examples of pulse shapes

- SiPM pulse : Q=160 fC, C_d=100 pF, L=0-10 nH, R_S=5-50 Ω
- Sensitivity to parasitic inductance
- Choice of R_S : decay time, stability
- Small R_S not necessarily the fastest
- Convolve with current shape… (here delta)

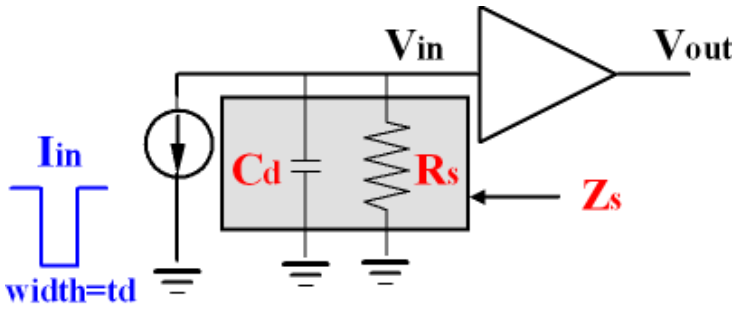




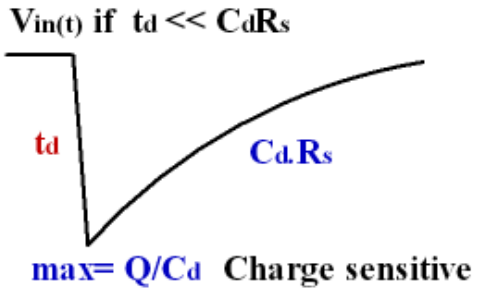


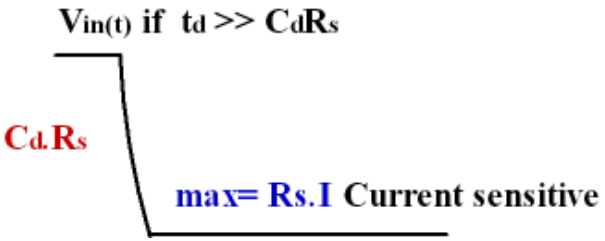
Detector impedance and input voltage

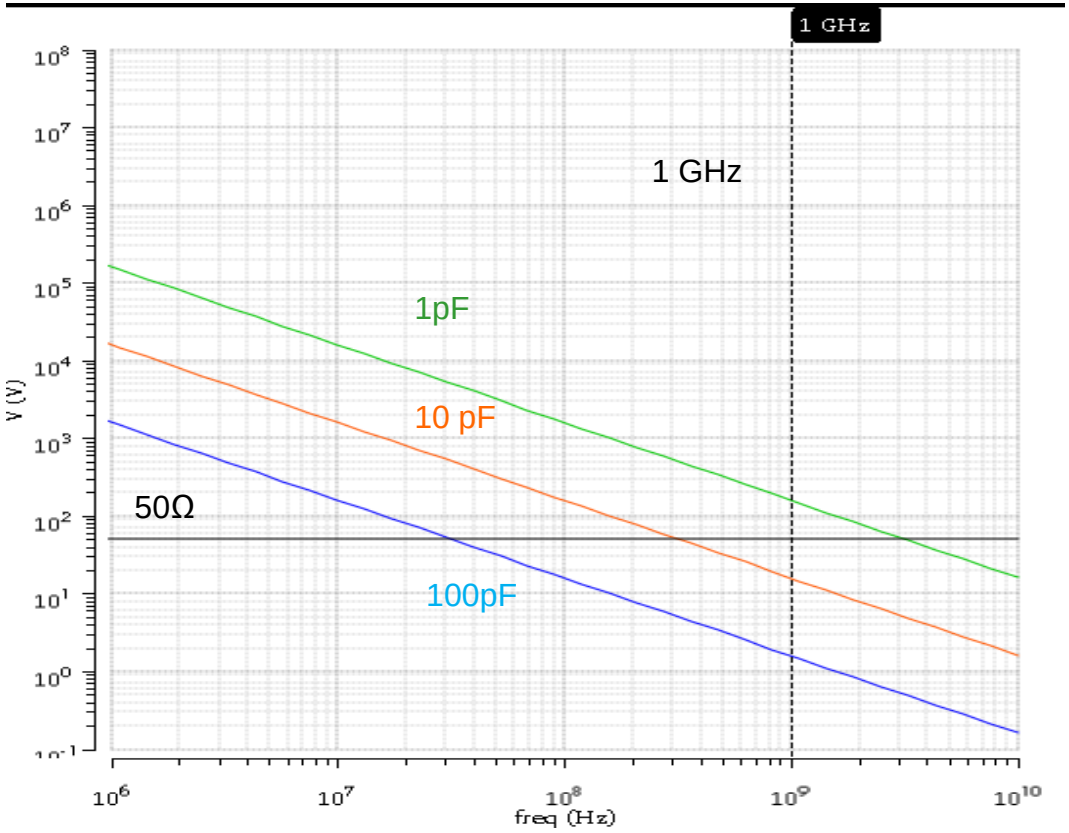
- 1 GHz, Cd=few tens of pF, input signal width <1ns
- Cd>1 pF, Zs@1GHz dominated by Cd
- Rise time: tr= td when td<< $R_S C_d$ and tr= $R_S C_d$ when td>> $R_S C_d$



At HF : difficult to beat the capacitance

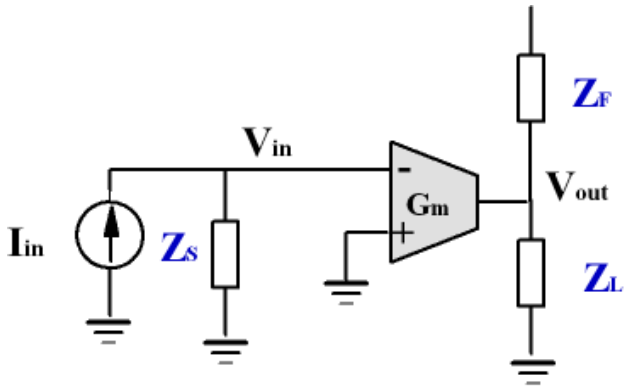




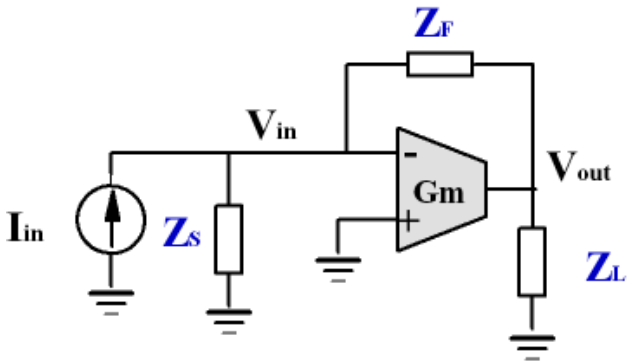


- Response to very short pulse

- Broadband
  - Zin=Rs (50 Ohm)
  - Vin = Q/Cin
  - $V_{OUT} = -G_m R_F \frac{Q_{IN}}{C_d}$



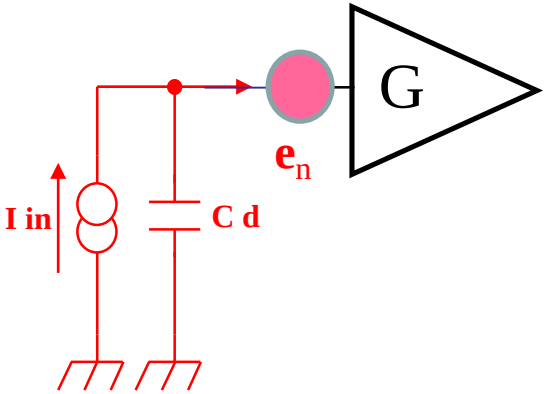
- Transimpedance
  - Zin ~ Zf/G ~ 1/gm
  - $V_{OUT} = \frac{\frac{1}{G_m} - R_F}{1 + j\omega\frac{C_d}{G_m}} I_{IN} \approx -G_m R_F \frac{Q_{IN}}{C_d}$



- Same response at High Frequency

Signal and noise in Broadband amplifiers

- Signal of duration t_d, across capacitance Cd with BB amplifier of impedance R_S



- Signal scales as 1/ C_d if $R_S C_d >> t_d$ and $C_{PA} << C_d$

$$S = V_{OUT} = G\frac{Q_{IN}}{C_d}$$

- Rise time is the convolution of signal duration t_d and amplifier risetime $t_{10\text{-}90\_PA}$

$$t_r \approx \sqrt{t_{10-90\_PA}^2 + t_d^2}$$

- Noise is given by the preamp noise density e_n and bandwidth

$$N = G.e_n\sqrt{\frac{\pi}{2}BW} = \frac{G.e_n}{\sqrt{2t_{10-90\_PA}}}$$

- Jitter is then :

$$\sigma_t^{\ J} = \frac{N}{dV/dt} = \frac{e_n C_d}{Q_{in}}\sqrt{\frac{t_{10-90\_PA}^2 + t_d^2}{2t_{10-90\_PA}}}$$

Jitter in Broadband amplifiers

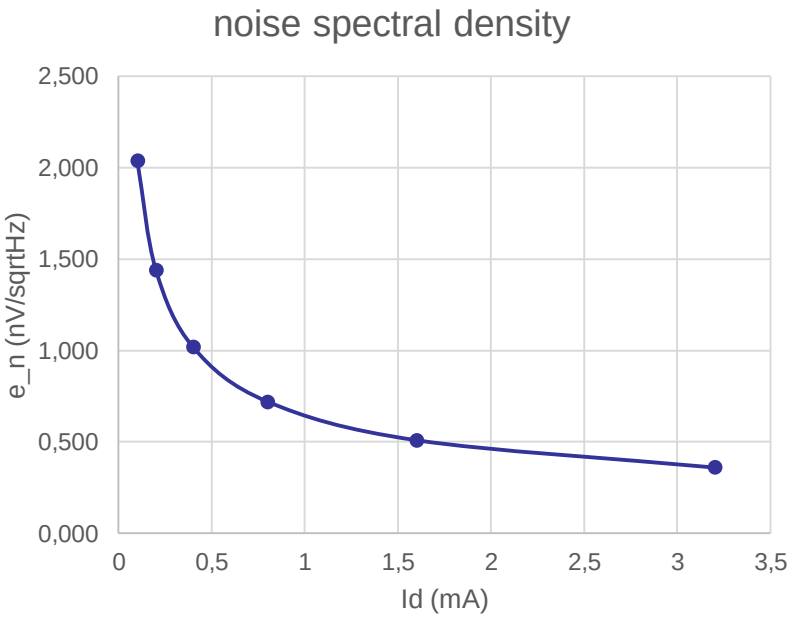
- Optimum value: $t_{10\text{-}90\_PA} = t_d$ (current duration)

$$\sigma_t^{\ J} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

Dominated by sensor
Electronics only gives e_n

- Electronics noise e_n given by input transistor transconductance g_m :
  - Typically ~1 nV/√Hz at I_D = 0.5 mA
  - Scales with the square root of current in transistor (weak inversion)

$$e_n = \sqrt{\frac{2kT}{g_m}} \approx \frac{2kT}{\sqrt{qI_D}}$$



Examples

$$\sigma_t^{\ J} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

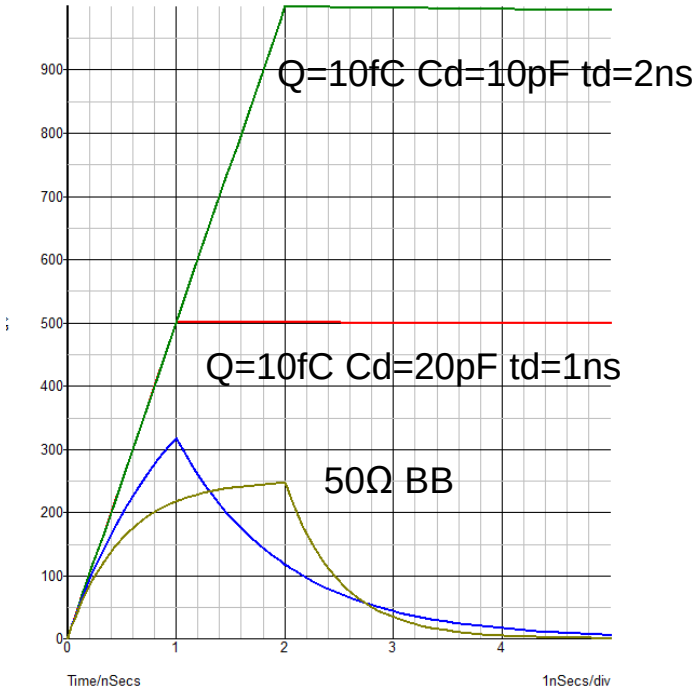
- CMS HGCAL : PIN diode thickness 300 µm A=25 mm²
  - C_d = 8 pF e_n = 1 nV/√Hz t_d = 3 ns σ = 420 ps/Q(fC)
  - 1 MIP = 3.8 fC => σ = 110 ps/#MIP (~200 ps measured)
- NA62 tracker : PIN diode thickness 300 µm A=0.09 mm²
  - C_d = 0.1 pF e_n = 11 nV/√Hz t_d = 3 ns σ = 60 ps/Q(fC)
  - 1 MIP = 3 fC => σ = 20 ps/#MIP (~60 ps measured)
- ATLAS HGTD : LGAD diode thickness 50 µm A= 2 mm² G = 10
  - C_d = 2 pF e_n = 2 nV/√Hz t_d = 0.5 ns σ = 50 ps/Q(fC)
  - 1 MIP = 5 fC (G=10) => σ = 10 ps/#MIP (~30 ps measured)
- SiPM G = 1^E6
  - C_d = 300 pF e_n = 1 nV/√Hz t_d = 100 ps σ = 3 ns/Q(fC)
  - 1 pe = 160 fC => σ = 20 ps/#pe (~60 ps measured)

Expected jitter with thickness

- Evaluate jitter(Q) with thickness (th)
  - At given Q, C_d ~1/th, t_d ~ th, expect j ~ 1/√th
  - dV/dt = Q / C_d.t_d = Cte
  - Better jitter : longer signal, smaller BW
  - Not seen in testbeam setup because 50 Ω amplifier not optimum at low capacitance
- Jitter(MIP) even better because more charge
- But more Landau fluctuations…

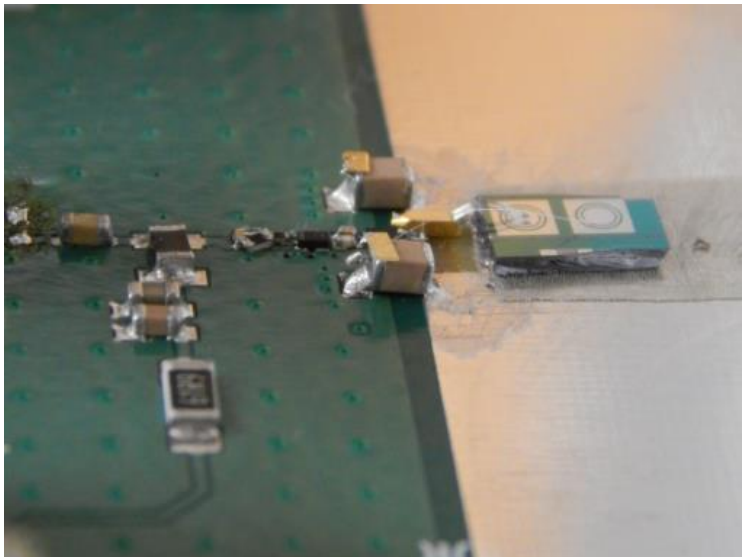
$$\sigma_t^J = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

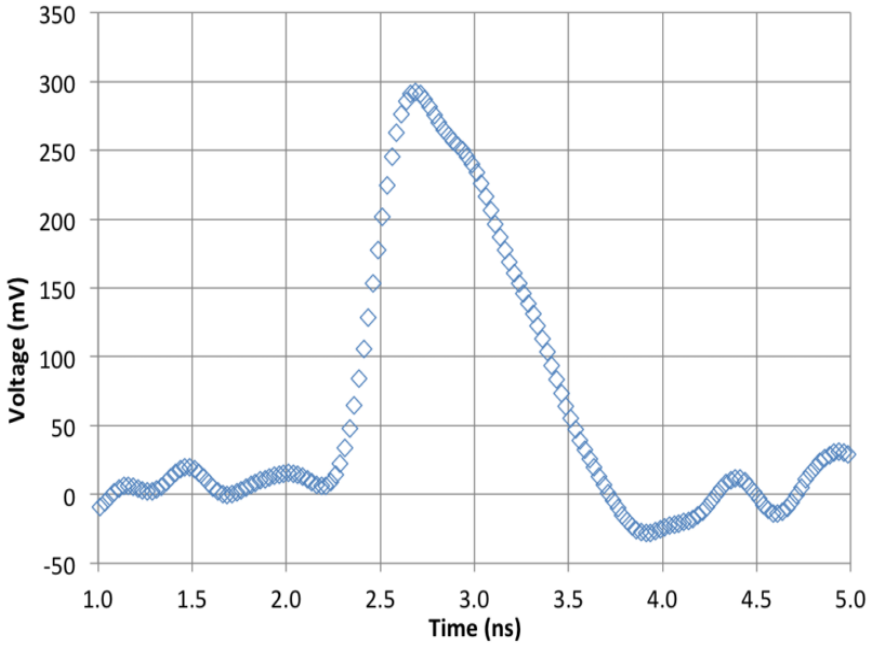
CMS	100um calc	200um calc	300um calc	200um meas
th (µm)	100	200	300	210
Cd (pF)	23	12	8	14
fC/MIP	1,3	2,6	3,8	2,7
en (nV/√Hz)	1	1	1	
td (ns)	1	2	3	
jitter/Q(fC)	727	514	420	1021
jitter/MIP	568	201	109	380

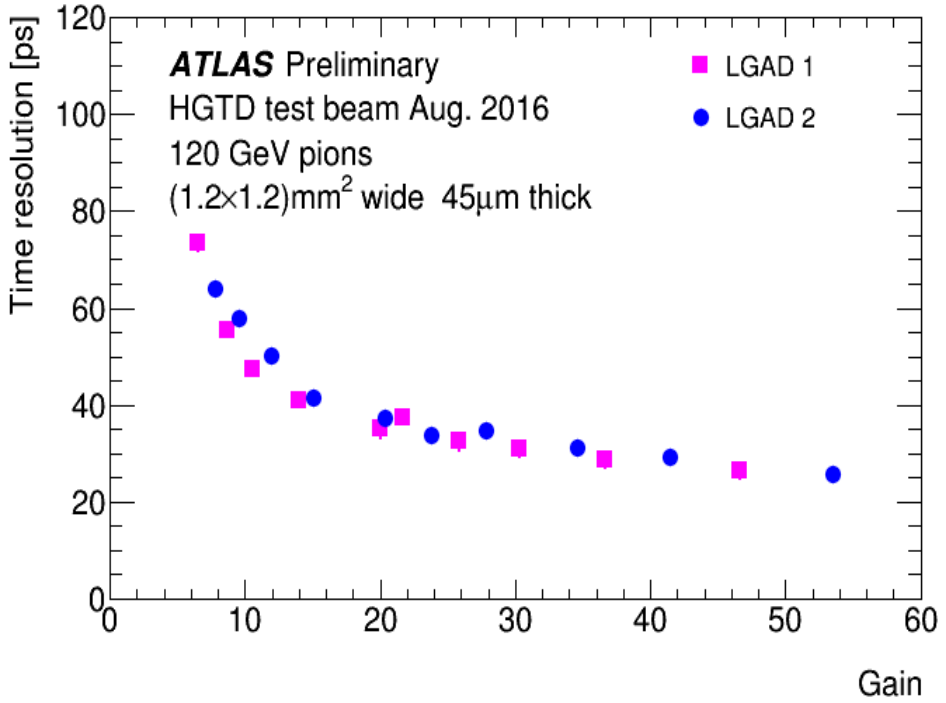


LGAD with SiGe hybrids

- 2 mm² LGAD 50 µm thick
- SiGe discrete readout BW = 2 GHz
- Jitter measured : j = 200 ps / Q(fC)
  - MIP = 4.6 fC at G = 10, t_d = 0.5 ns, C_d = 2 pF, e_n = 1 nV/√Hz
  - Theory : j = 50 ps/Q(fC)
- ATLAS HGTD will use 2 mm² LGADS for ~30 ps timing with G = 10-20







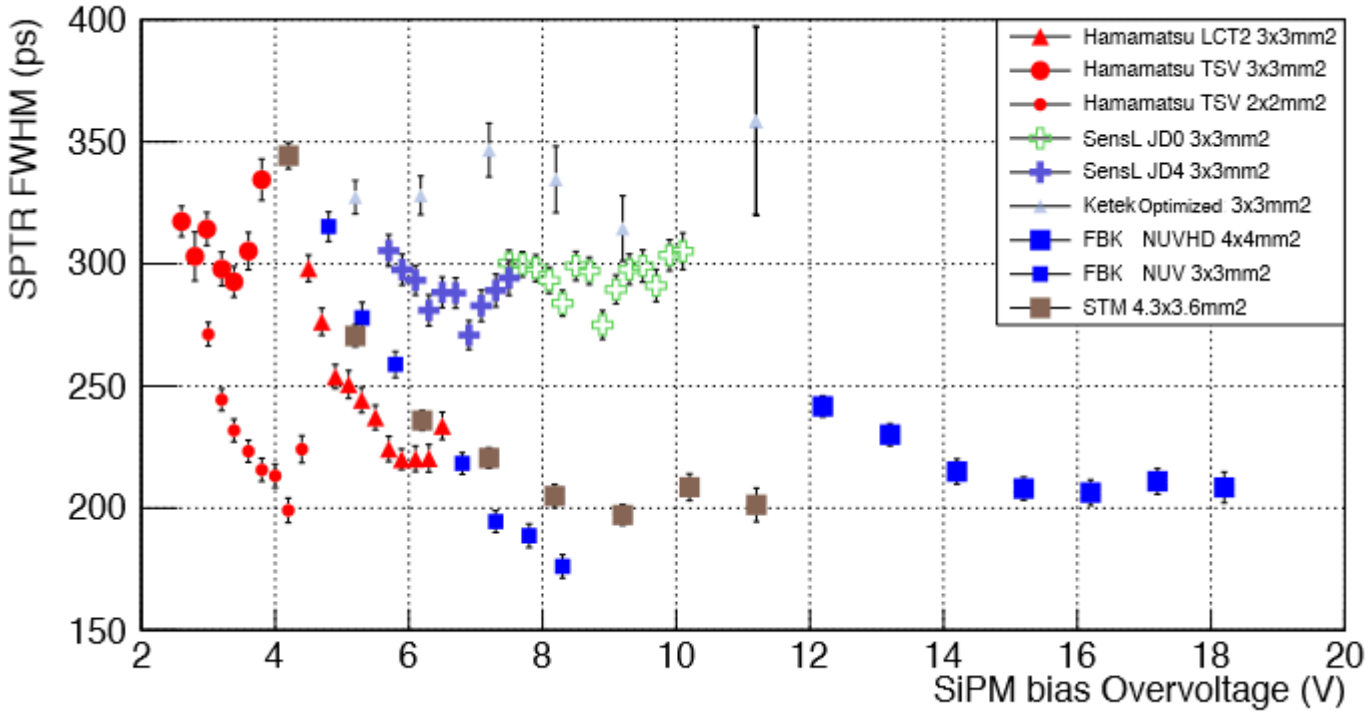
With SiPMs : SPTR [JINST 11 P10016]

- SPTR
  - FWHM ~200 ps
  - Rms ~ 80 ps

Single photon time resolution of state of the art SiPMs

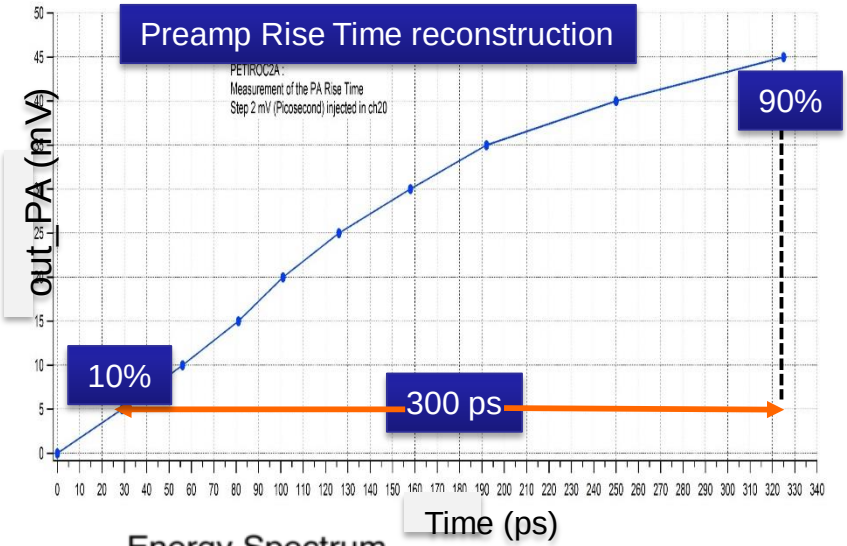
M.V. Nemallapudi,[1] S. Gundacker, P. Lecoq and E. Auffray

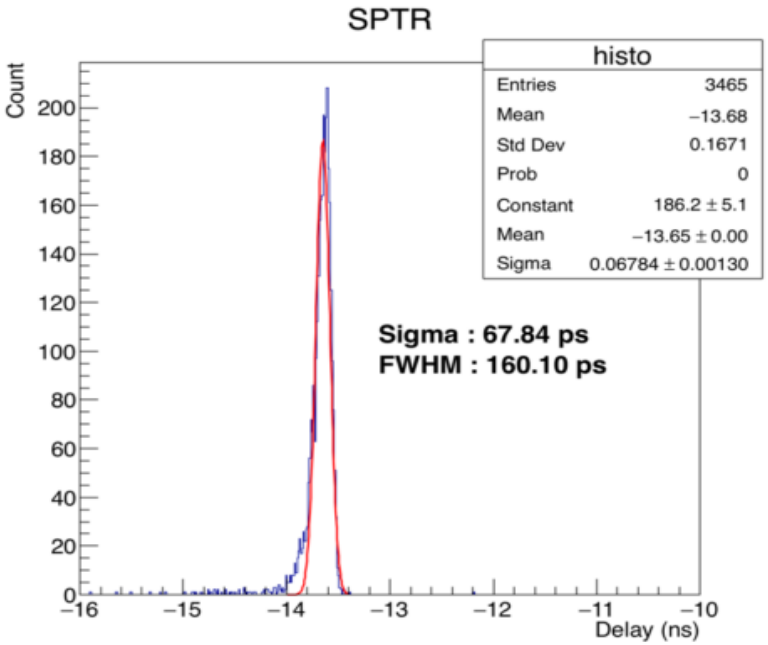
CERN,
23 Rue de Meyrin, Geneva, 1211-CH

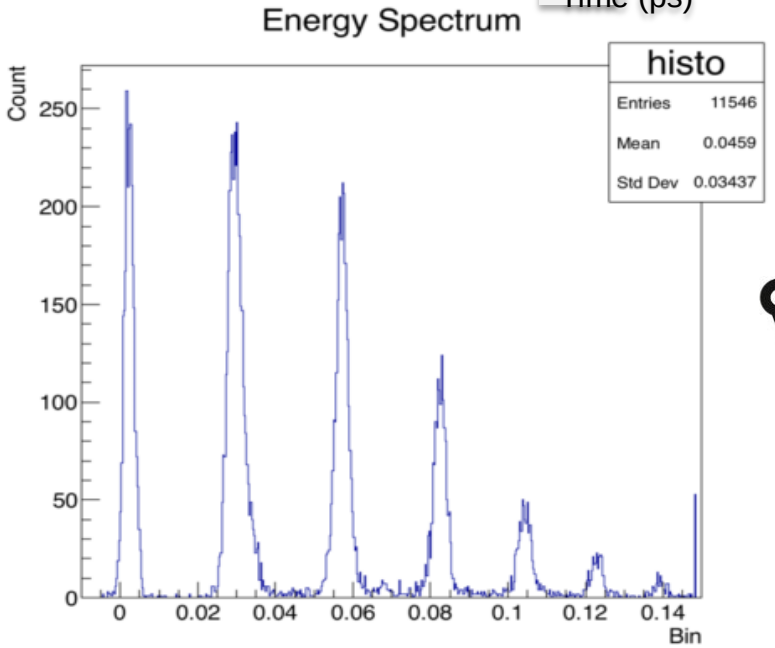


Going to lower SPTR

- Expect ~ 20 ps/pe
- NINO risetime ~1 ns
- Test with PETIROC2 (tr = 300 ps)
  - SPTR = 67 ps rms (180 ps FWHM)
- Possible effect of stray inductance
- Furhter studies in FAST framework







weeroc

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Summary

- Imaging calorimeters ramping up !
  - Require highly integrated R/O electronics : System On Chip
  - Low power, low noise, high speed, large dynamic range
  - Timing capability down to a few tens of ps
  - Lots of system issues

- Timing performance dominated by sensor characteristics
  - Capacitance, duration, MIP charge
  - Theory predicts :
  - Electronics affects only $g_m \sim Id/2U_T$

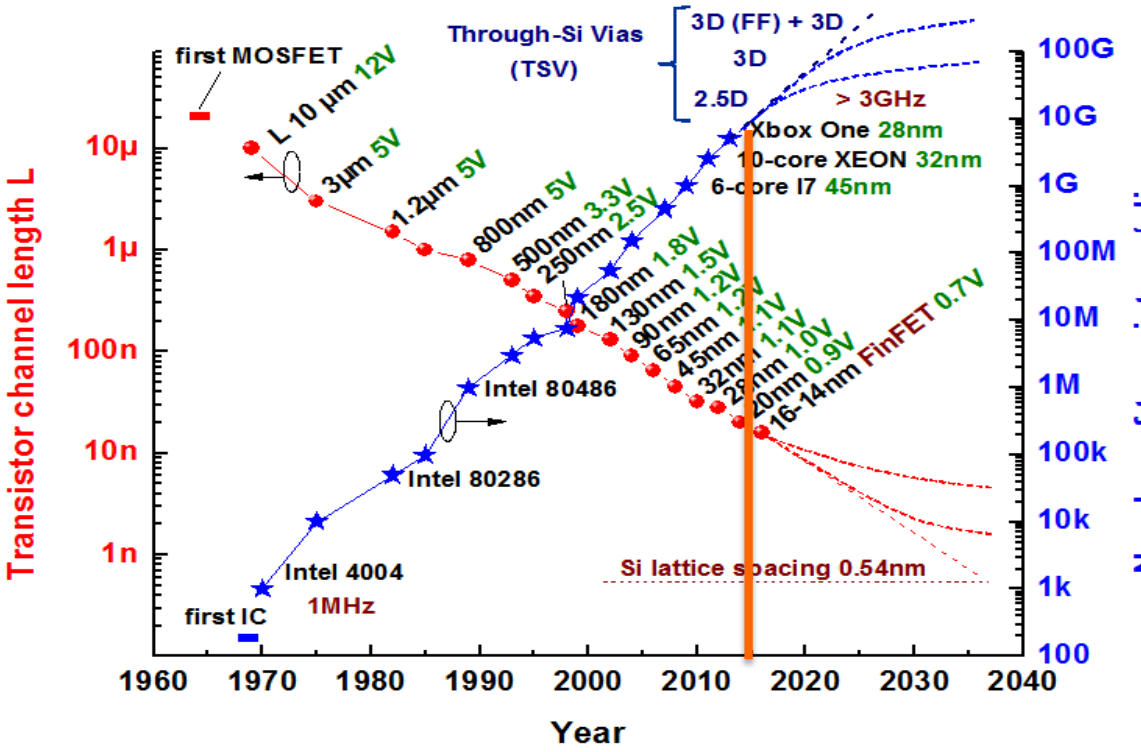
$$\sigma_t^{\ J} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

- Work getting organized towards 10 ps (1 ps ?) timing

backup

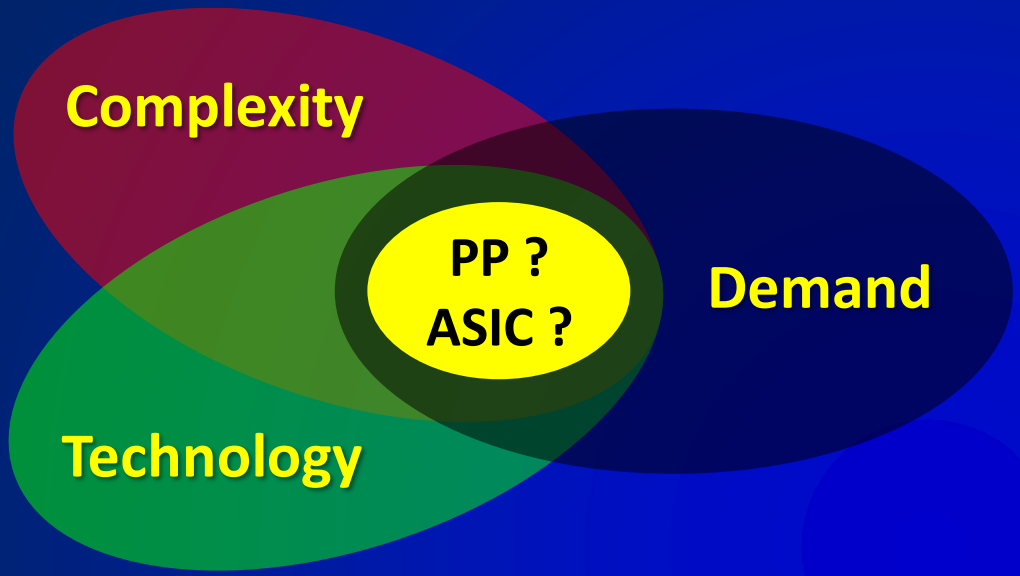
Evolution of technologies

- More and more functions are integrated inside chips (ASICs)
- Evolution of technologies make them more and more performant but more and more complex
- Cost increases …
  - MPW costs :
  - 350 nm : 1 k€/mm²
  - 130 nm : 2 k€/mm²
  - 65 nm : 6 k€/mm²
- Chip size also…
- CERN targets 65/130 nm
- SiGe in AIDA2020



10 ans d'évolution des spécifications techniques pour la réalisation

The PP-ASIC Paradigm



Collaborations ?
- only part of the solution
- communication
- overhead
- lead of large group

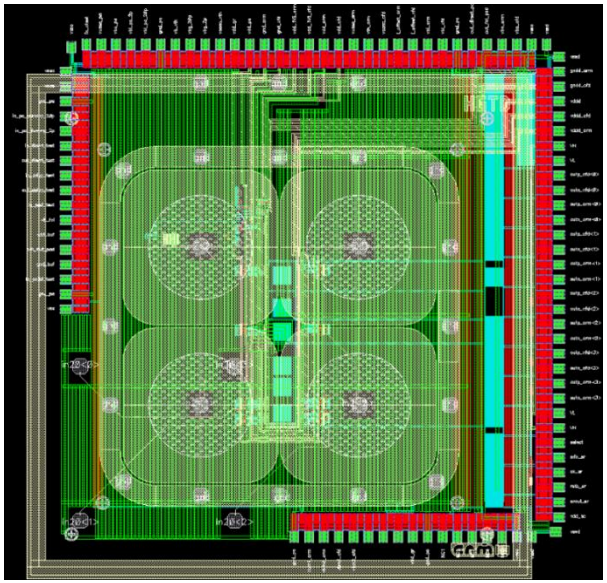
The number of ASIC designers has to increase !

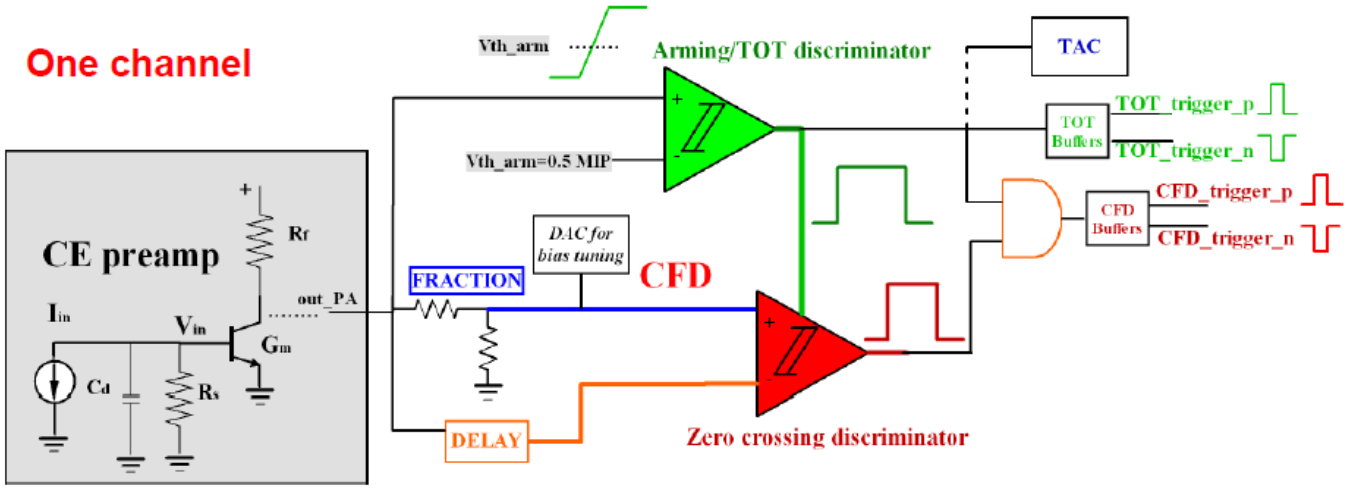
involve non-PP ASIC groups

increase size of PP ASIC groups

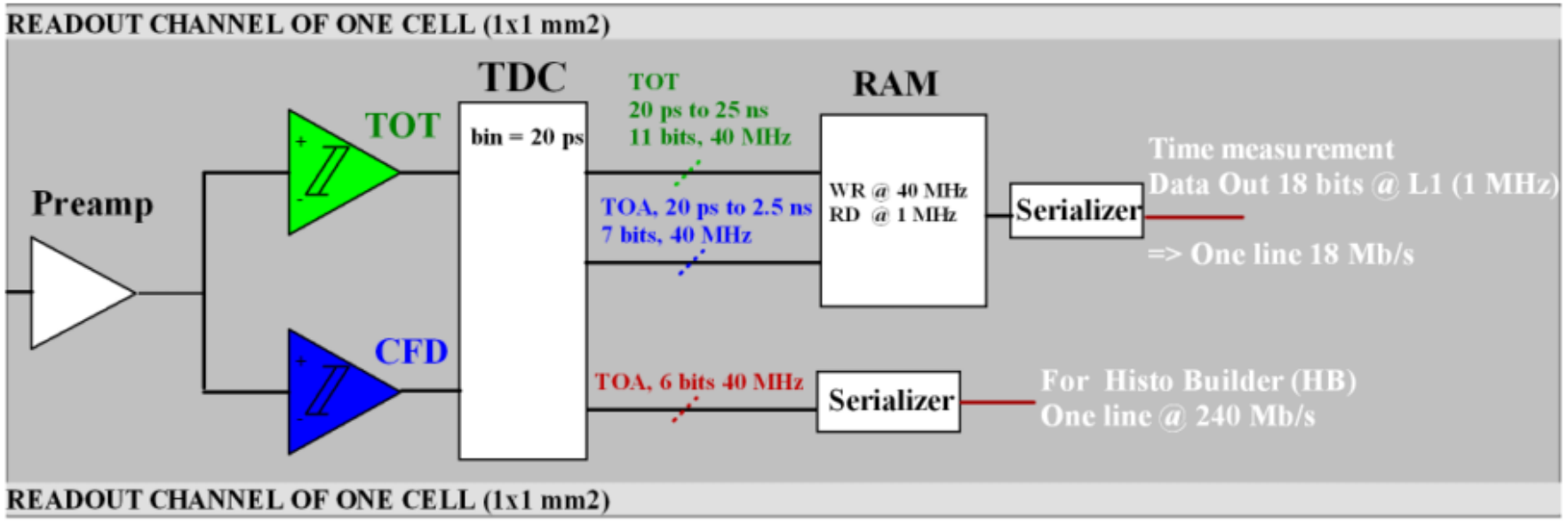
ALTIROC

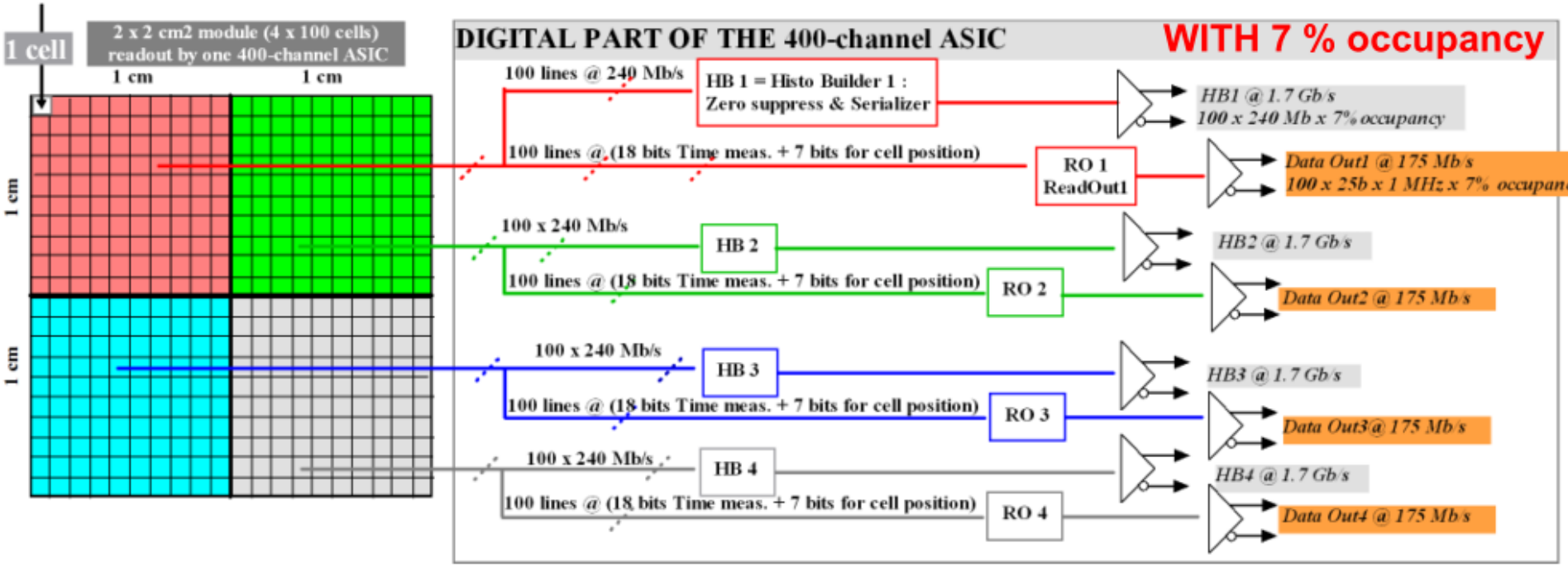
- ALTIROC = ATLAS LGAD Timing ROC
  - 20 ps timing measurement with LGAD sensors for ATLAS HGTD
  - Jitter : j = 110 ps/Q(fC) @ Cd=2 pF
  - Test chip bondable to sensors of 1x1 mm² and 2x2 mm², submitted in dec 16 in TSMC 130n
  - High speed preamp (1 GHz) + constant fraction discriminator (20 ps)
- Will evolve to 400 ch chip
  - With internal TDC, bump bonded to sensor. Collaboration with SLAC





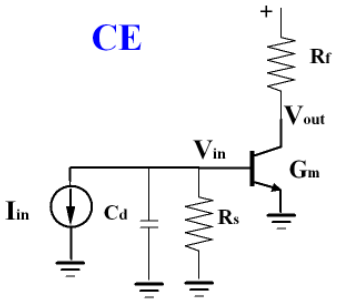
HGTD architecture

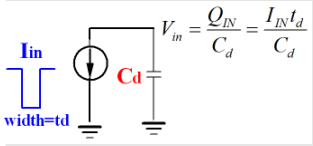




CE in SiGe 130nm and in TSMC 130 nm

- Broad Band amplifier CE configuration
- Same current (Ic=700 µA), same Rf=4K, vdd=1.2V
- Higher gain with SiGe but larger noise due to rbb'



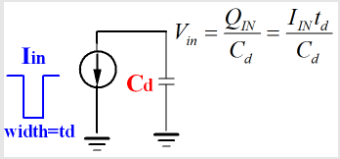
	CE 10pF TSMC 130 nm	CE 10pF SiGe 130nm Trans size= 20
td=10ps Qin=Iin.td= 100µA.10ps=**1fC** 	out=3.7mV tr=220ps BWa=1.6 GHz rms=1.3 mV S/N=2.8 σj=220ps/2.8=78 ps	out=8.95 mV tr=176 ps BWa= 2GHz rms=3.14mV S/N=2.85 σj=176ps/2.85=60 ps
td=1ns and tr_ampli=td CL=100fF Qin= 1µA.1ns=**1fC**	out=3.52mV(CL=100fF) tr=1.1ns BWa=440MHz rms=0.66mV S/N=5.3 σj=1100ps/5.3=206 ps	out=7.5mV (CL=110fF) tr=1.1 ns BWa=440MHz rms=1.4 mV S/N=5.4 σj=1.1ns/5.4=204 ps

CE in TSMC 130 nm: jitter vs tr (BW) and td

- With I source trans (0 for 2 pF or 1.8mA)
- Follower (connected to a discriminator)
- Normalization to 1 fC, square pulse.
- LGAD signa would give 6 fC/MIP

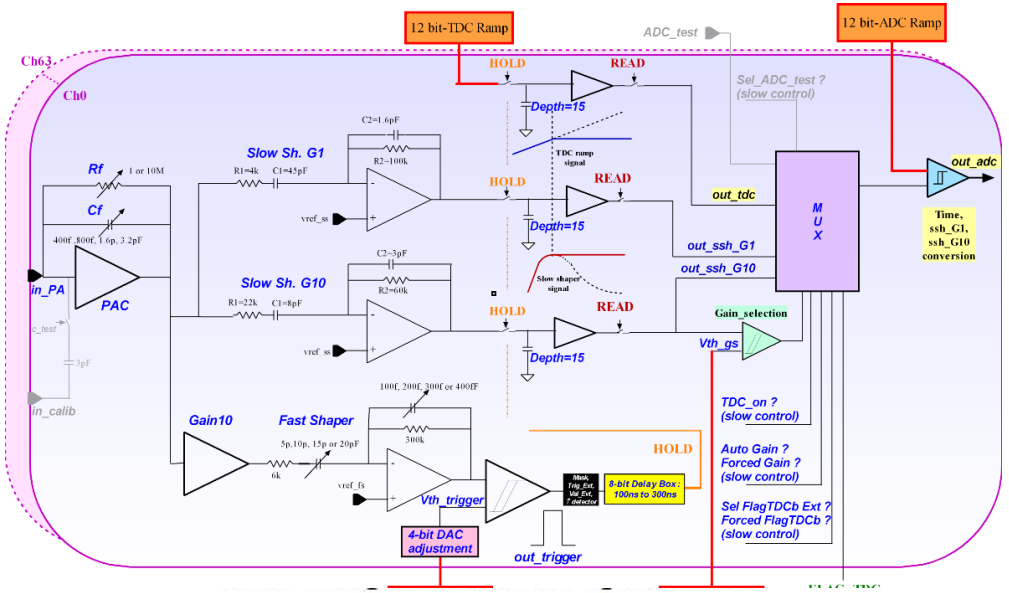
$$\sigma_t^J = \frac{\sigma_N}{\frac{dV}{dt}} = \frac{t_r}{\frac{S}{N}} = \frac{\sqrt{t_{r\_ampli}^2 + t_d^2}}{\frac{S}{N}}$$

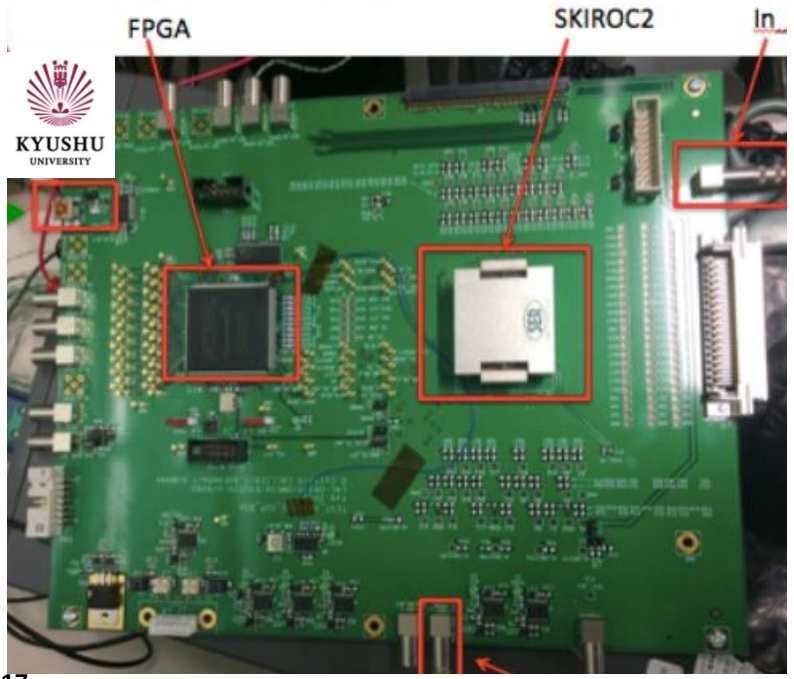
POWER: 0.5mW/ mm²

CE	Cd=2pF (Id=220 µA)	Cd=20pF (Id=2.1 mA)
td=10ps Qin=Iin.td= 100µA.10ps=**1fC** 	out = 6.9 mV out_fol=6.1 mV tr_fol=284 ps BWa=1.2 GHz rms=0.485 mV S/N=12.6 σj=284ps/12.6=23 ps	out=3.37 mV out_fol=3.1 mV tr_fol=290 ps BWa=1.2 GHz rms=1.2 mV S/N=2.6 σj=290ps/2.6=110 ps
td=1ns and tr_ampli=td CL=100fF Qin= 1µA.1ns=**1fC**	out=6.4 mV out_fol=5.9 mV tr_fol=1.1ns BWa=410 MHz rms=0.39 mV S/N=15 σj=1.1ns/15=73 ps	out=3.2 mV out_fol=3.05 mV tr_fol=1.1 ns BWa=440 MHz rms=0.8mV S/N=3.8 σj=1.1ns/3.8=288 ps

SKIROC2_CMS for HGCAL

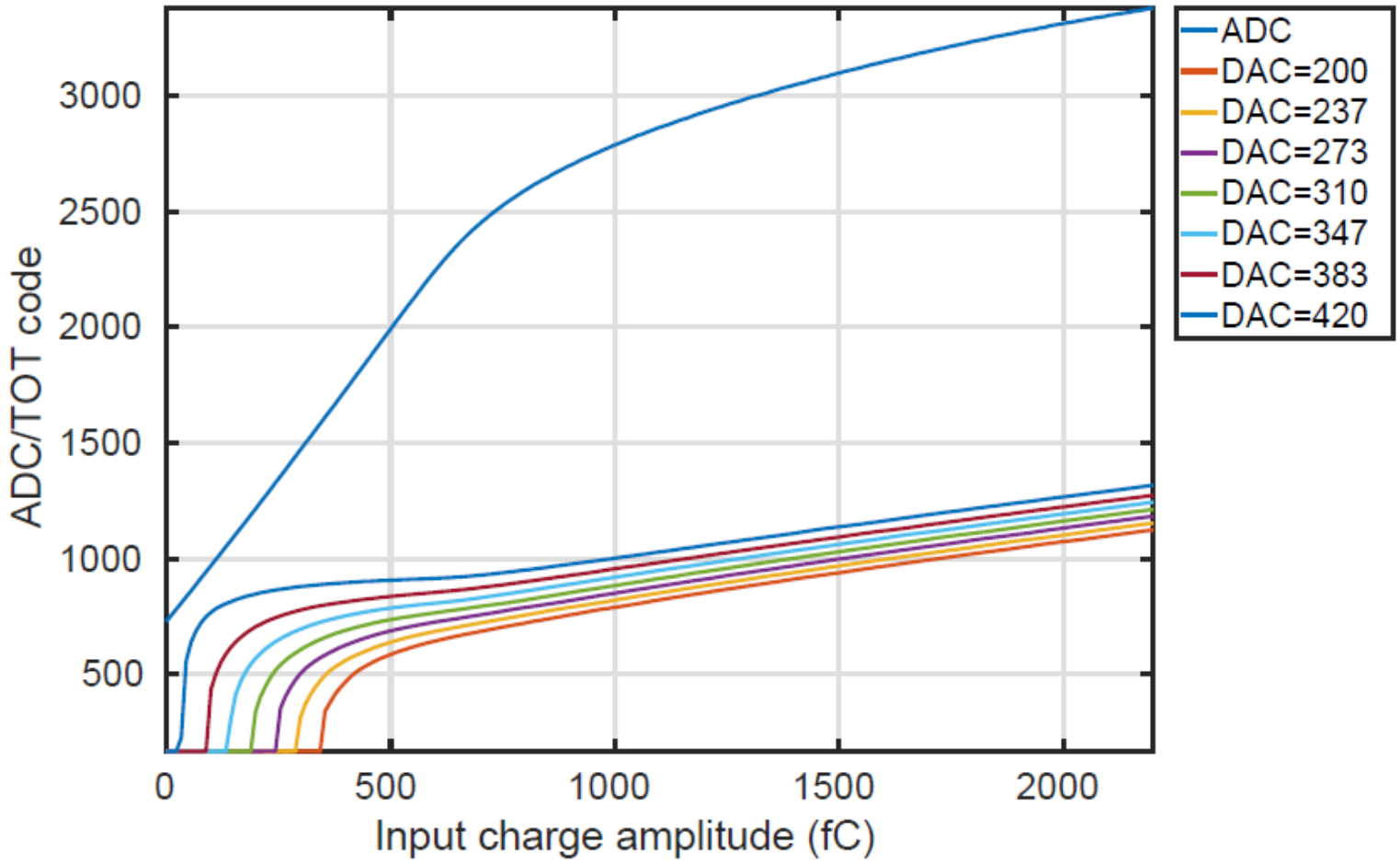
- new SKIROC2 for CMS
  - Optimized version for CMS testbeam, pin to pin compatible
  - Dual polarity charge preamplifier
  - Faster shapers (25 ns instead of 200 ns)
  - 40 MHz circular analog memory, depth= 300 ns
  - TDC (TAC) for ToA and ToT , accuracy : ~50 ps
  - Submitted jan 2016 SiGe 350nm
- Tests :
  - First tests on BGA testboards
  - 4-5 boards will be equipped





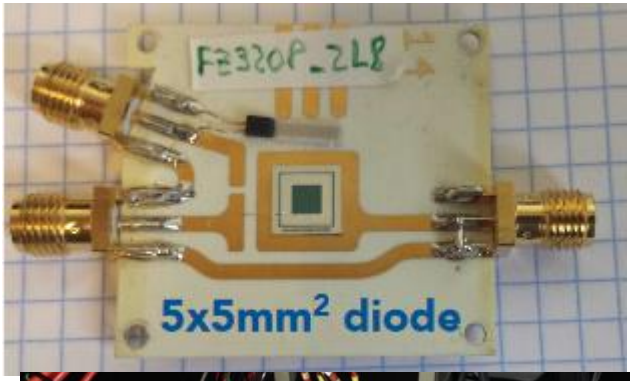
Time over Threshold (ToT)

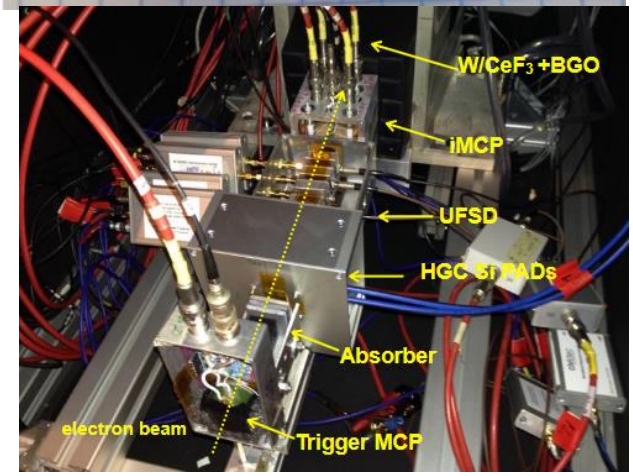
- TOT measured in current sensitive config : Rf=20k Cf=300f
- ADC range : 0-500 fC TOT above
- energy reconstruction around 500 fC, calibration, pedestal evaluation

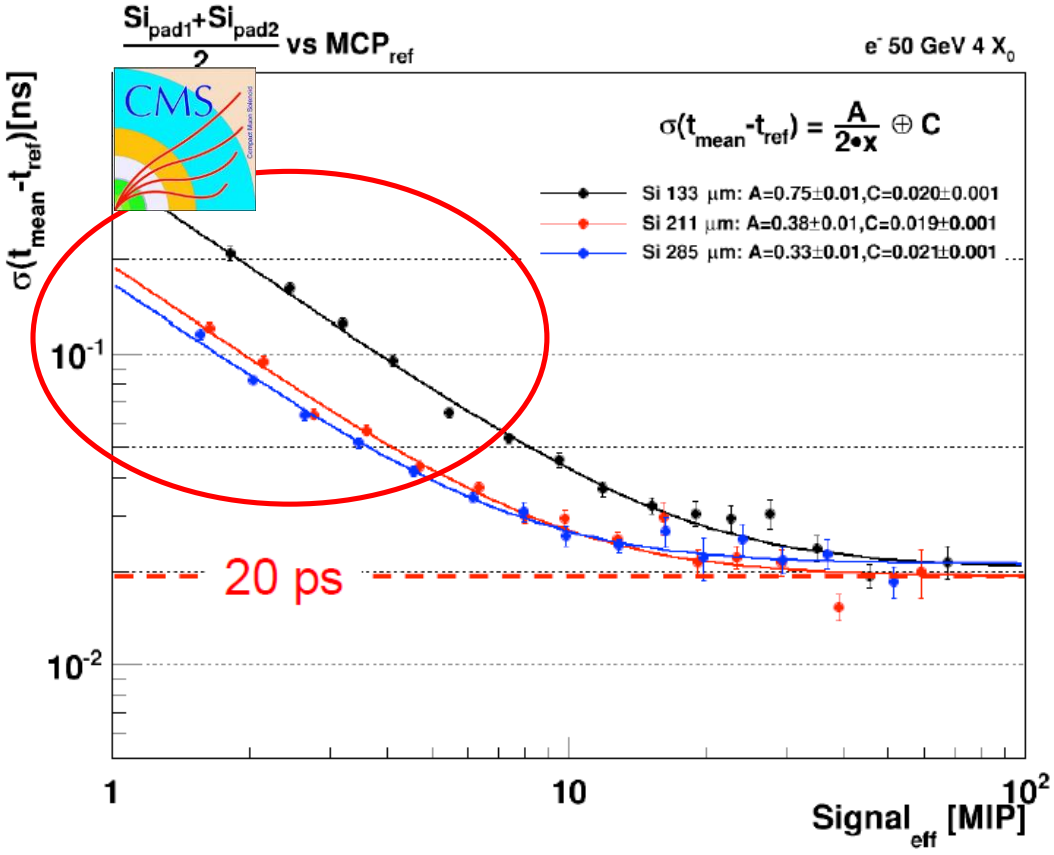


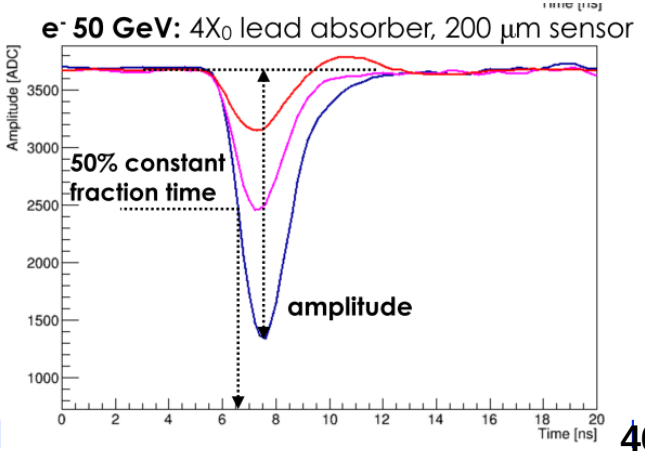
Results : CMS pin diodes caracterization

- Measured jitter In testbeam [A. Martelli et al.] :
  - jitter ~ 1 ns/Q(fC) (+) 20 ps



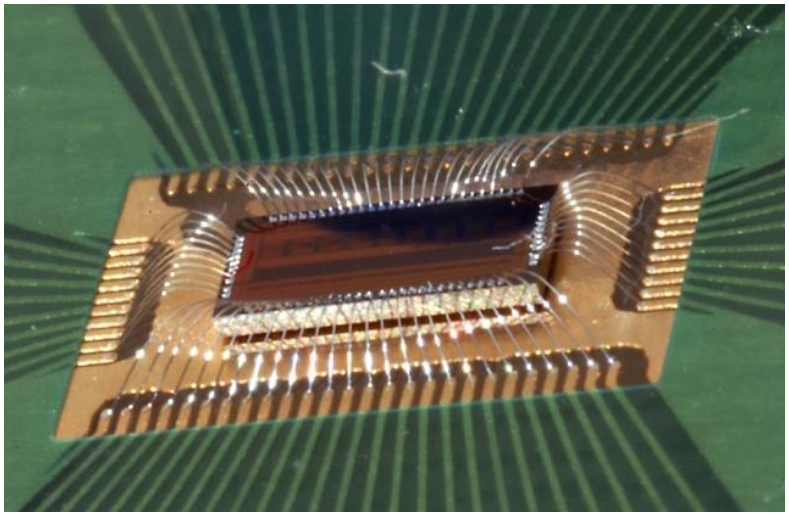






NINO chip

- NINO is a 8-ch preamp/discriminator chip
- Design : F. Krummenacher, F. Anghinolfi et al. (NIM A533 2004)
- Cd = 30 pF P = 30 mW/ch IBM 0,25 µm
- LVDS output to drive HPTDC (CERN)



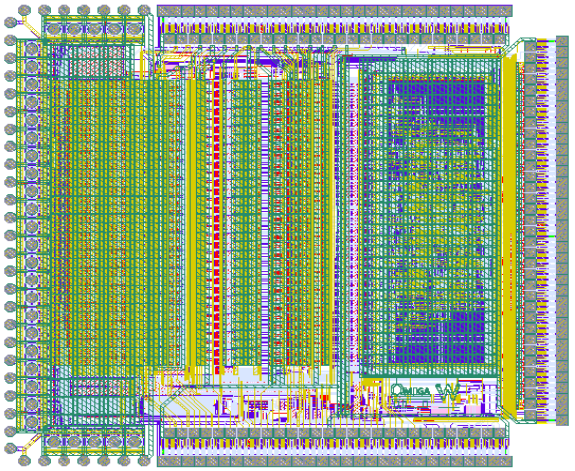
25 mm CMOS technology	8 channel/chip
Input impedance	~50 Ohm, adjustable
Power consumption	27 mW/channel
Supply voltage	+2.5 V
Input peaking time	1 ns
Timing jitter	~10 ps
Sustainable rate	>>10 MHz/chan
Input signal range	30 fC – 2 pC
Noise	< 2.5 x 103
Discriminator level	10 – 100 fC
Outputs	LVDS

- RICH detector NA62 CERN R7400 PMT readout Nucl.Phys.B, Proc. Suppl. 215 (2011) 125
- TOF analysis in PET Gundacker, S. et al. PoS PhotoDet2012 (2012) 016
- Multi-anode Micro-Channel Plate (MCP) PMT J. Instrum. 9 (2014) C02025
- TORCH time-of-flight detector In: J. Instrum. 9 (2014) C02025

PETIROC2 DESCRIPTION

- Time of Flight read-out chip with embedded TDC (25 ps bin) and ADC
- Dynamic range: 160 fC up to 400 pC
- 32 channels (negative input)
  - 32 trigger outputs
  - NOR32_chrage
  - NOR32 time
  - Charge measurement over 10 bits
  - Time measurement over 10 bits
  - One multiplexed charge output
- Common trigger threshold adjustment and 6bit-dac/channel for individual adjustment
- Variable shaping time of the charge shaper
- 32 8bit-input dac for SiPM HV adjustment
- Power consumption 6 mW/ch
- Front-end
  - Broad Band SiGe fast amplifier
  - Fast SiGe discriminator
  - 1 GHz overall bandwidth, gain = 25

AMS 0,35µm SiGe



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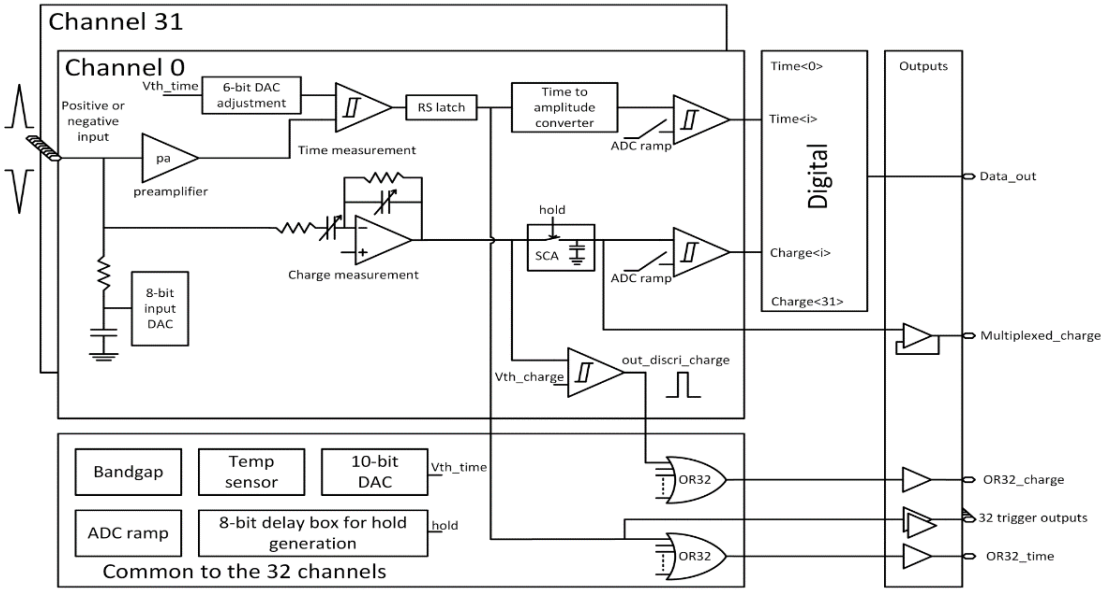
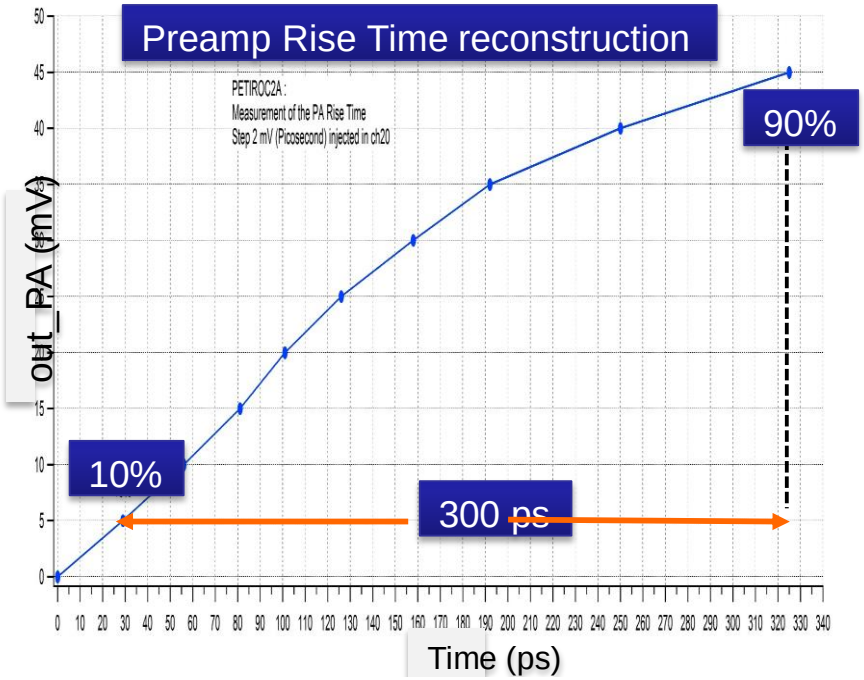
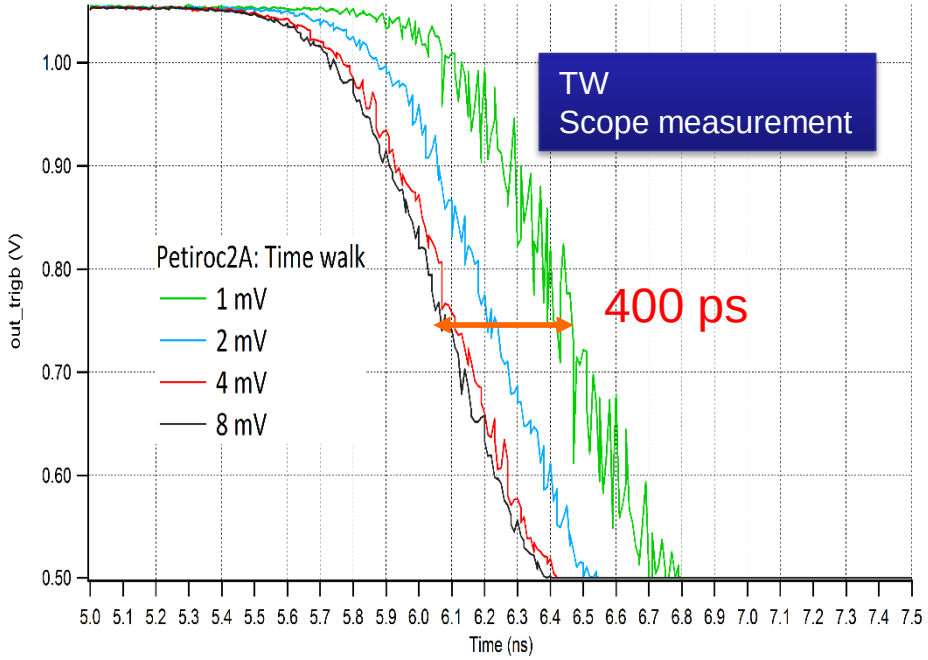
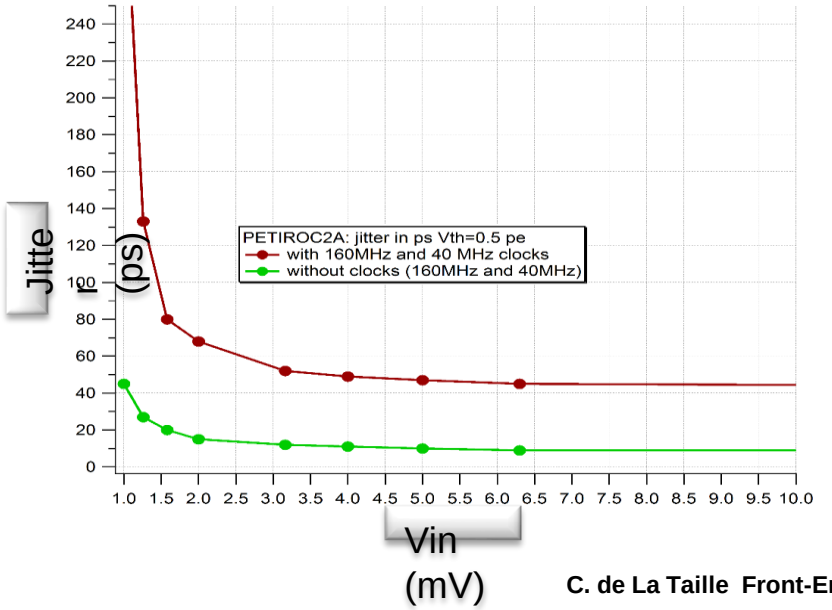
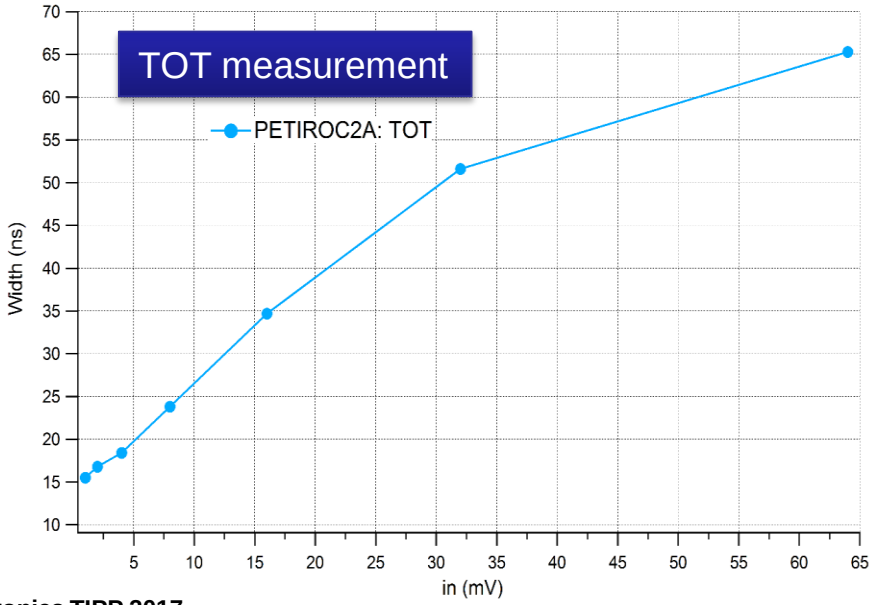


PETIROC2A: performance



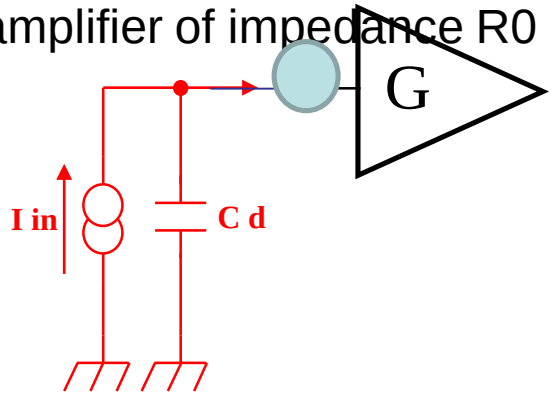






Signal and noise in Broadband amplifiers

- Signal of duration td, across capacitance Cd with BB amplifier of impedance R0



- Signal scales with 1/ Cd if R0Cd>>td and C_{PA}<<Cd

$$S = V_{OUT} = G\frac{Q_{IN}}{\mathbf{C_d}}$$

- Signal rise time is the convolution of signal duration td and amplifier risetime $t_{10\text{-}90\_PA}$

$$\frac{dV}{dt} == \frac{G.Q_{in}}{C_d\sqrt{t_{10-90\_PA}^2 + t_d^2}}$$

- Noise is independent of Cd

$$N = G.e_n\sqrt{\frac{\pi}{2}BW} = G.e_n\sqrt{\frac{\pi}{2}\frac{0.35}{t_{10-90\_PA}}} = \frac{G.e_n}{\sqrt{2t_{10-90\_PA}}}$$

- Jitter is given by

$$\sigma_t^{\ J} = \frac{N}{dV/dt} = \frac{e_n}{\sqrt{2t_{10-90\_PA}}} \frac{C_d\sqrt{t_{10-90\_PA}^2 + t_d^2}}{Q_{in}} = \frac{e_n C_d}{Q_{in}} \sqrt{\frac{t_{10-90\_PA}^2 + t_d^2}{2t_{10-90\_PA}}}$$

- Optimum value: $t_{10\text{-}90\_PA} = t_d$ (current duration)

$$\sigma_t^{\ J} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

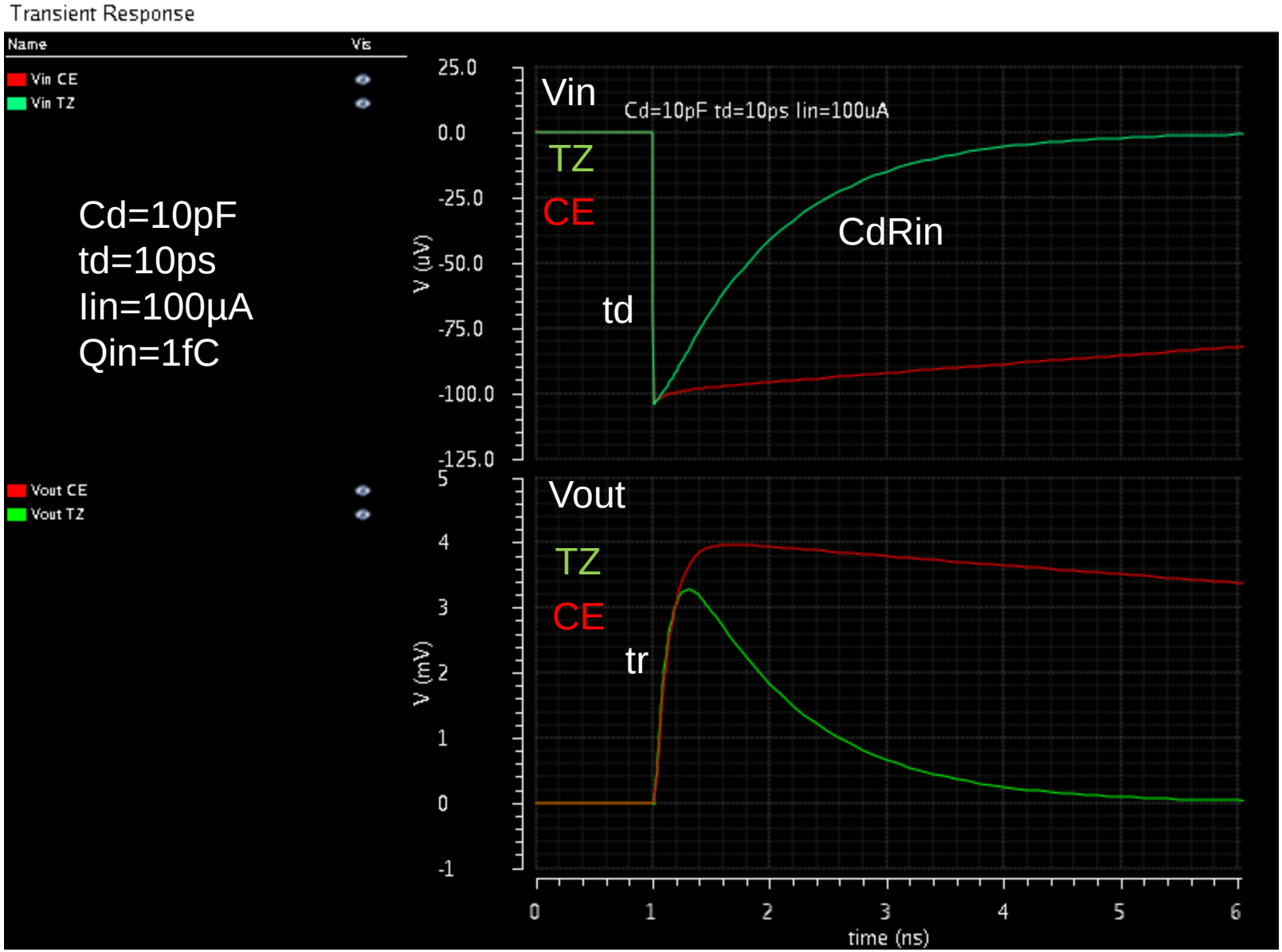
Dominated by sensor
Electronics only gives en

- Electronics noise en given by input transistor transconductance :

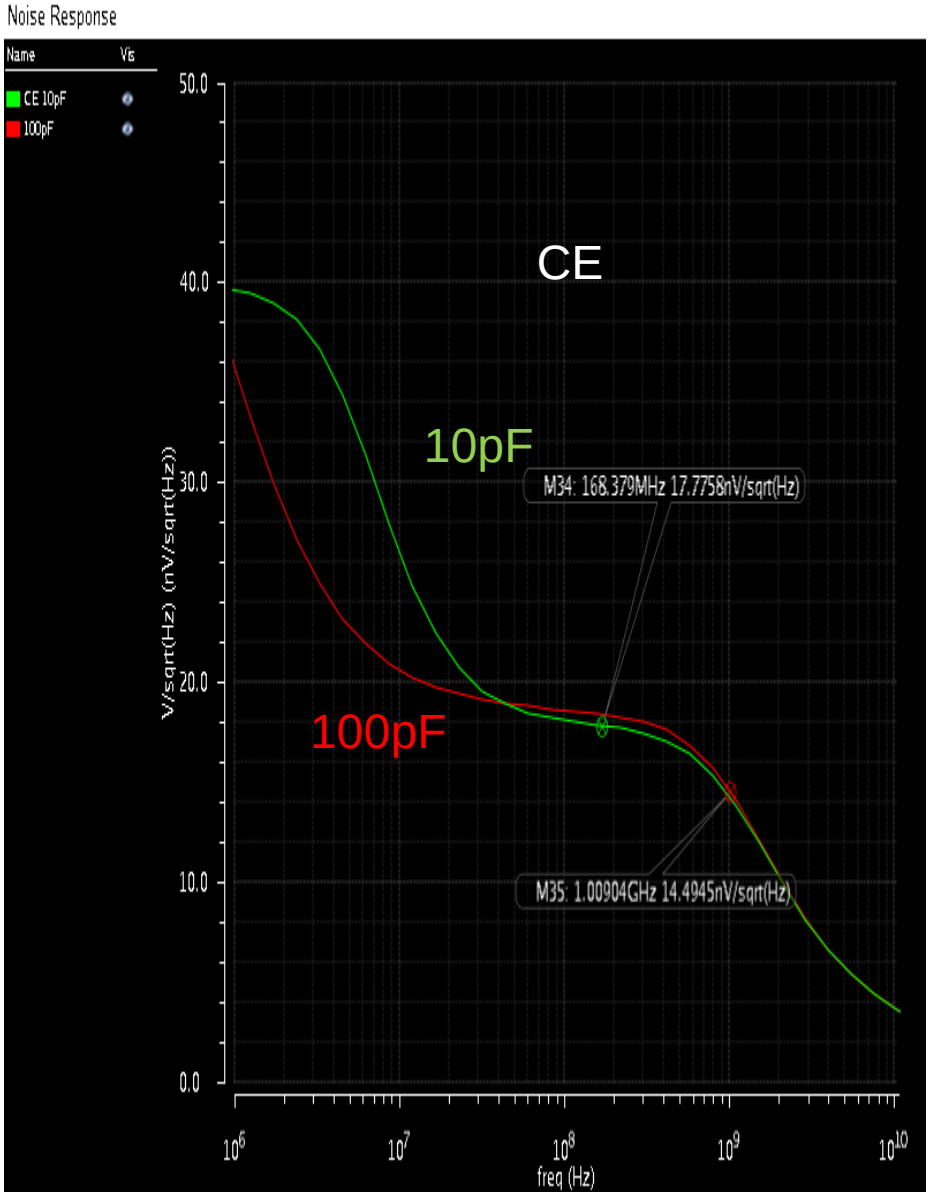
$$e_n = \sqrt{\frac{2kT}{g_m}} \approx \frac{2kT}{\sqrt{qI_D}}$$

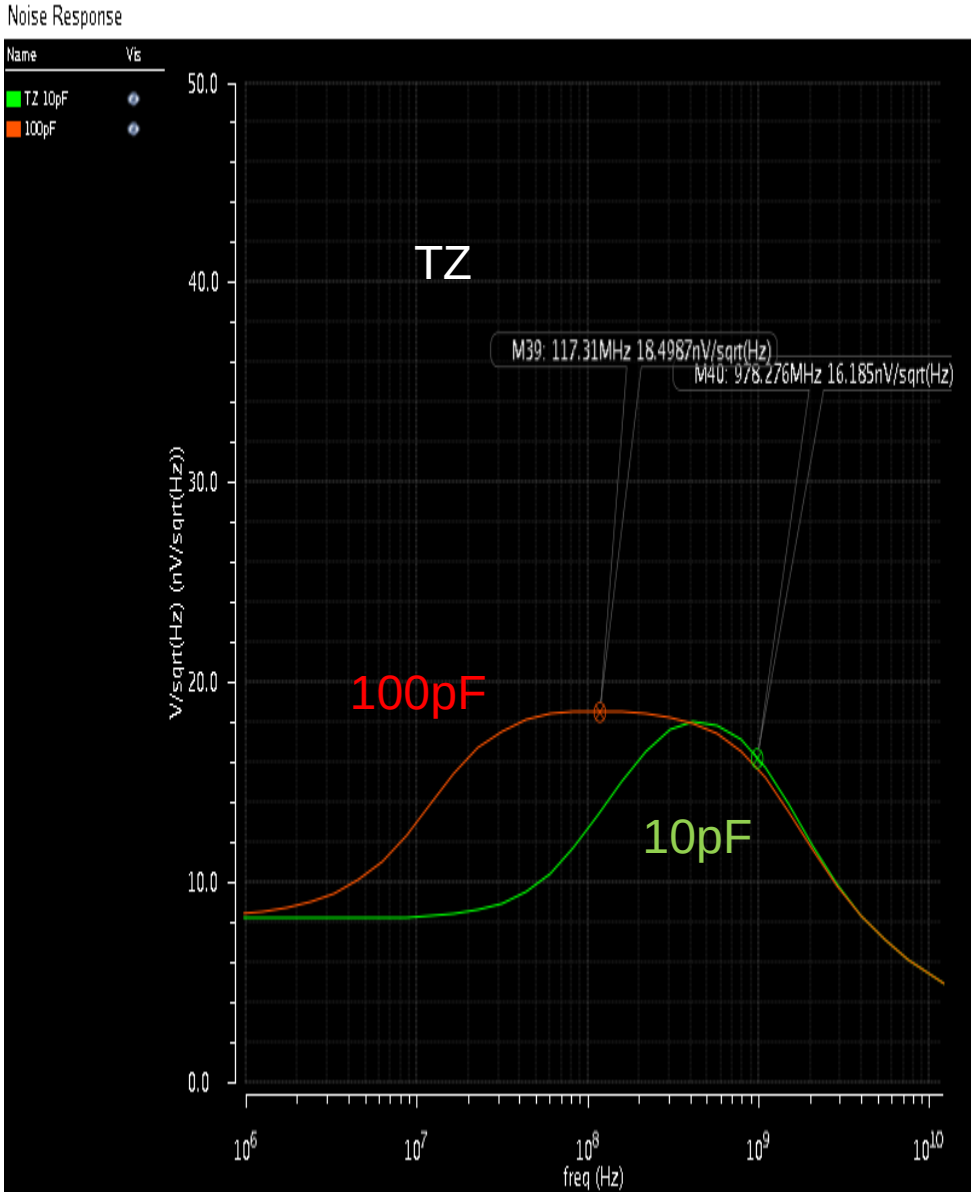
$$\sigma_t^{\ J} = \frac{C_d}{Q_{in}} \sqrt{\frac{2kT}{g_m} t_d}$$

Vin and Vout CE, TZ Cd=10pF td=10ps 1fC

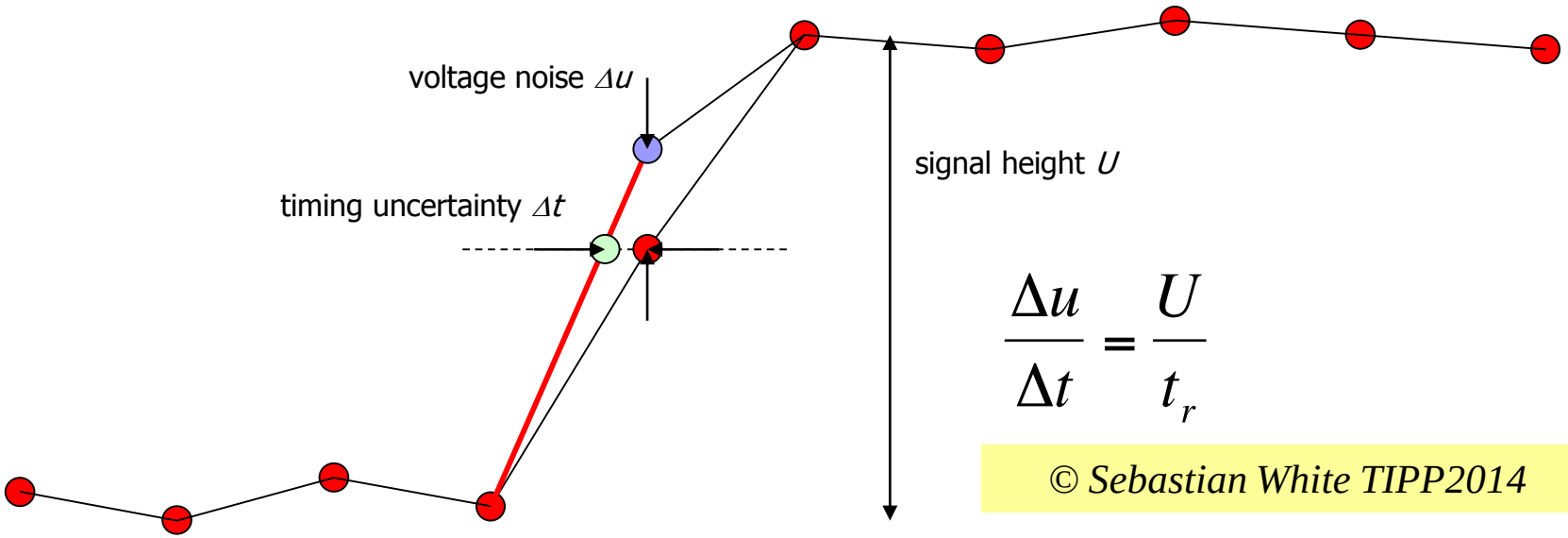


Output noise CE and TZ for Cd= 10pF 100pF





Timing with waveform samplers



$$\frac{\Delta u}{\Delta t} = \frac{U}{t_r}$$

$$\Delta t = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

Assumes zero aperture jitter

Optimistic for S/N and neglects noise autocorrelation

	U	Δu	f_s	f_{3db}	Δt
today:	100 mV	1 mV	2 GSPS	300 MHz	~10 ps
optimized SNR:	1 V	1 mV	2 GSPS	300 MHz	1 ps
next generation:	1V	1 mV	10 GSPS	3 GHz	0.1 ps