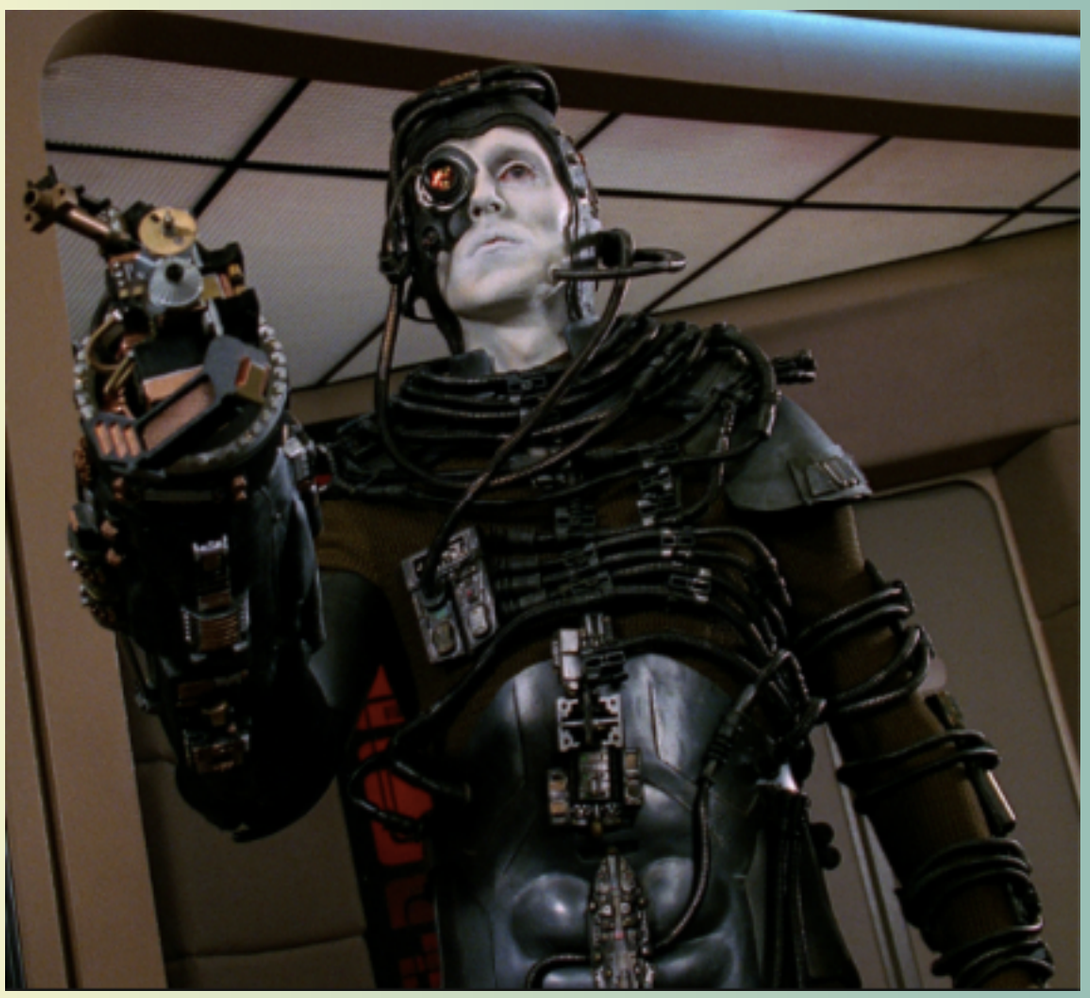
Mobile Technology for PMT readout



DEVELOPMENT FOR CHIPS AND ICE-TOP

J.Kelly, A.Loving, D.Tosi, J.Thomas, J.Troken-Tenorio, C.Wendt*

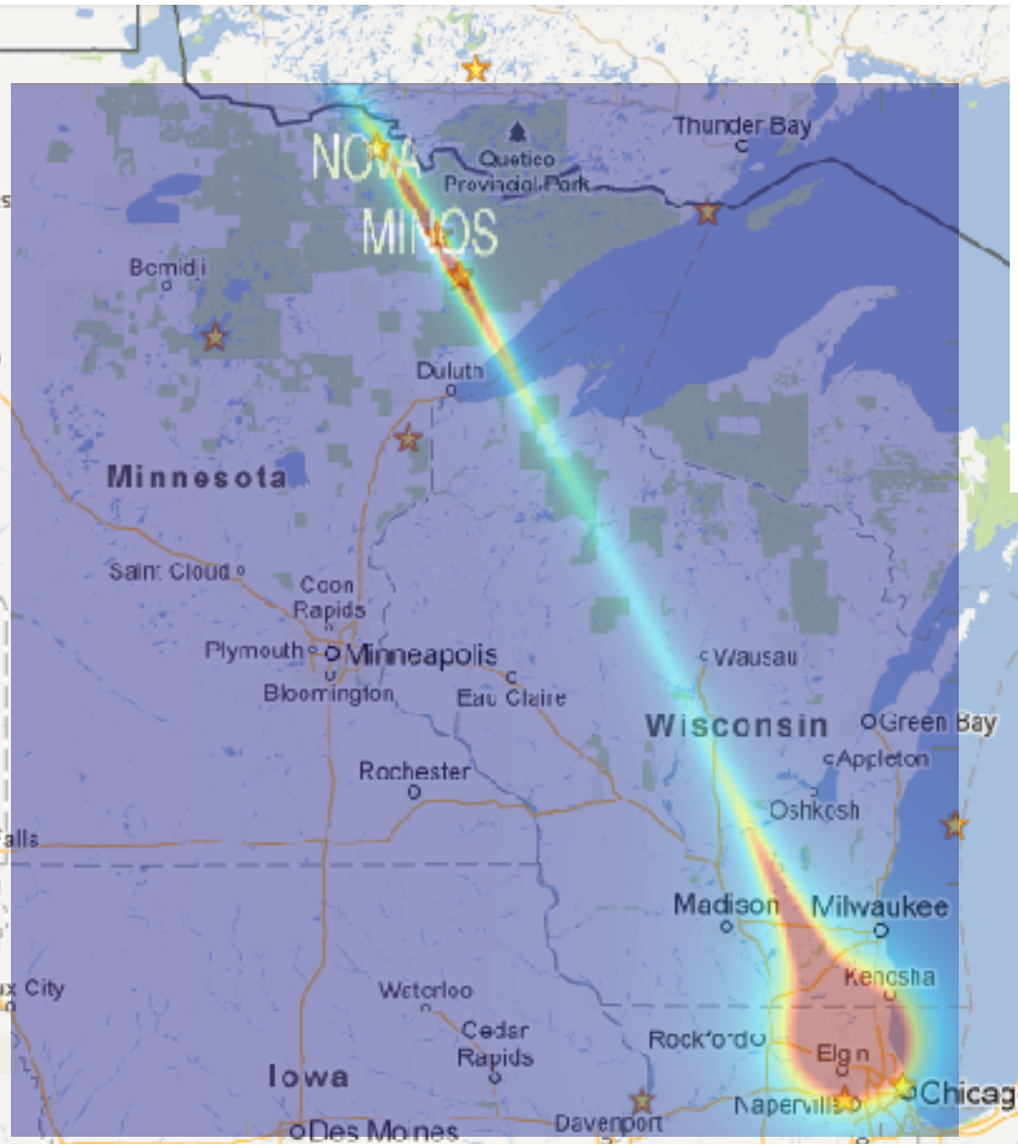
WIPAC (UW Madison) and UCL

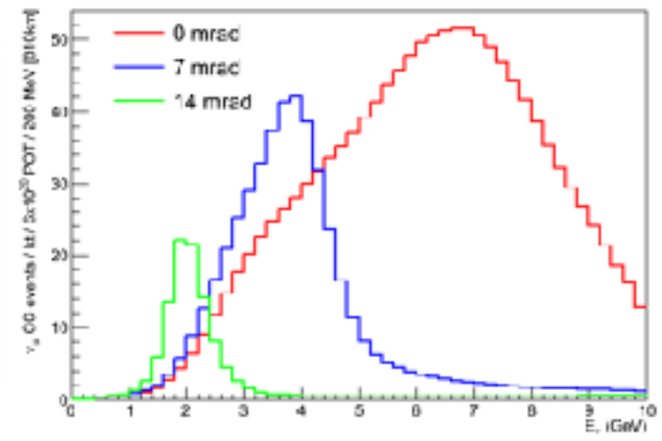
Outline

- Motivation and Orientation
- Architecture
- Timing measurement methodology
- Pulse shape measurement methodology
- Connection between ARM processors, WR
- Outlook

Motivation and Orientation

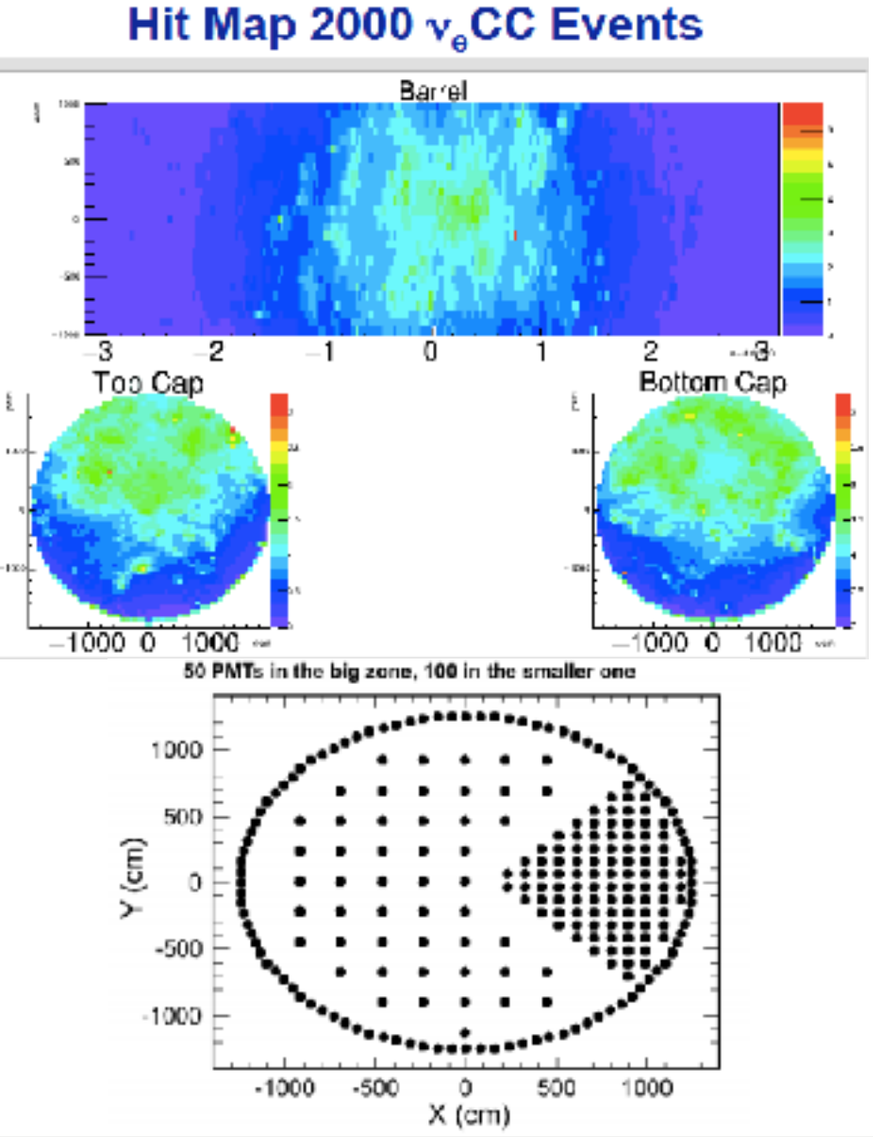
- The CHIPS goal
  - prove that water Cherenkov detector can do oscillation physics for a fraction of the cost of present neutrino detectors
    - to $200k/kt (presently $2-10M/kt water, $10-20M/kt Liquid Argon) including location/infrastructure etc
  - contribute to constraining δCP using NuMI neutrinos in the short term
- CHIPS will be sunk in a flooded mine pit in the path of the NuMI beam
- It starts with 5 kilotons in summer 2018,

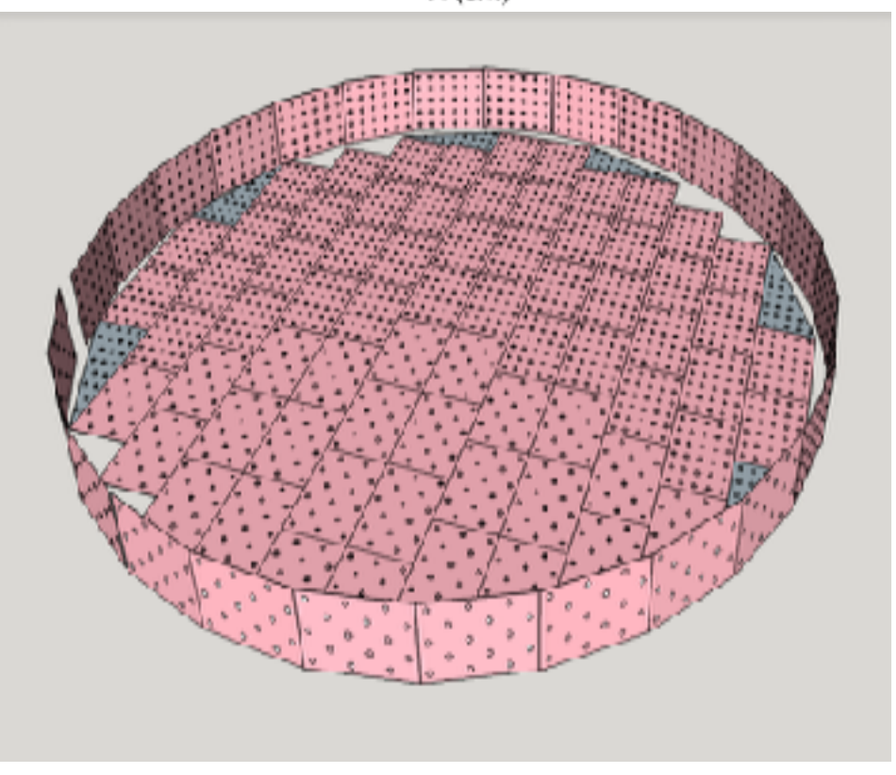


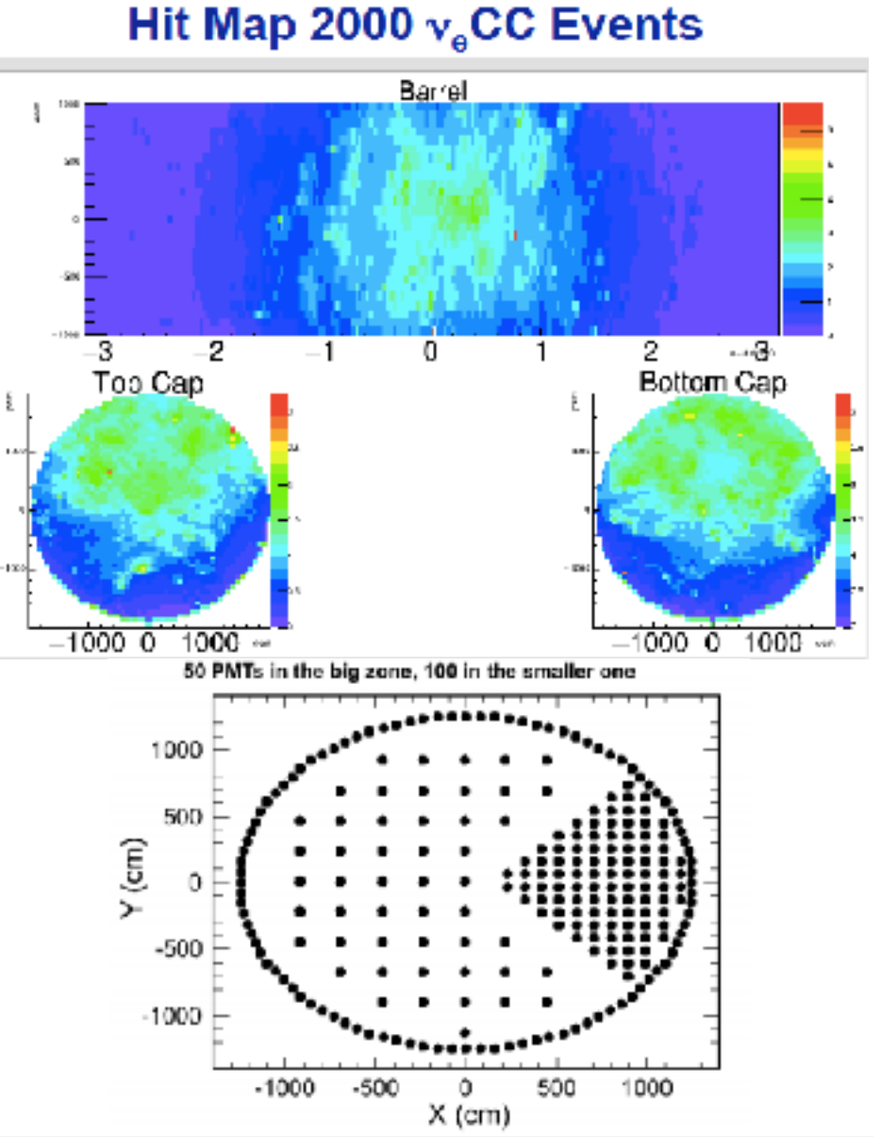


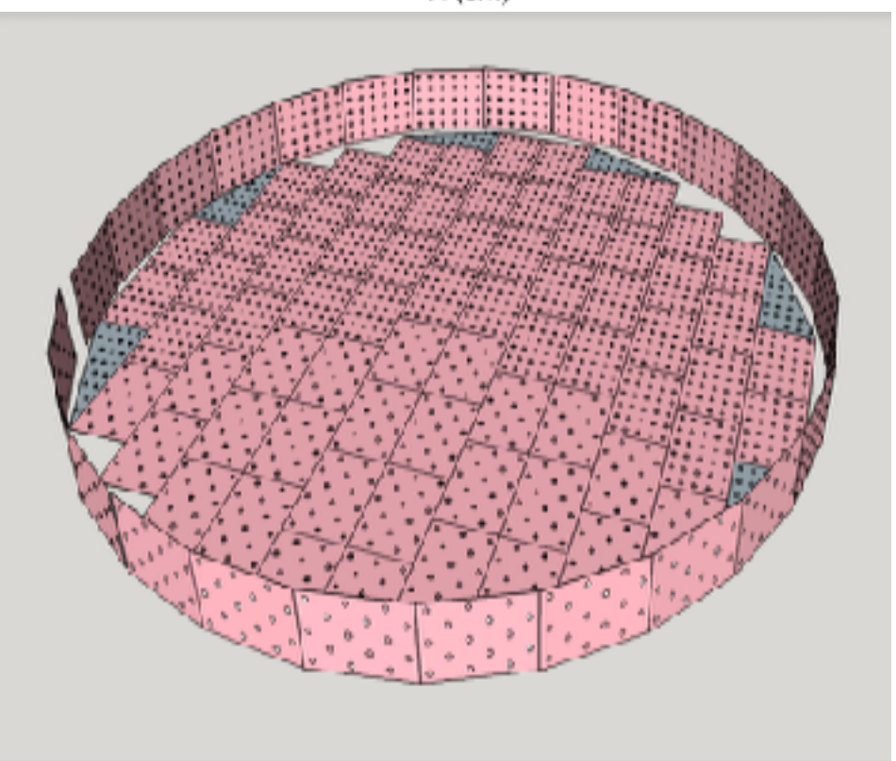
PMT Choice and Layout

- Traditional system would need
  - PMT+base+
  - HV system+
  - HV-cable+
  - connectors+
  - readout-cable
- This is prohibitive for thousands of PMTs, 100's m of cable per channel because of cost and cable bulk



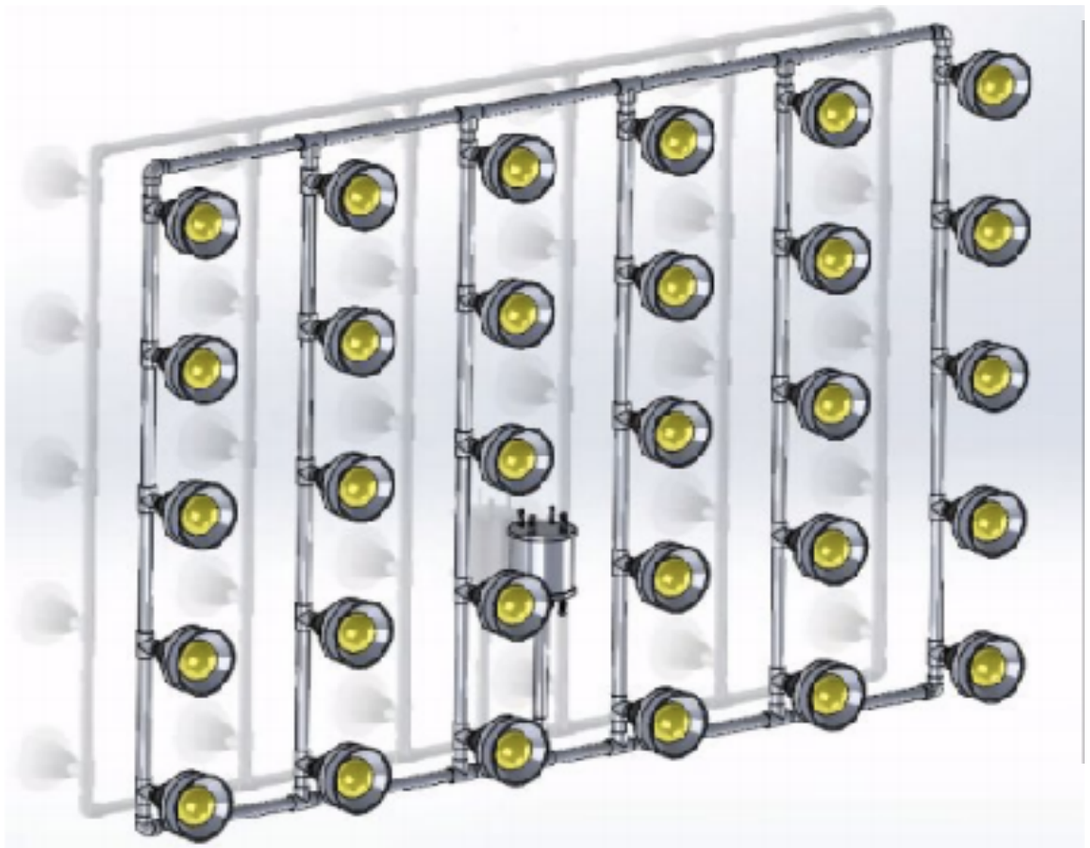




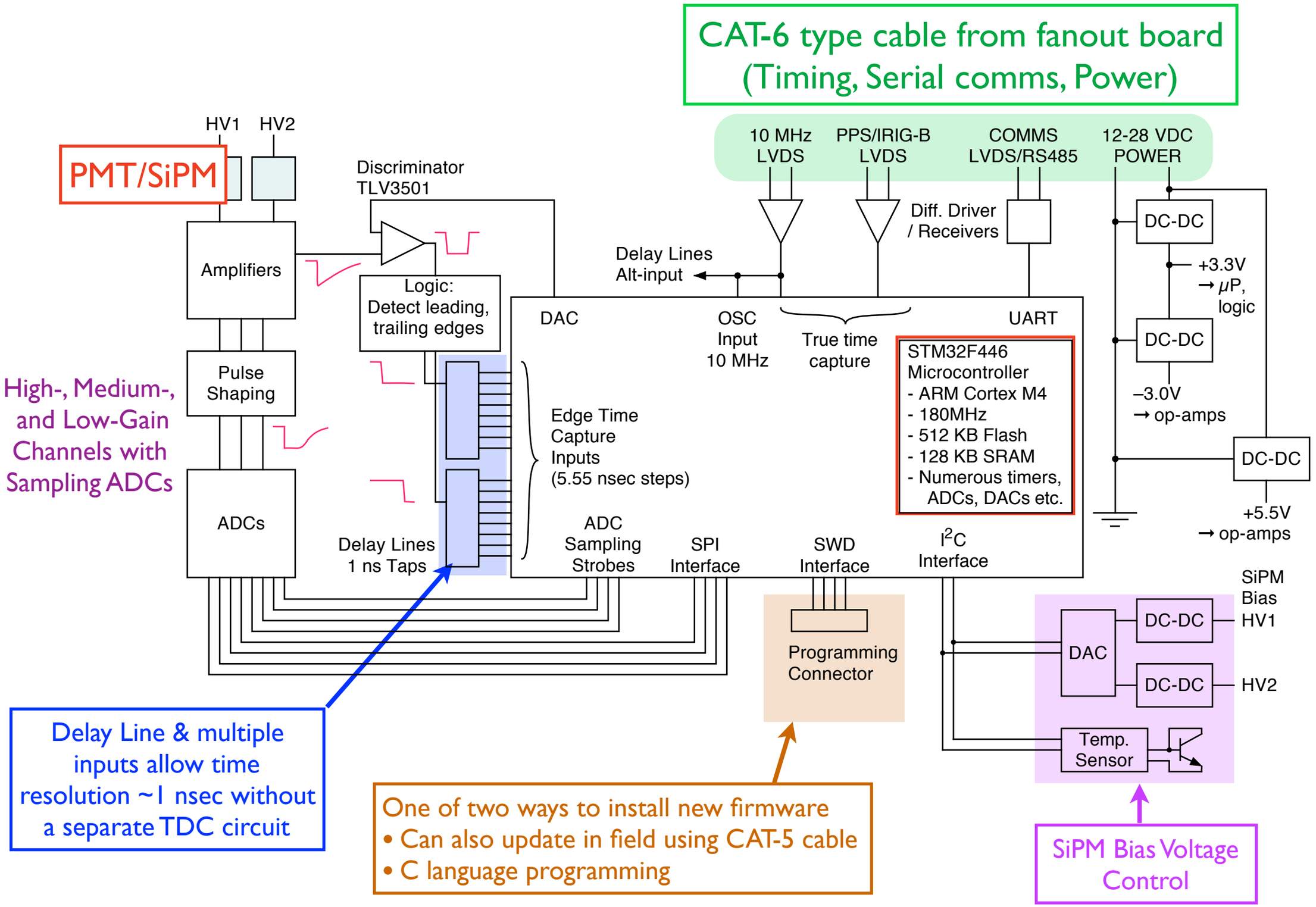


PMT Choice and Layout

- Layout will have both high and low density planes
- A big part of the instrumentation will just implement KM3Net technology
  - New 3” PMTs at 6% coverage in front and end caps, and 3% coverage back end cap region
  - ready designed electronics which does what we want
- Low density wall planes will be made with **donated NEMO-III 3” PMTs and Madison electronics.**
  - Old 3” PMTs at 3% coverage in back

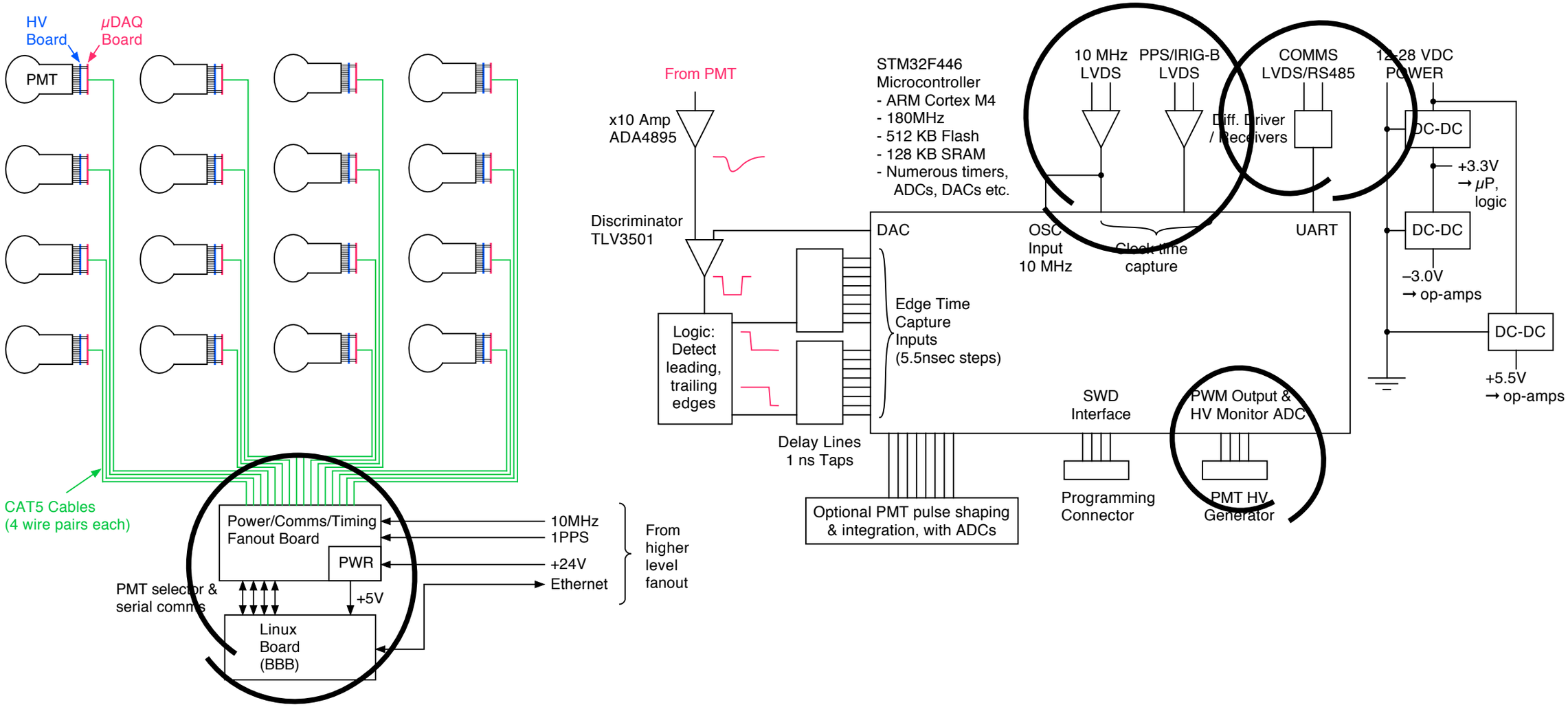


µDAQ Board Block Diagram : SiPM and PMTs



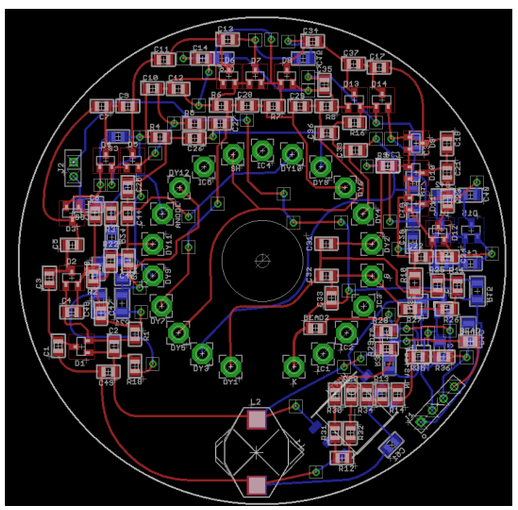
CHIPS specific

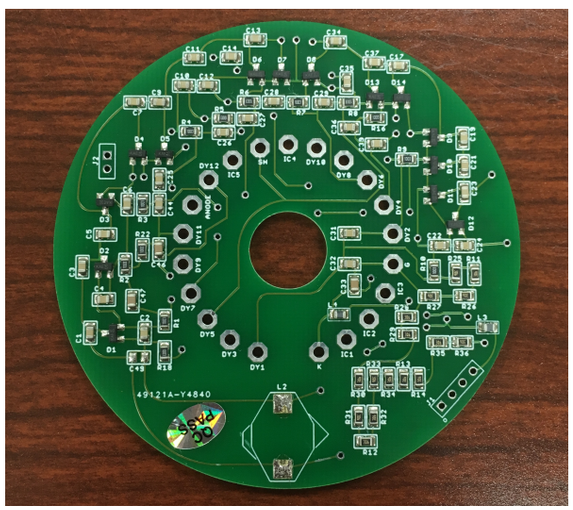
- Idea is to produce dedicated micro-processor for reading out the TOT on each PMT
- Each μDAQ board will have ~1ns absolute time signal from WR
- Will provide PWM input to CW base
- μDAQ will communicate with BeagleBone over LVDS
- BeagleBone will bundle up hit packets and send them on Ethernet to WR switch



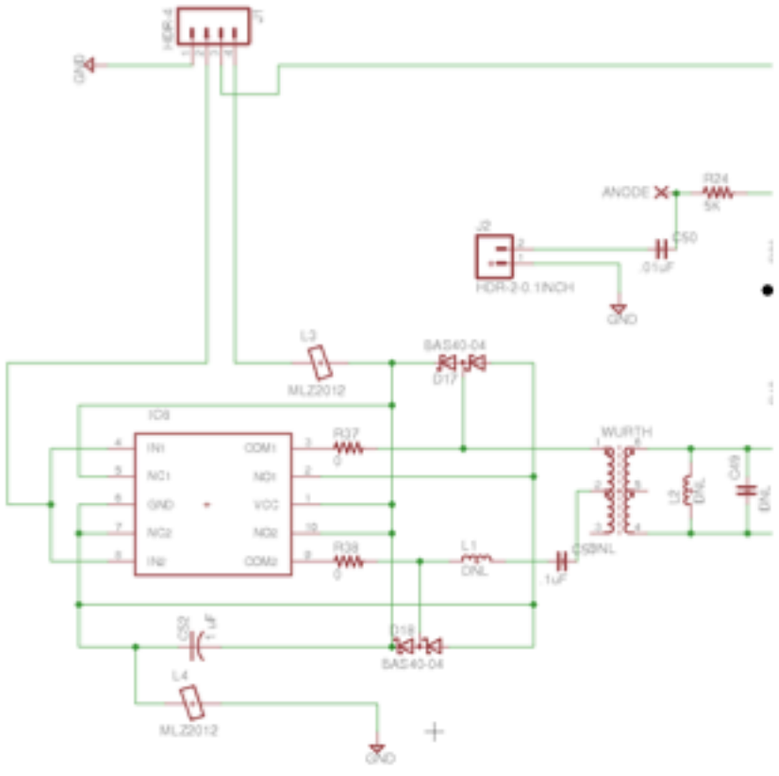
CHIPS CW-base for Hamamatsu R6091

- +ve CW base adapted from COUPP design at FNAL: added more stages

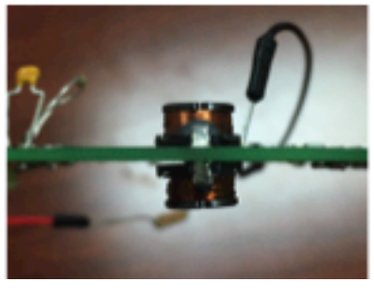




AC Voltage generator



- Circuit designed for COUPP
  - 5V power supply
  - NLAS4684 IC Switch changes output to transformer from +5V to -5V based on input signal
  - When run near resonant frequency of 207kHz it gives a sine wave (essentially a 5V AC Voltage)
- Instead of using the transformer in the schematic we used a design from Chris
  - Two unshielded inductors coupled through the board

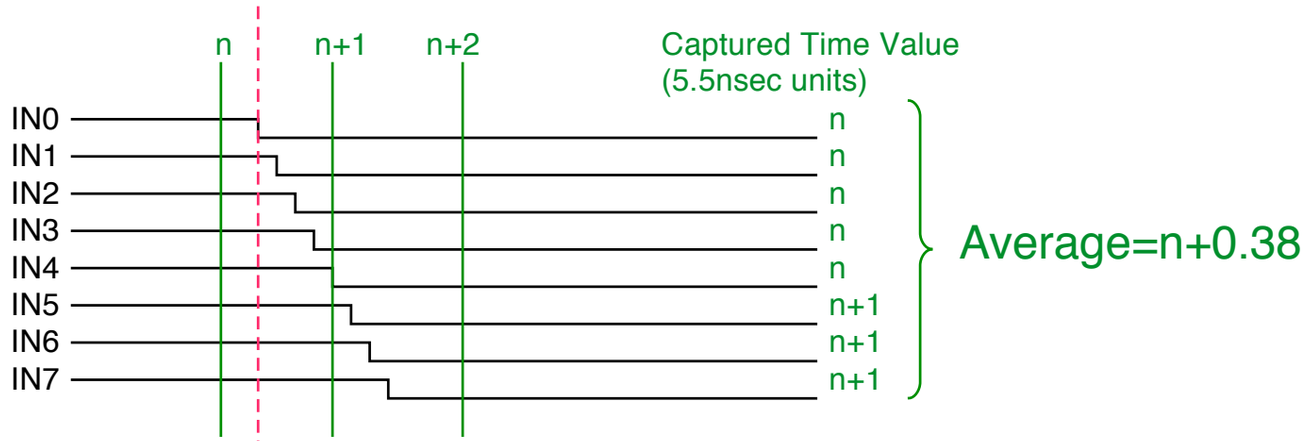


Averaging multiple delayed inputs gives finer time bins

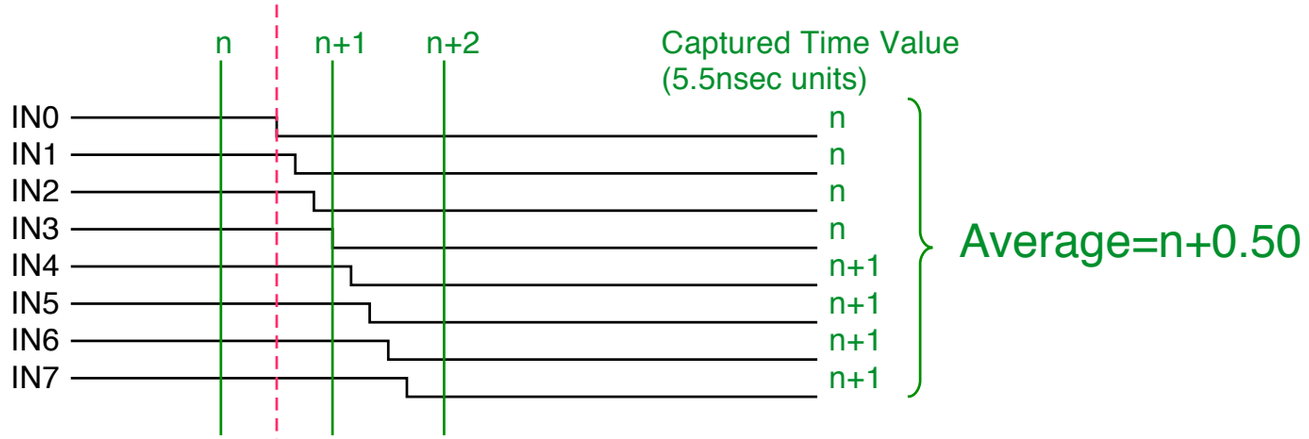
Diagram of captured counter values (=time)

- Eight registers record each edge... average value tells more precisely when the edge arrived
- Clock time 5.555ns

Response for edge at time T



Response for edge 1 nsec later

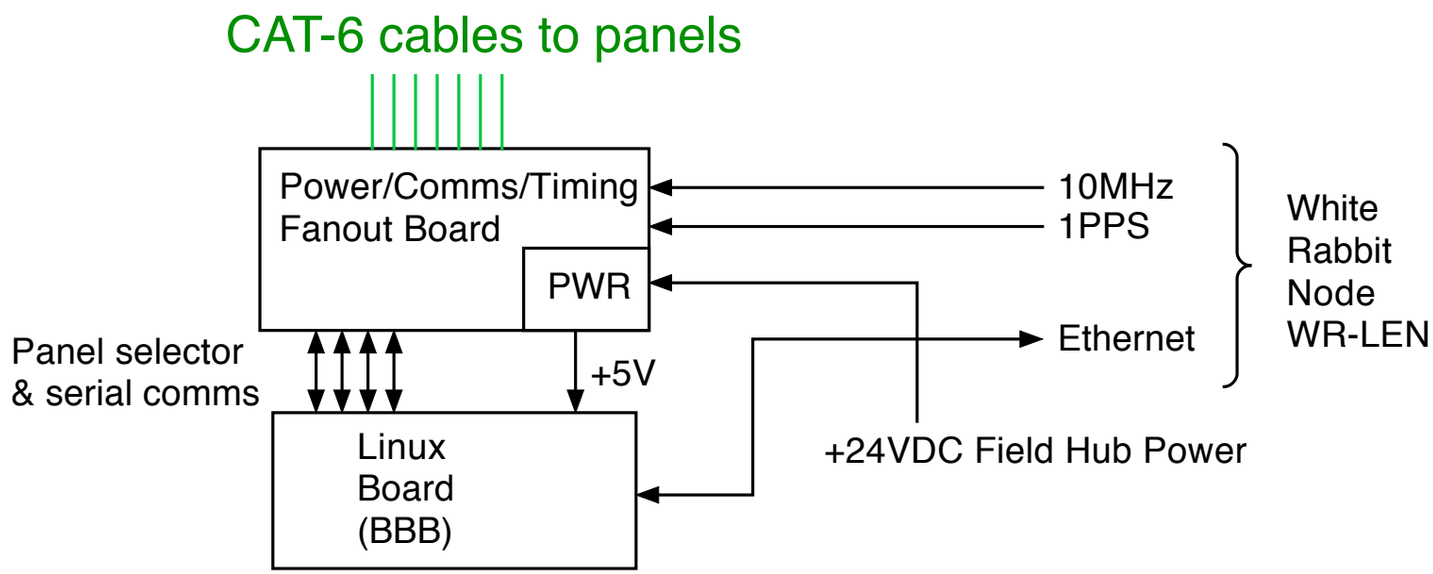


Possible values for average are n, n+0.13, n+0.25, n+0.38, n+0.50, ...
➠ Allows time resolution ~ 1 nsec even though n increments each 5.5nsec

- Exact mapping from N_{avg} to time will be calibrated from from occupancy histogram of 8 possible N_{avg} values

Linux Board and WR Fanout Board

- All communications with ICL go through the Linux board (BeagleBone, “BB”)
  - BB polls the 16 PMT µDAQs forwards data as regular ethernet traffic over optical fiber (White Rabbit)
  - BB also needed for reprogramming with software updates (bootloader)



- Fanout Board has a CAT-6 style connection to each MicroDAQ board, carrying:
  - Timing signals from White Rabbit node (WR-LEN)
    - 10MHz & PPS/IRIG-B
  - 24VDC power, each PMT can be switched on/off by BB control signal
  - LVDS communication with BB
    - Requires multiplexing, because BB provides only 4 serial ports
    - Alternate pathways can be enabled by BB control to allow full-duplex communication with bootloader in each µDAQ

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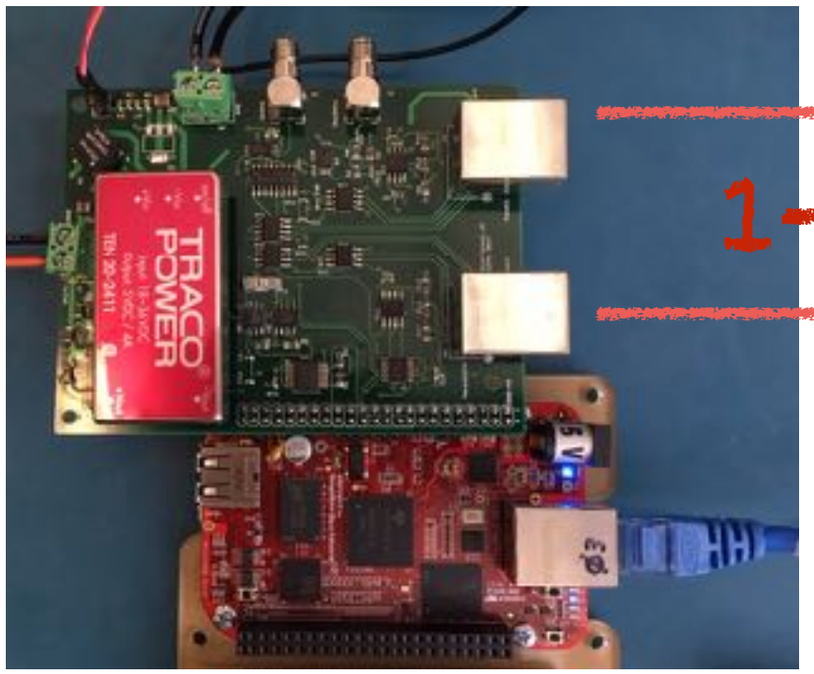

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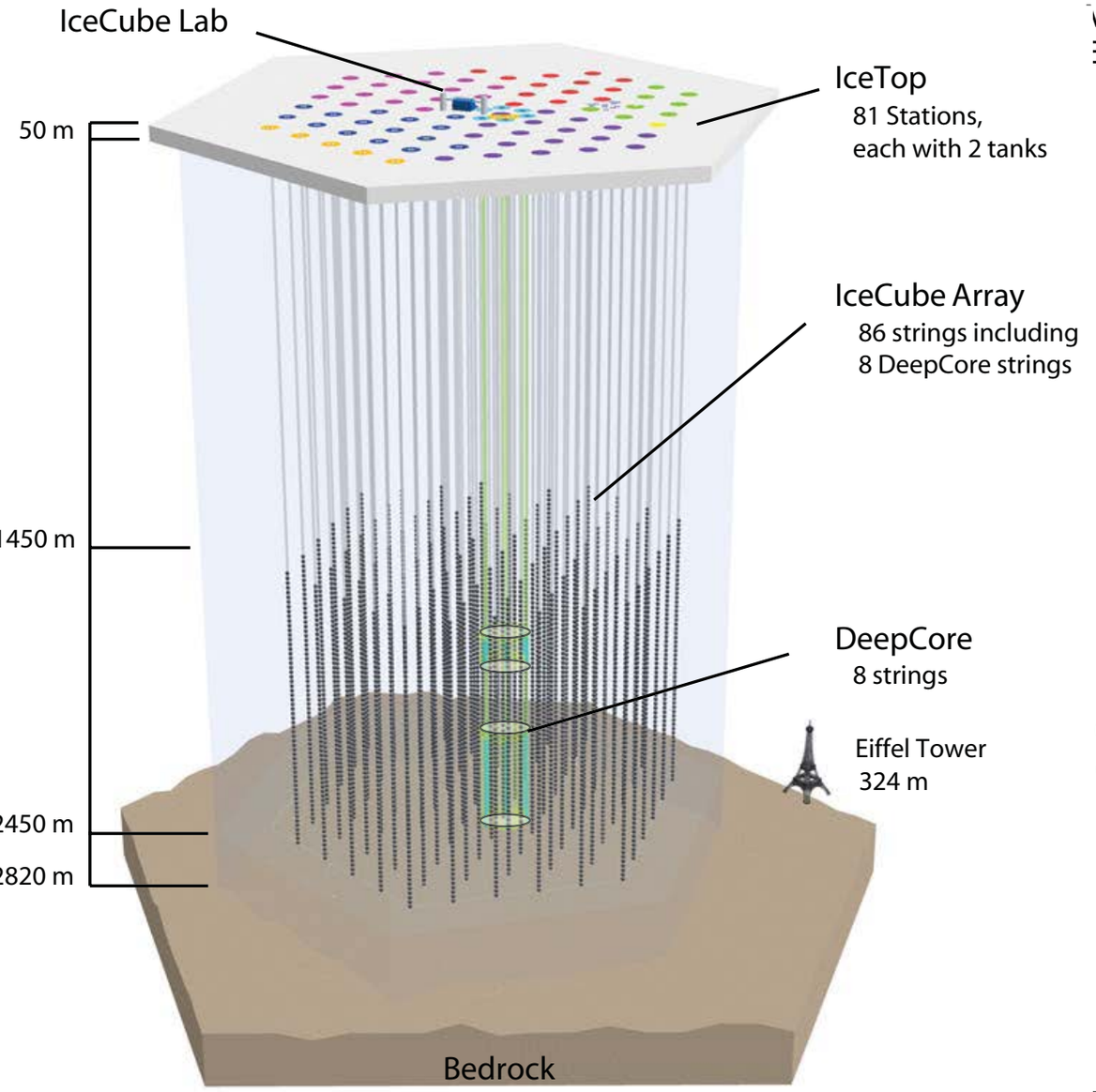
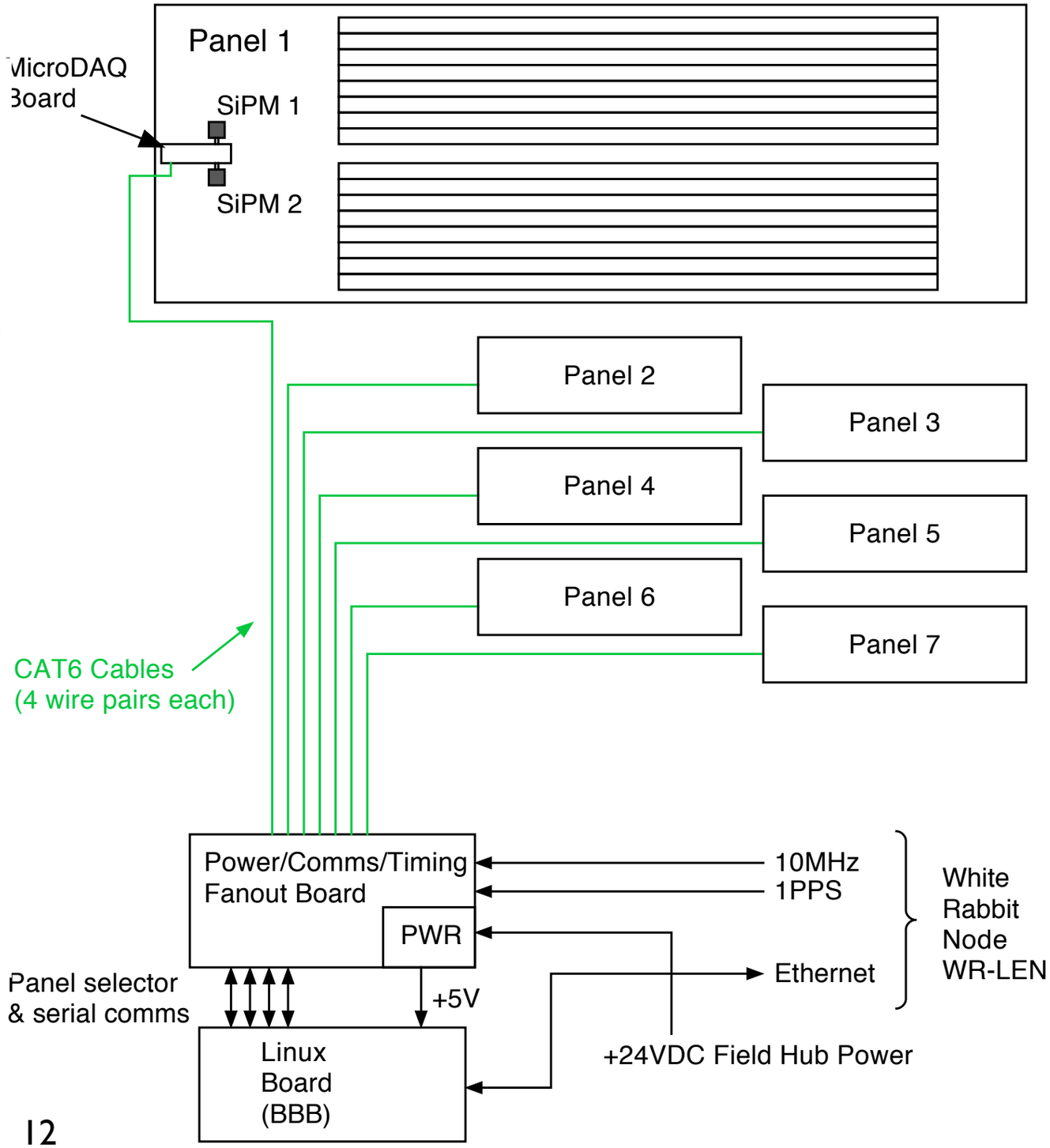
Ice-Top overview



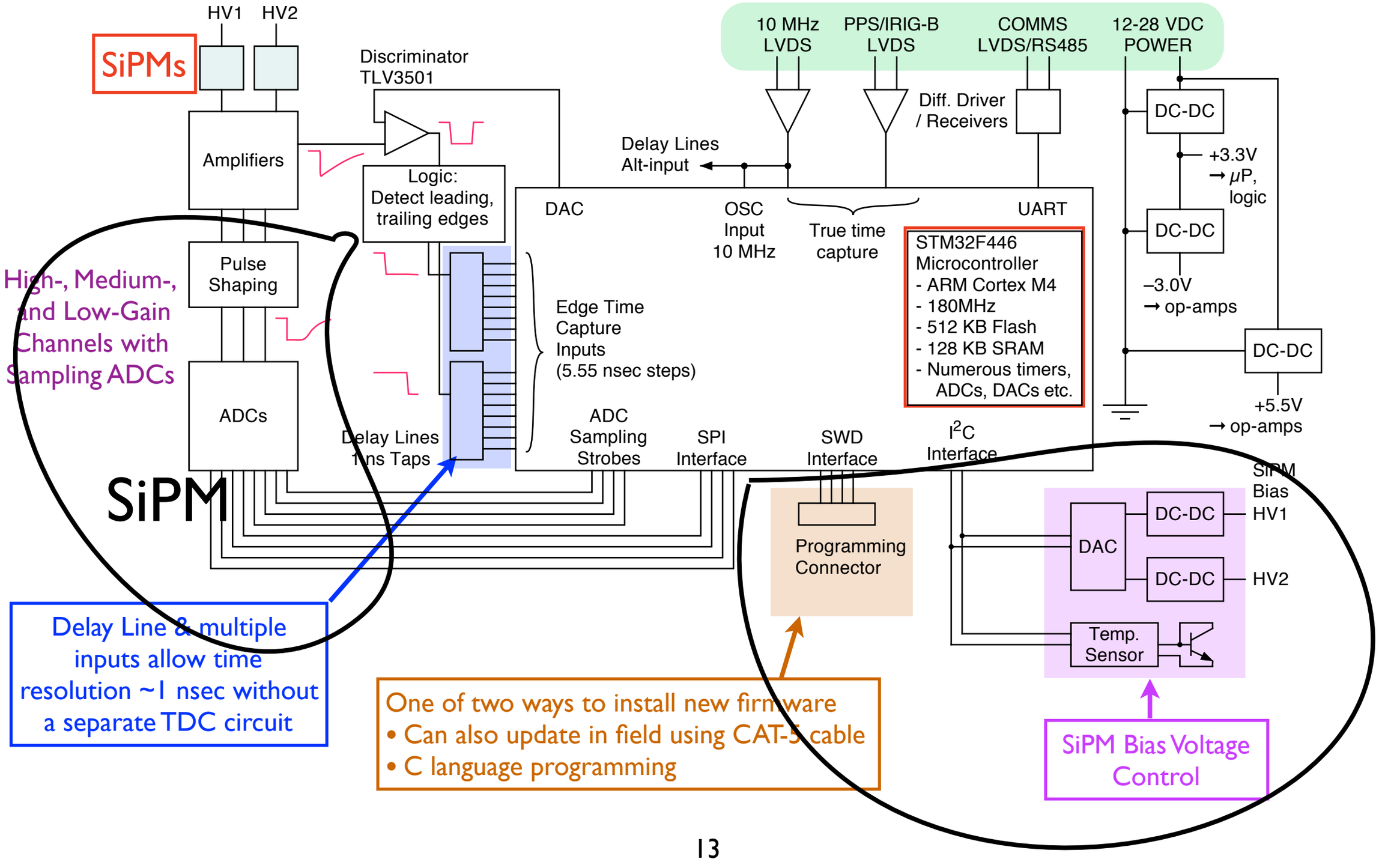
µDAQ in IceTop Scintillator Station



µDAQ Board Block Diagram : specific for Ice Top

SiPM specific

CAT-6 type cable from fanout board
(Timing, Serial comms, Power)



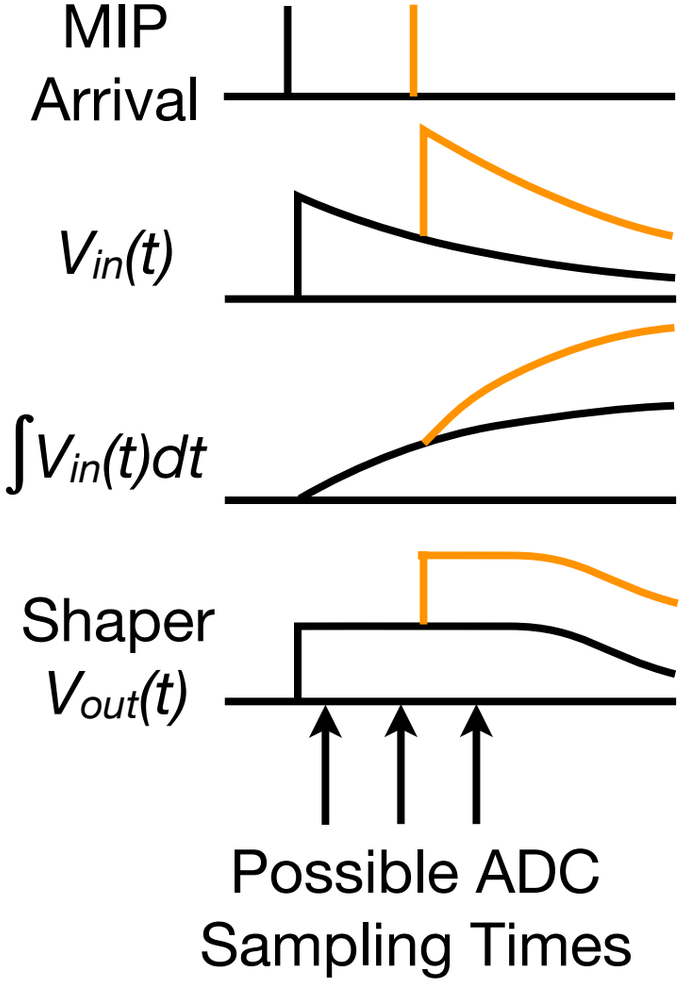
Delay Line & multiple inputs allow time resolution ~1 nsec without a separate TDC circuit

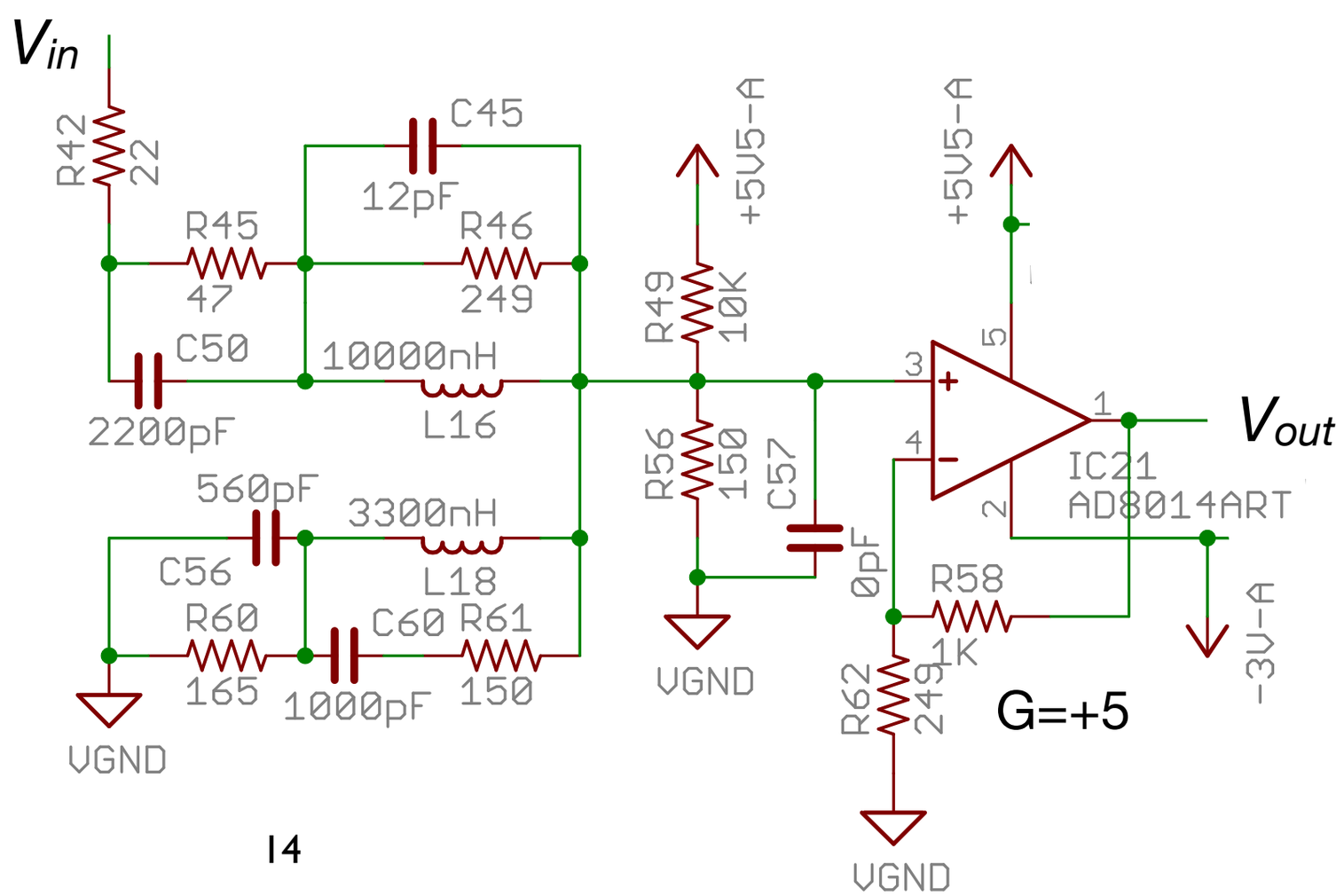
One of two ways to install new firmware
- Can also update in field using CAT-5 cable
- C language programming

SiPM Bias Voltage Control

Pulse Shapers for Sample & Hold ADCs

- Shaper is included after one or more stages of amplification, before 12 bit ADCs
- Linear (RLC) network, instantaneous output measures integral of #SPEs
- Similar in concept to simple integrator, but tuned for SiPM signal shape and exhibits flat top response followed by quick return to baseline
  - Measured charge will not vary much if sampling time is shifted by 5.5 nsec (such shifts can happen due to the scheme of using μP to program sampling delays)
  - Samples at times T_i measure $\int (dN/dt)\, dt$ from 0 to T_i ➠ Arrival time profile



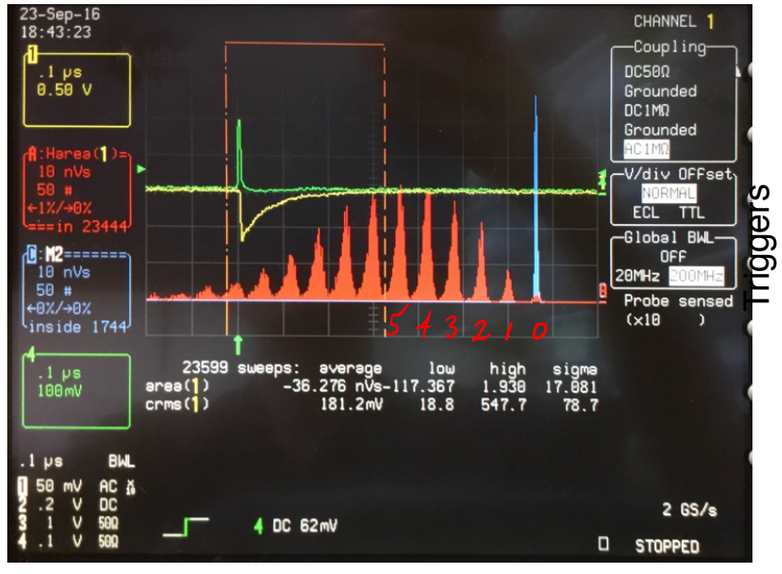


Amplifiers Testing & Redesign Experiences

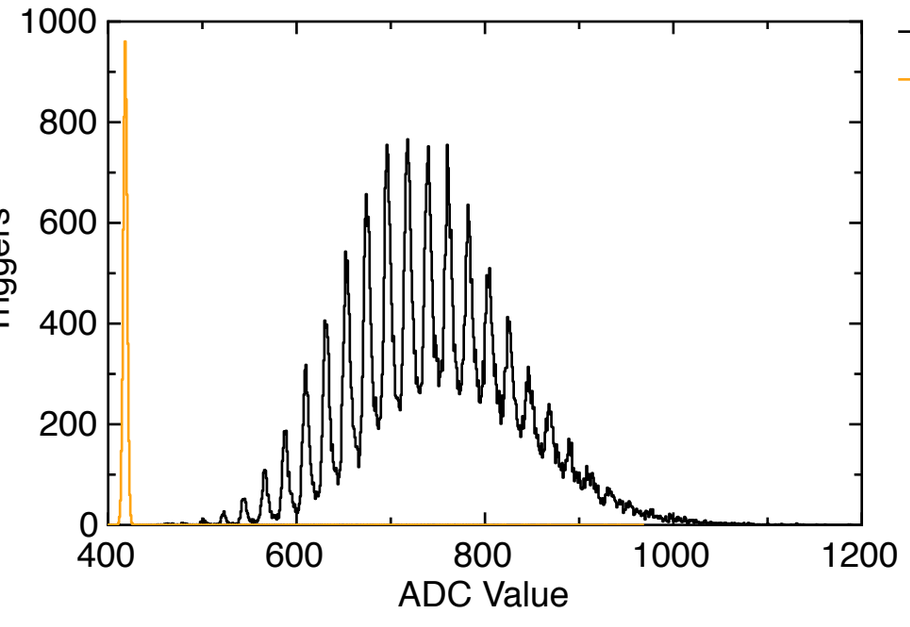
- Illumination is laser diode, pulses with ~16 SPE delivered via optical fiber
- Using SensL 6mmx6mm, μDAQ in freezer (-62C)
- Bias generated with μDAQ supply, set for 26.3 volts
- SPE amplitude is 15mV at discriminator input; still easily resolve peaks
  - High gain ADC would register around 19 counts per SPE
  - Low gain channel should saturate around 70000 SPE

Amp. output, rising edge
20%–80% in 1.4nsec

Low input impedance,
good rise time & low noise



SiPM+ μDAQ charge spectrum



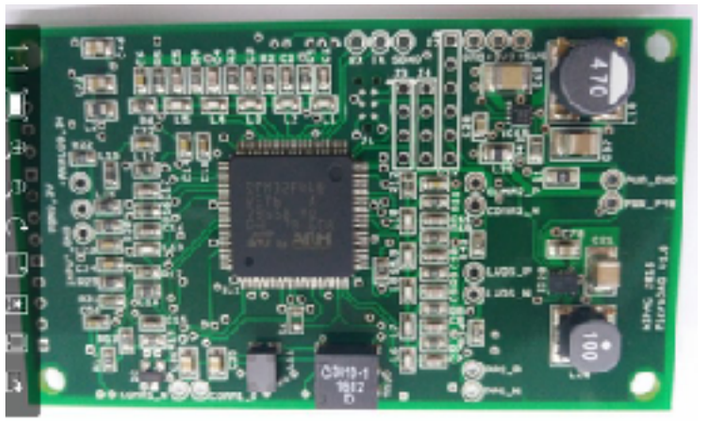
µDAQ Board Prototype Versions 1 & 2 …& 3

uDAQ V2

Board size
1.75” x 5”

- V2 adds amplifiers and bias voltage for two SiPMs, also wide dynamic range
- Many smaller changes ➠ completely new layout

uDAQ V1

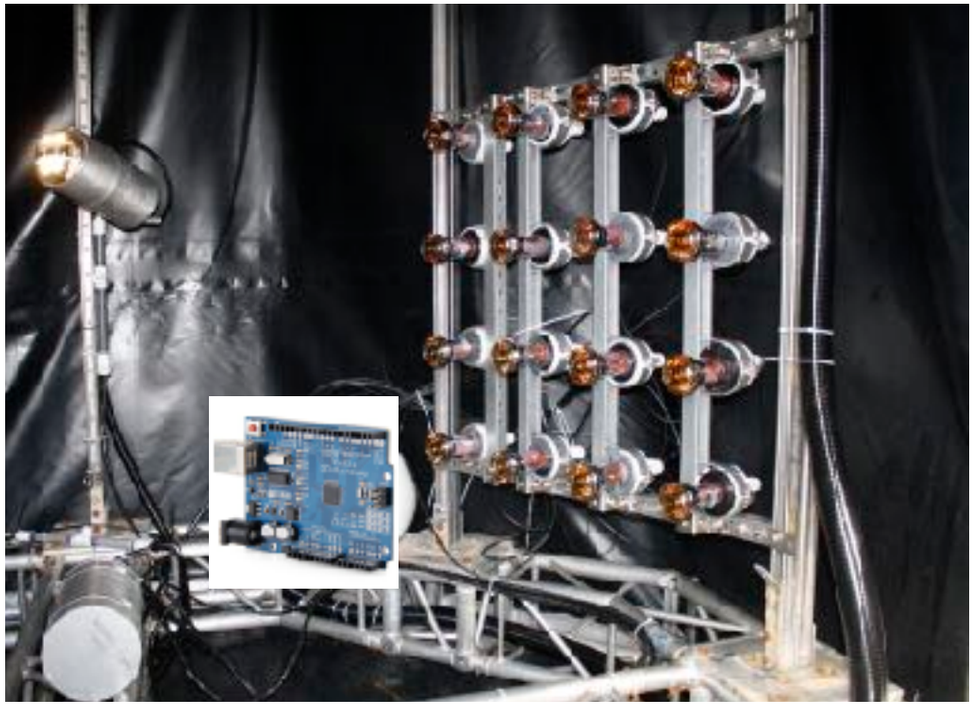


Board size
1.75” x 3”

- V1 had a single preamp for a PMT, no SiPM-specific circuitry
- Used for testing amplifier & discriminator, time capture concept, communications (& lower level items like power circuit, µP programming interface, etc)
- Hosted various add-on prototyping boards to test SiPM preamp options
- V3 coming soon : just CHIPS functionality, lower power, smaller (150mW)

Summary

- PP can ride a revolutionary wave in electronics development
  - ARM processors, both on PMT and as controller (BB or Rpi) to collect signals and transmit to Ethernet
  - Each PMT provides ToT and receives 1ns absolute timing signals (10MHz and PPS) from WR system $25/channel total (CW,mD,WR)



- Side comment: Industrially available ASICs in version 100 (ish): home grown electronics is typically in version 2-5.
- The combination of cheap processors such as Raspberry Pi, BeagleBone and Arduino, combined with the WWW means progress goes incredibly fast as solutions are known instantaneously
- Developers are like the Borg: and **resistance is futile..**

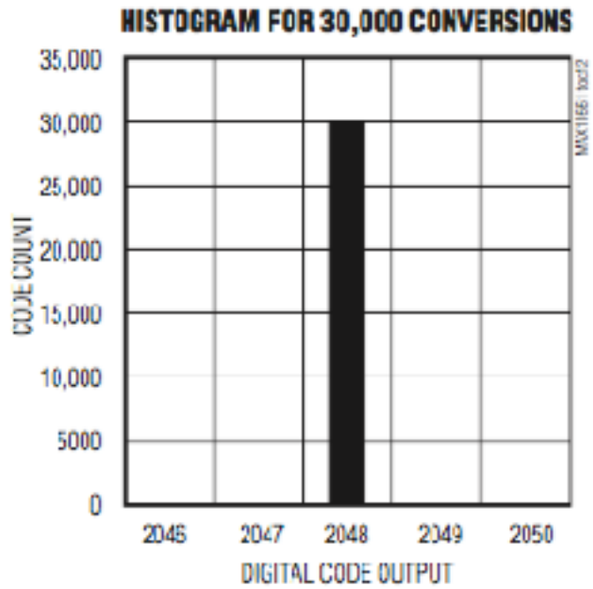
Sample & Hold ADCs

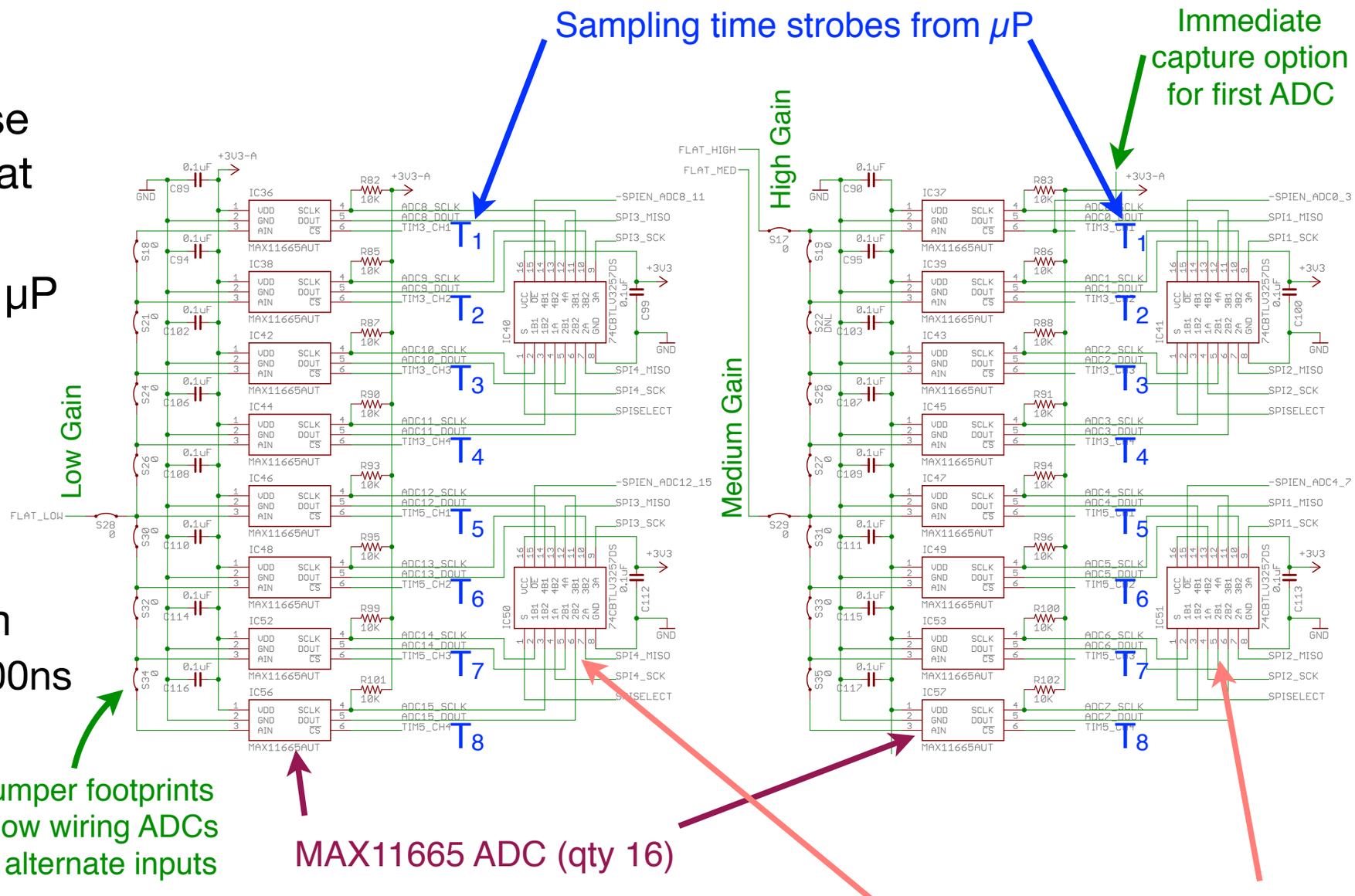
- Each ADC is single 12-bit sample
  - MAX11665 / Analog bandwidth 40MHz / $2
  - V2 board has 16 of these, can be wired to low, medium or high gain preamp/shaper output
  - Readout via SPI, 2µsec

- Timing signals from µP close the sample & hold window at certain delays after T_{start}
  - Utilizes circuits built into µP
  - Eight individual times available in V2 design

- Delays set up in software, *e.g.,* measure integrals from 0–10ns, 0–30ns, 0–50ns, 0–100ns

➠ Arrival time profile

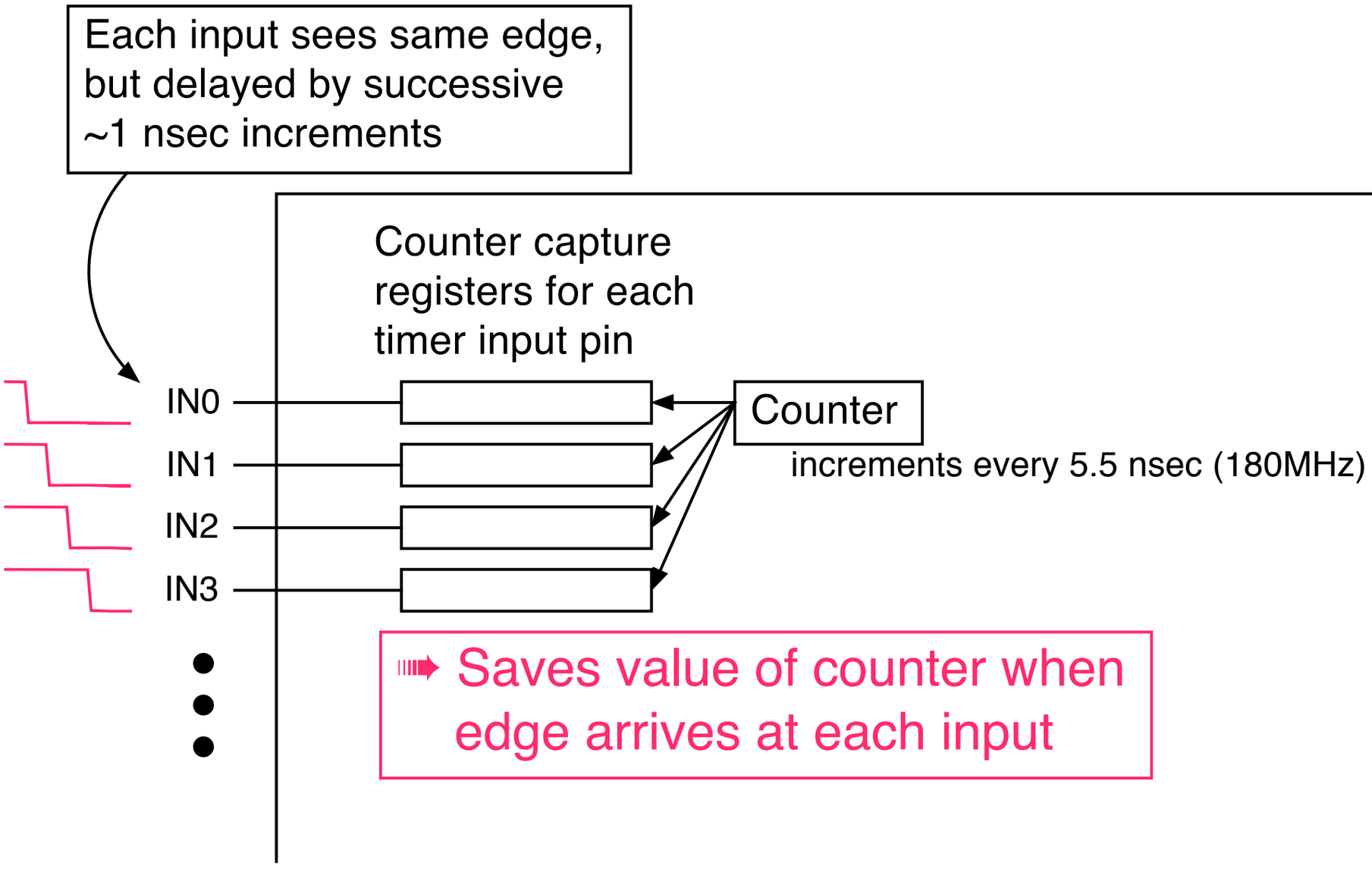




How time capture works

- Internal microprocessor clock is synchronized to White Rabbit via timing inputs
- Internal clock counters increment +1 after every 5.55nsec
- Use built-in “counter capture” registers to record photodetector pulse times

  ➡ Integer multiple of 5.55nsec



Response to a Discriminator Trigger

Discriminator Trigger

Hardware

- Output of delay line triggers μP time capture events (rising & falling edges)

➡ μP Interrupt

- μP generates ADC sample stops after programmed delays

Software

- Read time capture registers
- Compute average time
- Read ADC values via SPI interface (8Mbps, 4 chan's)
- Package hit data, add to buffer (128KB RAM)
- Reset trigger logic & enable