A fast monolithic pixel detector in a SiGe Bi-CMOS process

Lorenzo Paolozzi

On behalf of the **TT-PET collaboration**

The TT-PET project

The TT-PET collaboration

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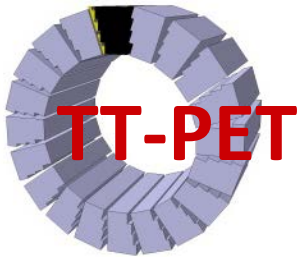
A 3-year project financed by SNSF to produce a PET Scanner for small animals **based on silicon detector technology,** insertable in an MRI machine and with 30ps RMS time resolution. The project started in March 2016.

The TT-PET collaboration:

- University of Geneva ⟹ Front End Electronics and detector design.
- University of Bern
- Hôpital cantonale de Genève
- INFN of Roma Tor Vergata ⟹ Front End Electronics and detector design.
- CERN
- Stanford University

Other collaborators:

- Ivan Peric – Karlsruhe Institute for Technology
- IHP Microelectronics



The Thin-TOF PET Scanner

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A compact and thin Time Of Flight PET detector device for small animals with Depth-Of-Interaction measurement capability.

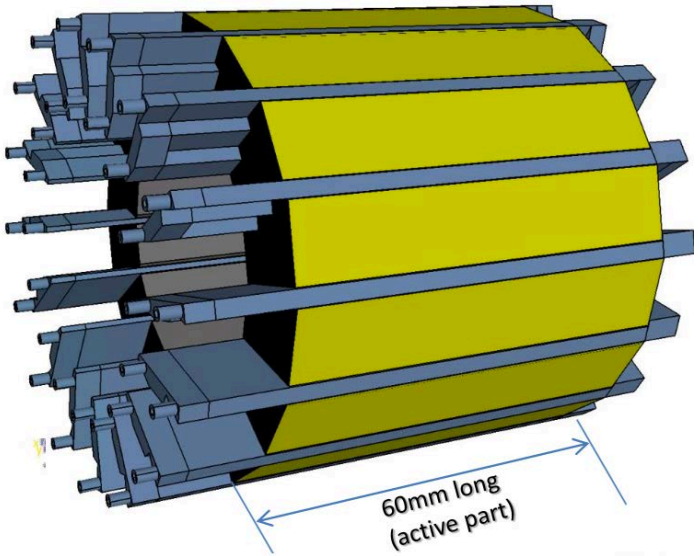
- Total thickness: **2 cm** → To be inserted in an MRI scanner.
- 3D photon-detection granularity of **1.0 x 1.0 x 0.2 mm^3** → Negligible Depth-Of-Interaction error.
- TOF measurement on annihilation photons at **30ps** level → ~1cm resolution along Line-Of-Response; reduction of image background.
- **Silicon** technology for particle detection → Use in magnetic field and future possibility to extend scanner field of view.
- **Monolithic** sensor integration → Simpler implementation of the layered structure for a PET scanner.

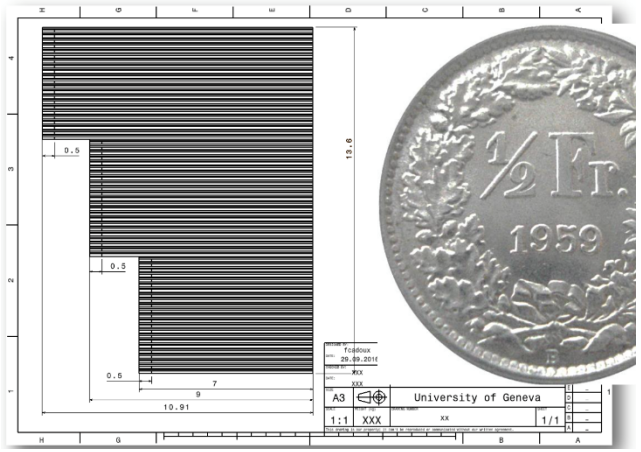
Sensor layout

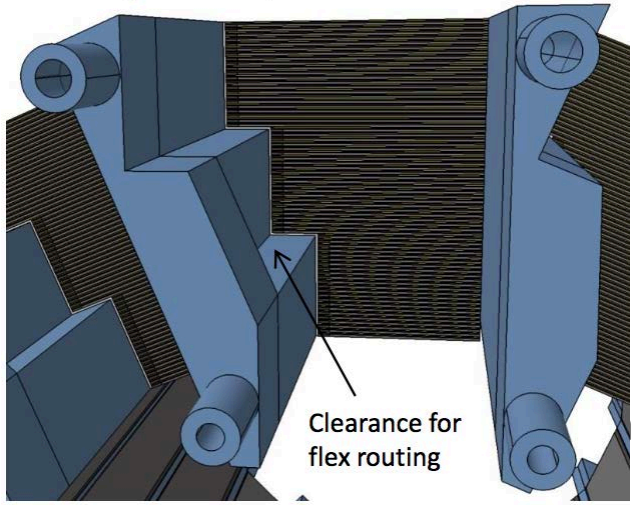
- **Dielectric** for signal extraction, capacitive decoupling and low energy electron absorption
- **Large PAD** (1mm^2) readout to ensure uniform electric and weighting field
- **Thin sensor** (100µm) to minimize time-walk correction
- **Monolithic technology**: the electronics is embedded in the sensor. No need of wire bonding
- **High Z converter**, thickness optimized with dedicated simulation

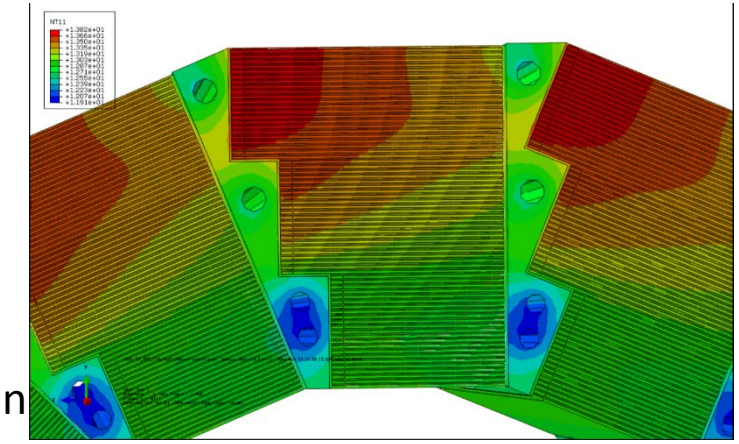
Monolithic integration of SiGe Bi-CMOS technology will lead to low cost production of fast, solid state sensors.

Scanner layout









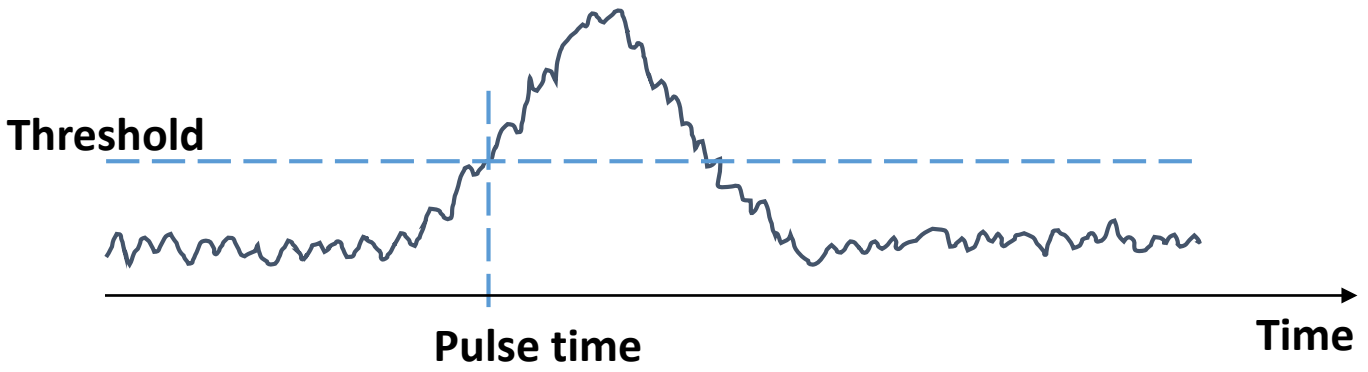
- 16 wedge-shaped units, called “cells”.
  - ↳ A cell is a stack of up to 100 detection layers
- **Cell efficiency for 511 keV photons: up to 50%.**
- More than 600.000 channels on 2112 chips synchronized at 10ps.
- FEA simulations performed
- Cooling Block is currently under revisions for production and tests
- Flex design finalized, first prototype in production soon.

Strategy for time measurement

Amplifier contribution to time resolution

Detector time resolution depends mostly on the amplifier performance.

$$\sigma_t = \frac{\sigma_V}{\frac{dV}{dt}} \cong \frac{t_{rise}}{Signal/Noise}$$



Minimization of ENC for a fast integrator

Fast integrator: $BW \cong 100\ MHz$ ⟹ Avoid larger analogue bandwidth

$$ENC^2 \propto \left(2q_e I_C + \frac{4kT}{R_P} + i_{na}^2\right) \cdot \tau + \boxed{(4kTR_S + e_{na}^2) \cdot \frac{C_{in}^2}{\tau}} + 4A_f C_{in}^2$$

Dominating term

Excellent performance in terms of series noise for fast shaping are achievable with the BJT technology

$$ENC_{series\ noise} \propto C_{in} \sqrt{2kT\langle SNI \rangle \left[\frac{h_{ie}}{\beta} + R_{bb}\right]}$$

Transistor ENC contribution depends on current gain and base spreading resistance

SiGe technology for very low-noise, fast amplifiers

Amplifier current gain can be expressed as (NPN BJT)

$$\beta = \frac{i_C}{i_B} = \frac{\tau_p}{\tau_t}$$

τ_p = hole recombination time in base

$\boldsymbol{\tau_t}$ = **electron transit time (E to C)**

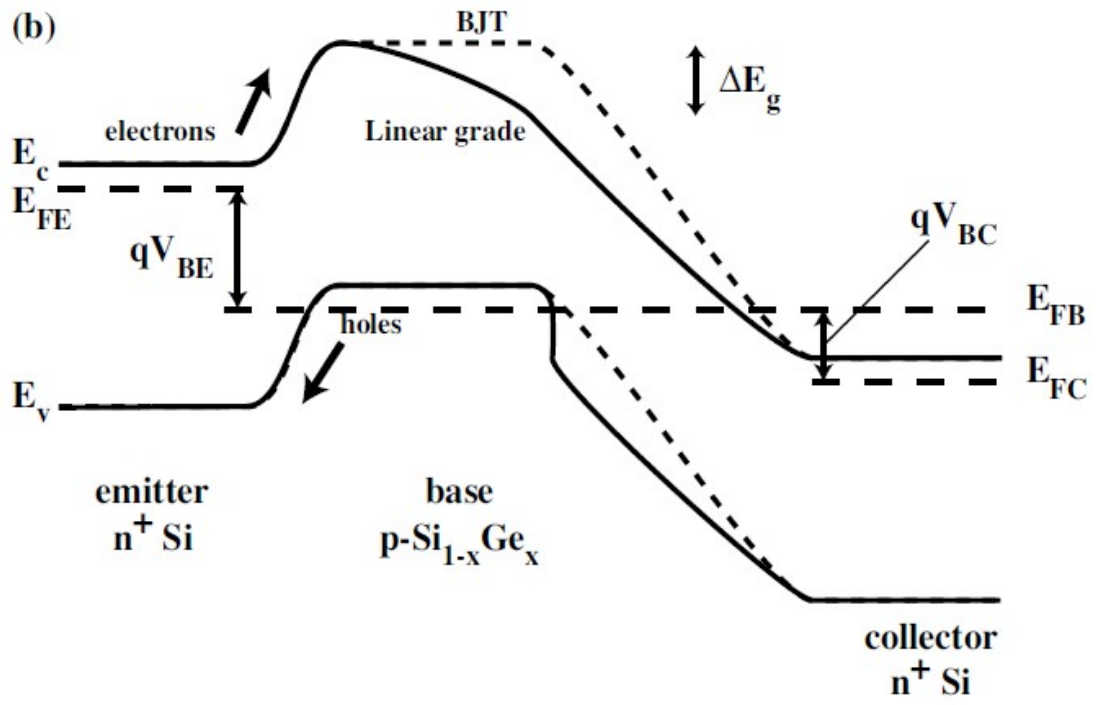
Need to minimize electron transit time in the base

Increase gain ⟺ Reduce base width ⟹ Reducing base doping

Spreading resistance increases!

SiGe technology for very low-noise, fast amplifiers

A possible approach: changing the charge transport mechanisms in the base from diffusion to drift.



Equivalent to introducing an electric field in the base.

SiGe heterojunction bipolar transistor technology.

The technology we chose is **SG13S from IHP:**

$\beta = 900$

$f_t = 250\ GHz$

Why SiGe Bi-CMOS – Signal amplification

- An intrinsically low series noise → excellent performance for fast pulse integration
- High f_t at low collector current → fast amplifiers with very low-power consumption
- Small size transistors with high β at high f →
  - High gain amplifiers on large capacitance
  - Performance improvement on small capacitance
- Fast growing technology → 700 GHz f_t transistors under development

Target performance for the SiGe amplifier in ASIC

- $ENC \cong 700\ electrons\ RMS\ on\ 1mm^2\ pads$
- $T_{rise} \lesssim 1\ ns.$
- $W \cong 14\ mW/cm^2$
- $\frac{dV}{dQ} = 90\ mV/fC$

Design in IHP SG13S technology.
Several MPW runs (see below).
First measurements compatible with simulations

To start with, we designed a SiGe amplifier, and produced it with discrete components.

Measured performance:

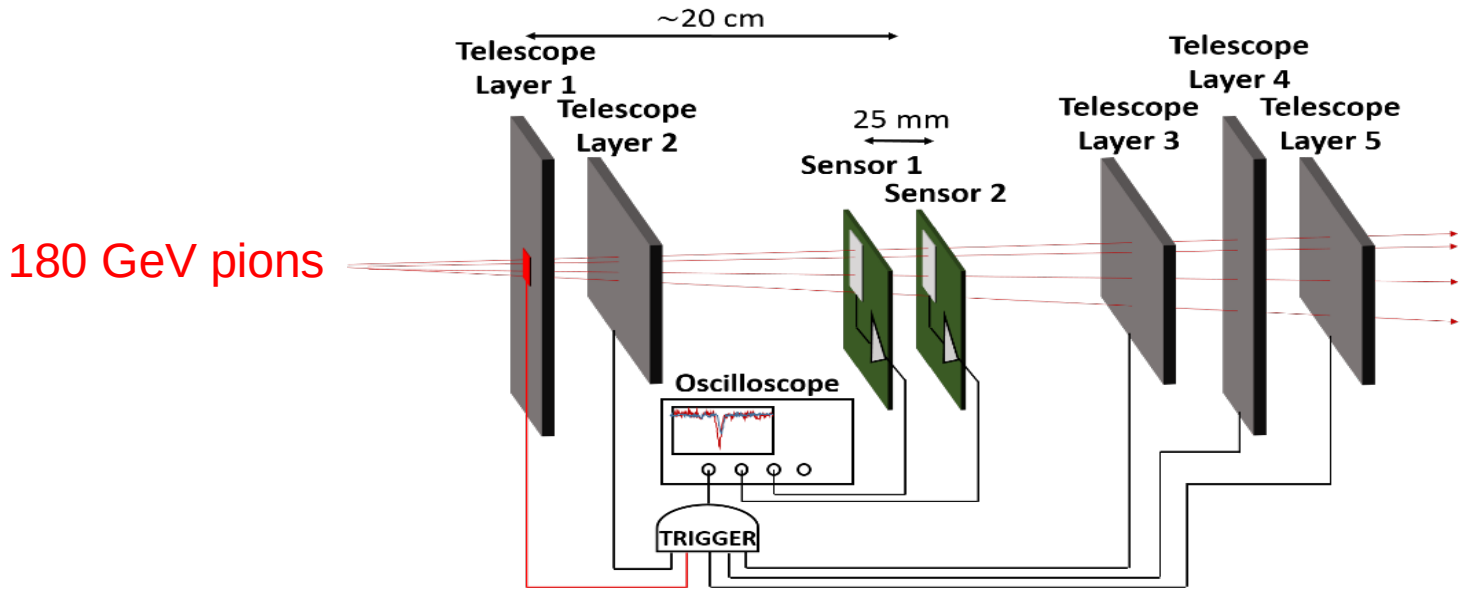
- $ENC \cong 550\ electrons\ RMS\ on\ 1\ pF$
- $T_{rise} \cong 1.0\ ns.$
- $W \cong 14\ mW/channel$

100 ps time resolution measured in these working conditions.

Time resolution measurement with MIPs at CERN SPS

using 100µm thick silicon sensors

Testbeam experimental setup



Detectors under test:

- **100µm thick** p-on-n VTT silicon sensors with **1mm^2** area readout pad ($\gtrsim$ **1 pF** capacitance).
- Signal amplified by means of custom amplifier with commercial SiGe HBT transistors.
- Amplifier is used with inverse dynamics due to constraints on sensor polarization.

Signal digitized with Lecroy WaveMaster 820zi oscilloscope.

Trigger produced by the external telescope.

Trigger area limited to 500µm x 500µm (centered on test detectors) by the first telescope layer, to evaluate efficiency.

Testbeam experimental setup

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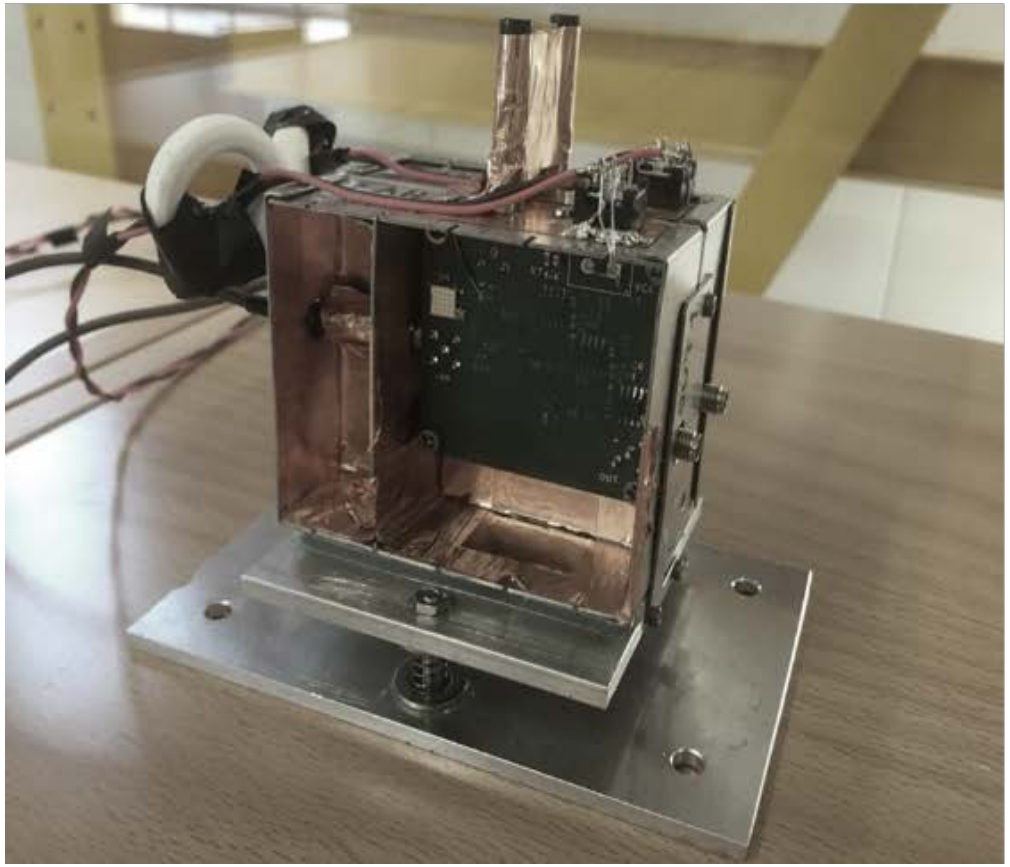
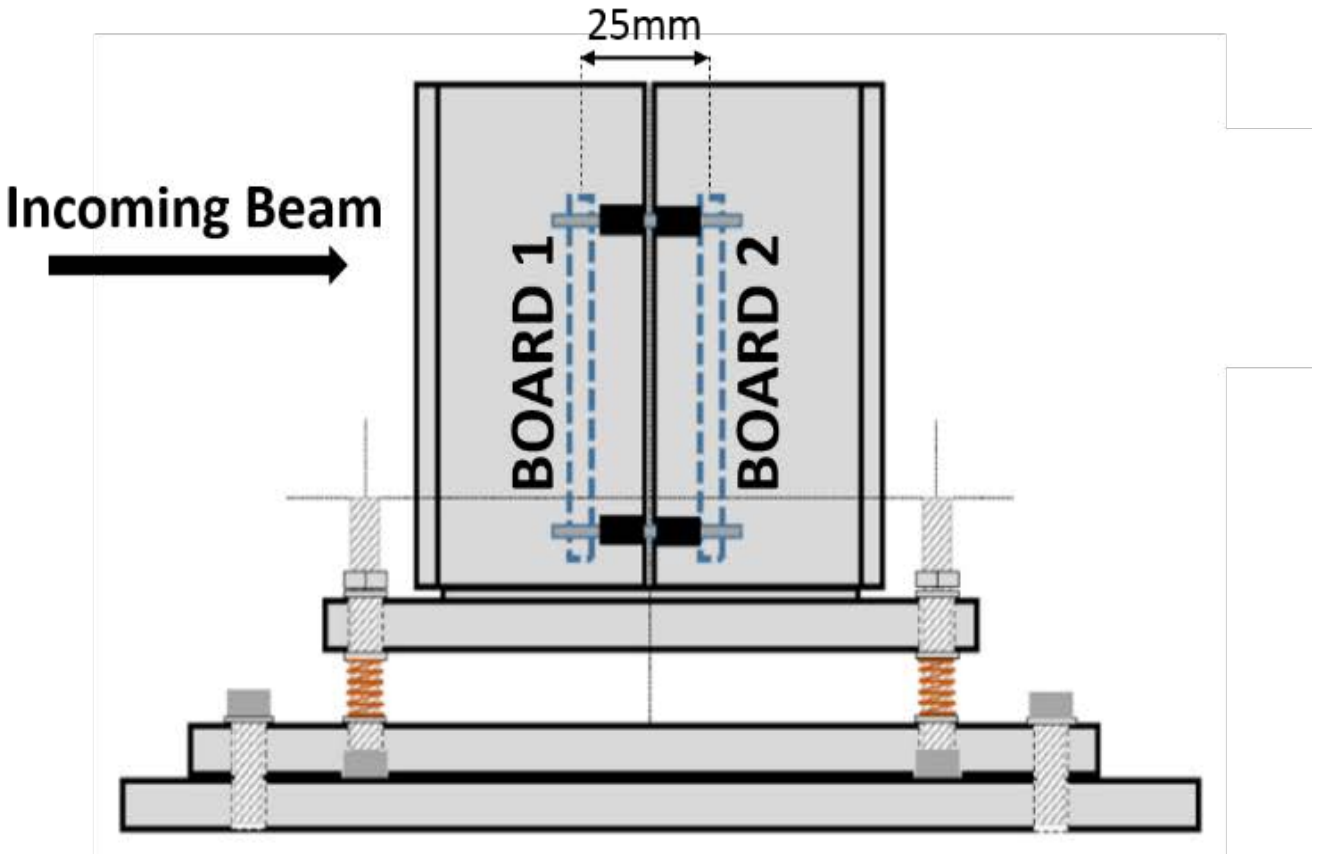
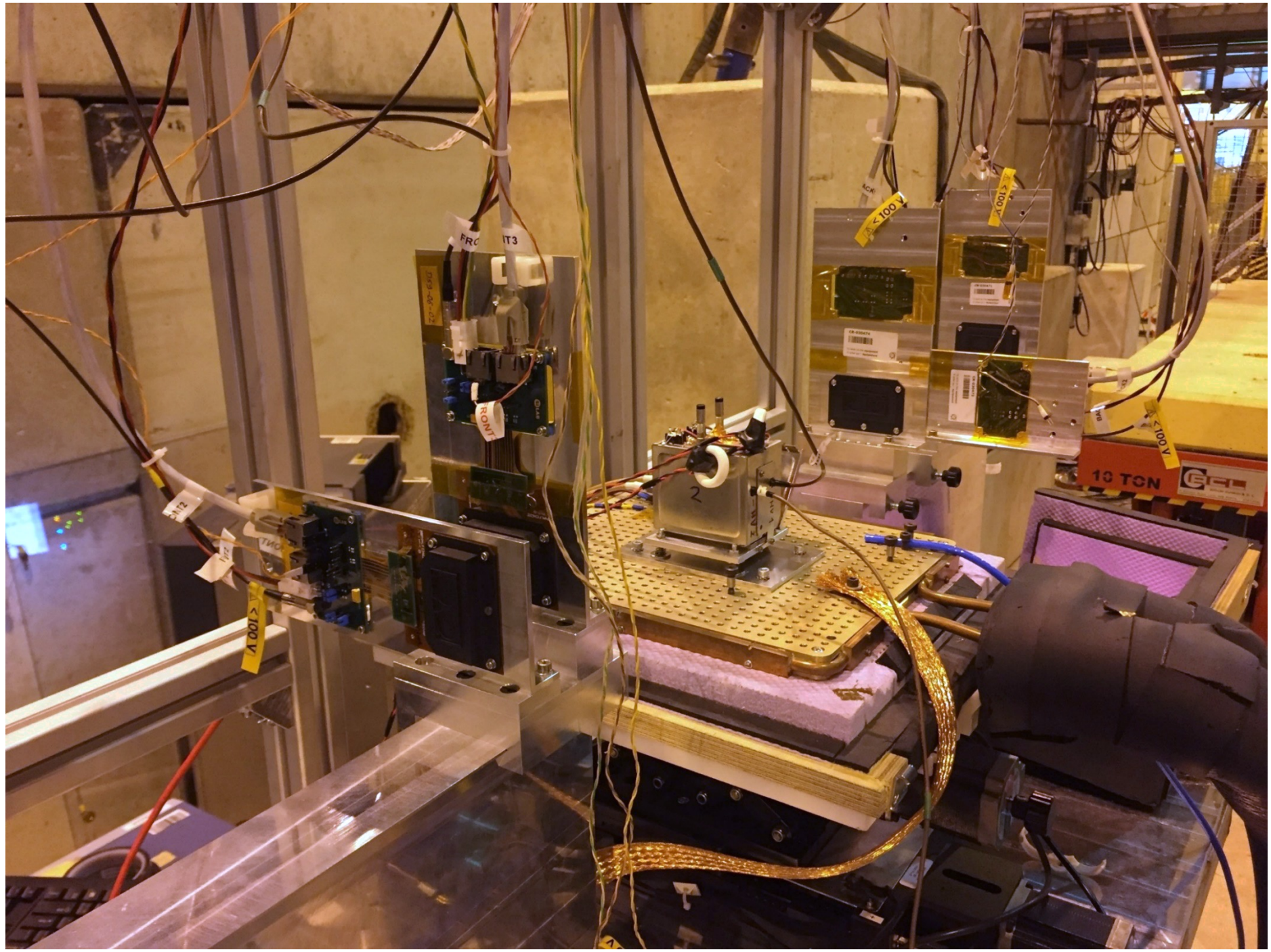
Mechanical support



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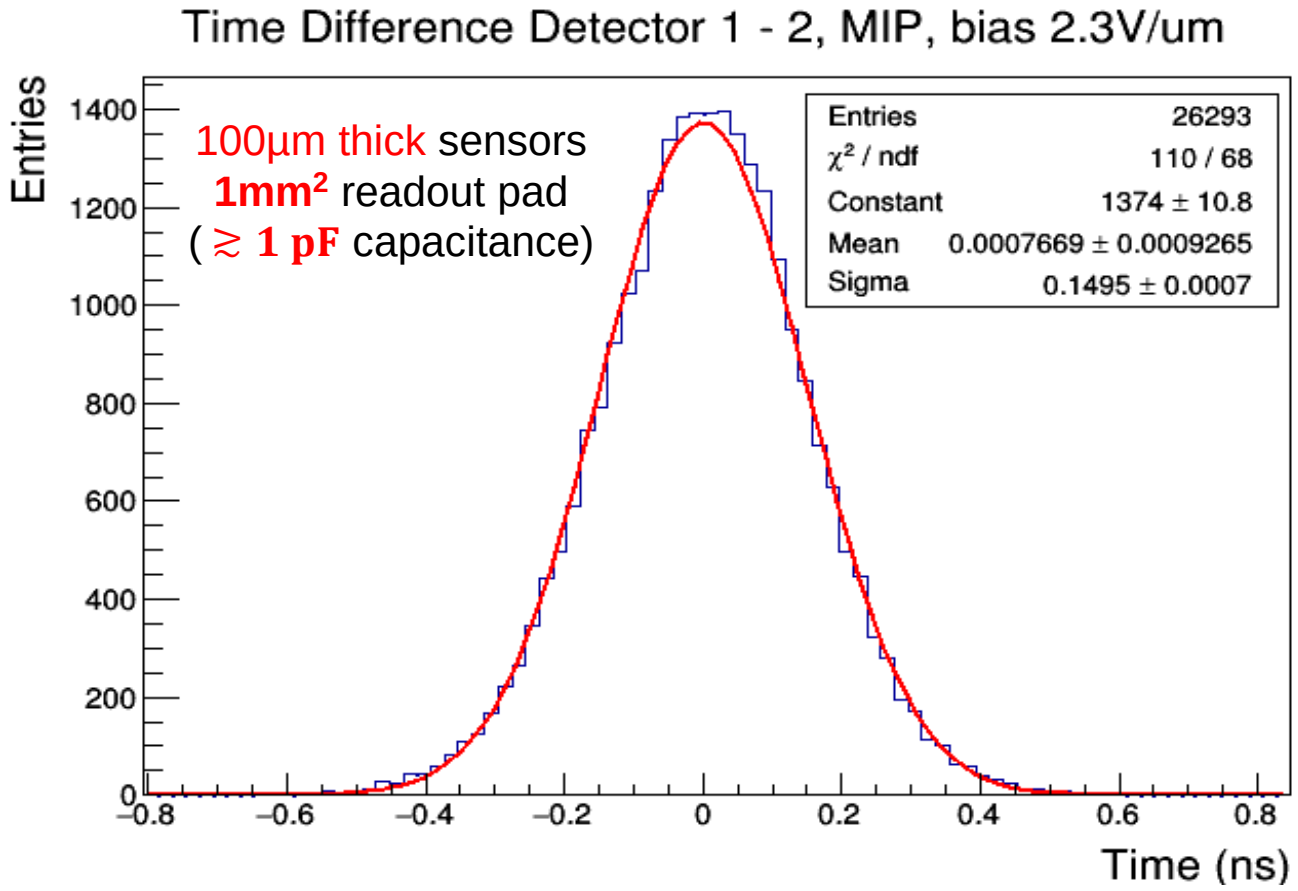
First measurement of time resolution for minimum ionizing particles with VTT silicon detectors and our discrete component SiGe amplifier



Result for MIPs:
(assuming both detectors have same time resolution)

$$\sigma_t = \frac{(150 \pm 1)ps}{\sqrt{2}} = (106 \pm 1)ps$$

Largely dominated by the sensor resolution

Published in:

JINST P03011, Vol. 11, 2016
http://dx.doi.org/10.1088/1748-0221/11/03/P03011

"100ps time resolution with thin silicon pixel detectors and a SiGe HBT amplifier"

Meets the goal of the TT-PET project: simulation shows that this result corresponds to 24ps in the case of 511keV photons

SiGe ASIC development

Towards a monolithic ASIC:

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Sensor and analogue components development

- A monolithic detector with 30ps time resolution
- A sub-ns rise-time amplifier with 700 electrons RMS noise operating on 1pF capacitance and with $14 mW/cm^2$ power consumption
- A $20 ps$ TDC with low power consumption ($\sim 1 mW/channel$) (and a very simple schematic)

Towards a monolithic ASIC:

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First Challenge: Time resolution of 30ps for a PET scanner.

- This target value seems to be achieved from calculations and extrapolating from test-beam results.
- A 20ps TDC with $1mW/channel$ power consumption is being developed.

Second challenge: The power consumption.

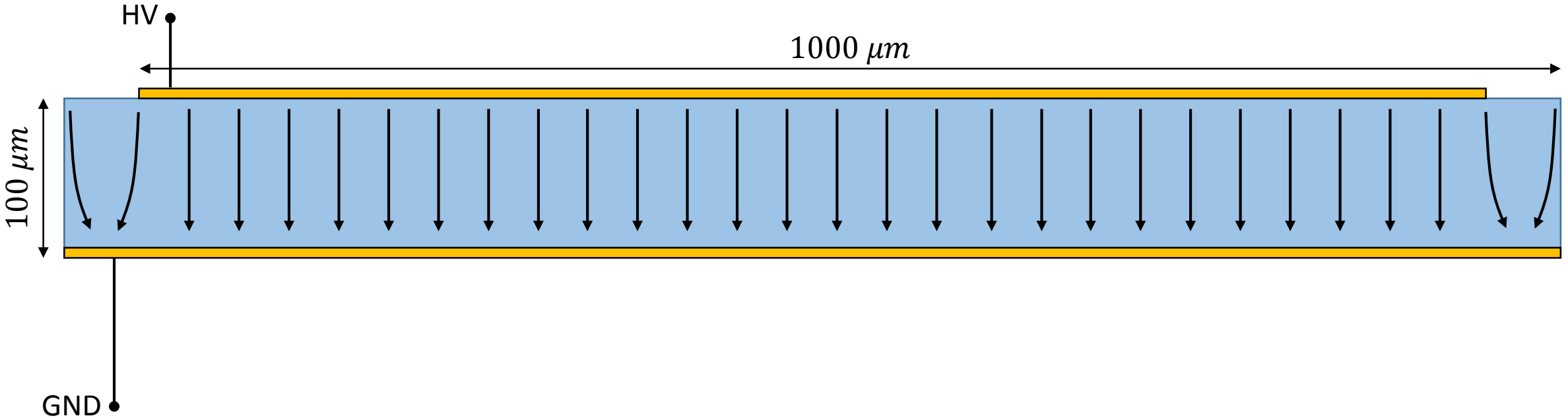
- The test-beam results shown were obtained with a power consumption of $\sim 14mW/channel$.

  ⟹ The target power consumption is $140\mu W/channel$ ($14mW/cm^2$).

Third challenge: Monolithic integration.

- The monolithic integration requires to define a strategy on the sensor design to have a simple and effective structure, a detailed simulation work and collaboration from the foundry.

Sensor optimization for time measurement



Fundamental parameters:

- Uniform electric field (charge transport)
- Uniform Ramo Field (signal induction)
- Charge drift velocity saturation

Intrinsic time fluctuations independent from the particle trajectory.

Sensor structure

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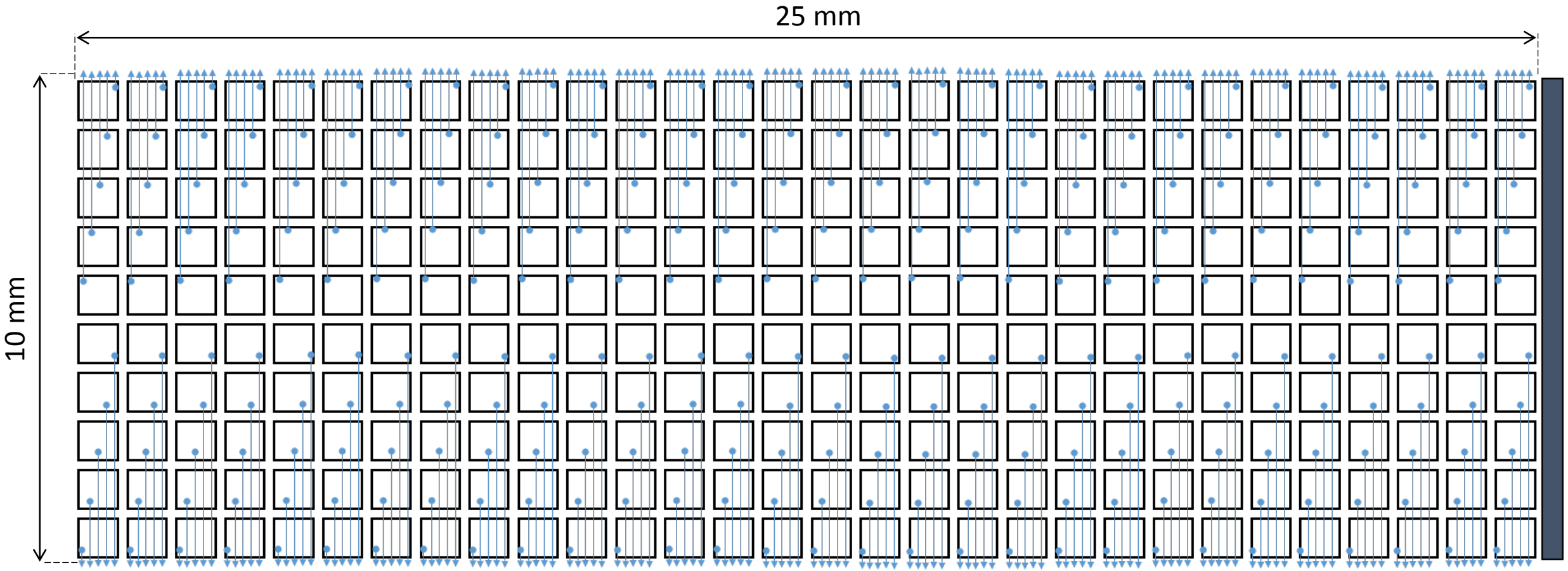

- HV applied on the pads, inside the Guard Ring.
- Amplifiers and comparators as close as possible to the pad.
- Time digitization and logic on the short side of the chip.

Status of the project: foundry MPW submissions

- April 2016
  - **Amplifier design.**
- September 2016
  - **Monolithic test and full analogue chain.**
- December 2016
  - **TDC and Read-Out logic.**
- April 2017
  - **Demonstrator.**

Technology:

SG13S by IHP microelectronics

SiGe HBT performance:

- $f_t = 250\ GHz$
- $\beta = 900$

First ASIC submission: April 2016

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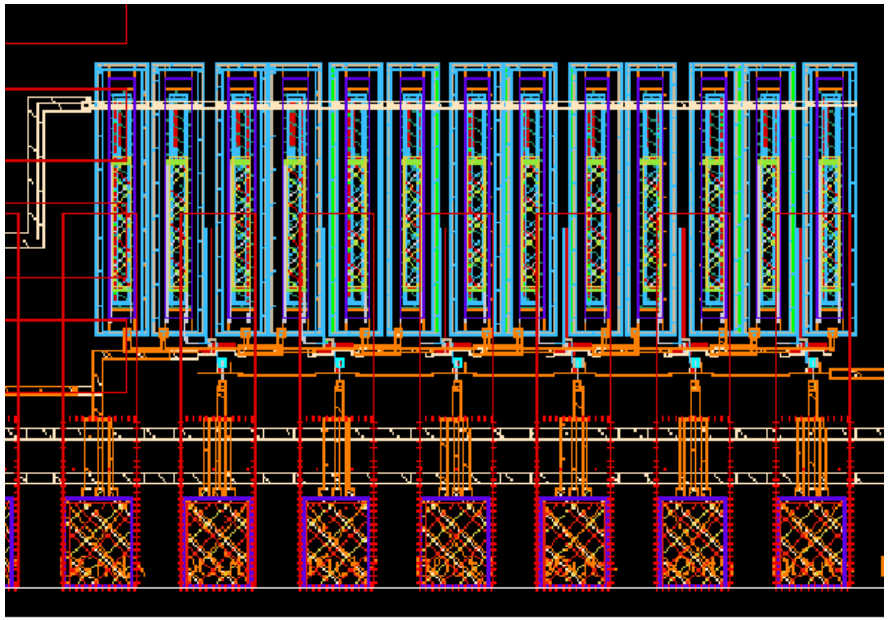
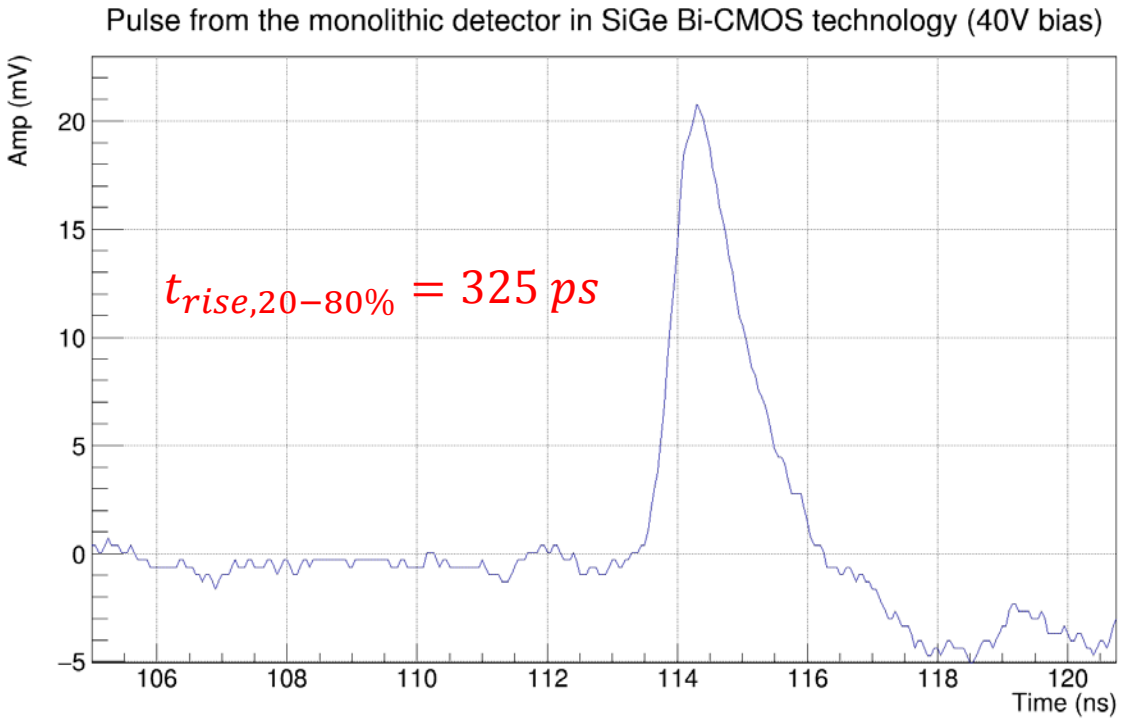
- Amplifier in IHP SG13S technology
- TDC core elements
- Monolithic sensor – Low voltage (~40V) sensor
  (expertise on monolithic sensor design from Ivan Peric)

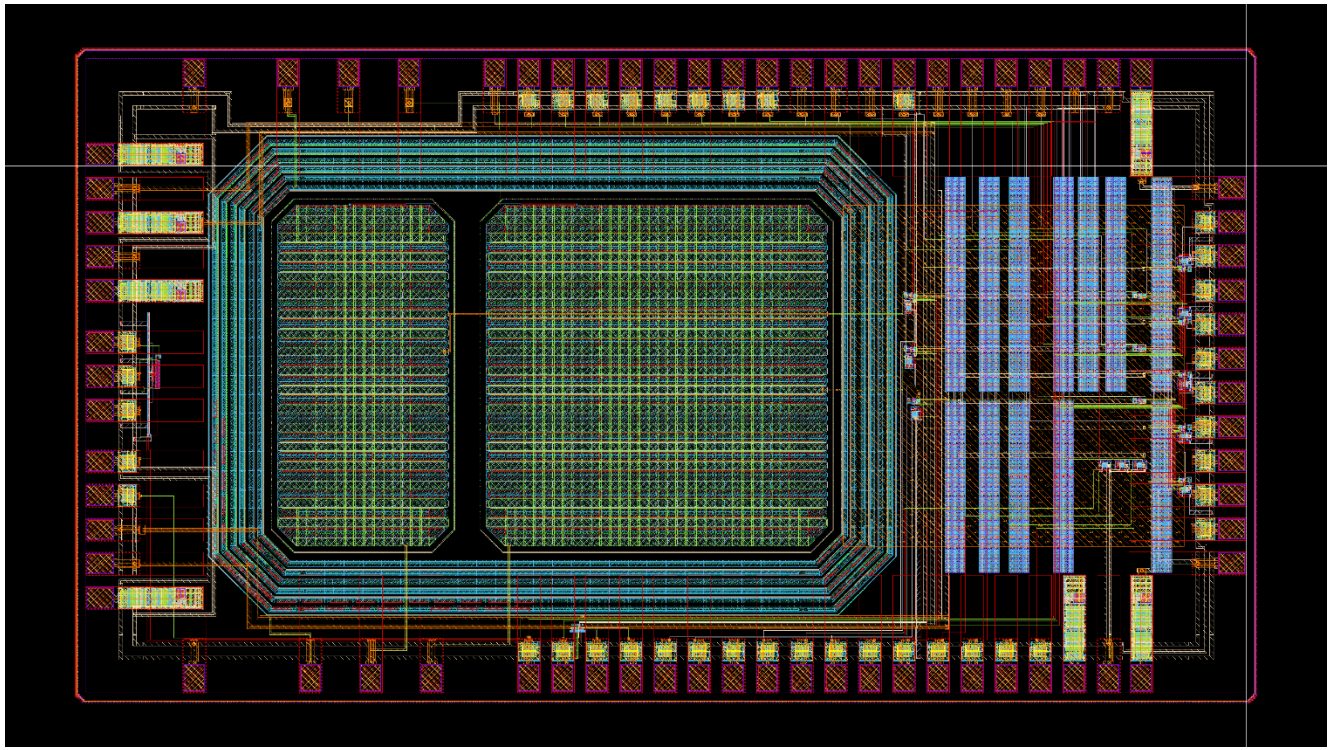




- The sensor is functional. First implementation of a monolithic sensor in SiGe Bi-CMOS technology.
- The amplifier performs very fast integration with very low power consumption (estimated: ***150µW/channel***).
- The core elements of the TDC are working properly.
- Sensitivity to ESD; to be improved.

Second ASIC submission: September 2016

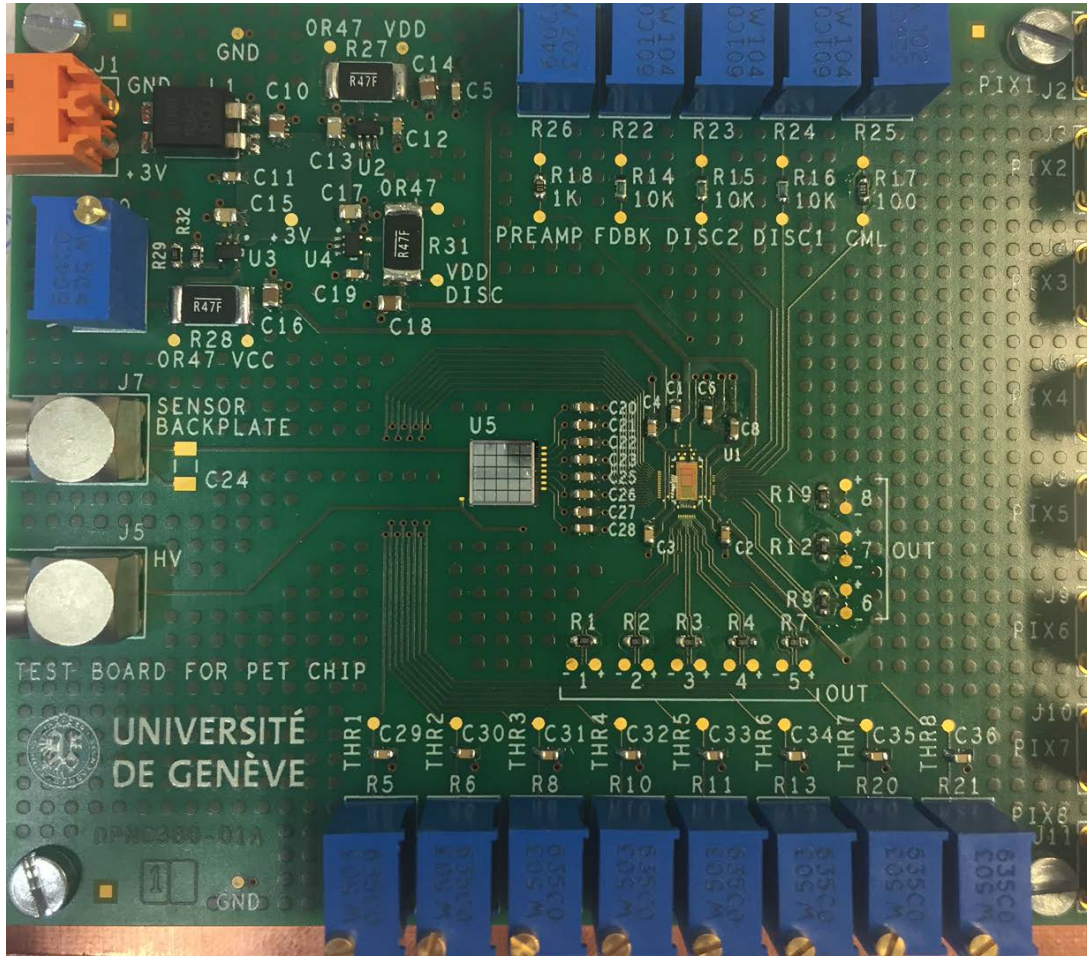
- Discriminator in SG13S (MOSFET) technology
- Monolithic sensor, final design – Two pads with independent FE chains
- Guard Ring
- Full analogue electronic chain



- The sensor can be read either with a front-end chain directly connected into the chip or with an external pad.
- Full depletion of $100\ \mu m$ sensor thickness for substrate resistivity $\rho \geq 500\ \Omega\ cm$.
- The guard ring should withstand a potential of 300V on a resistivity of $1\ k\Omega\ cm$. The potential of the inner ad outer rings can be forced.

Second ASIC submission: September 2016

Test of the full analogue chain with pulsed signal: preliminary results.



Full analogue chain is stable, no oscillation nor significant cross talk observed

Gain: $\gtrsim 80\ mV/fC$.

ENC: $\lesssim 1000\ e^-\ RMS$ at $1pF$ capacitance

Analogue pulse rise time: $1.2\ ns$

Power consumption: $14\ mW/cm^2$

Tests with Strontium source on a $100\ um$ thick sensor in progress.

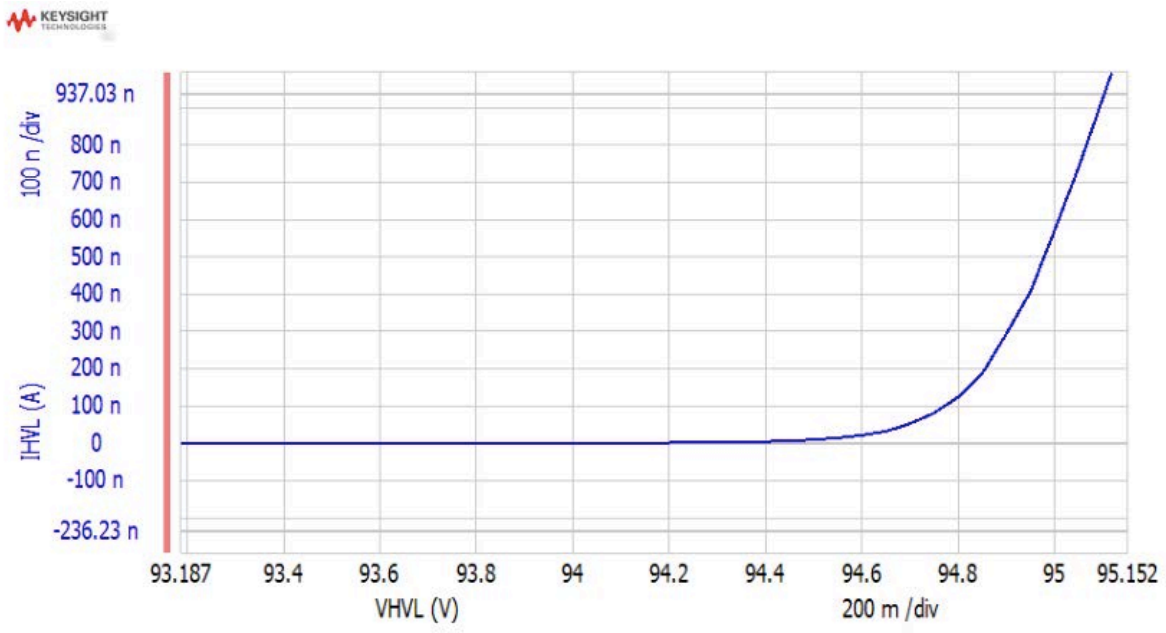
Second ASIC submission: September 2016

- Discriminator in SG13S (MOSFET) technology
- Monolithic sensor, final design – Two pads with independent FE chains
- Guard Ring
- Full analogue electronic chain

TEST OF THE GUARD RING

Low resistivity wafer ($50\ \Omega \cdot cm$).

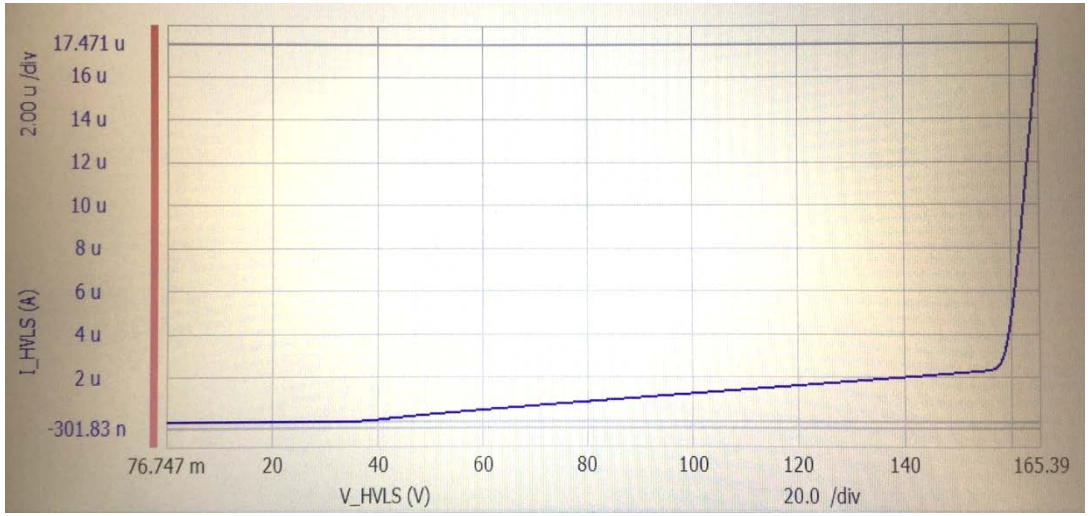
I-V curve compatible with simulation.



High resistivity wafer ($1\ k\Omega \cdot cm$).

High current at 40V due to poor backside contact.

Guard Ring BD at 165V, (over 200V by controlling the GR voltage)



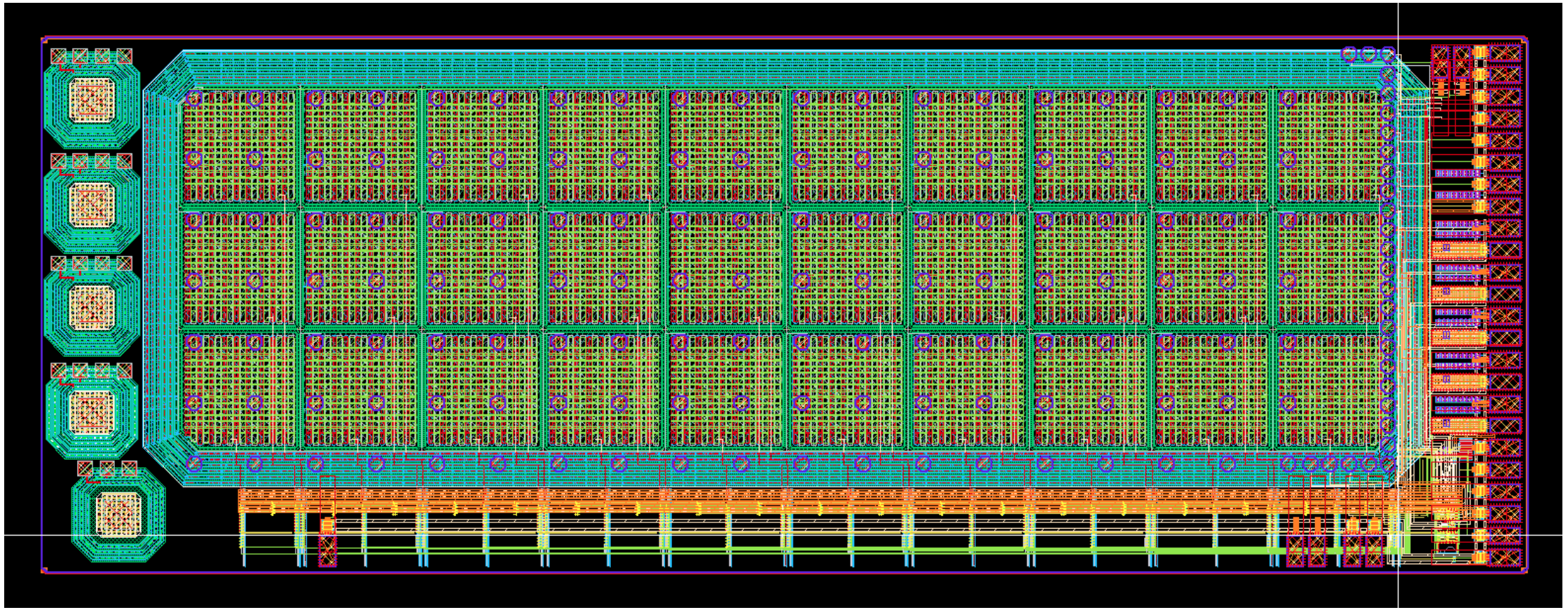
Third ASIC submission: December 2016

- Full TDC chain based on MOSFETs ($20\ ps$ time binning).
- TDC core elements based on HBTs ($\sim 5\ ps$ time binning).
- ESD protection structures.
- Readout logic.

Received in May 2017, tests in preparation…

Fourth ASIC submission: April 2017

- Demonstrator.
- Pixel Matrix with Guard ring, full analogue chain and TDC.
- On-chip timing data processing.
- Special Guard Ring test structures.



Status of the project: foundry MPW submissions

- April 2016 (delivered 08/2016)
  - Amplifier design ⟹ Working, but sensitive to ESDs
  - TDC ring oscillator, latch and decoder ⟹ Working within specifications
  - Single-side monolithic structure ⟹ Working at 40V

- September 2016 (low resistivity delivered 01/2017; high resistivity delivered 02/17)
  - Full Front-End chain ⟹ Preliminary: stable, compatible with simulations.
  - Double-sided monolithic structure ⟹ Preliminary: diode has characteristic curve and is sensitive to light
  - Guard ring ⟹ Breakdown above 200V. Backside processing to be improved.

- December 2016 (delivered 05/2017)
  - ESD protection structures
  - ReadOut logic
  - Complete TDC in MOSFET technology
  - TDC elements in BJT technology

Engineering run foreseen in November 2017

- April 2017 (Submitted 04/2017)

In a demonstrator:
- Full chain (sensor to digital)
- Multiple 0.5mm^2 pixels (3x10 matrix)
- On-chip timing data processing

In a separate chip
- Test structures
- Guard rings / ESD protections
- Differential receivers

Conclusions

- Very fast and low-power SiGe amplifier designed
- Testbeam measurements show time resolutions for MIPs of 100ps with standard silicon sensors
- Monolithic ASIC implementation in IHP SG13S process with 1mm pixel pitch ongoing, through several Europractice MPW
- Engineering run foreseen in November 2017
- Further improvement is possible thanks to the fast developing SiGe technology.

Thank you!

Extra Material

Why SiGe Bi-CMOS – Time digitization

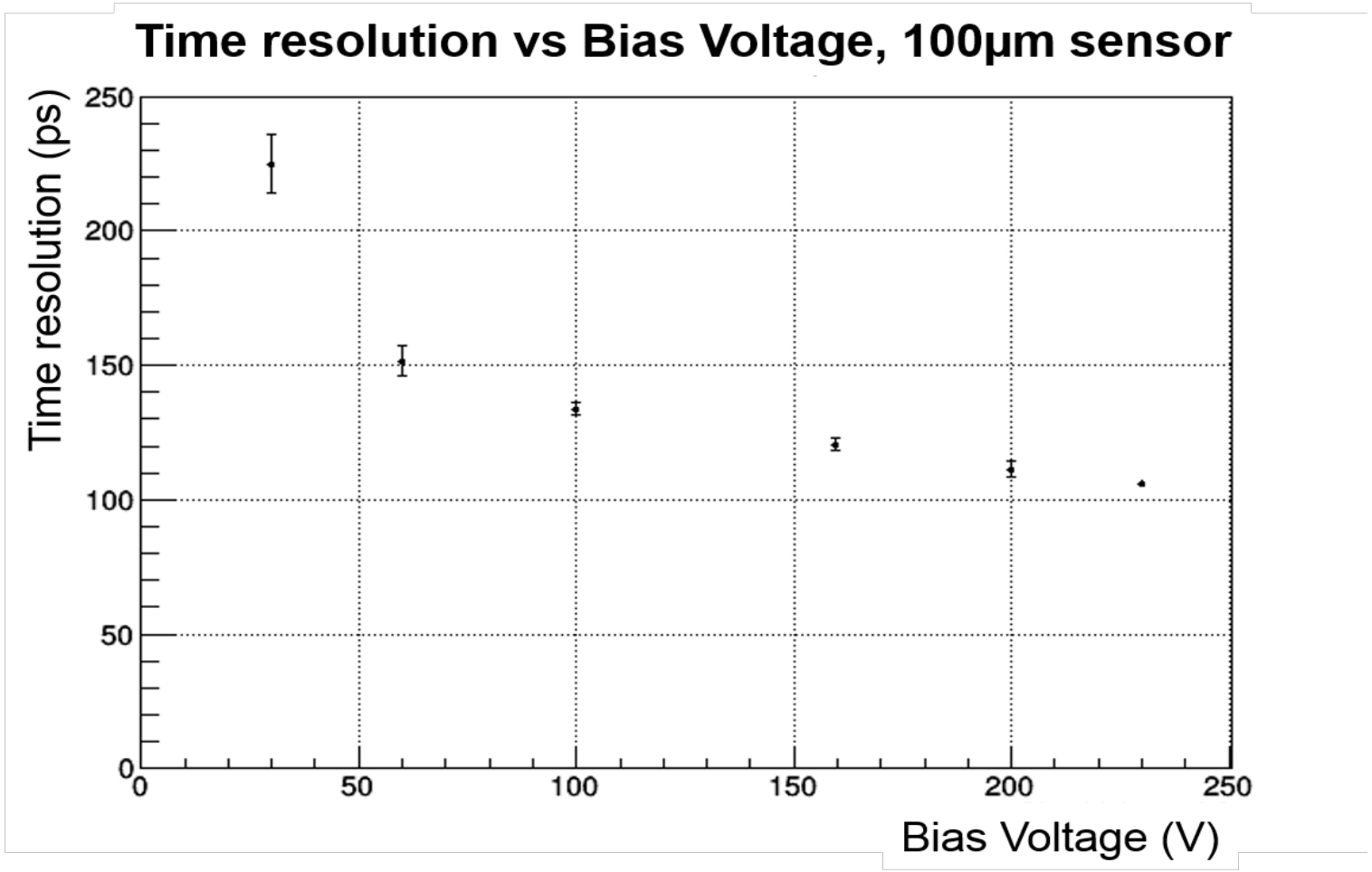
Exploit the properties of state of the art SiGe transistors to produce extremely precise TDC.

IHP SG13S technology: transistor performance $f_t = 0.25\,THz$ $f_{max} = 0.3\,THz$ $\beta = 900$

- Few picosecond buffer delay (down to 8ps with this technology).
- Delay precision of the order of ~ 100 fs.
- $> 40\,GHz$ oscillation frequency can be easily achieved with a purely digital schematics.

TDCs with a time binning down to 4ps and a power consumption of $\sim 1 \frac{mW}{channel}$ can be designed with a very simple schematic.

Time resolution studies



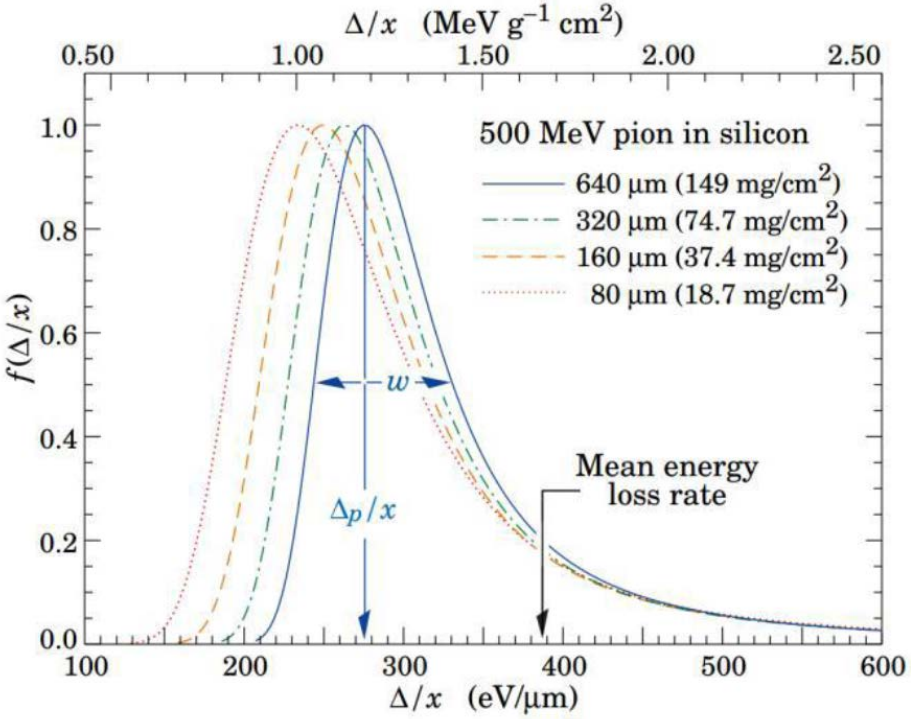
All measurements are done in the same experimental conditions.

Charge collection noise

- Time resolution for semiconductor detectors with planar readout depends on signal to noise ratio.
- The noise introduced by the source is typically negligible with respect to the one from the amplifier itself.

For a time resolution **below $100\ ps$**, another source of noise should be introduced, that we can call **charge collection noise**[1].

When the ionizing particle traverses the detector, ionization occurs following Landau statistics.



From PDG

Most of the produced clusters have a small charge.
Few events with very large transferred energy are possible.

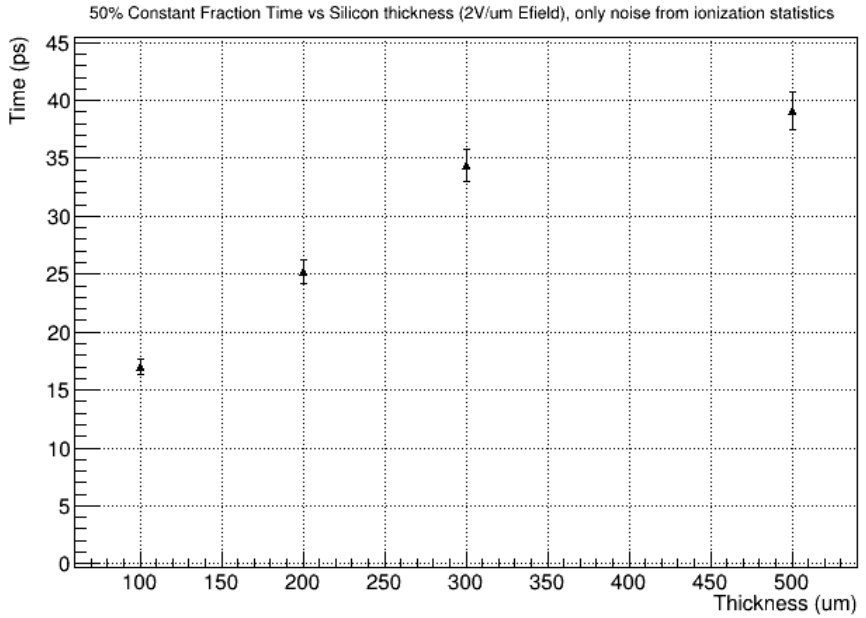
[1] L. Paolozzi, *Development of particle detectors and related Front End electronics for sub-nanosecond time measurement in high radiation environment.* PhD thesis, University of Roma Tor Vergata (December 2014)

Charge collection noise

The induced current for a parallel plate readout, from Shockley-Ramo's theorem is:

$$i_{ind} = -\frac{qv}{D}$$

When the large clusters are absorbed at the electrodes, their contribution is removed from the induced current.
The statistical origin of the variability of the induced current makes this effect irreducible, so that it can be considered as an equivalent noise current.



Simulation: Time jitter introduced by the charge collection noise (or Landau noise) for a silicon detector traversed by a Minimum Ionizing Particle (MIP).