

The hardware fast-track trigger for the ATLAS High Luminosity Upgrade

The expected factor of 10 increase in peak luminosity of the upgraded High Luminosity LHC will force the ATLAS experiment to increase early stage trigger selection power. The agreed strategy is to implement precise track reconstruction, through which sharper trigger turn-on curves can be achieved for primary single-lepton selections, while contributing to b-tagging and tau-tagging techniques as well as multi-jet rejection.

The challenge in such a project comes from the development of a fast custom electronic device integrated with the hardware-based first trigger level of the experiment, with repercussions propagating as far as the detector read-out philosophy. This talk will discuss the requirements, architecture and projected performance of the system in terms of tracking capability, latency and trigger selection, based on detailed simulations. Studies are carried out comparing two possible geometries of the new ATLAS silicon tracker, whilst testing a set of different trigger configurations obtained by varying the detector granularity, coincidence layers and implemented algorithms. Based on these studies, we give an initial estimate of the latency and of the bandwidths of such a system as required at each step of the processing.

Summary

(Summary material in attached PDF)

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Track Classification: Trigger and data acquisition systems