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The Phase-1 Upgrade of the ATLAS First Level Calorimeter Trigger

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The ATLAS Level-1 calorimeter trigger is planning a series of upgrades in order to face the challenges posed by the upcoming increase of the LHC luminosity. The hardware built for the Phase-1 upgrade will be installed during the long shutdown of the LHC starting in 2019, with the aim of being fully commissioned before the restart in 2021.

The upgrade will benefit from new front end electronics for parts of the calorimeter which provide the trigger system with digital data with a tenfold increase in granularity. This makes possible the use of more complex algorithms than currently used and while maintaining low trigger thresholds under much harsher collision conditions. Of principal significance among these harsher conditions will be the increased number interactions per bunch crossing, known as pile-up.

The Level-1 calorimeter system upgrade consists of an active and a passive system for digital data distribution and three different Feature EXtraction systems (FEXs) which run complex algorithms to identify electromagnetic energy deposits, taus, hadronic jets, large area jets as well as total and missing transverse momentum. These algorithms feature isolation criteria and pile-up subtraction techniques as well as multiplicity determination for large area jets. The algorithms are implemented in firmware on custom electronics boards with up to four high speed processing FPGAs. The identified trigger objects are transmitted to the topological trigger system, which counts the objects with energies above configurable thresholds and performs various topological trigger algorithms combining the properties of different objects.

The main characteristics of the electronic boards are a high input bandwidth up to several TB/s per module implemented through optical receivers and a large number of tracks (up to several hundred) providing high speed (up to 12.8 Gb/s) connections on the modules between the receivers and the FPGAs as well as between the FPGAs for data sharing. The PCB design uses modern materials and signal routing is supported by modern design tools to ensure a high level of data integrity. The used electrical power is estimated to be up to 400 W per module, which necessitates careful design of the power distribution and heat dissipation system. Extensive simulation studies are carried out to understand and optimise the characteristics of the modules. Prototypes have been built and extensively tested to prepare for the final design steps and the production of the modules. The contribution will give an overview of the system and discuss the module design challenges. Extensive tests of the boards, including tests of the data transmission between modules, will be reported.

Summary

Summary material available in attached document.

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