Development of CaRIBOu: A Modular Readout System for Pixel Sensor R&D

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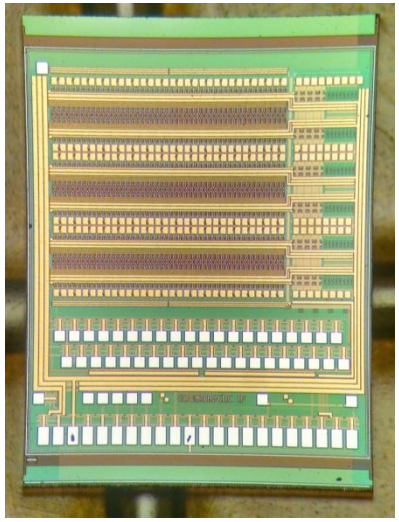
Outline

- Motivation
- Hardware
- Firmware & Software
- Testbeam Deployment

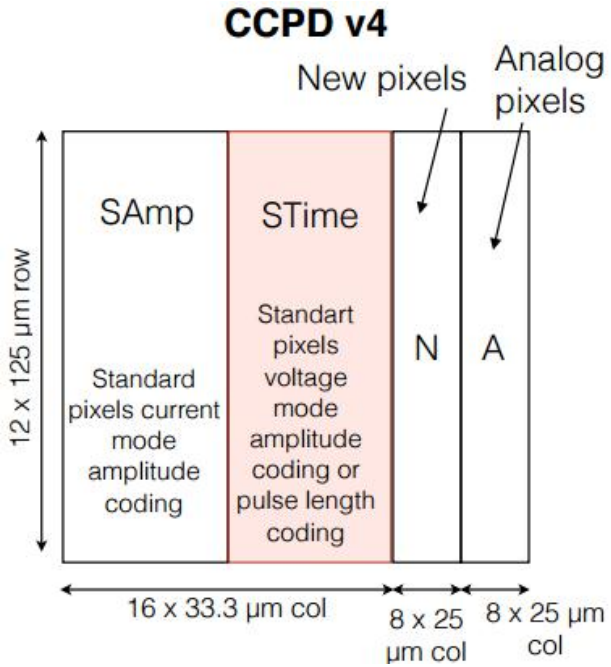
Motivation

- Develop a modular readout system for CMOS sensor R&D
  - Easily adapted to various sensors under development;
  - Carefully defined interface to minimize the effort of design revision for different sensors;
  - Module design tailored to a specific readout chip (e.g. FE-I4B);
  - ZYNQ FPGA with embedded ARM processor to simplify the firmware and software development;
  - Versatile interface to DAQ PC (e.g. GbE, PCIe);
- Open architecture welcomes contribution from collaboration
  - New module development is possible for new readout chip and new sensor;
  - Interface to official ATLAS TDAQ system (e.g. FELIX);
  - Make better use of different expertise (e.g. hardware, firmware, software and system integration);

Sensors to be Test - AMS 180nm



H18V4



- H18CCPDV4/5/6
  - 60 X 12 pixels;
  - Pixel Size: 50 x 250 um;
  - AMS 180nm High-voltage process ;
  - Configuration: LVCMOS18 x 4;
  - Readout through FE-I4B;

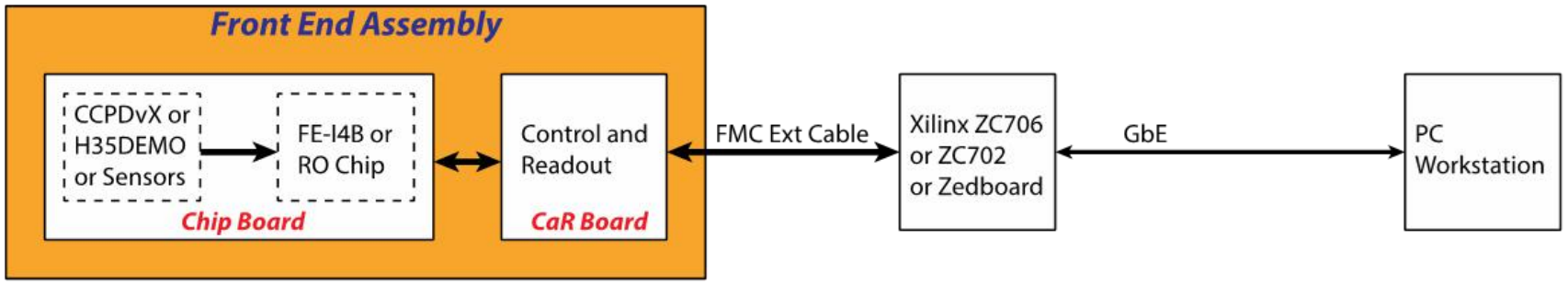
Sensors to be Test – AMS 350nm

LAYOUT of H35DEMO

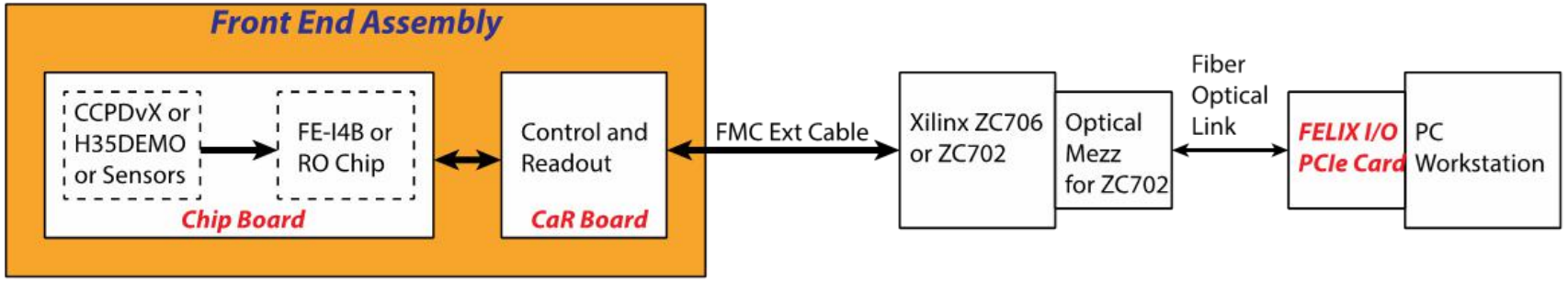
- H35DEMO
  - AMS High-Voltage 350nm process
  - Chip Size: 18.5mm x 24.4mm
  - Pixel Size: 50 x 250 um
  - 78 rows x 300 columns
  - 4 x independent matrixes
    - 2 x Standalone matrix
      - 16 rows x 300 columns
    - 2 x Analog matrix
      - 23 rows x 300 columns
  - All matrix can be readout through FE-I4B;
  - nMOS and CMOS matrix has stand alone readout capability;

System Overview

Configuration 1

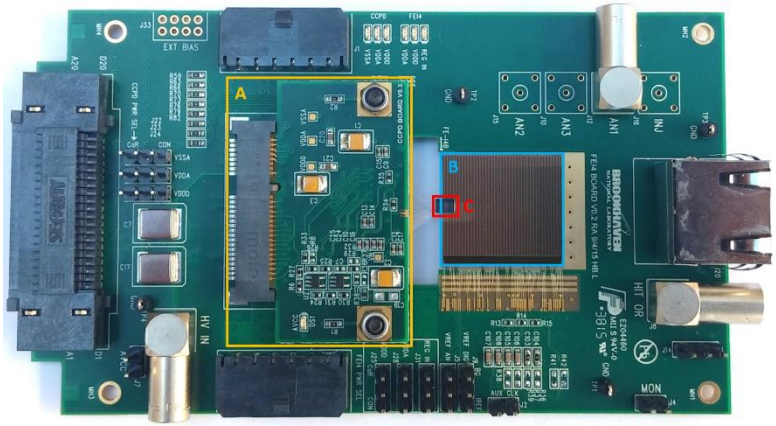


Configuration 2

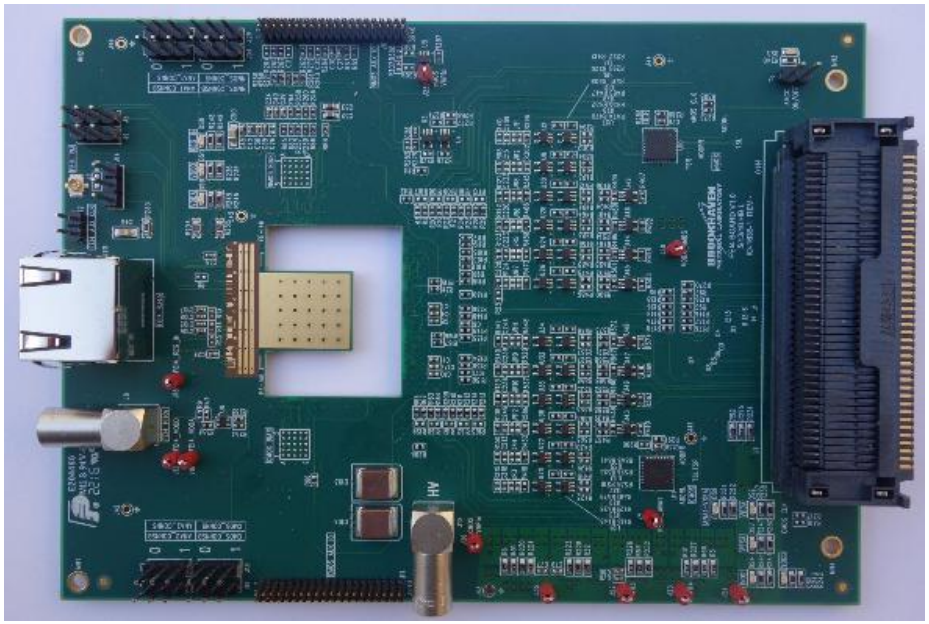


- Two configurations have been implemented;
- Two versions of CaRIBOu hardware:
  - CaRIBOu V0: small scale sensor test => H18V4/5/6
  - CaRIBOu V1: full scale sensor test => H35DEMO

Hardware – Chip Boards



FEI4 Board V0 with CCPD board plugged in. (A: CCPD board; B: FE-I4B; C: CCPD H18V4 sensor;

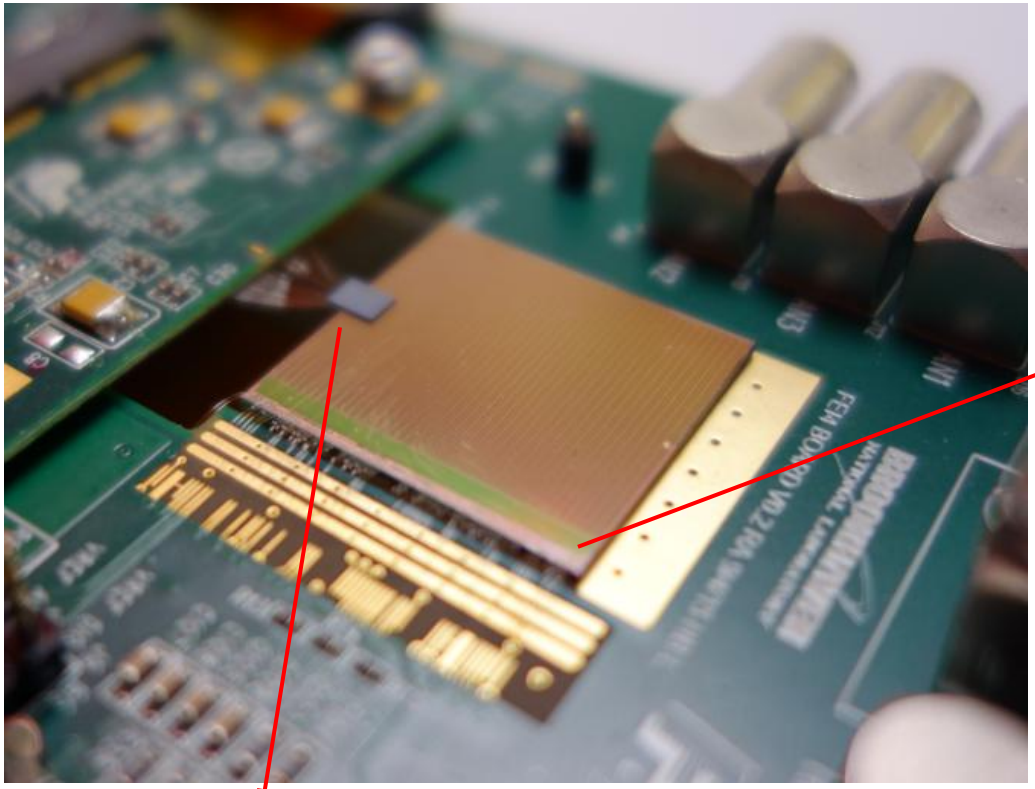


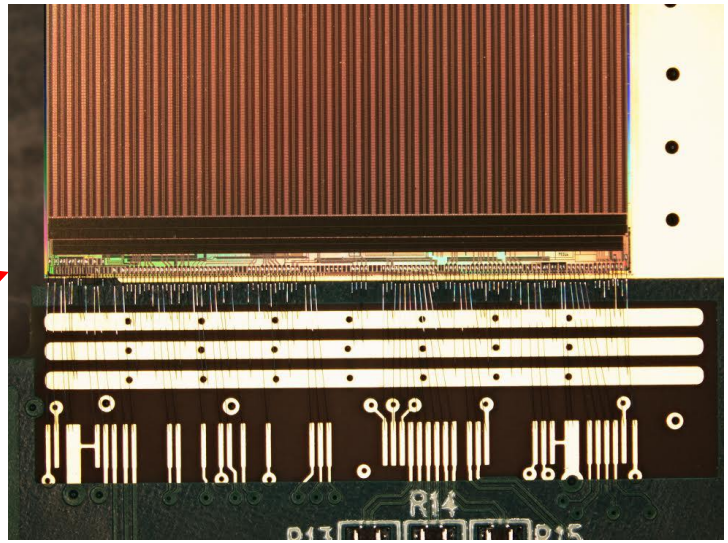
FEI4 Board V1

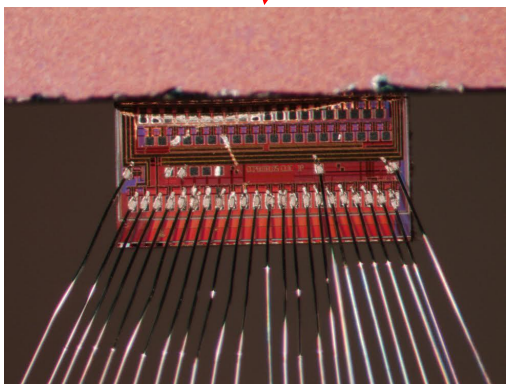
Features of CaR (Control and Readout) Board

- Chip Boards are sensor specific board;
- The sensor and read out chip are mounted on this board;
- Connections from sensor and readout chip to the chip board are implemented with aluminum wire bonding;
- Samtec SEARAY right-angle connector is used to connect with the CaR board;

Hardware – Chip Board Sensor Assembly



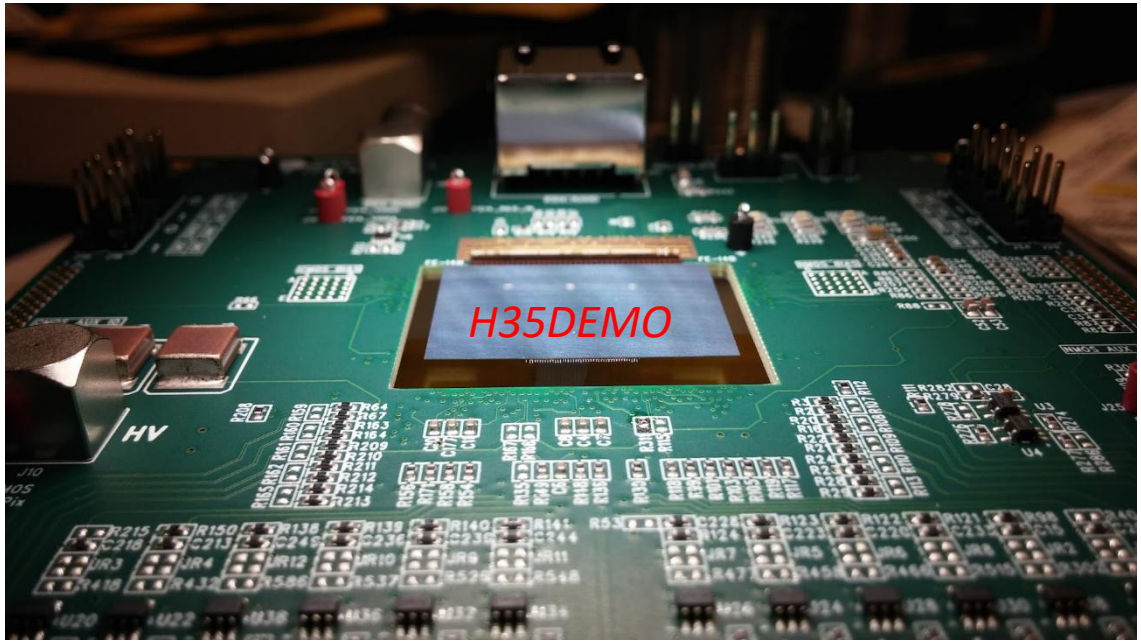




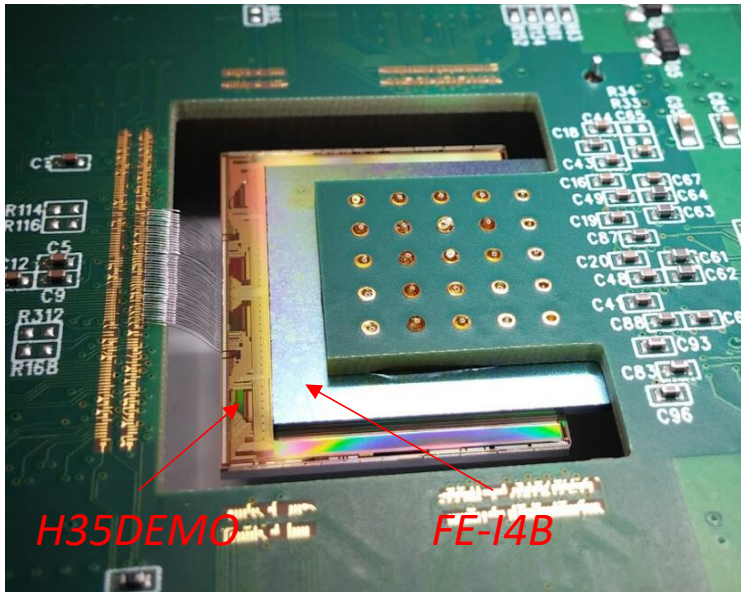
Assembly and wire bonding of CaRIBOu V0

- CCPD sensor is glued on FE-I4B chip, and wire-bonded to the bottom side of the CCPD board;
- FE-I4B is glued on the FEI4 board, and wire-bonded to the top side of the FEI4 board;

Hardware – Chip Board Sensor Assembly



FEI4 Board V1 (top side)



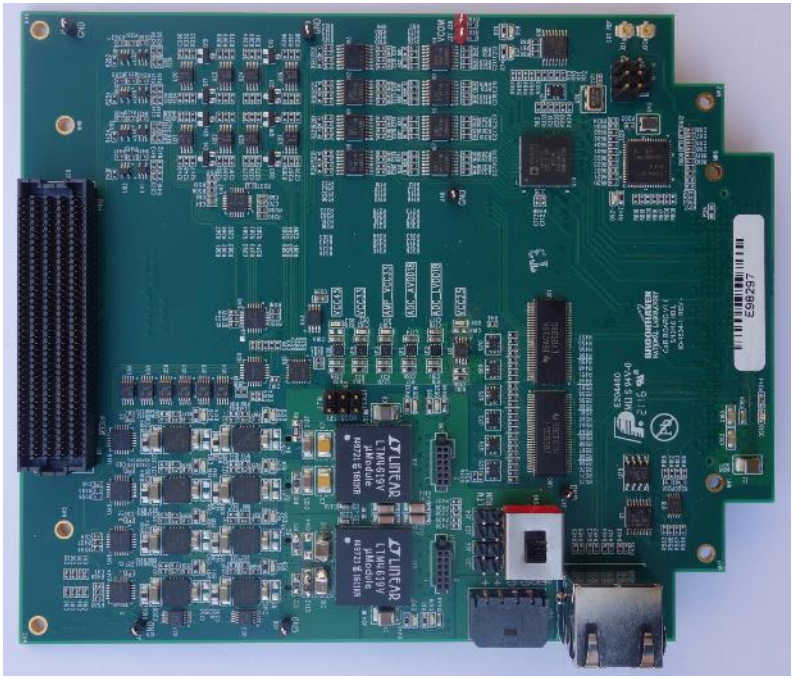
FEI4 Board V1 (bottom side)

Assembly and wire bonding of CaRIBOu V0

- The sensor H35DEMO can be glued on or bump bonded to the pixel readout chip FE-I4B;
- The wires for the H35DEMO are bonded to the bottom of the PCB board from three side;

Hardware – Control and Readout Board

CaR Board V0



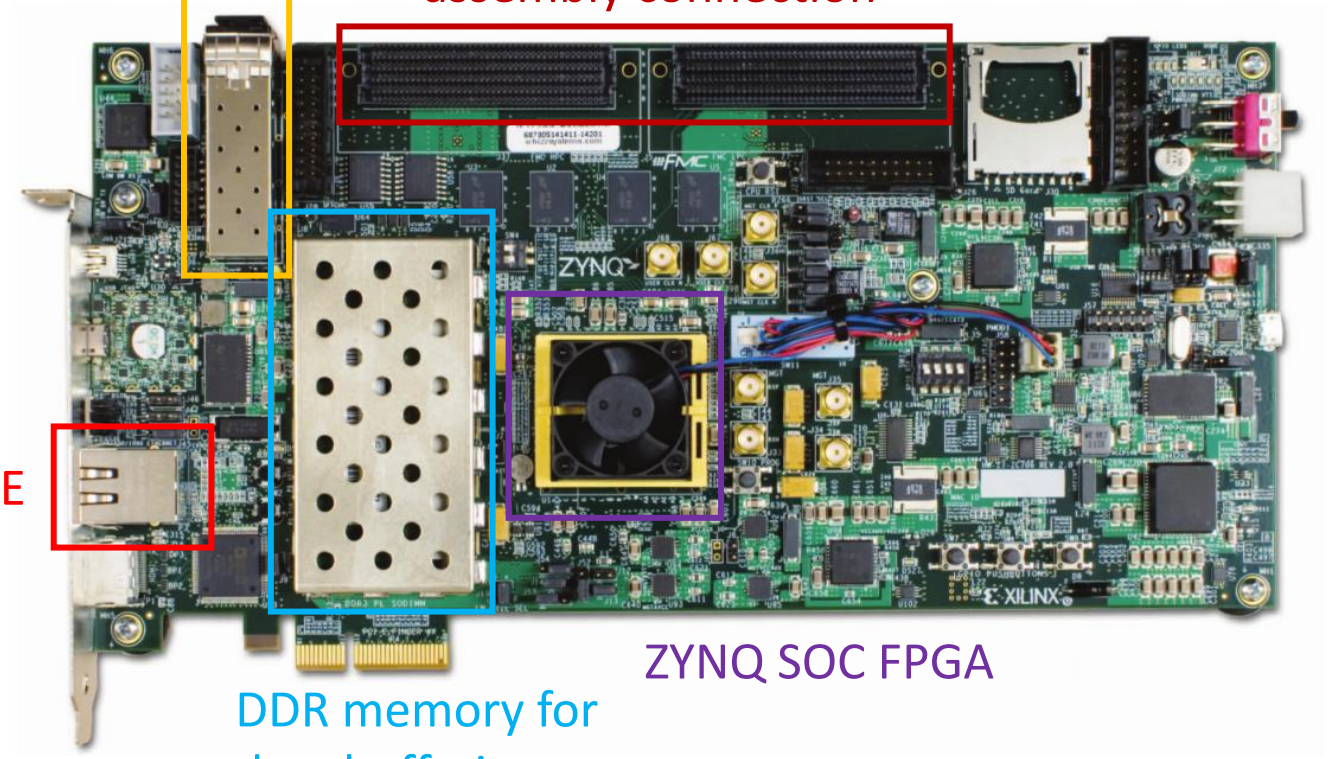
CaR Board V1

Features of CaR (Control and Readout) Board

- Adjustable power supplies with monitoring for chip board;
- Bias generators for sensor under test;
- Pulse generators for charge injection;
- High-Speed ADC for analog signal sampling;
- CMOS signals for sensor configuration;
- LVDS pairs for FE-I4B/sensor readout;
- Clock generator (only V1);
- Transceiver links available for chip boards;

- CaR Board V0: Less resources, more flexibility, can support two chip boards;
- CaR Board V1: More resources, but need a full FMC HPC connection;

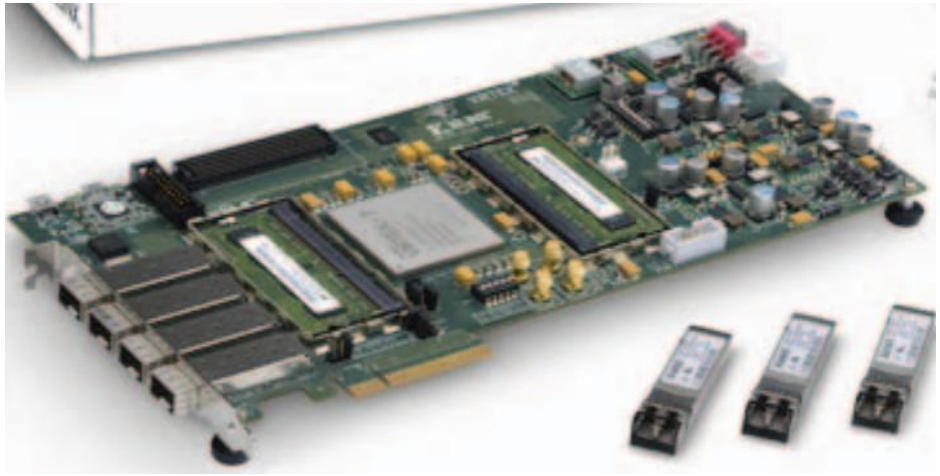
Hardware – Central Interface Board



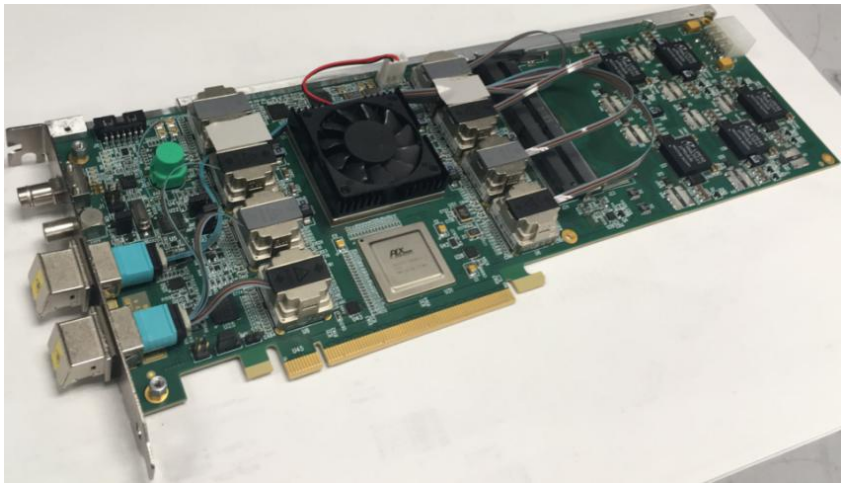
- Currently the Xilinx ZC706 Dev. board is used as the central interface board between the front-end and back end;
- Cost effective for small volume test setup;

Hardware – FELIX I/O PCIe Card

Xilinx VC709

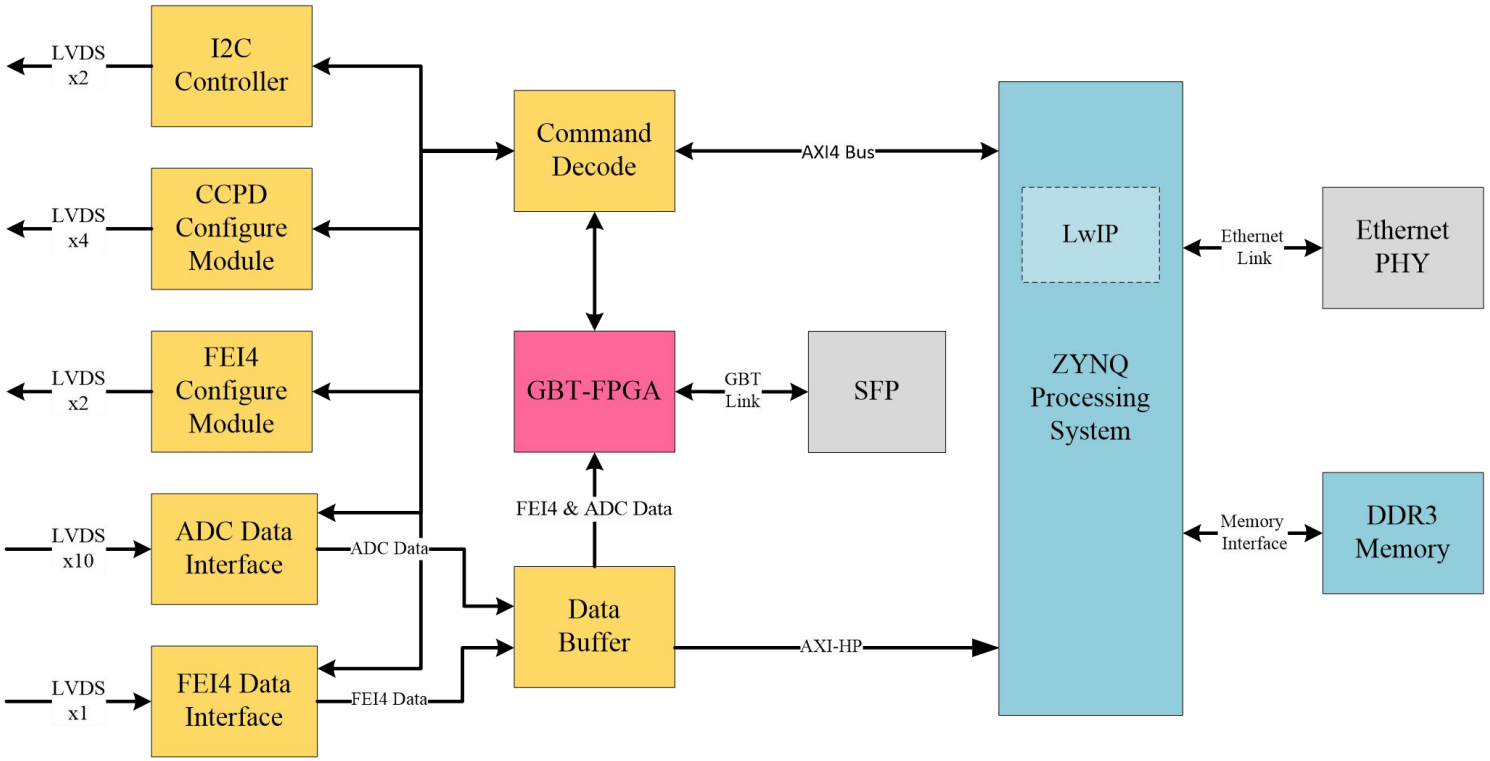


BNL 711



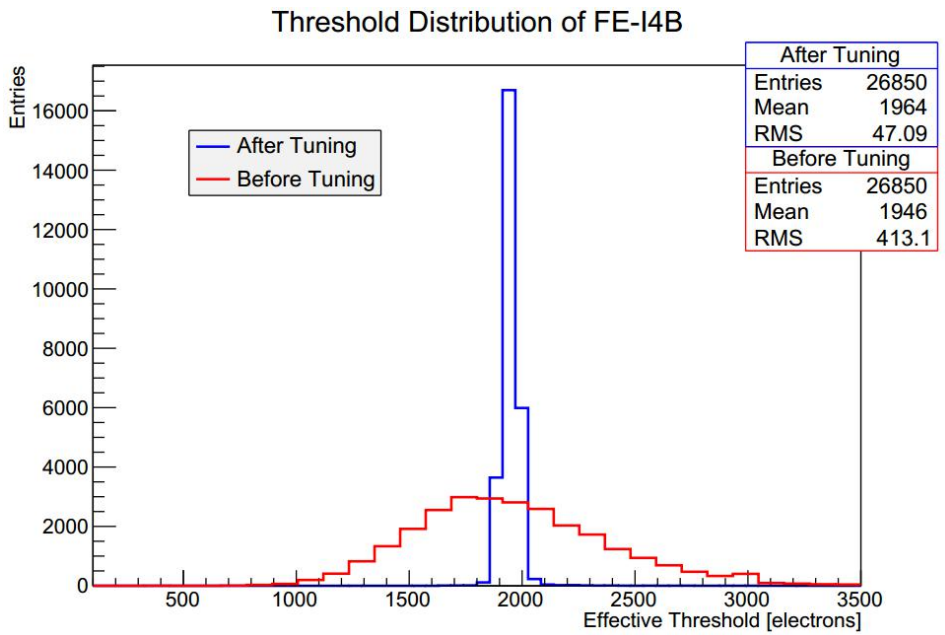
- Xilinx VC709: Gen3 x 8 lane PCIe card with 4 duplex fiber optical links
  - Vertix 7 FPGA: XC7VX690T-2FFG1761C
  - 4 x SFP+ modules, total 4 transceivers
- BNL-711: Gen3 x16 lane PCIe card with 48 duplex fiber optical links
  - Kintex Ultrascale FPGA: XCKU115-2FLVF1924E
  - MiniPOD: 4 TX and 4 RX modules, total 48 transceivers
  - Broadcom PEX8732: 32-lane PCIe Gen3 switch to avoid special requirements on PC mother board
- Both supported by the FELIX collaboration;

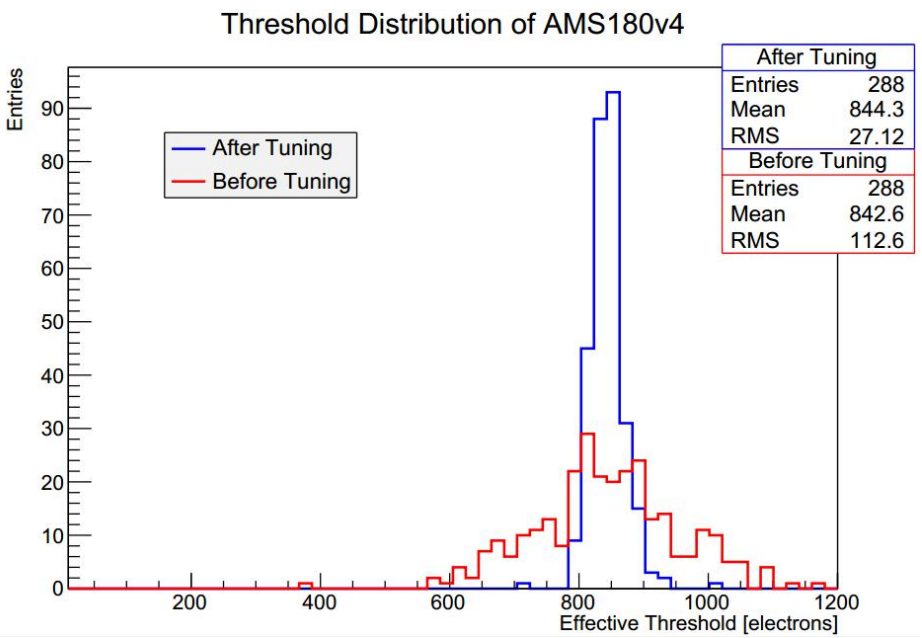
Firmware on ZC706



- Sensor configuration, interface for the pixel readout chip FE-I4B, I2C controller and ADC data interface are implemented in ZC706;
- Two slow-control pathes: GbE or GBT link;
- Test beam data DAQ: GBT link;

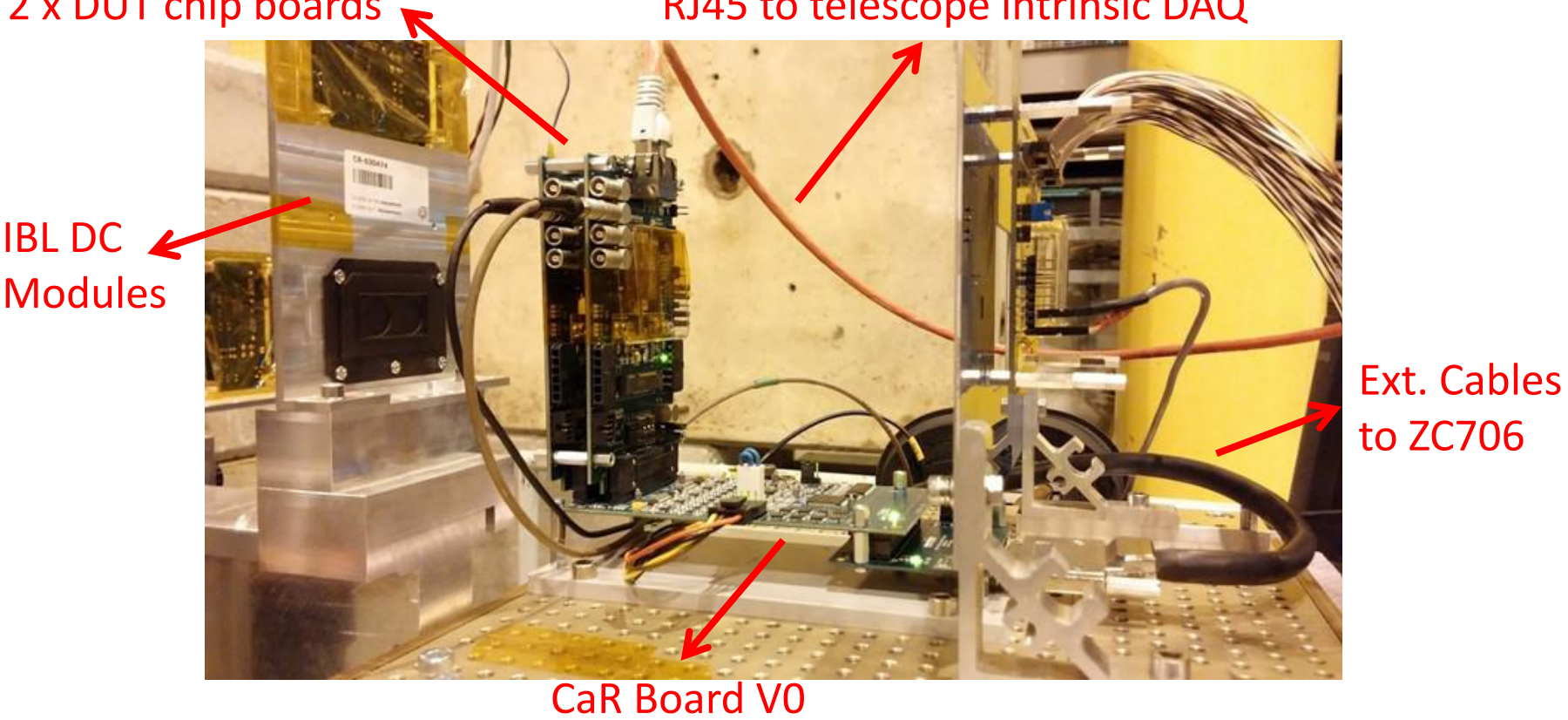
Software





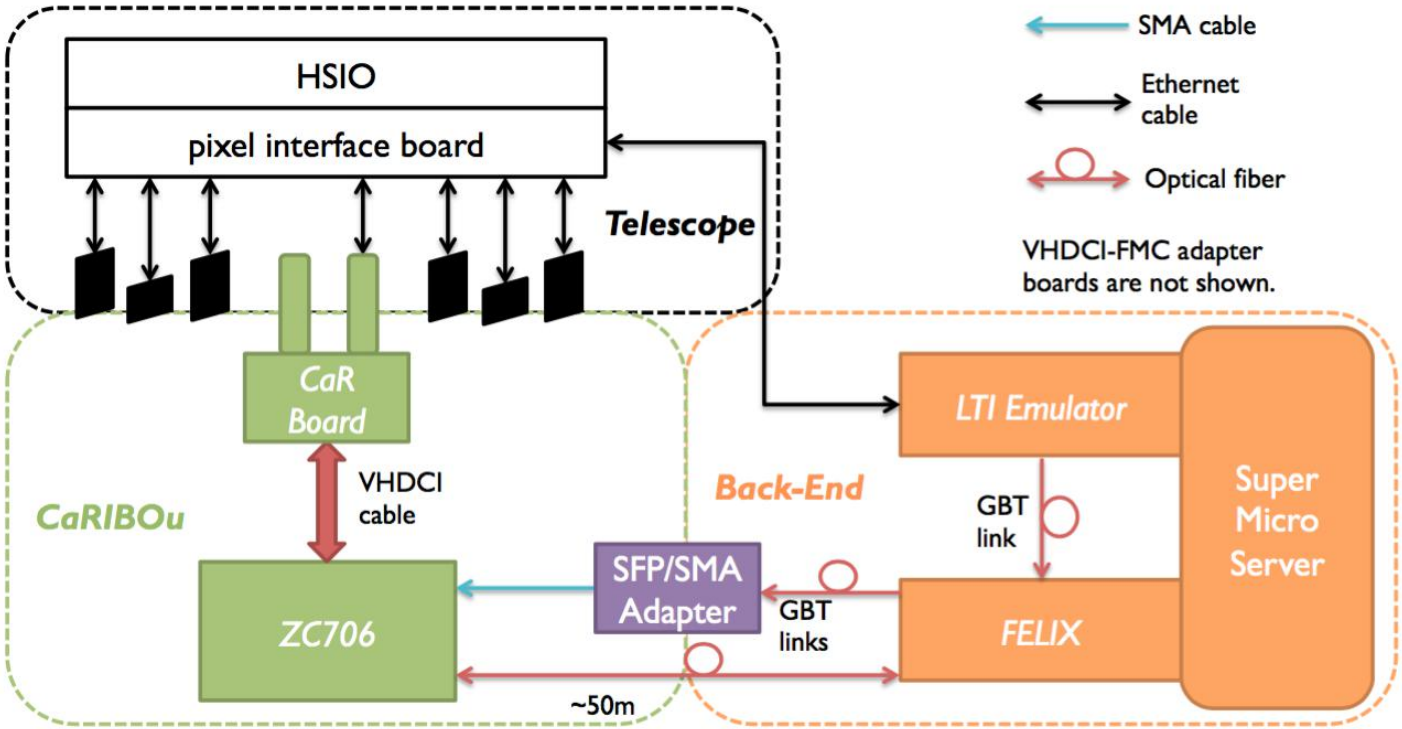
- Developed by Python script, optional FELIX software combination for DAQ;
- Component level and function level software driver (python script) available;
- Parameter tuning algorithm implemented: FE-I4B fast tuning (threshold and TOT within 5 minutes), H18Vx threshold tuning etc.
- FELIX tool fdaq can continuously stream testbeam data into disk;

Testbeam Deployment – Use Telescope DAQ



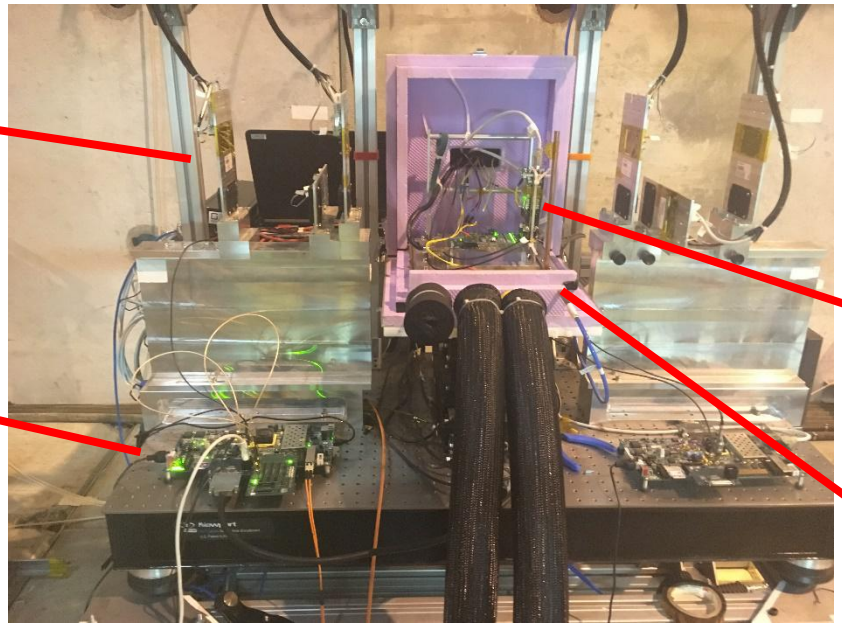
- First testbeam deployment in Nov. 2015 for H18V4 test at CERN SPS H8 beam line;
- Use CaRIBOu to control and tune the H18V4 sensor under test, telescope intrinsic readout system as DUT and telescope panel DAQ;

Testbeam Deployment – FELIX as DUT DAQ



- **CaRIBOu has been integrated with FELIX DAQ successfully in the 2016 Aug. testbeam;**
- FELIX as the DAQ system for one DUT sensor & readout chip;
- System clock & TTC commands are from LTI emulator, and are extract from the telescope intrinsic readout system;

Testbeam Deployment – FELIX as DUT DAQ



6 x IBL DC Module

ZC706

RJ45 to FMC adapter card

LTI emulator VC-709

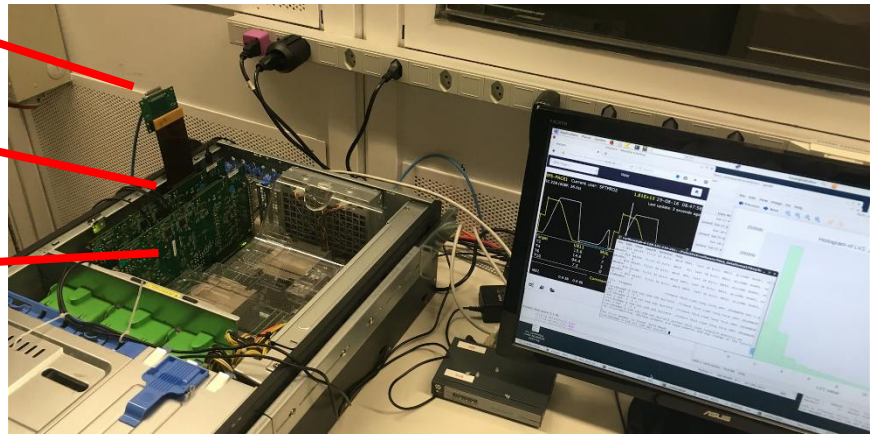
FELIX I/O VC-709

FELIX I/O VC-709

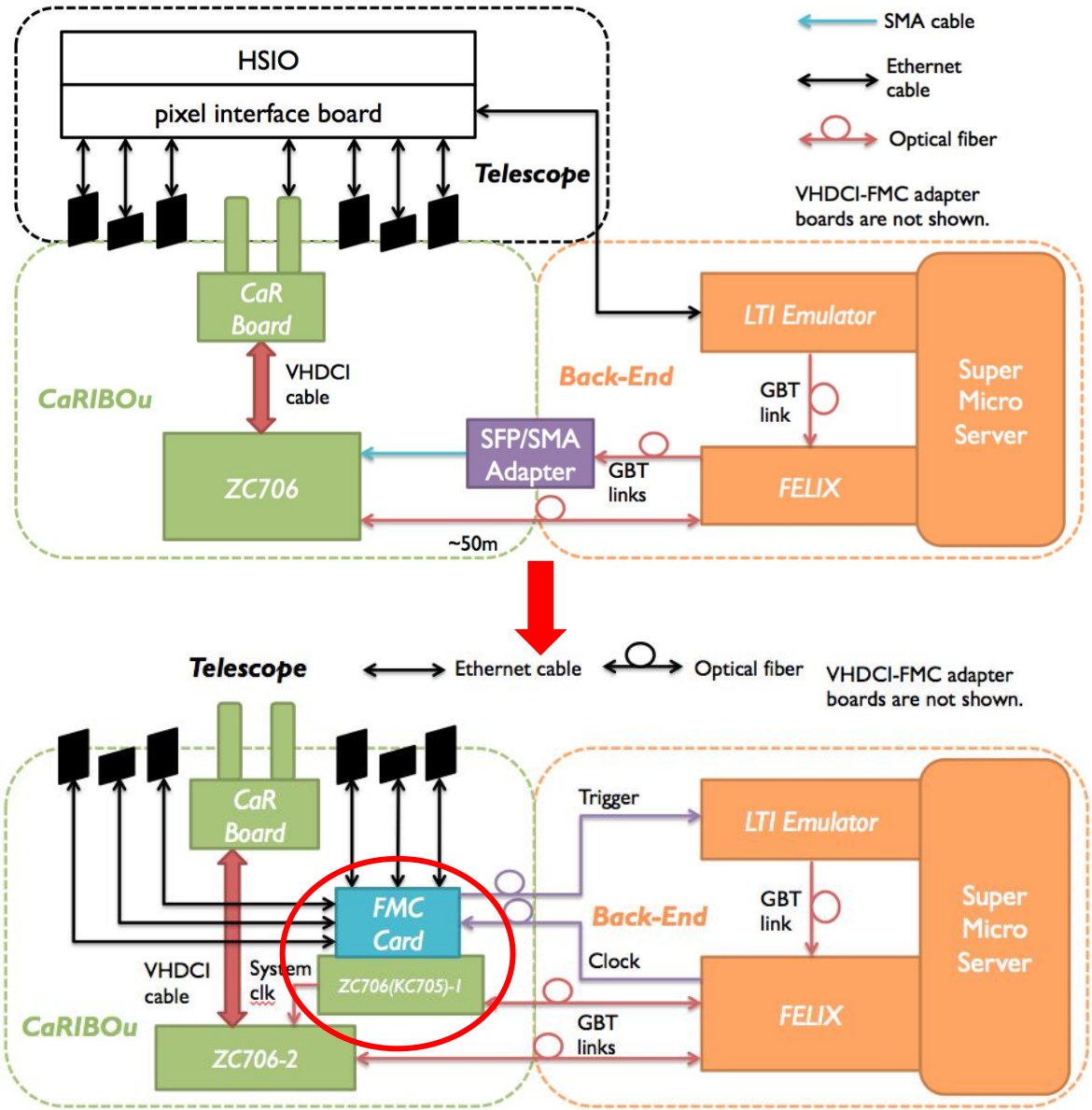
Beam direction

With a CaR board & 2x DUT inside

Climate Chamber

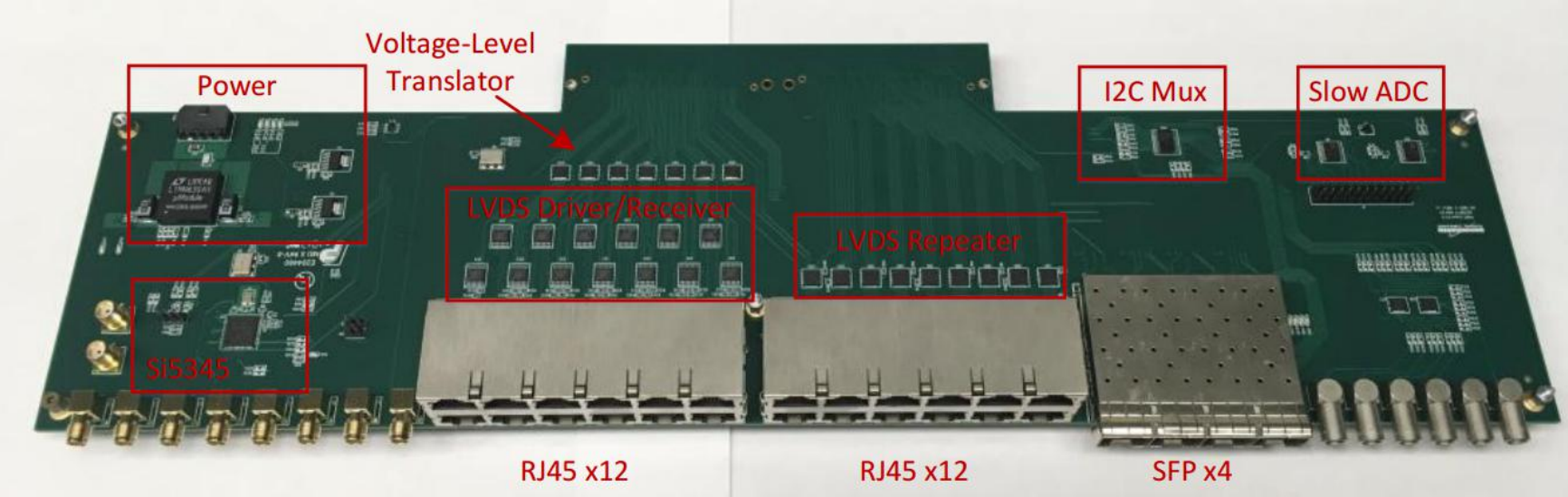


Full Testbeam Readout Implementation



Readout the telescope panels at the same time!

New Hardware – Telescope Readout Card



- FE-I4B and MIMOSA based telescope;
- 12 x FE-I4B readout links;
- 3 x MIMOSA MAPS module control and readout links;
- 4 x SFP as GBT link expansion;
- SiLabs SI5345 for low jitter clock distribution;
- ZC706 or KC705 as carrier board;

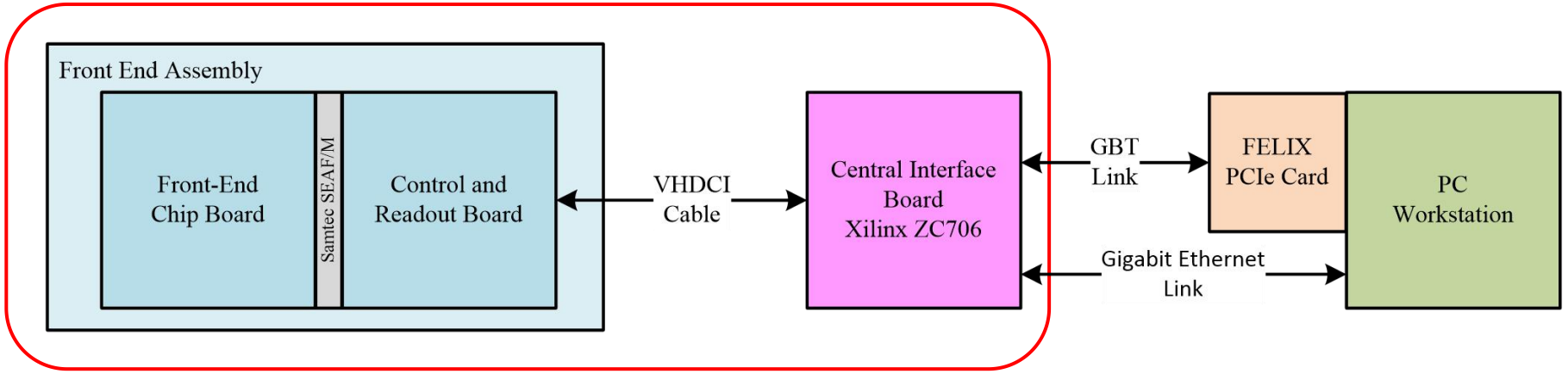
Summary

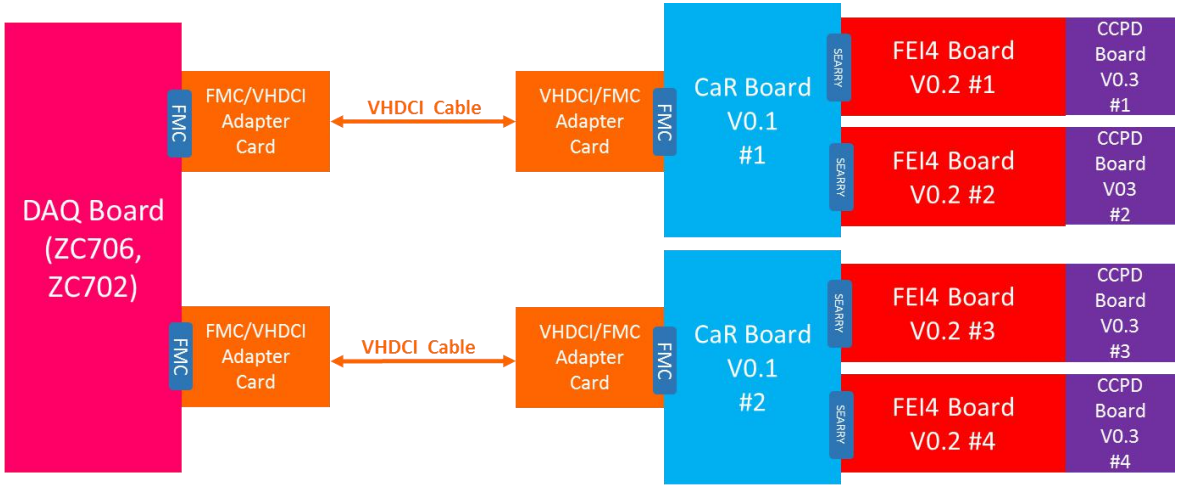
- CaRIBOu developed for the Pixel Sensor R&D
  - Chip boards: sensor and readout chip specific;
  - Control and Readout board: CaR board V0/1;
  - Central interface board: ZC706 (ZYNQ);
  - Telescope readout card: up to 12 FE-I4B module;
- DAQ scenario: telescope intrinsic, FELIX;
- FELIX DAQ successfully integrated in last Aug. testbeam;
- Development of FEI4 telescope readout by CaRIBOu is onging…
- Testbeam deployment: AMS H18 series, AMS H35DEMO;
  - See Mateus's talk on Wednesday: Capacitively Coupled Pixel Detectors: From design simulations to test beam
- Adaptation for the test of other sensors: CLICpix2
  - See Adrian's talk on Tuesday: A multi-chip data acquisition system based on a heterogeneous system-on-chip platform
- New users are very welcome!

Thanks for your attention!

Backup Slides

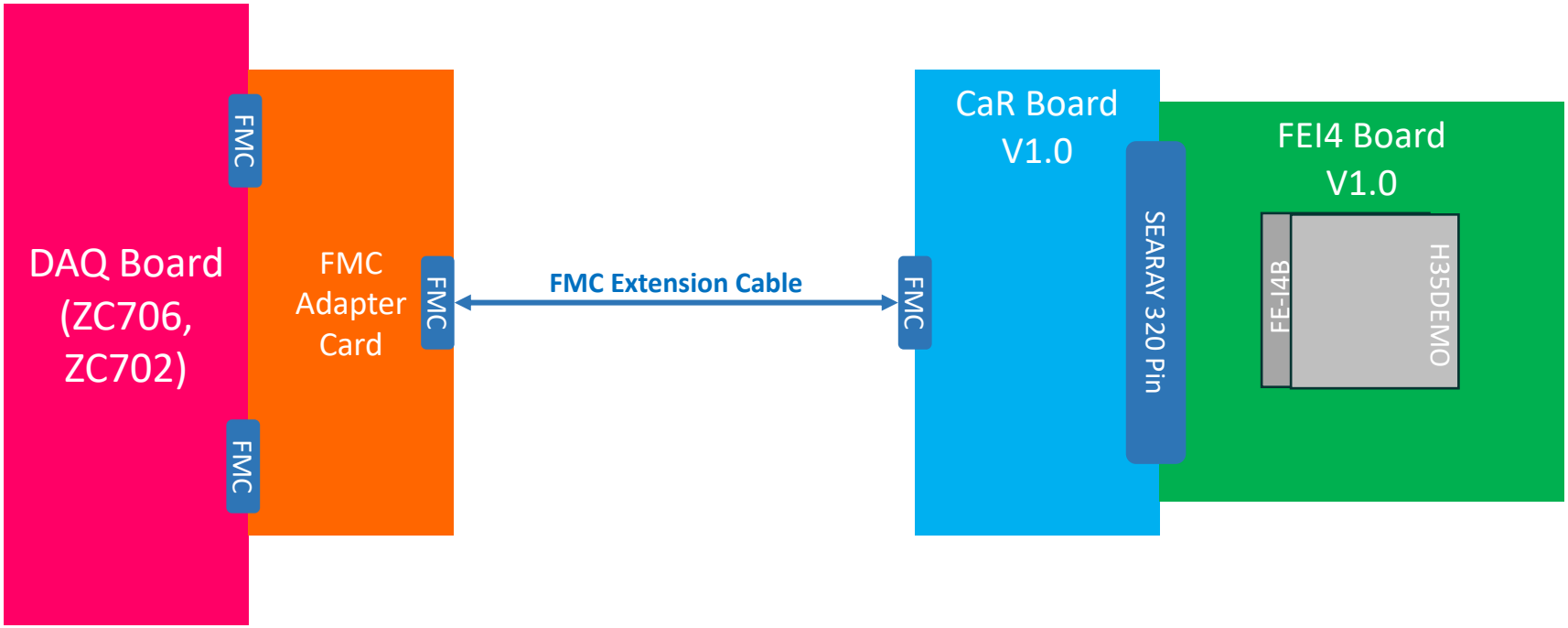
Hardware Overview - CaRIBOuV0





- 5 Custom boards have been designed for CaRIBOu V0
  - CaR Board (Control and Readout)
  - FEI4 Board (Chip Board)
  - CCPD Board (Chip Board)
  - FMC2VHDCI & VHDCI2FMC Adapter Card
- For the test of sensor prototype H18V4/5/6;

Hardware Overview - CaRIBOuV1



- Primarily designed for the test of H35DEMO, compatible with H18V4/V5;
- CCPD board is eliminated due to high density and high quantity of the IO pads of H35DEMO;
- Use FMC extension cable to replace the VHDCI cable used in CaRIBOu V0;