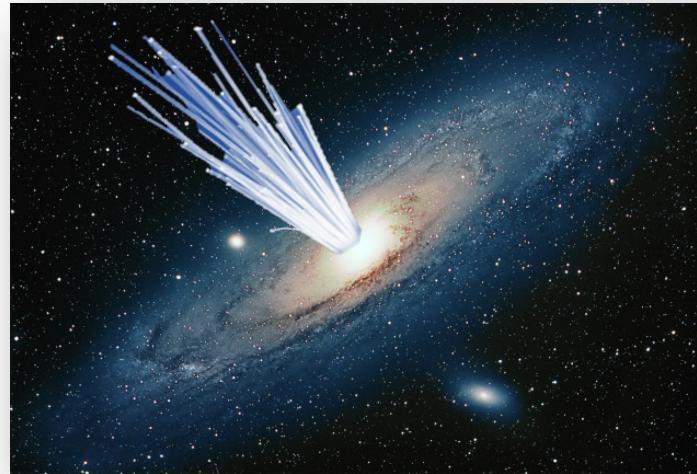




TIPP'17

Beijing, People's Republic of China – May 22-26, 2017

R&D on a Scintillating Fiber Tracker with SiPM array readout for Application in Space



P. Azzarello, F. Cadoux, D. La Marra, C. Perrina, X. Wu
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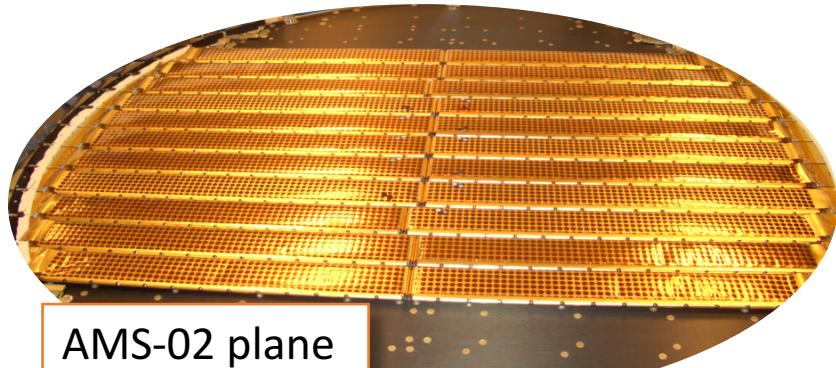
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DE GENÈVE

State of the Art

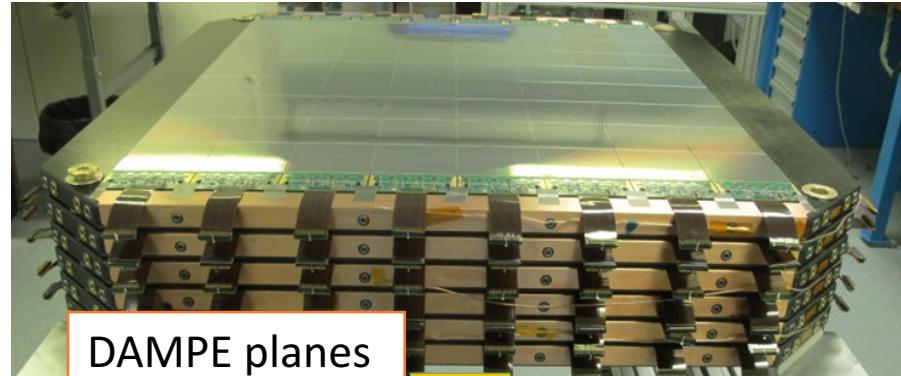
- Astroparticle physics and high energy astrophysics are in a “golden” era thanks to a series of very successful and long-running space and ground based experiments (*eg.* PAMELA, Fermi, AMS-02, H.E.S.S., Auger, IceCube, ...)
 - The multi-messenger/multi-wavelength/multi-platform approach is opening up new possibilities in observation and discovery
 - The hot topics are still: dark matter, cosmic ray origin, antimatter
- The future of ground-based observation is very brilliant with approved new projects (CTA, LHASSO) and proposed projects (KM3NeT, IceCube Gen2, ...)
- Need complementary future space missions
 - Direct cosmic ray detection: getting to the “knee” (**HERD**, ...)
 - Close the gamma-ray “MeV” gap (PANGU/e-ASTROGAM, ...)
 - Antimatter and DM search with antiparticles > TeV (ALADINO, ...)

Our experience

- The University of Geneva has long experience in **silicon** tracker detectors in **Space** (AMS-01, AMS-02, DAMPE).

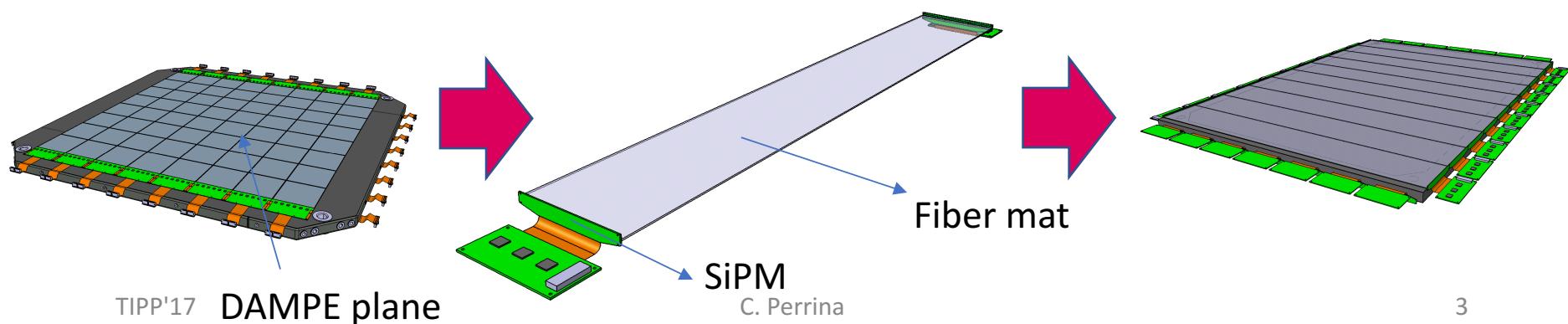


PoS(Vertex2014)028



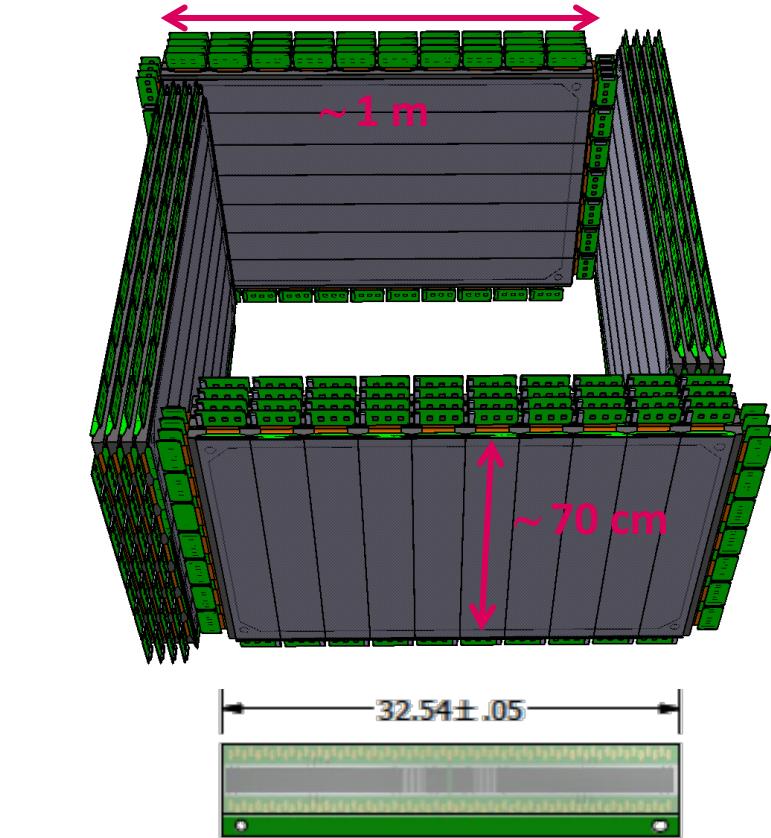
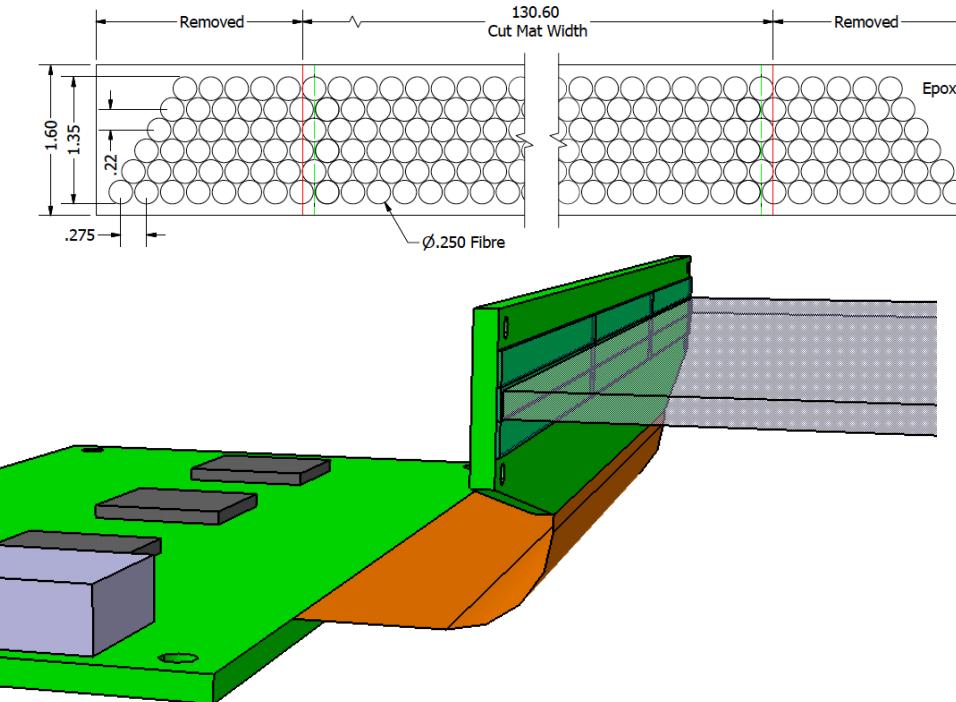
PoS(ICRC2015)1192

- New technologies to replace silicon detectors are under study:
 - Our idea is to use scintillating fiber mats instead of silicon strip detectors.



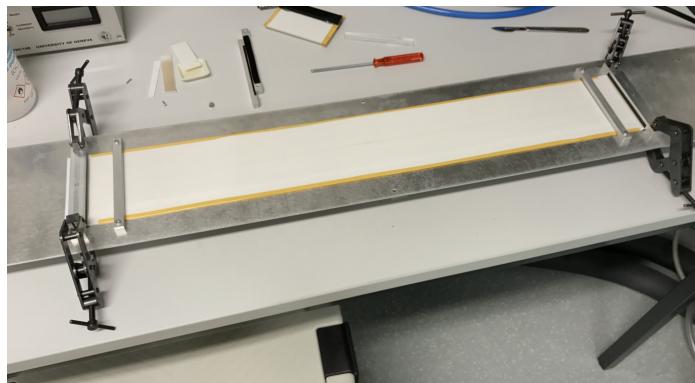
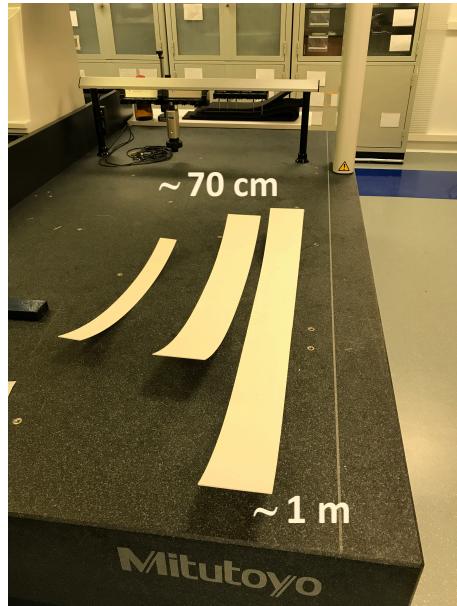
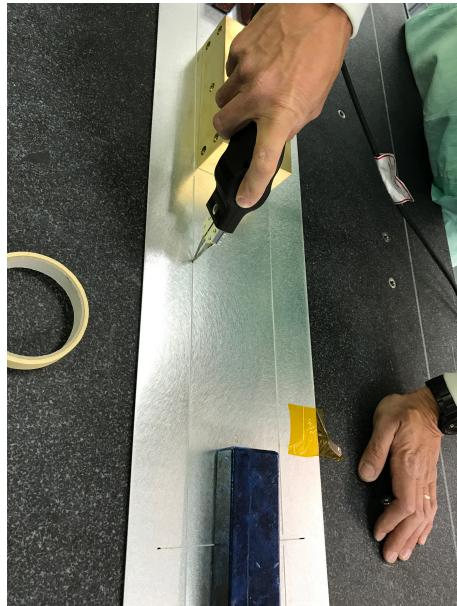
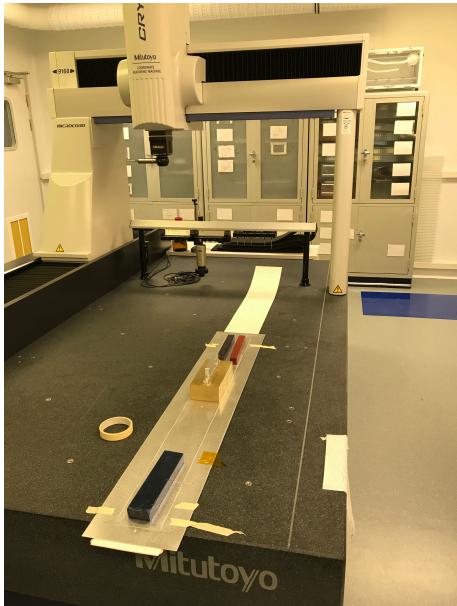
The SciFi project for Space

- Six fiber layers in each mat
- 250 μm diameter, Kuraray SCSF-78M (LHCb)
- 2 lengths
- SiPM on each end of the fiber mat to measure particle with $Z = 1$ on one side and $Z \leq 20$ on the other (two different gains)
- ~ 9.8 cm width to match for 3 SiPM arrays



- SiPM multi-channel array from Hamamatsu S10943-3183(X)
 - 128 channels per array
 - 96 pixels per channel
 - Pixel size: $57.5 \mu\text{m} \times 62.5 \mu\text{m}$
 - Channel size: $230 \mu\text{m} \times 1500 \mu\text{m}$

From the project to reality (1)

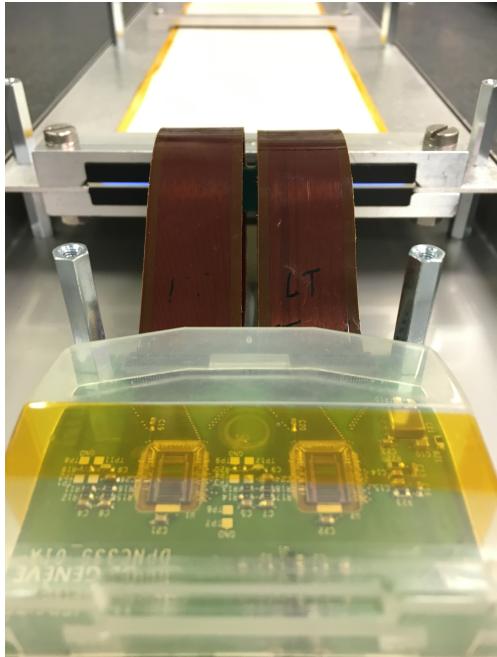
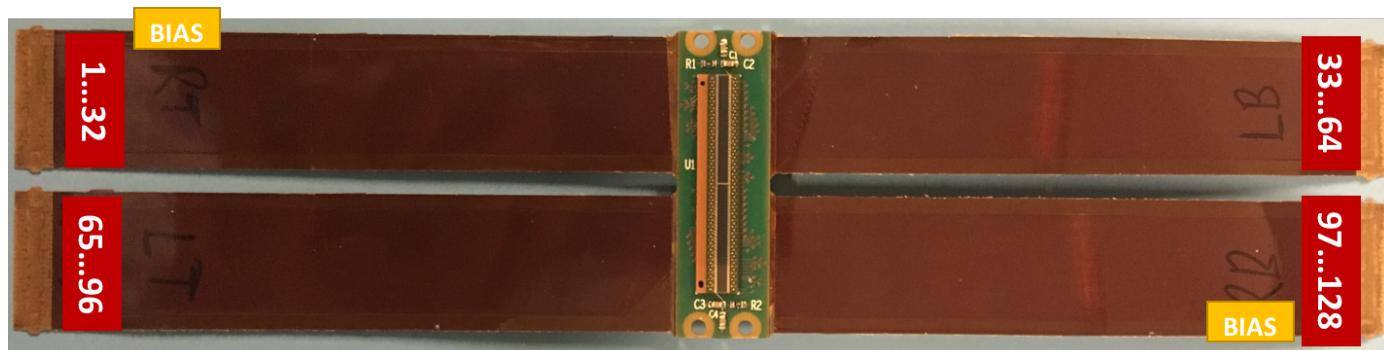


Extremities
polished at
EPFL
(Lausanne, CH)
with diamond
head

From the project to reality (2)

Printed Circuit Board

The 128 channels of each SiPM array are split in
4 x 32 lines
with flex cables going in opposite direction.

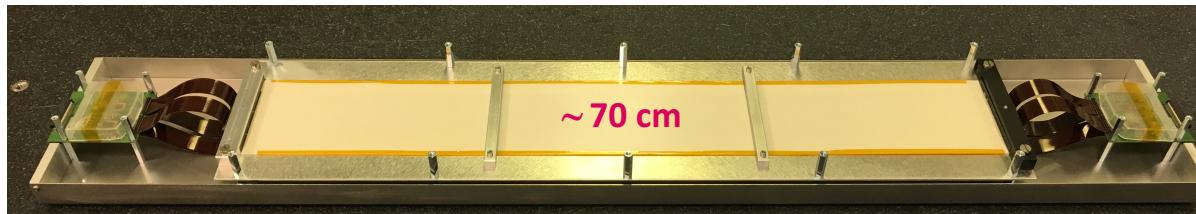


Front-end electronics board
2x VATA 64 HDR 16, to readout
the 128 MPPC channels.

Four zero-insertion-force (ZIF)
sockets to connect the MPPC
board.



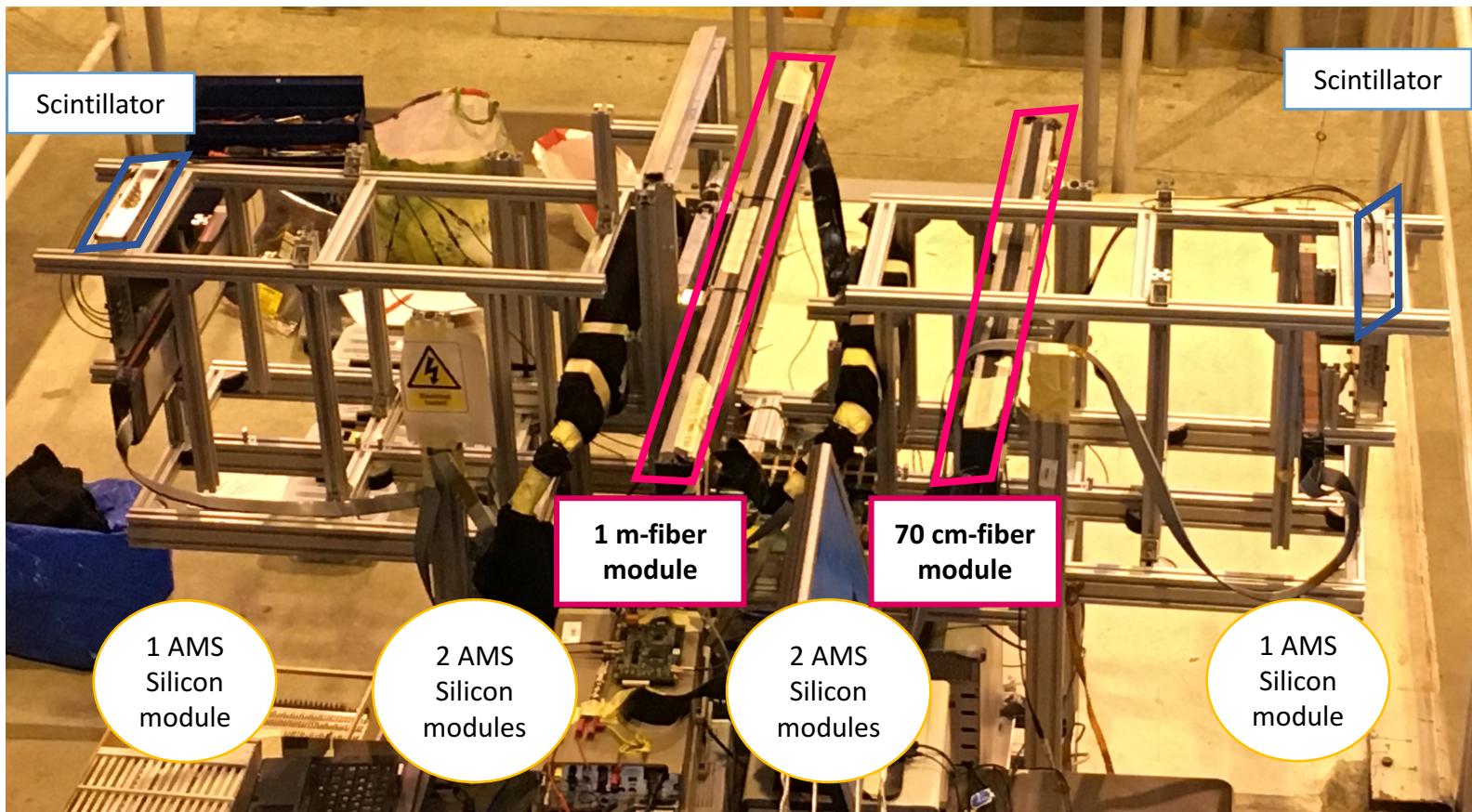
Fiber module prototypes



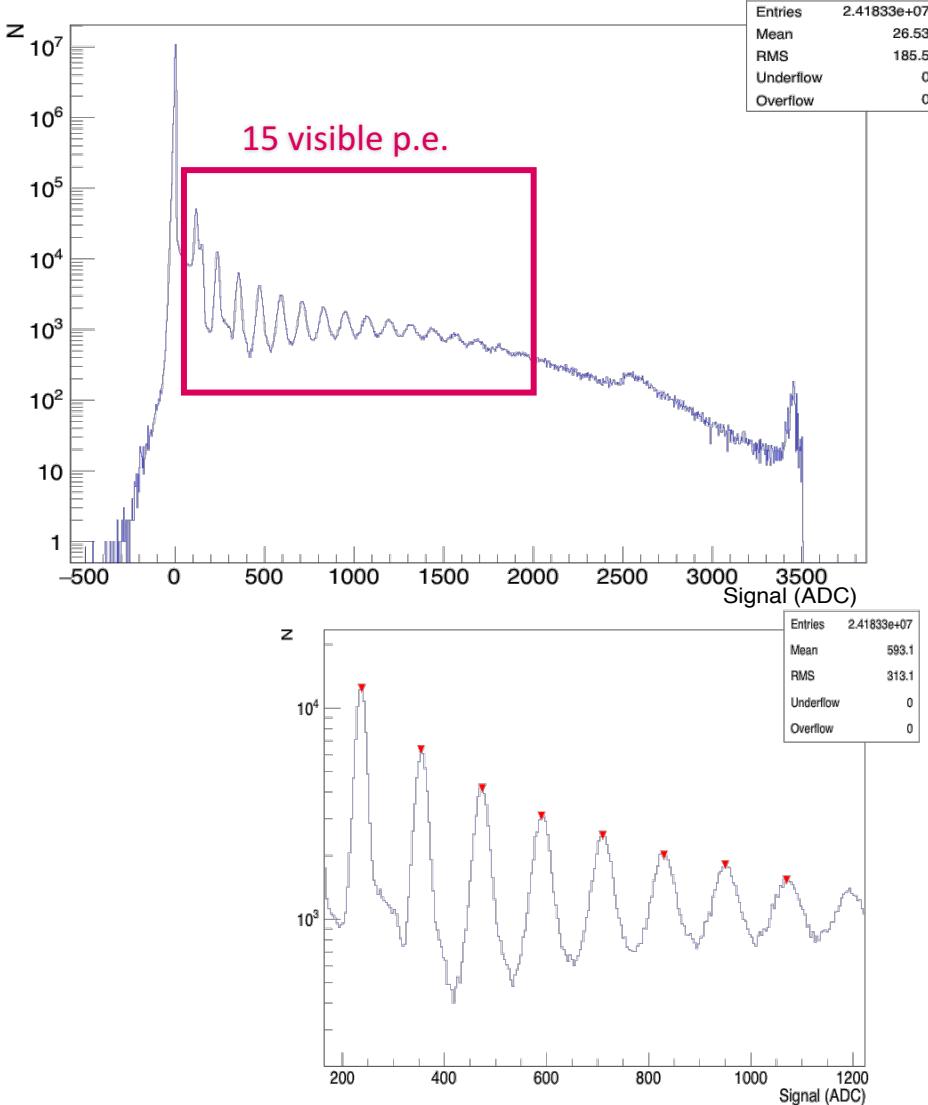
- Two fiber modules **ready** and **tested** during a test beam (May 15 - 19, 2017) at CERN with a hadron beam of 100 GeV/c.

- 4 millions events collected

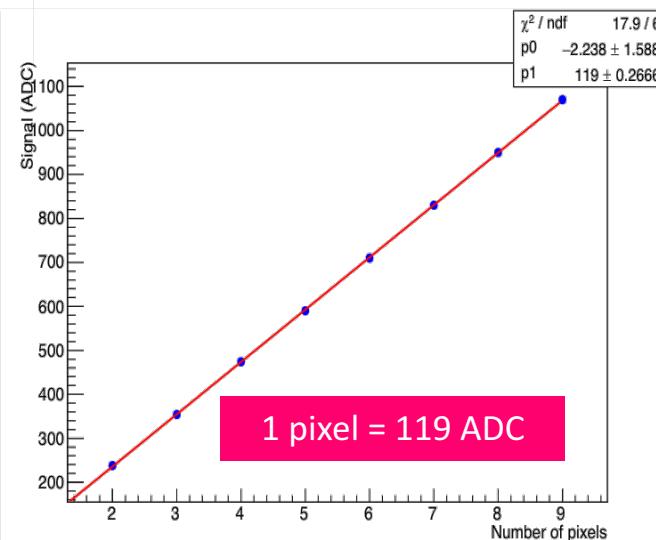
- Data analysis just started



Preliminary results: Signal distribution



- Signal distribution **integrated** over the 128 channels of a SiPM.
- **No clusterization** performed.
- First peak = no signal.
- **One peak corresponds to one photo-electron (p.e.).**

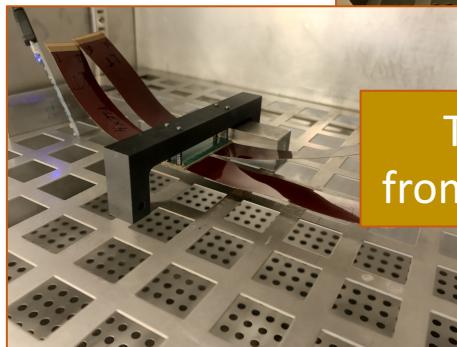


From the signal distribution we can compute the signal for one pixel.

Space qualification

This kind of detector (fiber + SiPM) has never been used in Space.

- Needed space qualification tests
 - Thermal tests;
 - Vacuum tests;
 - Vibrations.

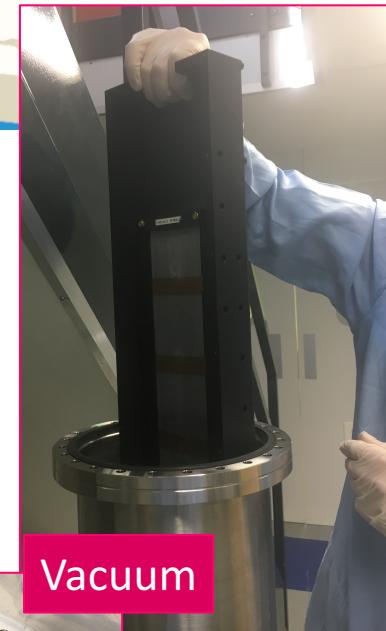


Thermal cycles
from -30 °C to +60 °C

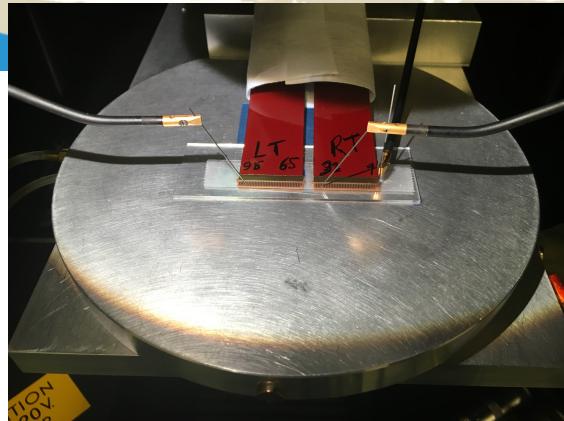
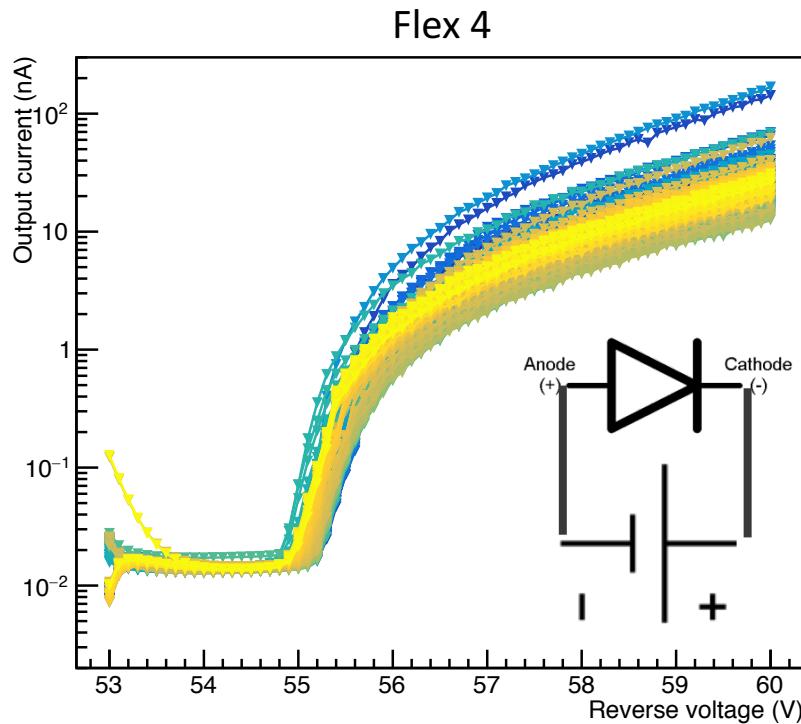


Vacuum

- Tests on
 - SiPMs;
 - SiPMs mounted on PCB;
 - fiber mats.



SiPM V_{BD} measurements



The V_{BD} for each channel can be found by plotting (Inverse Logarithmic Derivative method):

$$\frac{1}{I} \times \frac{dI}{dV}$$

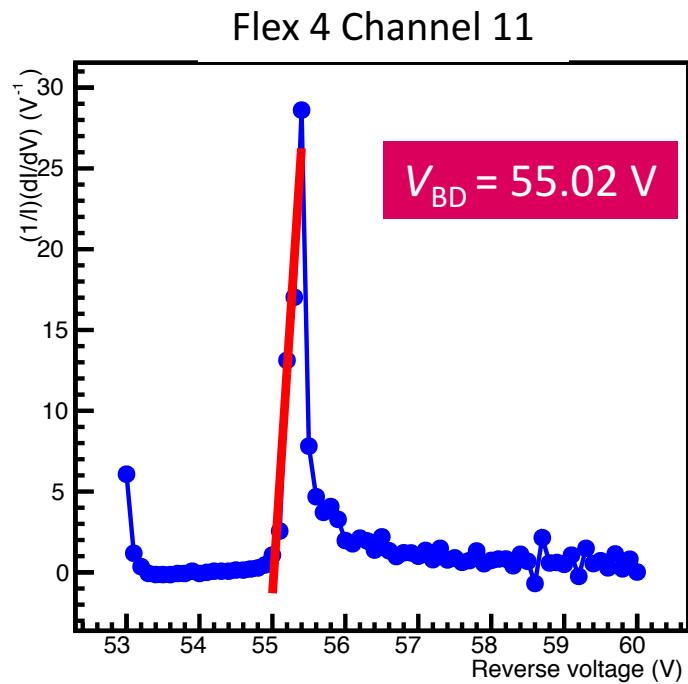


PoS(TIPP2014)070

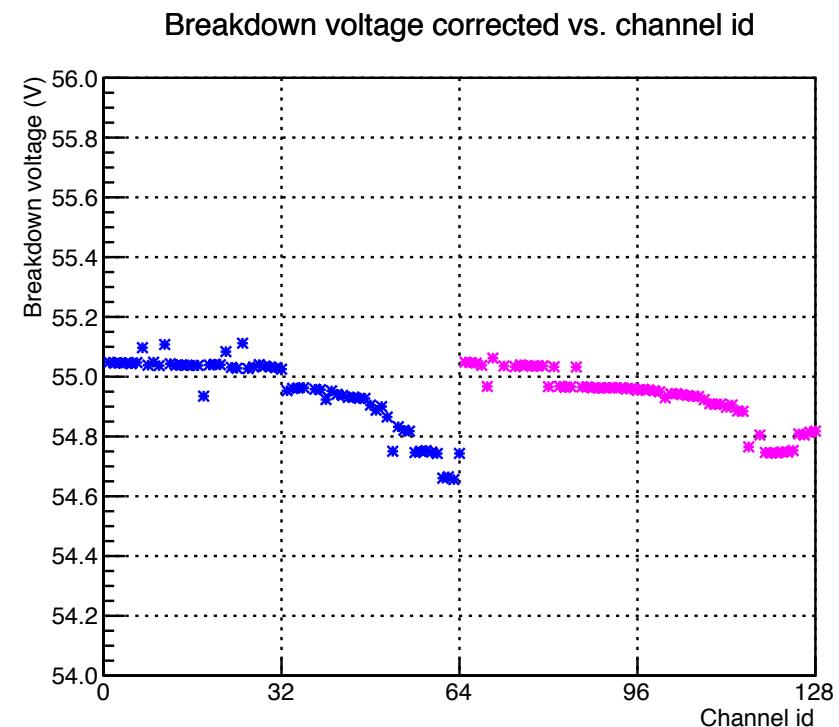
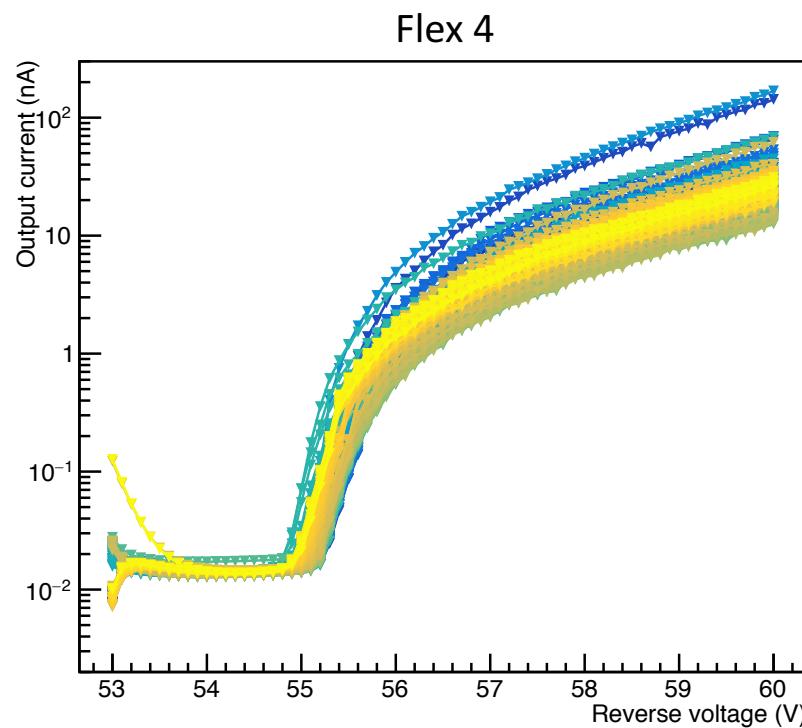
V_{BD} is given by the V for which the linear fit crosses zero.

TIPP'17

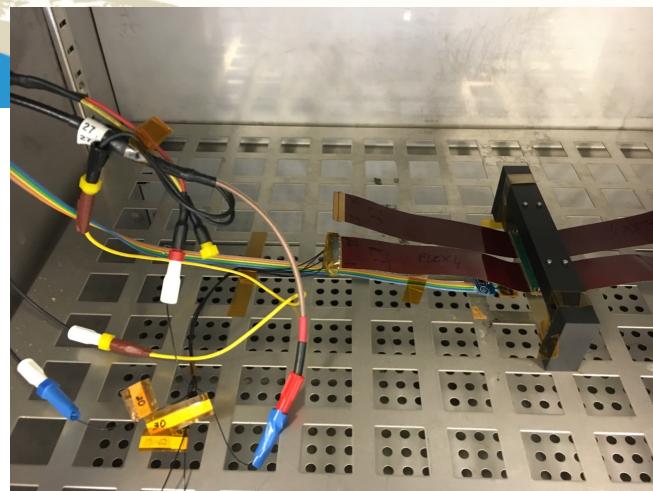
C. Perrina



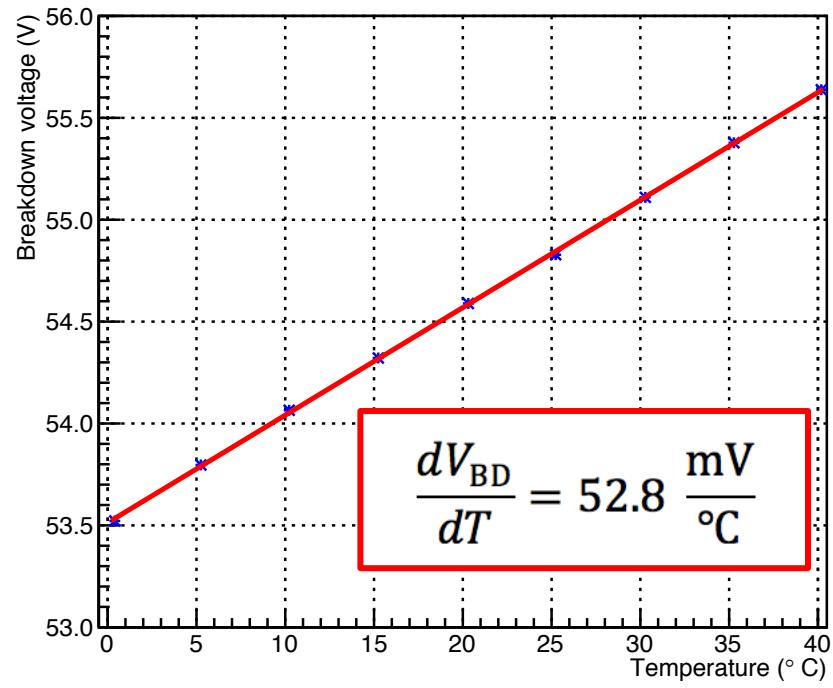
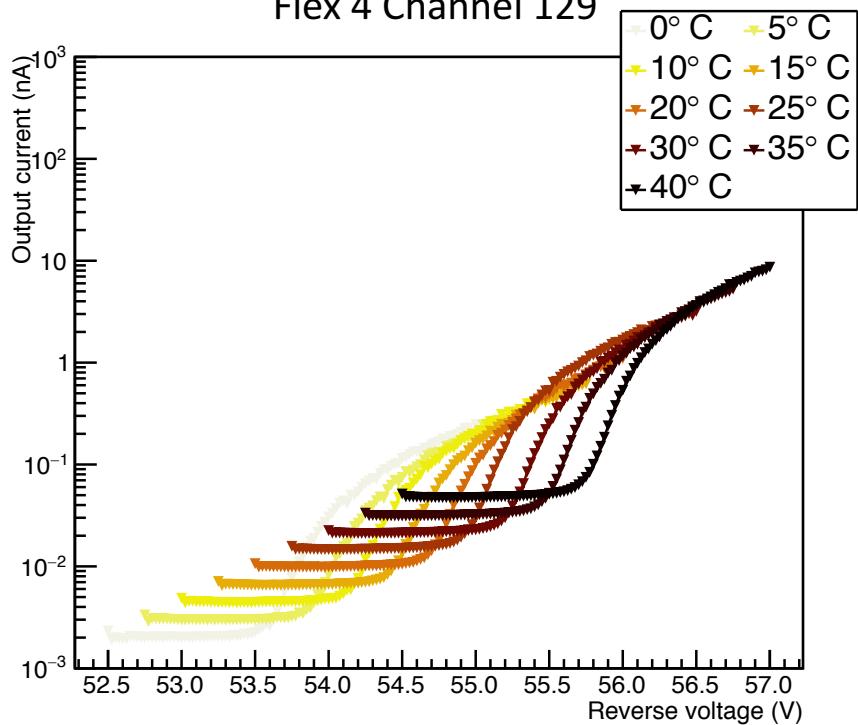
Flex 4 V_{BD} corrected for 25 °C



V_{BD} vs. Temperature



Flex 4 Channel 129

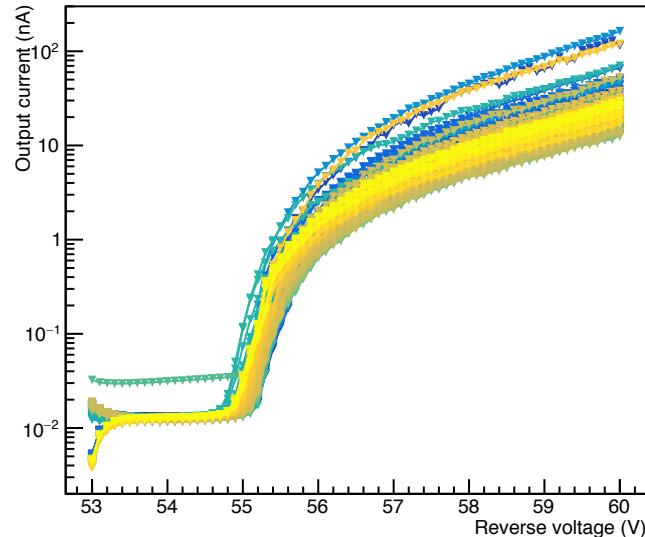


Flex 4 after thermal cycles V_{BD} corrected for 25 °C

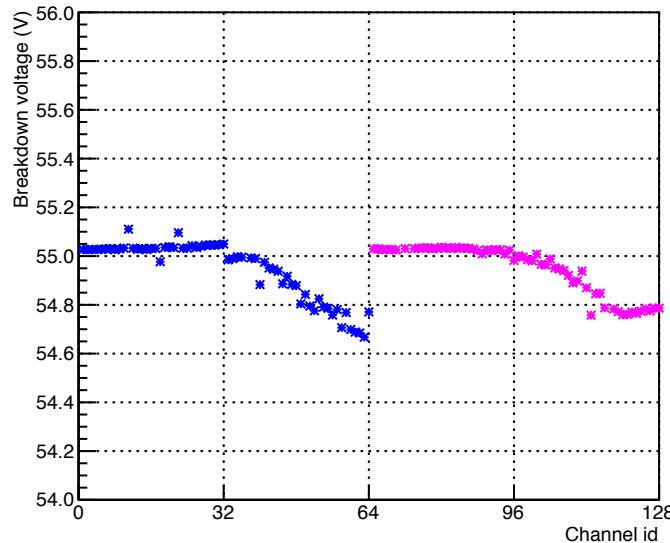


Thermal cycles
5 x (-30 °C -> +60 °C)

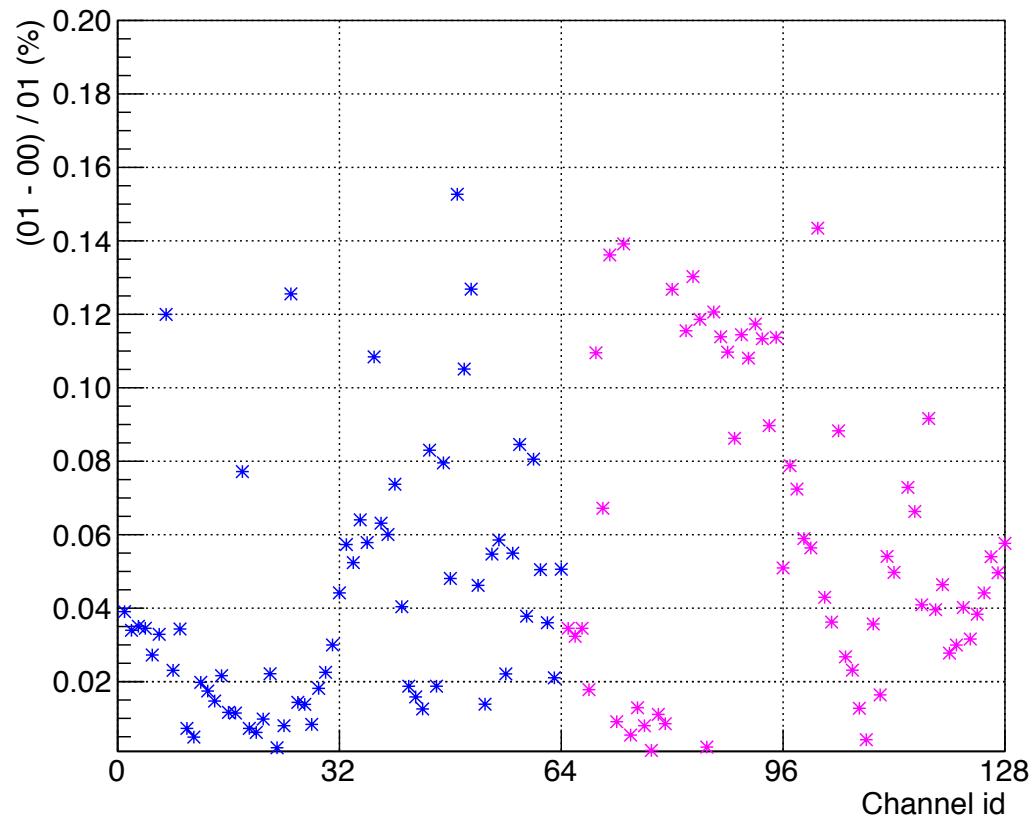
flex 4 iv 01 5s



Breakdown voltage corrected vs. channel id



V_{BD} evolution after thermal cycles



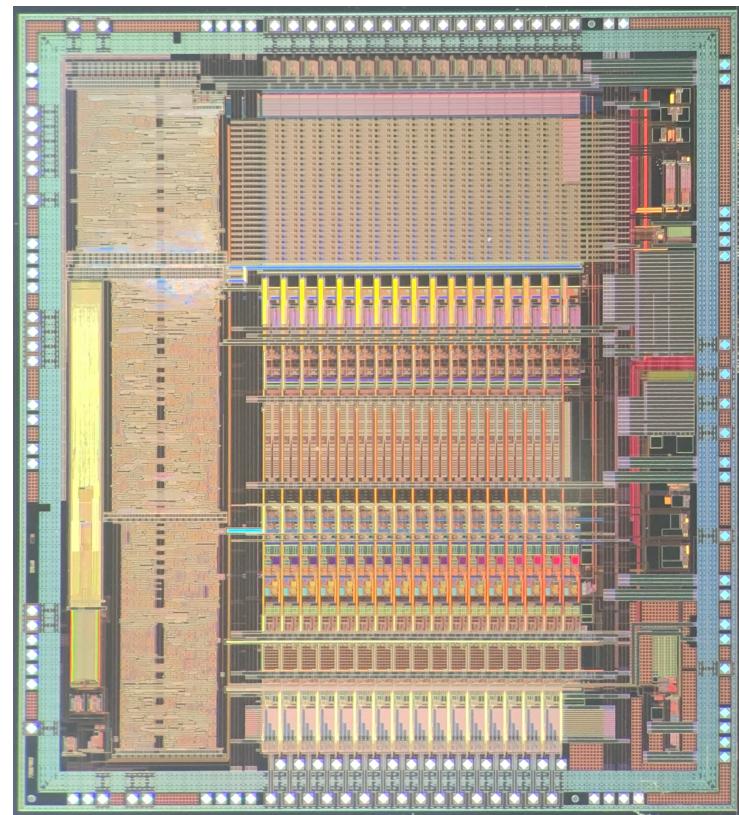
The discrepancy
between V_{BD}
measured before
thermal cycles
and after is
< 0.16 %

Readout improvement: SIPHRA chip



AMICSA&DSP2016

- SIPHRA = “Silicon Photomultiplier Readout ASIC”
- New ASIC from IDEAS for space applications
- The circuit has been designed under contract from the ESA with support from the Norwegian Space Center and the University of Geneva.
- **12-bits ADC included.**
- One line to readout and digitize one PT100 temperature sensor.
- One single power supply voltage: **3.3 V.**
- Various operation modes available.
 - It can provide in output only the channels with a signal higher than a programmed threshold (one for each channel).
 - Data reduction at ASIC level!
- 1 mW power consumption per channel.
- **Test board for SIPHRA chip is being produced and tests will start in the next weeks.**



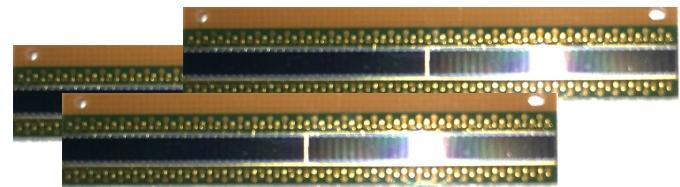
Conclusions



Advantages



- Less fragile;
- Flexible geometry;
- No wire bonds;
- Single photon response;
- High detection efficiency;
- High gain at low bias voltage;
- Together with SIPHRA: simplified DAQ electronics;
 - No Op-amp needed, data reduction done at ASIC level;
 - Only 3.3 V power line needed (apart from bias line).



Disadvantages

- Low Technology Readiness Level (TRL);
- Effects of dark count;
- Dependence of SiPMs on temperature.

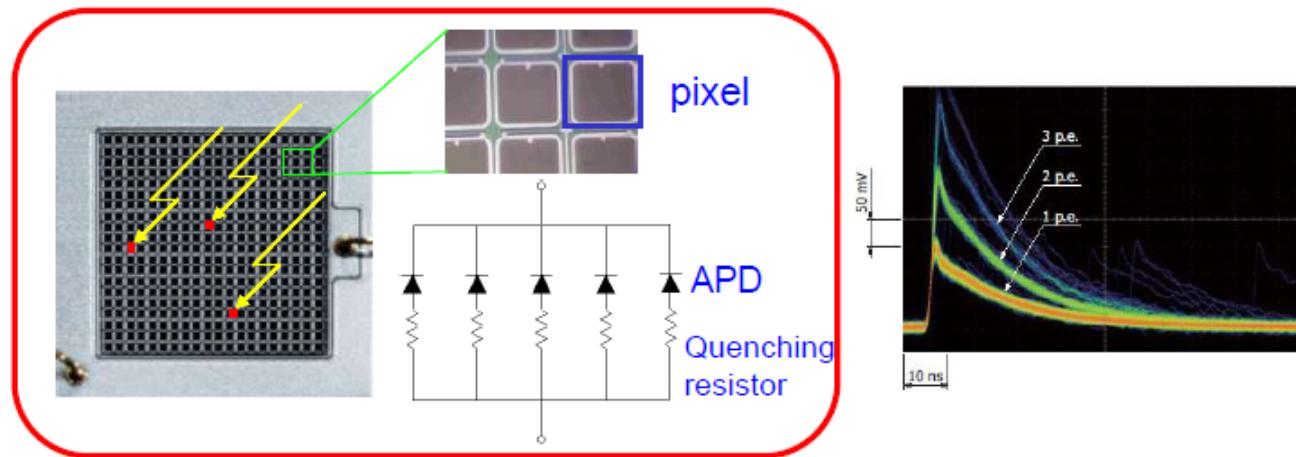
Future

- More complete diagnostic tool will be introduced
 - Calibration with LEDs;
 - Calibration with radioactive sources;
- Space qualification tests to increase the TRL
 - Thermal tests;
 - Vacuum tests;
 - Vibrations.
- Tests on
 - SiPMs;
 - SiPMs mounted on PCB;
 - Fiber mats;
 - Complete modules;
 - Planes made of more modules.



Back-up

Principle of operation



➤ Basic operation

- Each pixel operates separately in Geiger-mode
- Each pixel outputs a same amplitude pulse
- Pulse generated by multiple pixels are output while superimposed onto each other (detected at the same time)
- No position information

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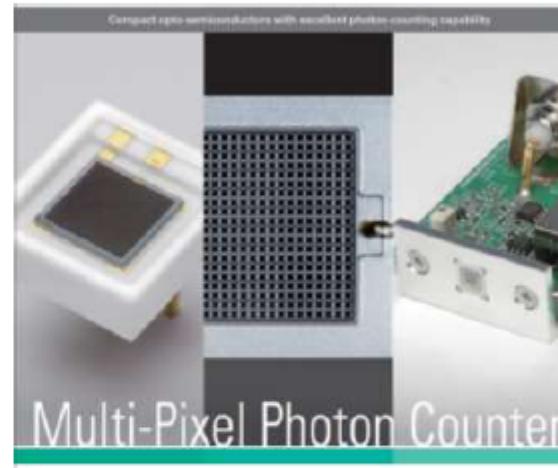
MPPC Technology Overview

➤What is an MPPC?

- **Multi-Pixel Photon Counter**
a new type of photon-counting device
made up of multiple APD pixels
operated in Geiger mode

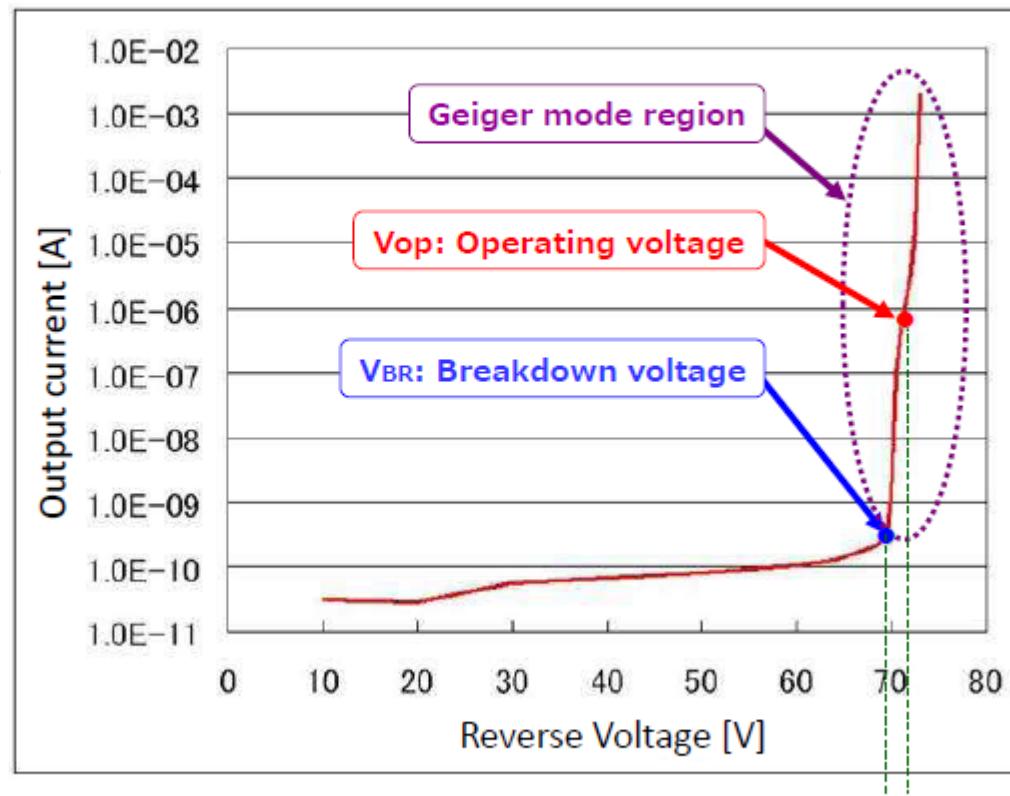
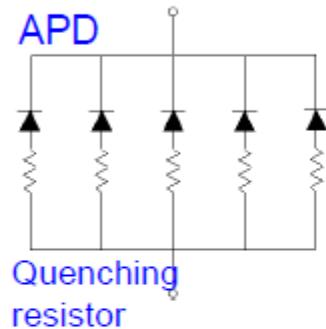
➤Features

- Small size / light weight
- Room temperature operation
- Low bias operation : ~70V
- High gain: 10^5 to 10^6
- Excellent timing resolution
- Insensitive to magnetic fields
- Simple readout circuit operation



Multi-Pixel Photon Counter

Geiger-mode operation



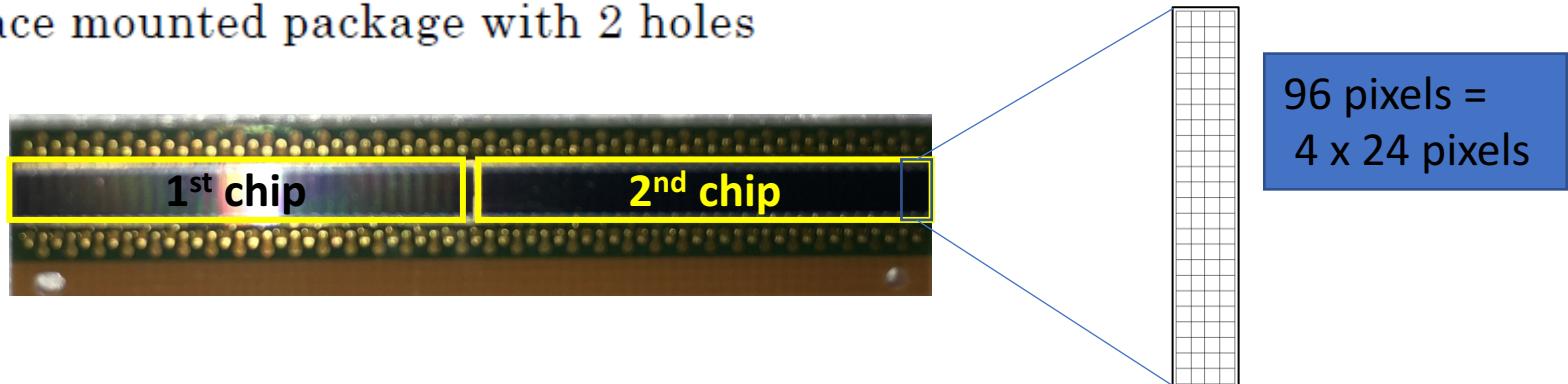
V_{ov}: Over voltage
V_{ov} = V_{op} - V_{BR}

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Our SiPM array

Product outline

- MPPC
- Effective photosensitive area $0.23 \times 1.5\text{mm}$, 128ch.Array ($64\text{ch}/\text{chip} \times 2\text{chip}$)
- Surface mounted package with 2 holes



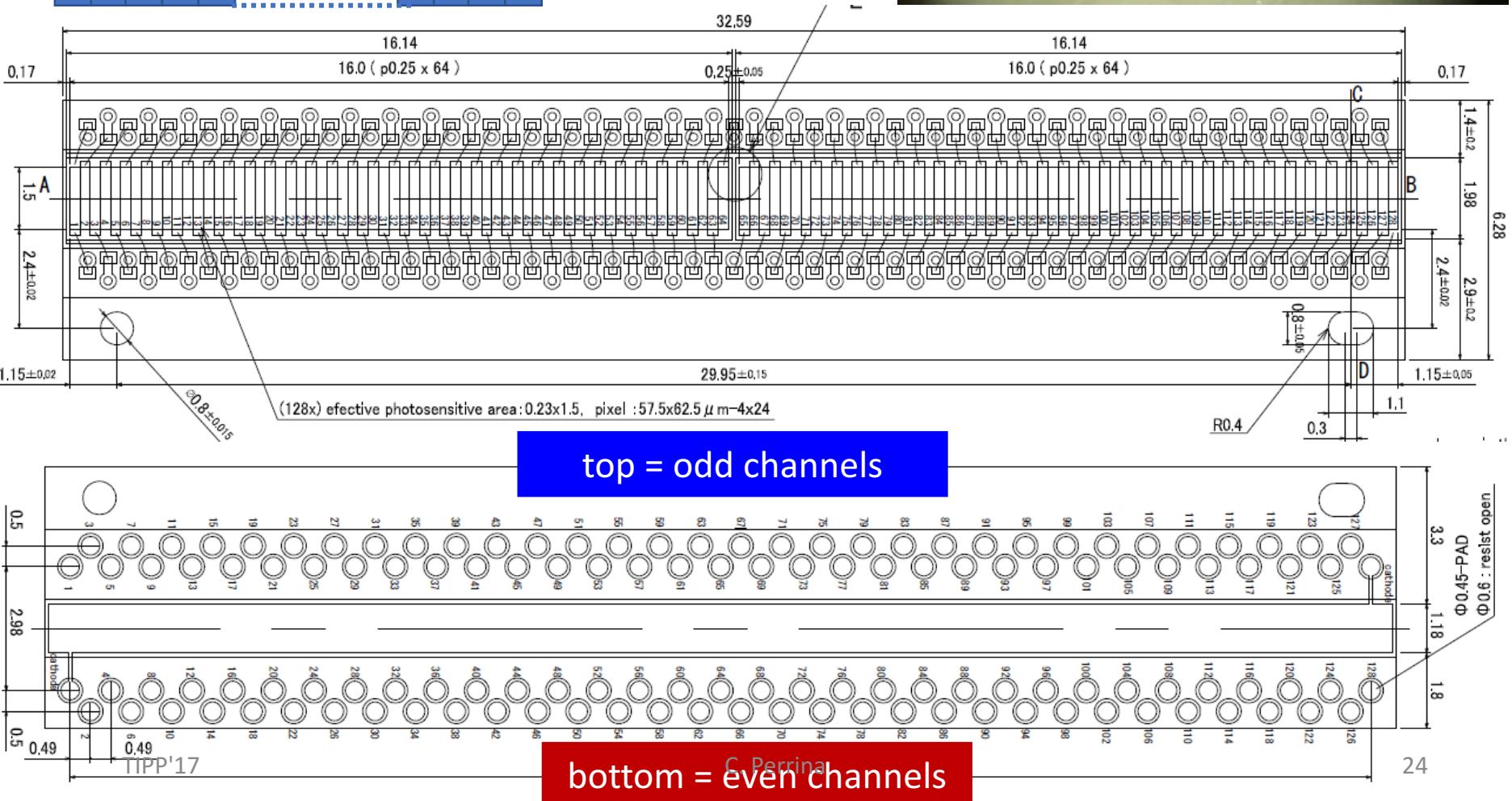
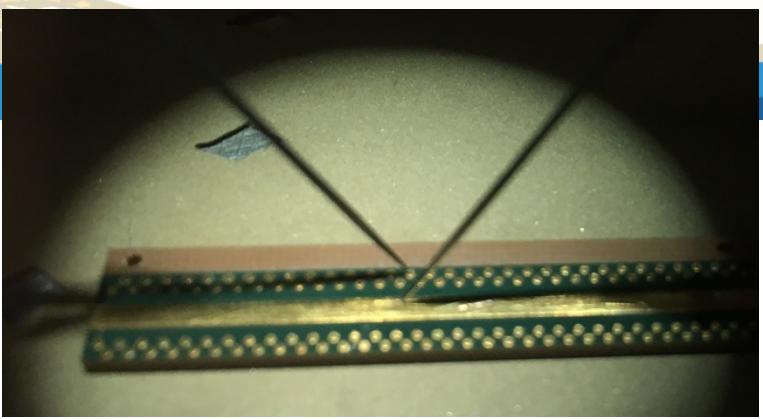
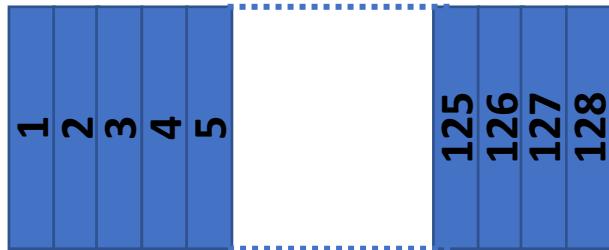
Parameter	Symble	Rating	Unit
Effective active area / channel	--	$230(\text{X}) \times 1500(\text{Y})$	μm
GAP between channels (on chip)	--	20	μm
GAP between channels (between chip)	--	250 ± 50	μm
Number of channels	--	128 ($64 \times 2\text{chip}$)	ch
Number of pixels / channel	--	$4(\text{X}) \times 24(\text{Y})$	--
Pixel size	--	$57.5(\text{X}) \times 62.5(\text{Y})$	μm

Properties of our SiPM array

Breakdown voltage	V_{BR}	--	40	--	65	V
Operating voltage	V_{op}	--		$V_{BR}+2.5$	--	V
V_{op} variation between channels	--	--	--	0.4	1.0	V
Dark current / channel	I_D	$VR=V_{op}$	--	20	100	nA
Cross talk	--	$VR=V_{op}$	--	8	15	%
Terminal capacitance / channel	C_t	$VR=V_{op}$ 100kHz	--	12	--	pF
Gain	M	$VR=V_{op}$	--	2×10^6	--	--
Quenching resistance	R_q		120	160	240	kΩ
Temperature coefficient of operating voltage	--	--	--	60	--	mV /°C

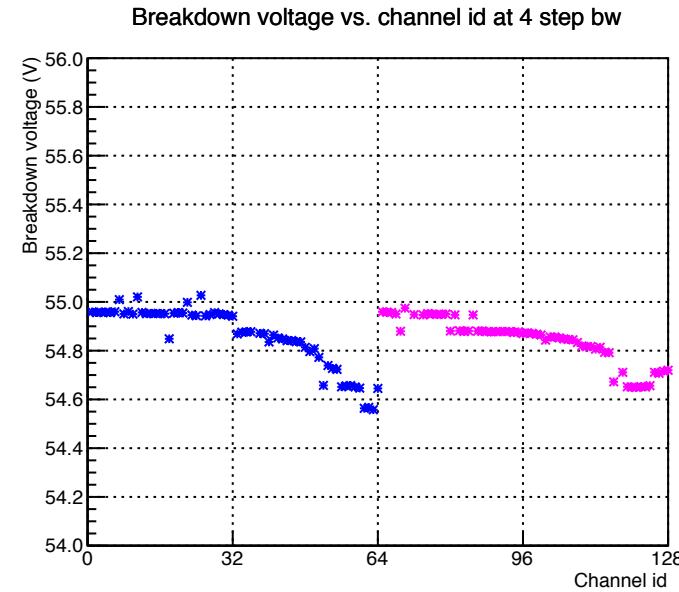
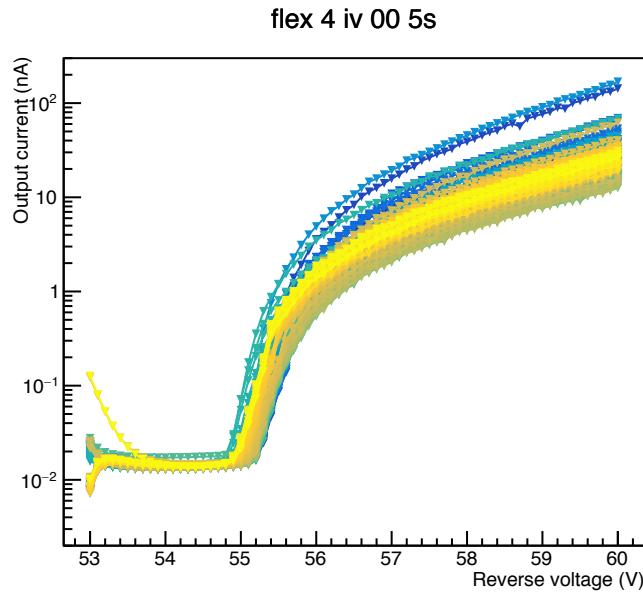
Spectral response range	λ	$VR=V_{op}$	320 to 900			nm
Peak sensitivity wavelength	λ_p	$VR=V_{op}$	--	450	--	nm
Photon detection efficiency at λ_p *1	PDE	$VR=V_{op}$	25	35	--	%

Layout of our SiPM array

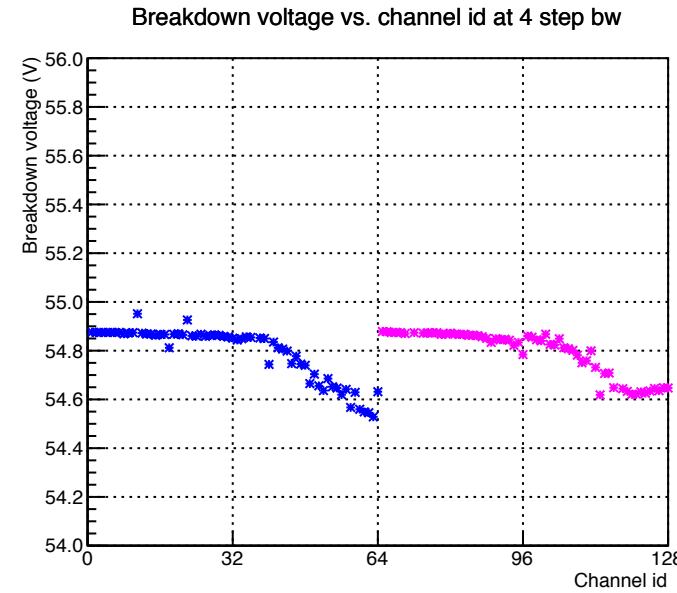
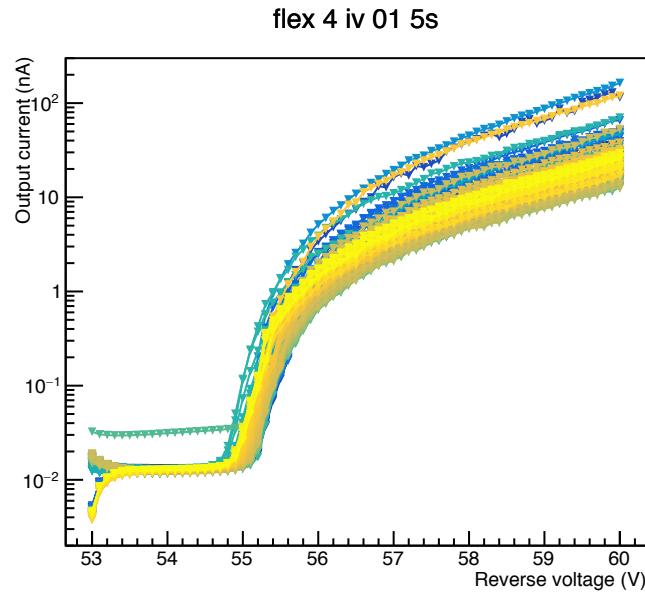


Flex 4 before thermal cycles

V_{BD} NON corrected by temperature



Flex 4 after thermal cycles V_{BD} NON corrected by temperature



DAQ board

- Altera Cyclone V FPGA.
- FEE board analogue signal digitization.
- Communication/data transfer via an USB3 port.
- DAQ architecture developed by the DPNC electronics group.
- Common digital interface and related control software, to be used by different experiments.

