

The Phase-1 Upgrade of the ATLAS Level-1 Endcap Muon Trigger

Tuesday, 23 May 2017 11:00 (18 minutes)

The LHC is expected to increase its instantaneous luminosity to $3 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$ after the 'Phase-1' upgrade, to take place from 2018-2020. In order to cope with the high luminosity, an upgrade of the ATLAS trigger system will be required.

The first-level Endcap Muon system identifies muons with high transverse momentum by combining data from fast a muon trigger detector, TGC, and some inner station detectors. In the Phase-1 upgrade a new detector, called the New-Small-Wheel (NSW), will be installed at the inner station region. Finer track information from the NSW can be used as part of the muon trigger logic to enhance performance significantly.

In order to handle data from both TGC and NSW some new electronics have been developed, including the trigger processor board known as 'Sector Logic'.

The Sector Logic board has a modern FPGA to make use of Multi-Gigabit transceiver technology, which will be used to receive data from the NSW. The readout system for trigger data has also been re-designed, with data transmission planned to be implemented with TCP/IP instead of a dedicated ASIC. This makes it possible to minimise the use of custom readout electronics and instead use some commercial PCs and network switches to collect, format and send the data.

This presentation will describe the aforementioned upgrades of the first-level Endcap Muon trigger system. Particular emphasis will be placed on the electronics and its firmware. The performance of the system and the trigger performance will be also discussed.

Summary

The LHC is expected to increase its instantaneous luminosity to $3 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$ after the 'Phase-1' upgrade, to take place from 2018-2020. In order to cope with the high luminosity, an upgrade of the ATLAS trigger system will be required.

The first-level Endcap Muon trigger system identifies muons with high transverse momentum from 40 MHz bunch crossings, using data from a fast muon trigger detectors, known as Thin Gap Chamber (TGC). The whole system is implemented on a special trigger circuit, which makes the trigger decision latency as short as 2.2 microseconds. In Run-2, the Endcap Muon trigger requires a coincidence between the TGC Big-Wheel (BW) at the middle station and the Small-Wheel at the inner station, in order to reduce the rate of fake triggers from beam-induced backgrounds caused by slow-particles from the endcap toroid or shields.

In the Phase-1 upgrade a new detector, called New-Small-Wheel (NSW), will be installed at the small wheel region. NSW will provide finer track position and direction information, which can be used in trigger selections by the newly developed trigger processor board known as "Sector Logic" to significantly improve performance. We aim to keep the trigger rate for muons with transverse momentum greater than 20 GeV/c, at the same level as it is now.

In order to handle data from both TGC and NSW some new electronics, including the 9U VME board known as 'Sector Logic', are being developed. The Sector Logic board has a modern FPGA to make use of Multi-Gigabit transceiver technology, which will be used to receive data from the NSW. The readout system for trigger data has also been re-designed, with data transmission implemented with TCP/IP instead of by a dedicated ASIC. This makes it possible to minimize the use of custom readout electronics and instead use some commercial PCs and network switches to collect, format, and send the data.

The new readout system was evaluated at the H8 test-beam line at the CERN SPS in November 2016, where data were collected properly and the new system integrated well with the ATLAS Trigger and DAQ infrastructure.

This presentation will describe the aforementioned upgrades of the first-level Endcap Muon trigger system. Particular emphasis will be placed on the new Sector Logic electronics and the firmware. The performance of the software readout system, and the latest results of the trigger performance study will be also discussed. We will present the estimated improvements in trigger performance for the new system with MC studies for LHC Run-3.

Primary author: SHUNICHI, Akatsuka (Kyoto University)

Presenter: SHUNICHI, Akatsuka (Kyoto University)

Session Classification: R3-Trigger and data acquisition systems(2)

Track Classification: Trigger and data acquisition systems