Upgrade of the ATLAS Monitored Drift Tube Frontend Electronics for the HL-LHC

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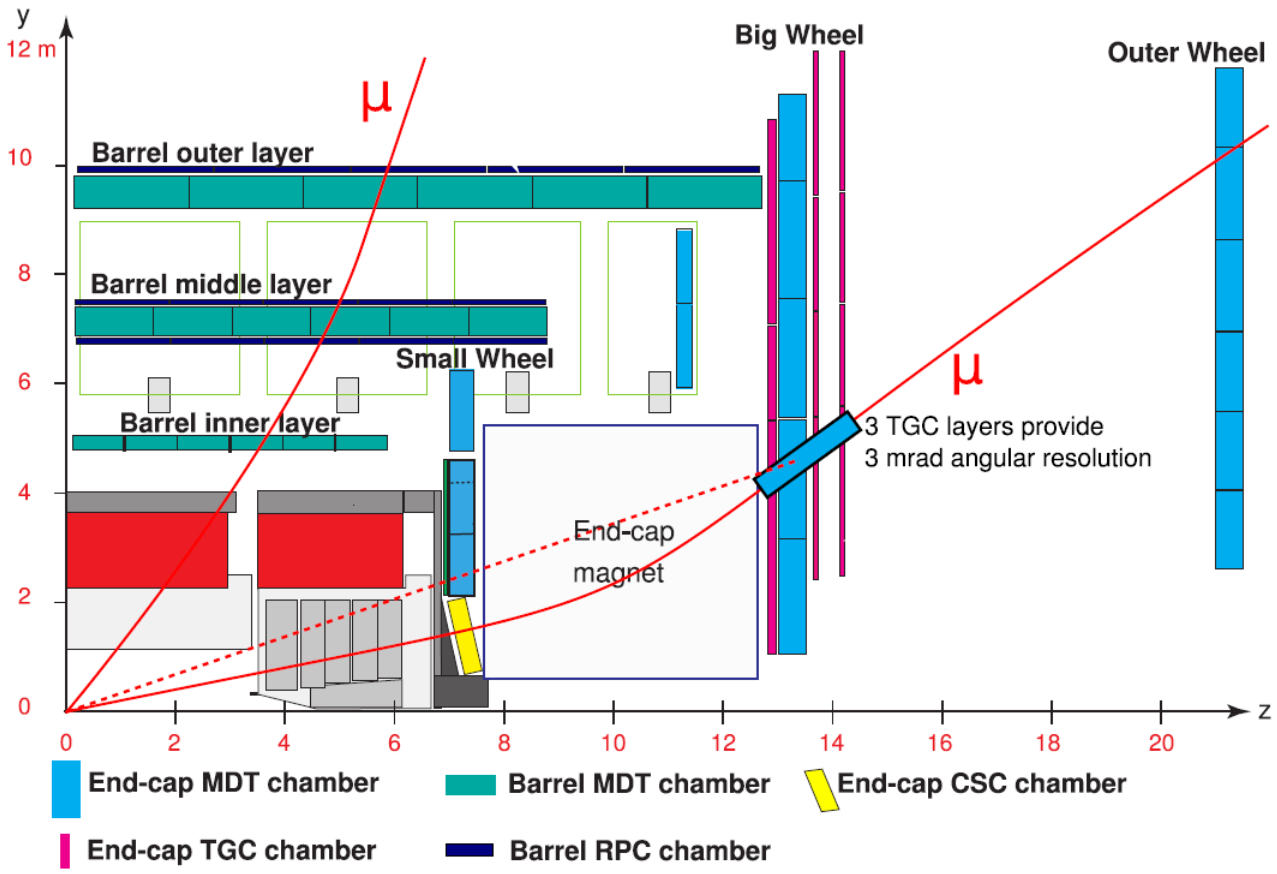
On behalf of the ATLAS Muon Collaboration

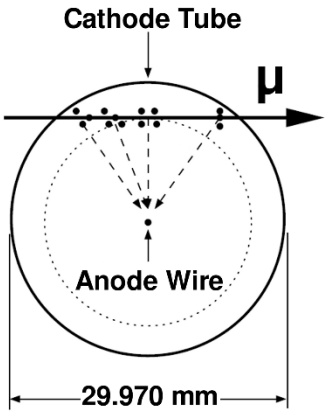
ATLAS muon spectrometer

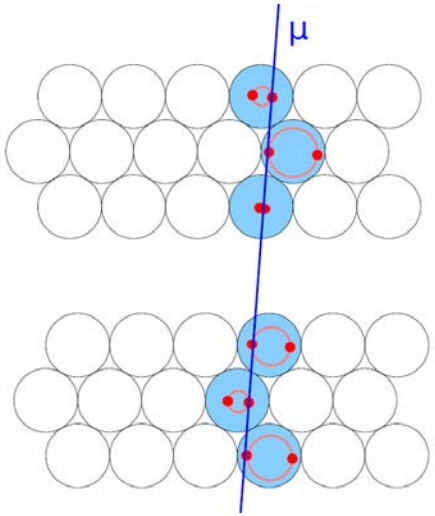
- The world's largest muon spectrometer for muon triggering, identification and momentum measurement
- RPCs/TGCs are used as primary trigger detectors
- MDTs/CSCs are used as precision trackers (10% momentum resolution for 1 TeV muon)

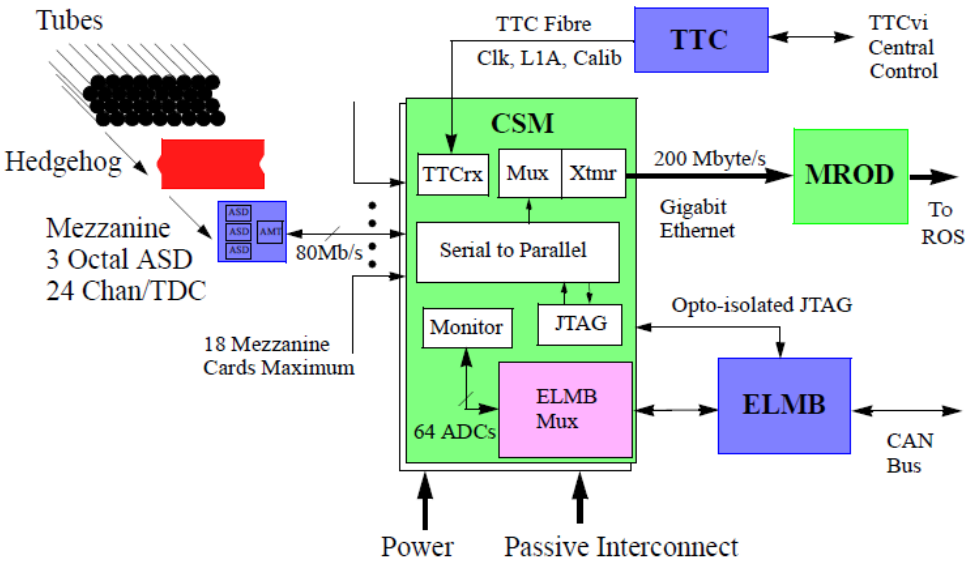


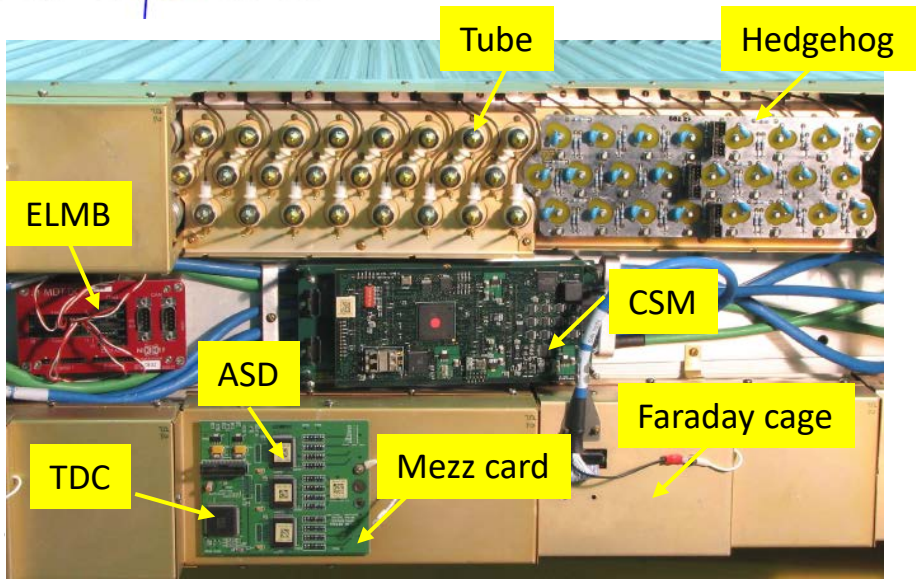
Monitored drift tube and its present readout system

- ~3 cm diameter, Ar/CO_2 (93:7) gas at 3 bar, maximum electron drift time 750 ns
- Average tube resolution of 80 µm
- About 354,000 tubes covering an area of 5000 m^2



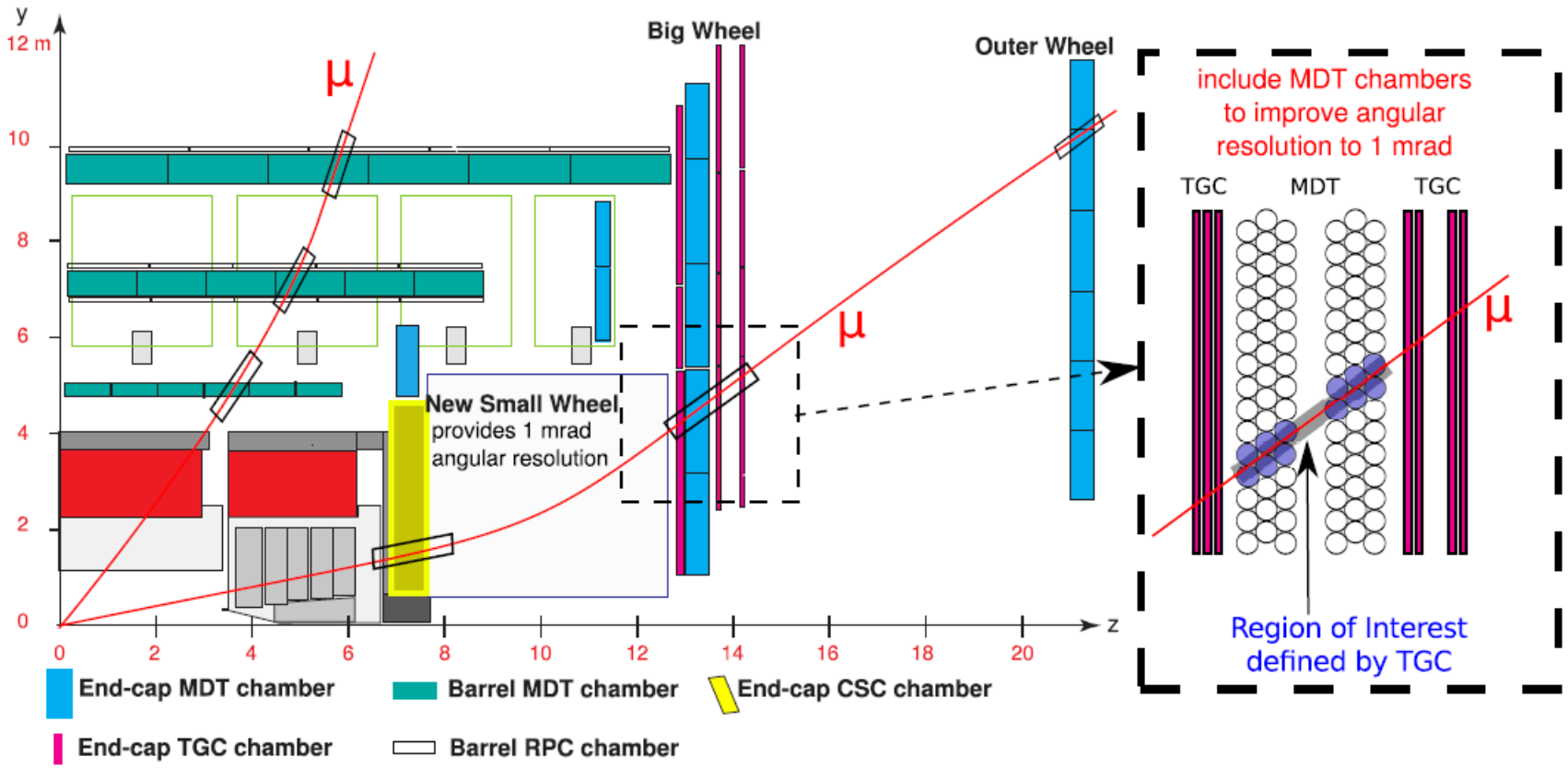




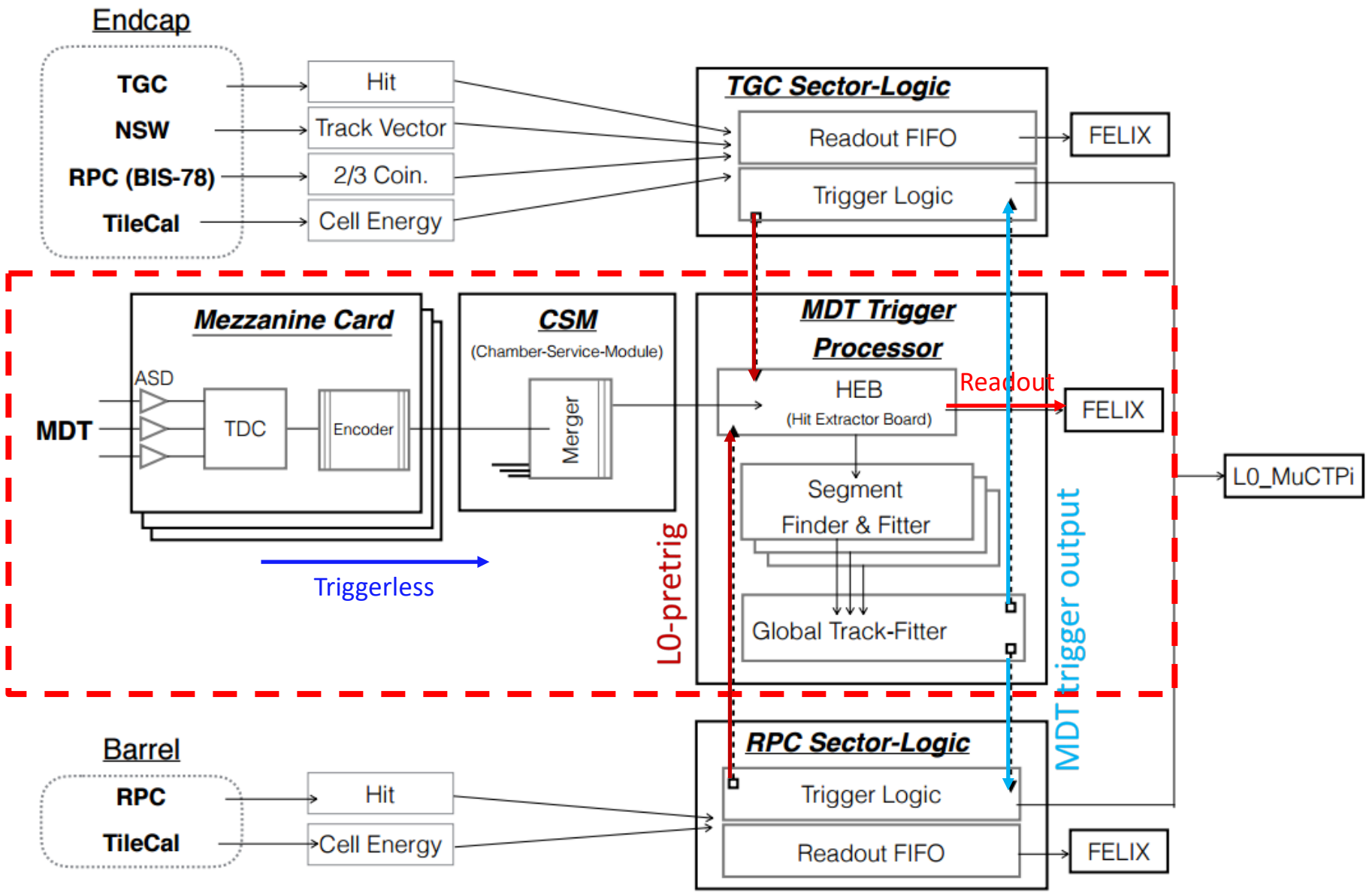


Muon triggering at HL-LHC

- New trigger and readout systems for MDT at HL-LHC
  - MDTs will be used at the first trigger level (L0) to improve the trigger muon momentum resolution and further reduce the amount of fake muons
  - Handle larger event rate and longer latency
  - RPCs/TGCs provide Bunch Crossing ID and regions of interest (L0 pre-trig)

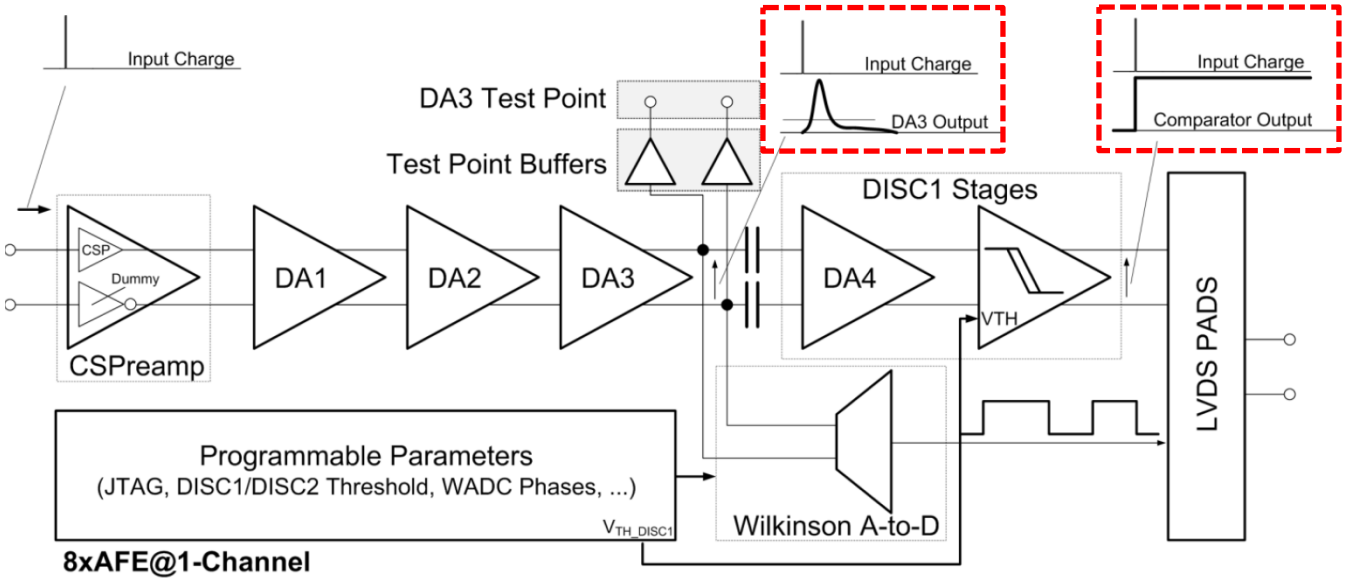


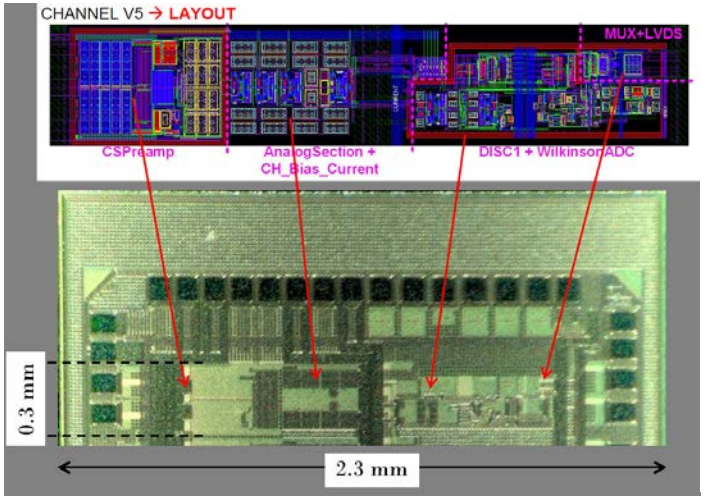
Proposed muon trigger and readout system



Amplifier-Shaper-Discriminator ASIC

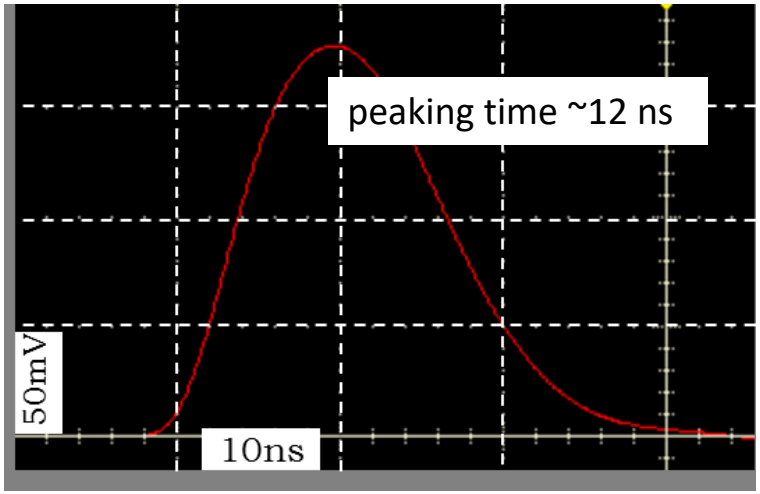
- 8-channel ASD developed using the GF 130 nm CMOS process (7.6 mm^2)
- Differential inputs, charge-sensitive pre-amplifier, differential-amplification (DA1-3), Wilkinson ADC, and discriminator (IEEE Sensors 2015)

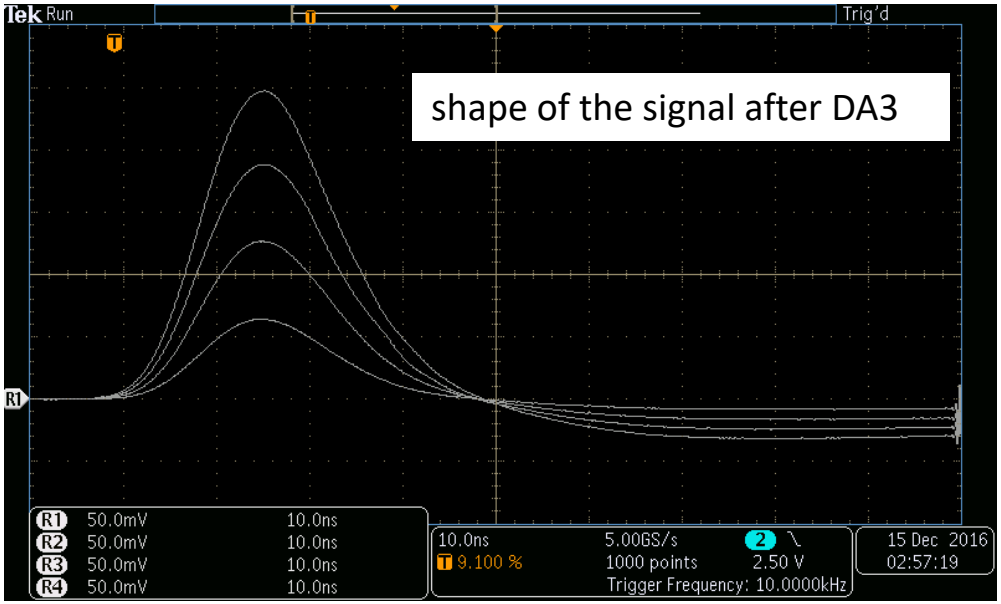


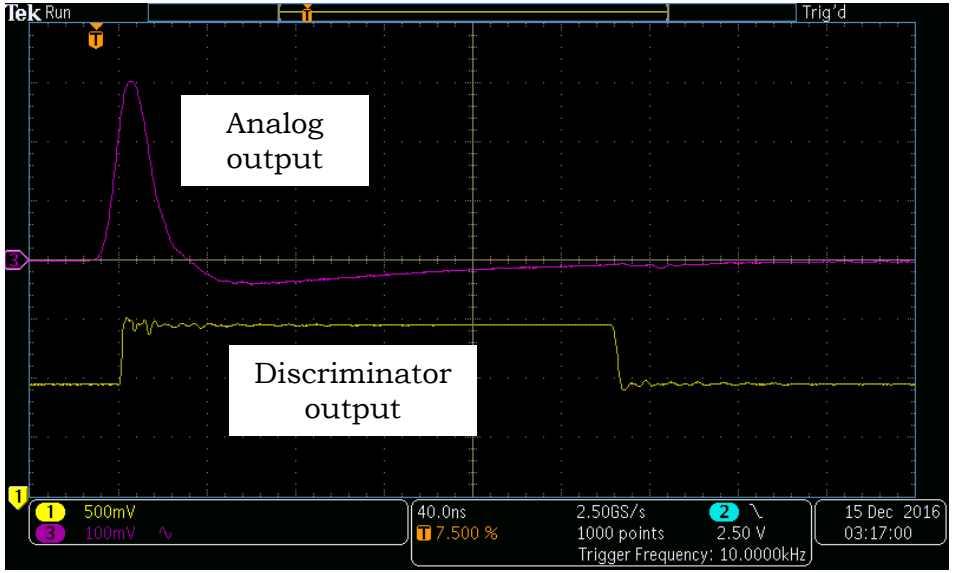


Parameter	This Work	Current TDC
CMOS Tech.	**0.13µm**	0.5 µm
Total Die Area	**6.38mm²**	11.9mm²
Supply Voltage	**3.3V**	3.3V
Channel Current Consumption	**10mA**	11mA
Detector Parasitic Cap.	**60pF**	60pF
Shaping Function	**Bipolar**	Bipolar
Input Charge	**5fC÷100fC**	5fC÷100fC
Front-End Delay at 100fC@Q_{IN}	**12ns**	~ 15ns
Front-End Sensitivity	**14mV/fC**	8.9mV/fC
ENC	**0.6fC**	1fC
SNR at minimum input charge	**15dB**	10.9dB

ASD DA3 and discriminator outputs

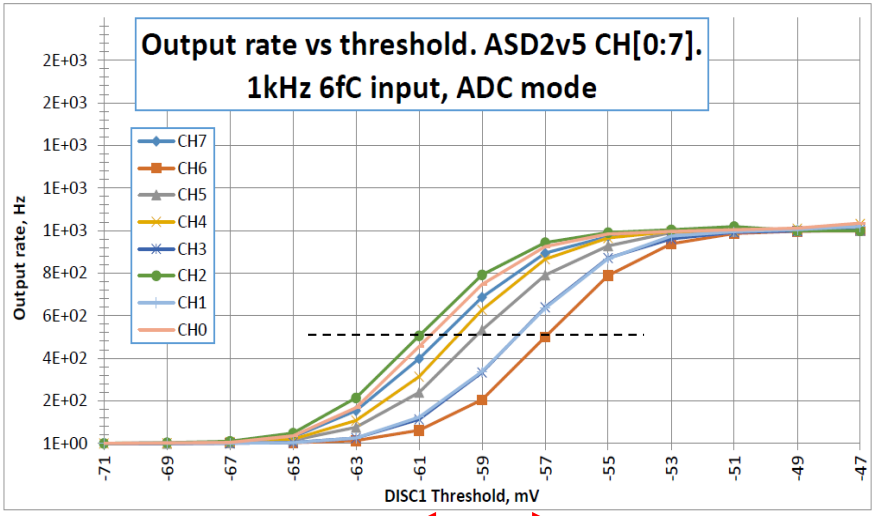




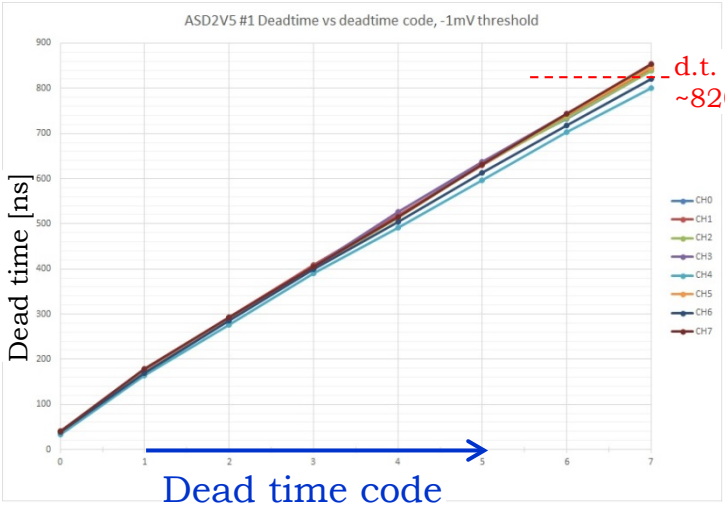


ASD DA3 and discriminator outputs

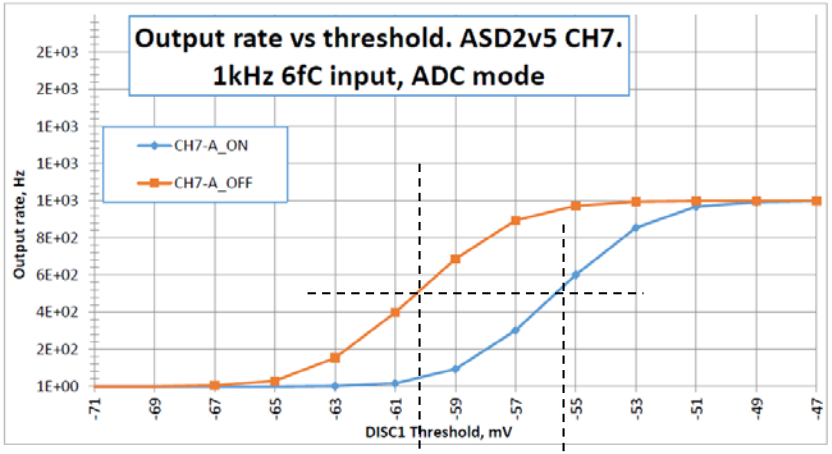
2. The spread of internal offset of channels is extremely low – 4mV. Channel 7 is in range with other channels.



~4 mV spread

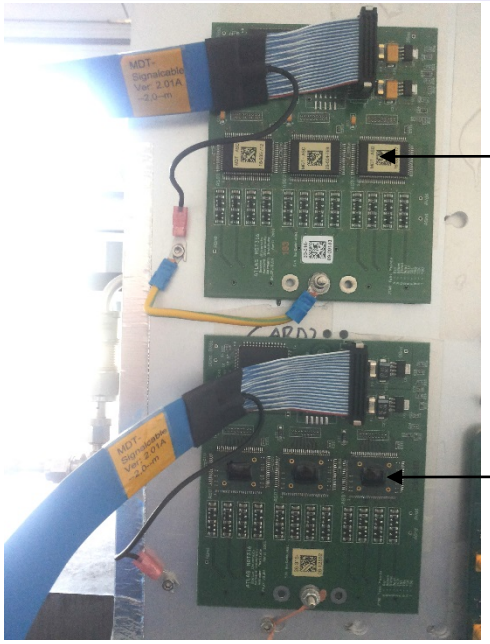


3. Enabling analog output on channel 7 adds very little load – effectively shifting threshold by 5mV



ON-OFF =~5 mV

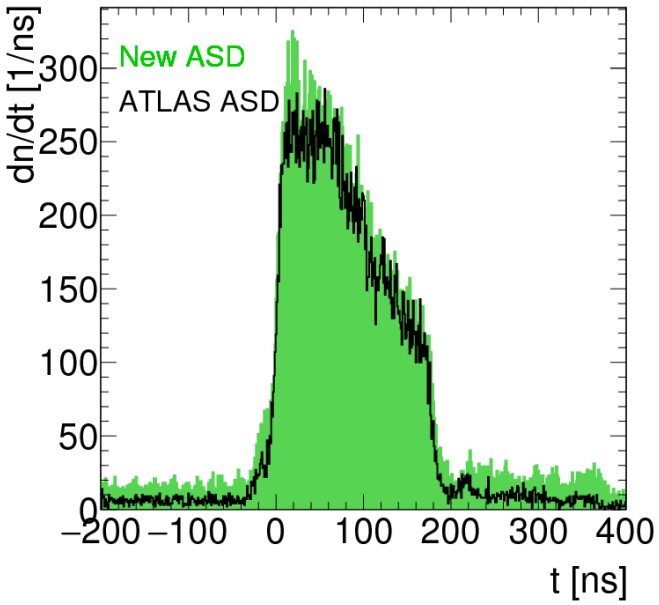
Cosmic-ray test of the new ASD



- Three new ASD chips were put on a mezzanine card for a cosmic-ray test on an sMDT chamber.

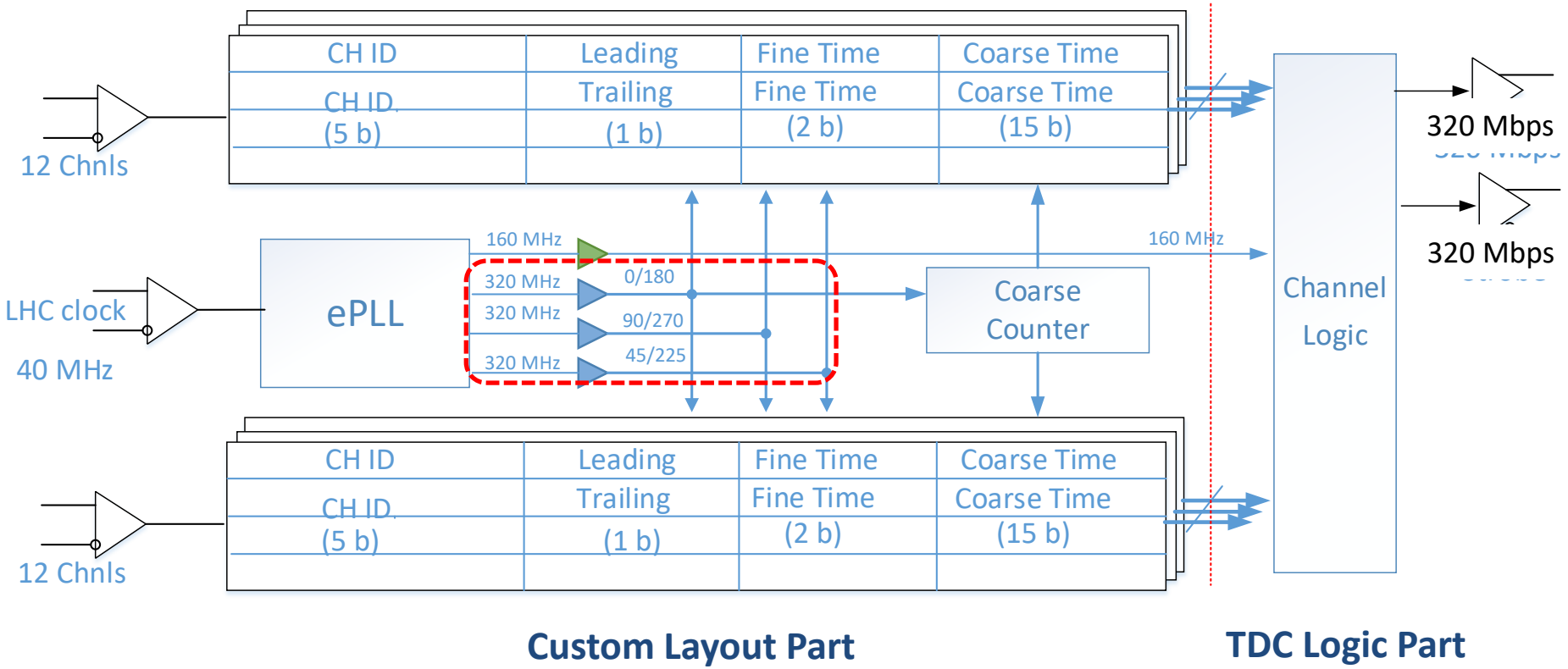
ATLAS standard mezzanine card as the reference

Mezzanine card with three new ASD chips



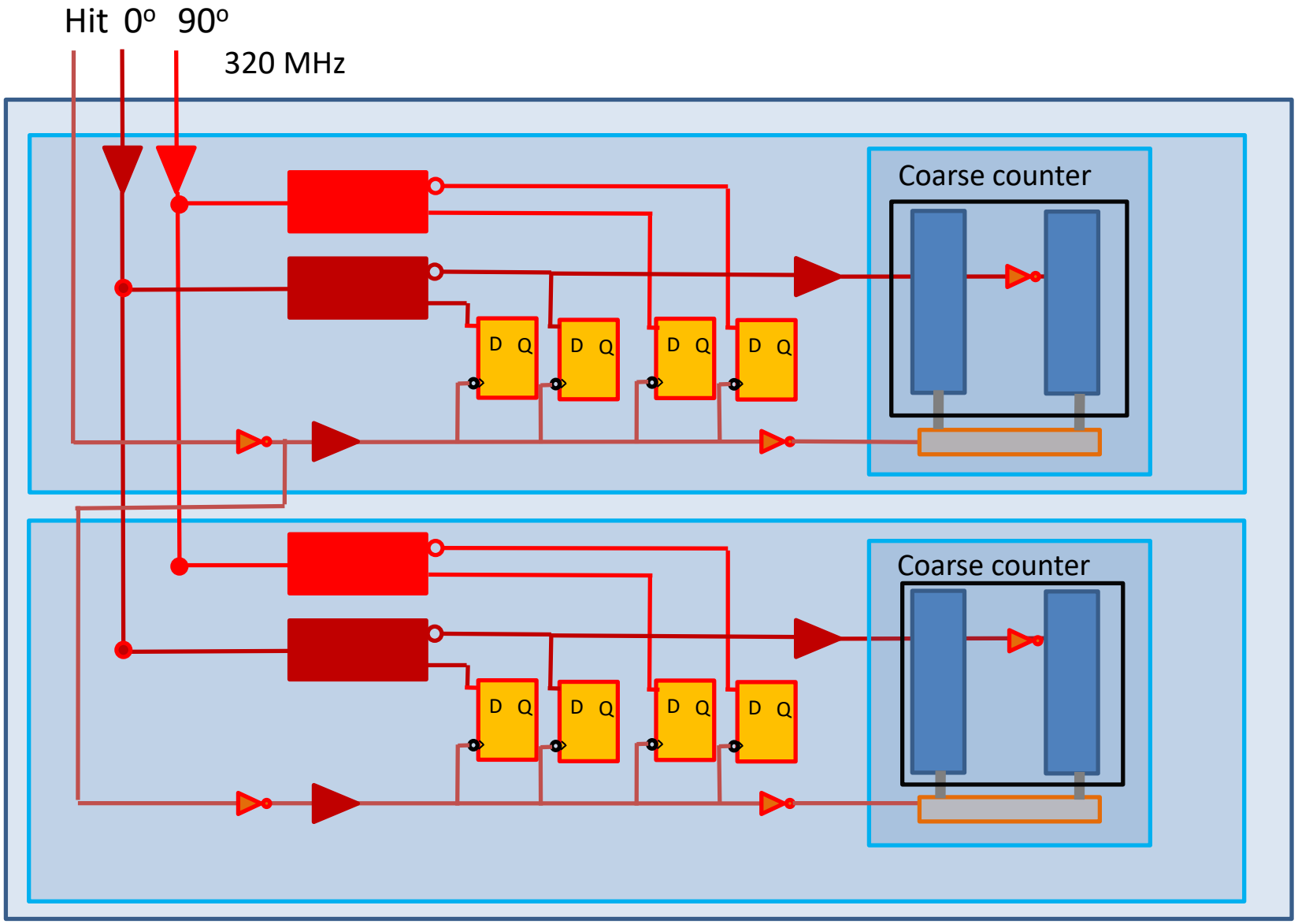
- Drift-time spectrum measured with the new ASD chips in excellent agreement with the drift-time spectrum measured with the present ATLAS ASD chips

Time-to-Digital Converter (TDC) ASIC

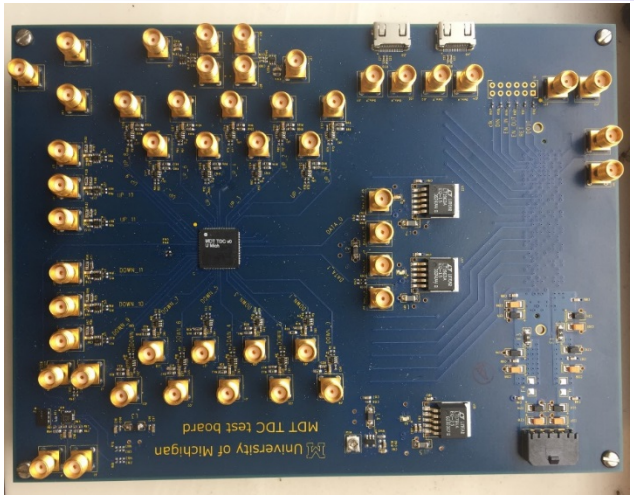


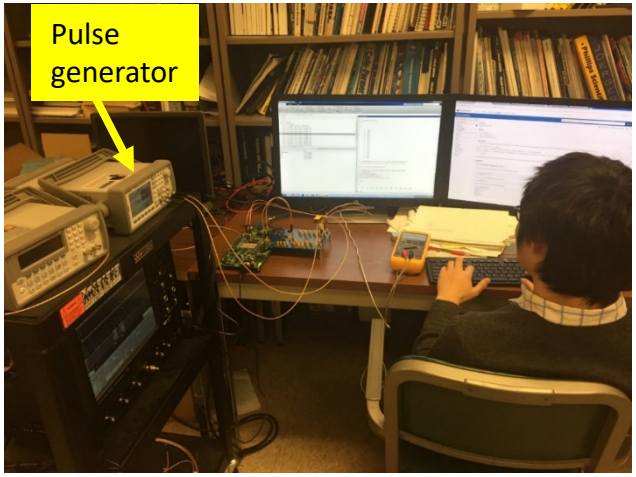
- Multiple clocks: 12 bits (25 ns, 40 MHz): 3 bits (3.125 ns, 320 MHz): 2 bits (0.78 ns, 4 phases of 320 MHz)
- Main components:
  - → Generation of multiple clock phases: ePLL (CERN, JINST 7, C12014, 2012)
  - → Time digitization (coarse + fine time)
  - → Time processing/calibration, output serial interface (TDC logic part)

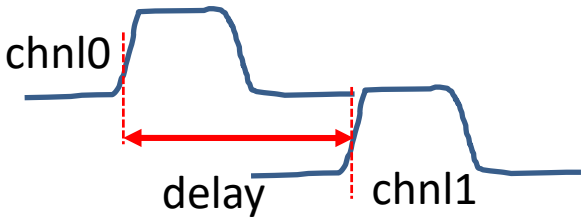
TDC time measurement

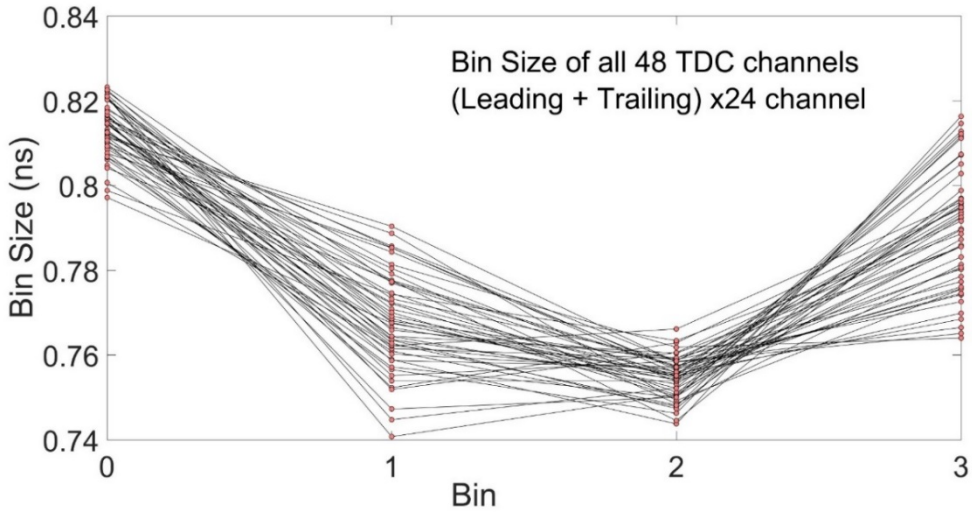


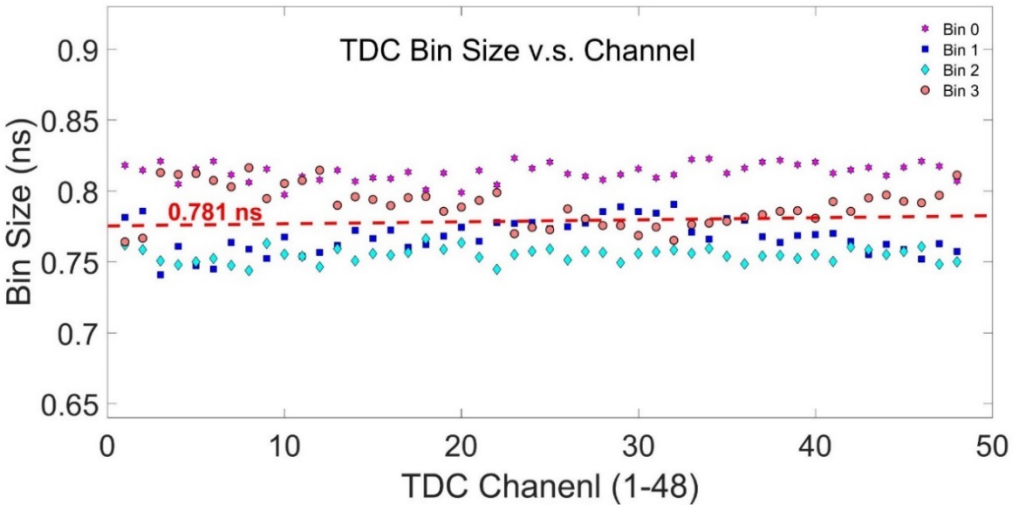
TDC performance





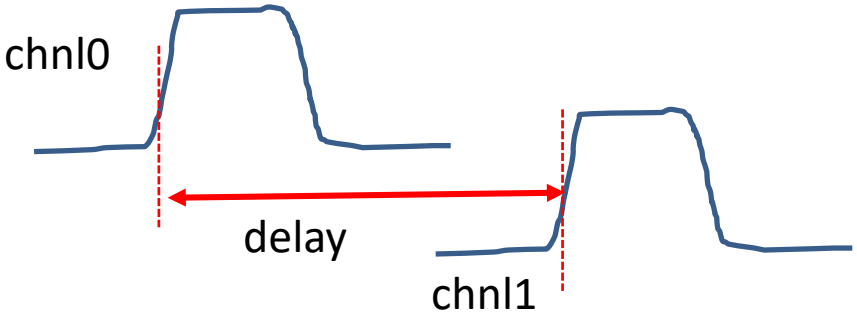


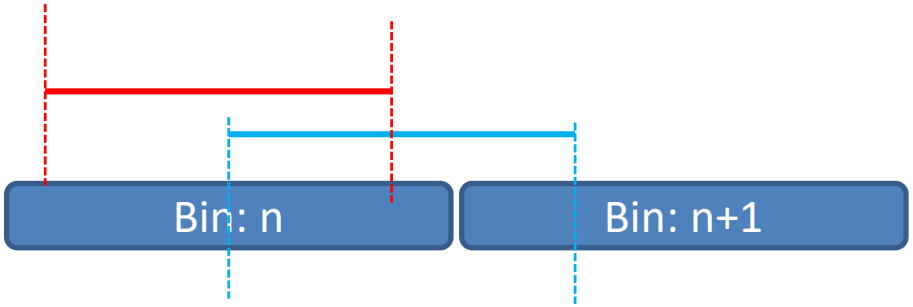




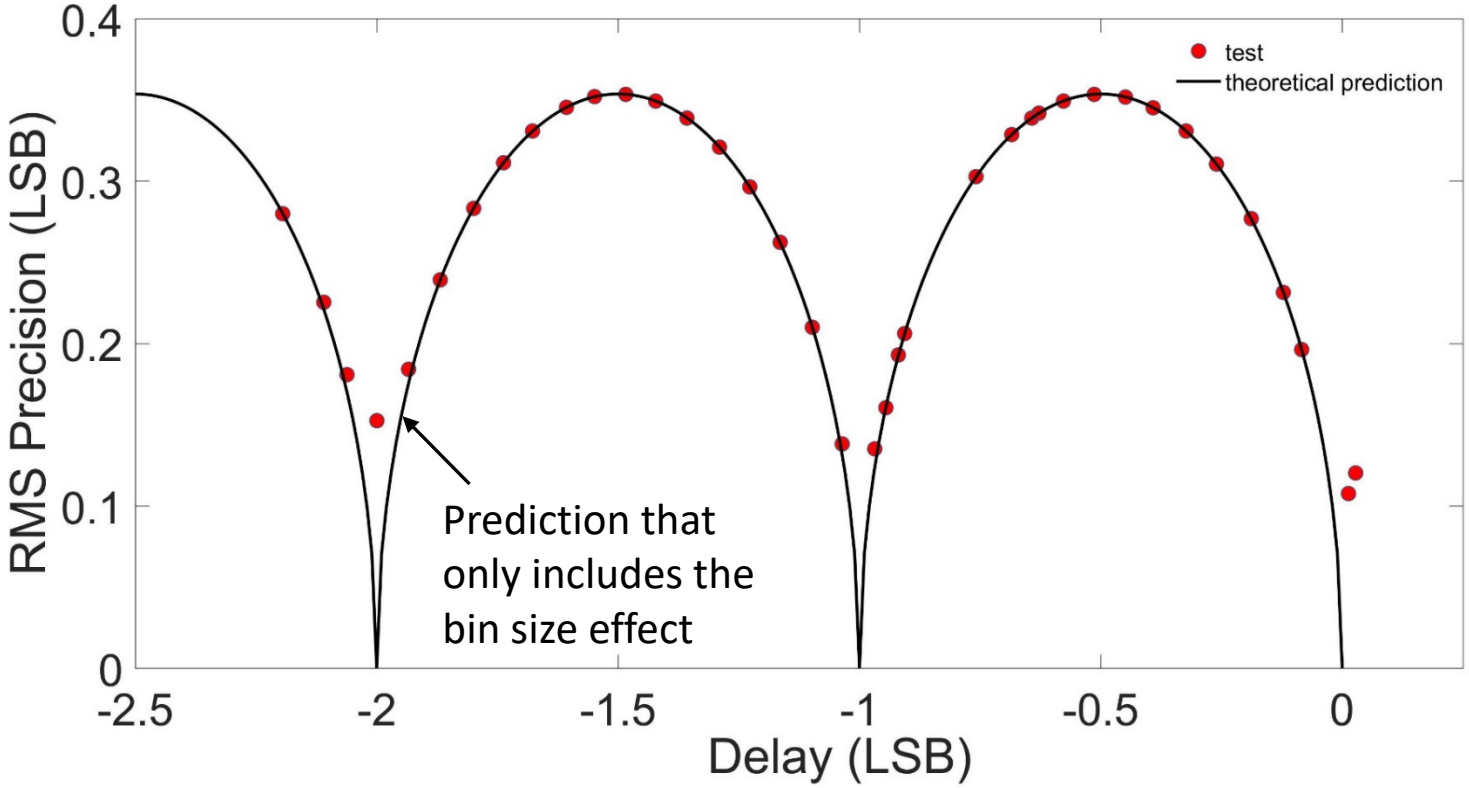
- Fabricated in GF 130 nm process (3.5 x 4.8 mm^2)
- Bin sizes for channels are within (0.78 ± 0.04) ns
- Integrated and differential non-linearity are less than 5% of the bin size

TDC performance



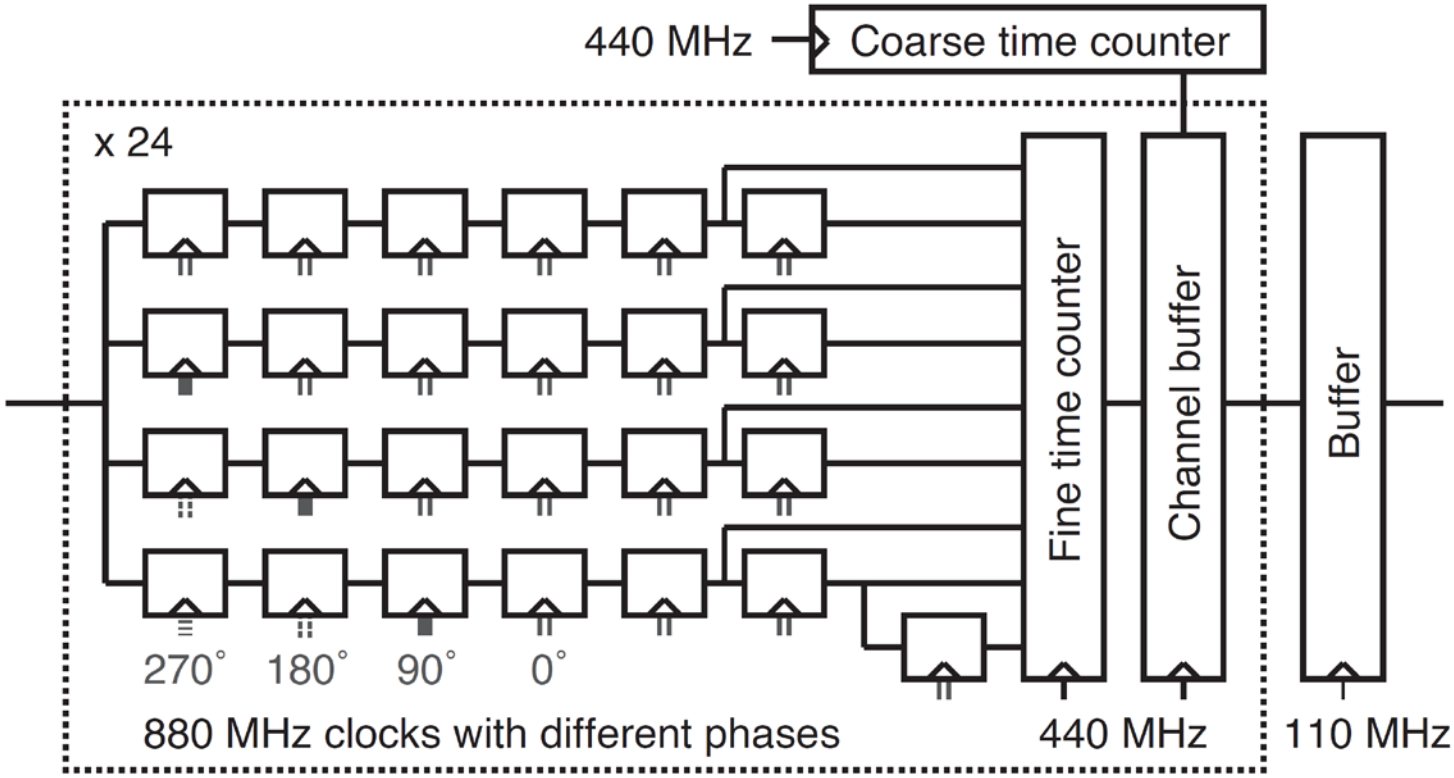


Theoretical prediction: sqrt[p(1-p)/2]
where p is the probability to fall in bin n+1



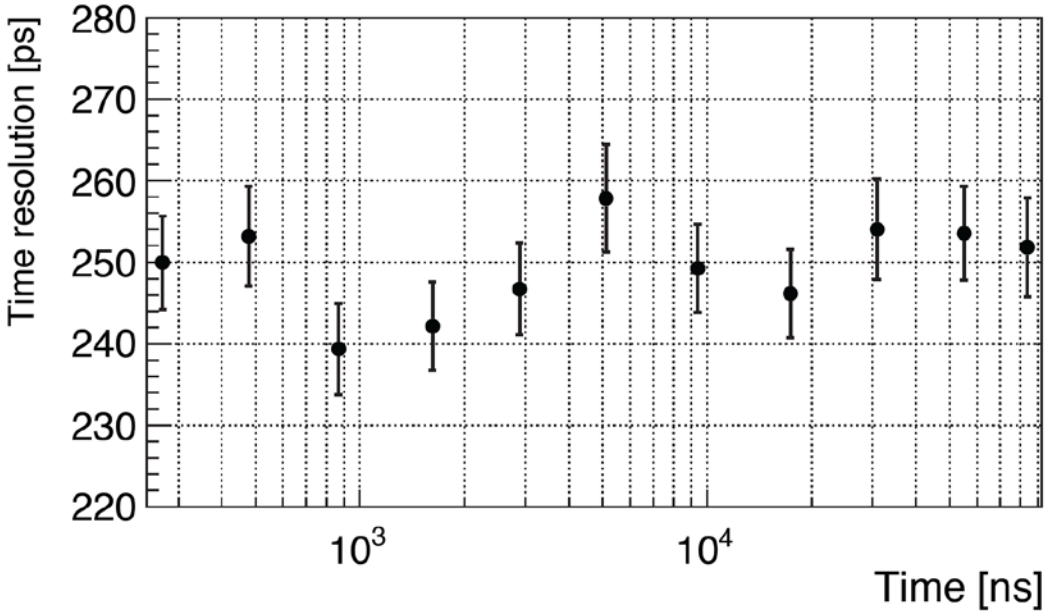
Time-to-Digital Converter (TDC) FPGA

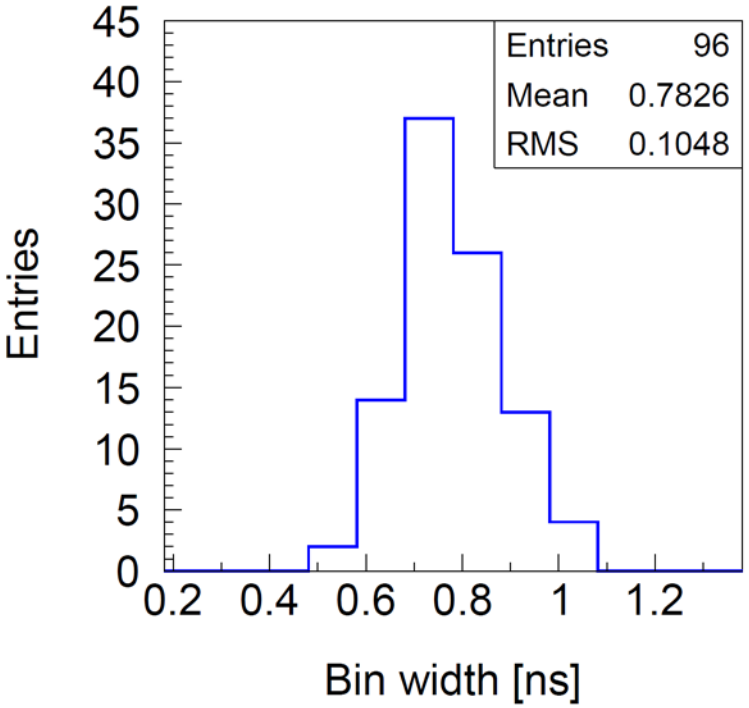
- FPGA TDC has the advantage of re-programmability and is an alternative option
- Performance studies using both Kintex-7 FPGA (0.28 ns bin size) and Microsemi IGLOO2 FPGA (0.78 ns bin size)
- Clocks at different phases are used to sample the hit
- Three-bit fine time measured with quad-phase clocks with 880 MHz frequency (for Kintex-7 FPGA)



Time-to-Digital Converter (TDC) FPGA

- PCBs with both Kintex-7 and IGLOO2 FPGAs were built
- IGLOO2 FPGA performance:
  - Measured time resolution is about 250 ps and close to the quantization error of 230 ps
  - Standard deviation for the bin width measurement: 100 ps
  - Differential and integral non-linearity is less than half of the bin size
  - Power consumption: ~0.5 W



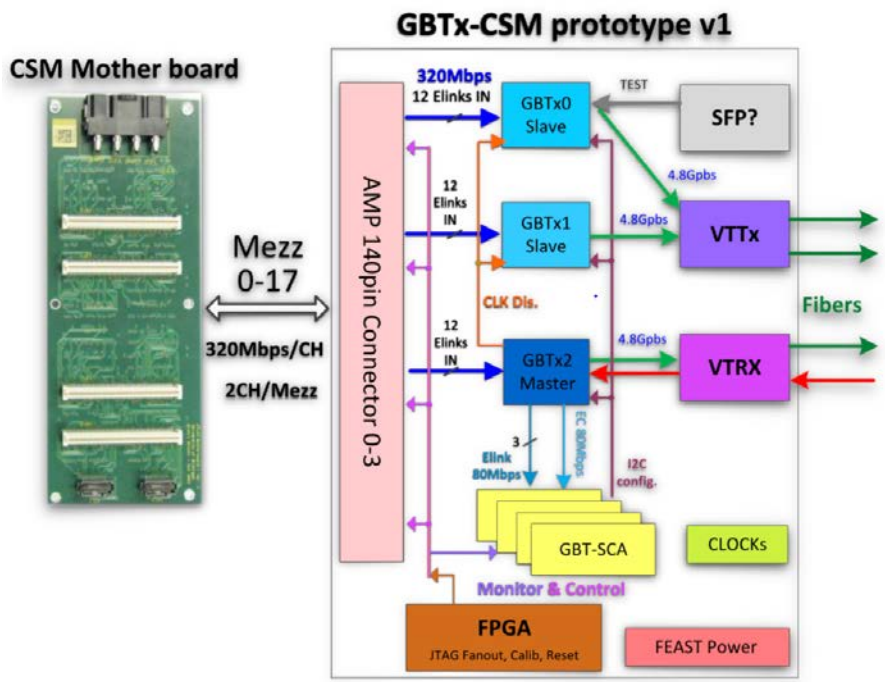


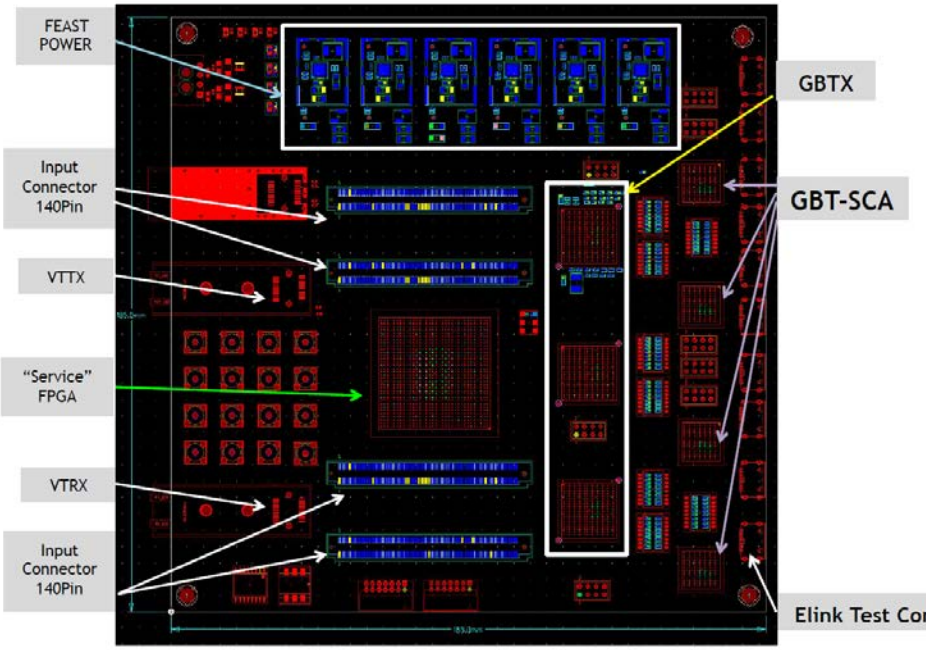
Chamber Service Module (CSM)

- Broadcast the Timing, Trigger and Control signals to the frontend mezzanine cards and send data from up to 18 mezzanine cards to USA-15 via optical links
- Two options under considerations:
  - FPGA-based CSM: flexibility and can easily handle old mezzs that can not be replaced at HL-LHC
  - GBTx-based CSM: radiation hard, natural choice for the FELIX system, require little maintenance after installation

GBTx-based CSM

- Use a service FPGA for JTAG configuration of all chips on mezzs
- One master GBTx to receive the signals from FELIX and HEB
- All three GBTxs send data to HEB via optical fibers
- SCAs used to configure slave GBTxs and provide monitoring information

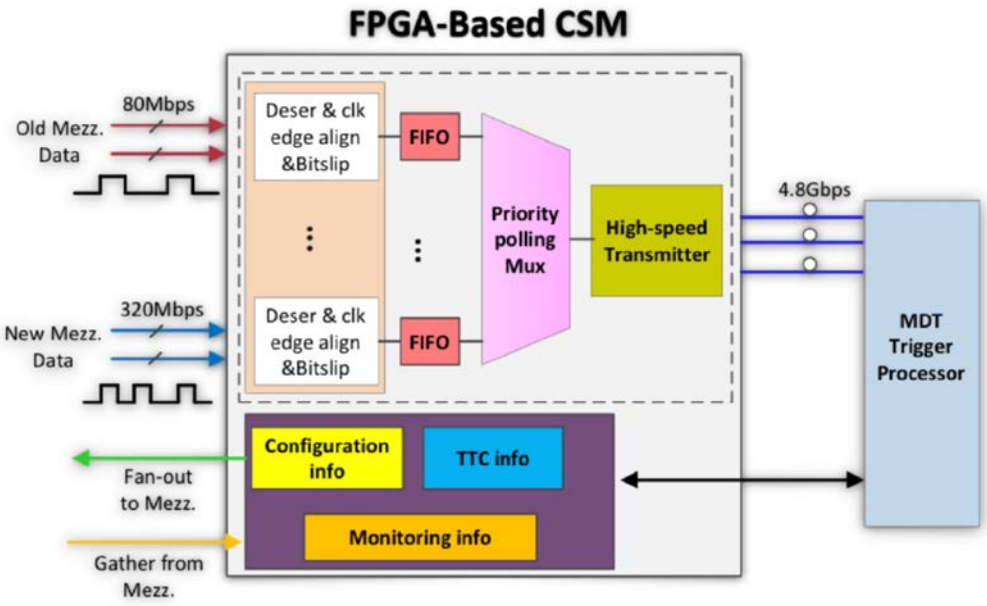


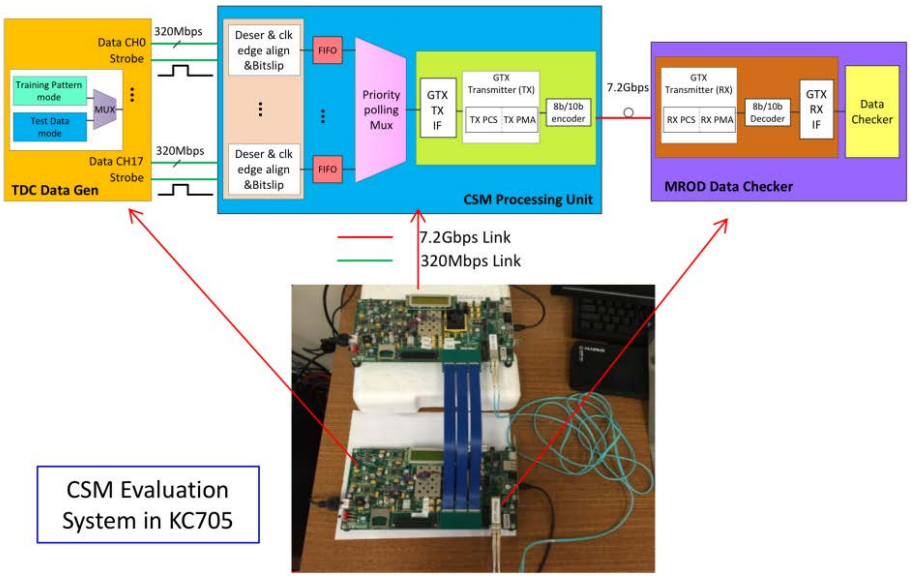


- A 1/3 demonstrator of the GBTx board has successfully shown to be able to pass data between GBTx and FPGA
- Fully prototype board is under development and will be connected to the current CSM motherboard

Chamber Service Module (CSM)

- Tested with a KC705 FPGA board with another KC705 to send mock signals from 18 mezzs
- Successfully demonstrated to handle 18 mezz cards with two lines running at 320 Mbps for each mezz
- Bit error rate found to be $<10^{-14}$





Conclusions

- Large dataset expected at the HL-LHC will increase the potentials to discover new physics at ATLAS
- ATLAS plans to use the MDT detector at the first trigger level to sharpen the trigger turn-on curve and reduce fake trigger muons
- Good progress made on all frontend electronics items
- Various working prototypes have been built
- Ongoing work with beam tests to demonstrate the whole trigger and readout chain