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Challenges and performance of frontier technology applied to an ATLAS Phase-I calorimeter trigger board dedicated to jet identification

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The 'Phase-I' upgrade of the Large Hadron Collider (LHC), scheduled to be completed in 2021, will lead to an enhanced collision luminosity of 2.5x10e34cm-2s-1.

To cope with the new and challenging accelerator conditions, all the CERN experiments have planned a major detector upgrade to be installed during the associated experimental shutdown period.

One of the physics goals of the ATLAS experiment is to maintain sensitivity to electroweak processes despite the increased number of interactions per LHC bunch crossing. To this end, the component of the first level hardware trigger based on calorimeter data will be upgraded to exploit fine-granularity readout using a new system of Feature EXtractors (FEXs), which each uses different physics objects for trigger selection. There will be three FEX systems in total, with this contribution focusing on the first prototype of the jet FEX (jFEX). This system identifies jets and large area tau candidates while also calculating global variables such as transverse energy sums and missing transverse energy.

The jFEX prototype is characterised by four large Xilinx Ultrascale Field Programmable Gate Arrays (FPGAs), XCVU190FLGA2577, so far the largest available on the market, capable of handling a data volume of more than 3 TB/s of input bandwidth. The choice of such large devices was driven by the requirement for large input bandwidth and processing power. This comes from the need to exploit high granularity calorimeter information and also run several jet identification algorithms within the few hundred nanoseconds latency budget (˜350 ns).

This presentation will report on the hardware design challenges and adopted solutions to preserve signal integrity within a densely populated high signal speed ATCA board. The parallel simulation activity that supported and validated the board design will also be presented. Particular emphasis will be given to the large FPGA power consumption effects on the boards. This was assessed via dedicated thermal simulation and cross-checked with a campaign of measurements. Preliminary results will also be presented from tests both at CERN and Mainz, based on the first jFEX prototype from December 2016.

Summary

Summary material in attached pdf.

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