

A multi-chip data acquisition system based on a heterogeneous system-on-chip platform.

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Content

The development of pixel detectors for future high-energy physics experiments requires flexible high-performance readout systems supporting a wide range of current and future device generations. The versatile readout system of the Control and Readout Inner tracking Board (CaRIBou) targets laboratory and high-rate test-beam measurements with a multitude of detector prototypes. Under the project umbrella, application-specific chipboards and a common interface card have been developed for a variety of pixel detector readout ASICs and active sensors. The boards are hosted by a commercial evaluation kit (ZC706). This talk focuses on the data acquisition system (DAQ) based on a heterogeneous Xilinx Zynq All Programmable System-on-Chip (AP SoC). The device integrates the software programmability of an ARM-based processor with the hardware programmability of an FPGA, enabling acceleration of the design, verification, test and commissioning processes. The CPU handles the slow control of the system, while the FPGA fabric performs data processing and data encapsulation in UDP datagrams moved by a Direct Memory Access (DMA) device through the High Performance Advanced Extensible Interface (AXI) port directly to the shared Random Access Memory (RAM). Further, data in RAM is accessed by the CPU for prompt analysis (data-quality monitoring, calibration, etc.) or is transferred eventually to a storage server over the Ethernet link using a standard Linux network stack and the DMA. Thanks to the fully capable dual-core processor running a Linux operating system, the DAQ board provides the unique user experience of a regular fully-functional remote terminal able to execute high level code (such as Python scripts). Moreover, as the code runs locally on the CPU integrated directly or indirectly (through the FPGA fabric) with the given ASIC, operations involving high input/output (I/O) activity (e.g. chip equalization) are not affected by network delays. The logic modules implemented in the FPGA fabric are available to the end user through the open source Linux device drivers maintained by the Xilinx community. In order to facilitate the creation of an embedded Linux distribution, CaRIBou provides a layer to the Yocto build framework supported by a large community of open-source and industrial developers. The talk presents the design of the SoC-based DAQ system, its building blocks and shows examples of the achieved functionality and performance for the CLICpix2 readout ASIC and the C3PD active CMOS sensor.

Summary

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