

A multi-chip data acquisition system based on a heterogeneous system-on-chip platform

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on behalf of the CLICdp collaboration

CERN, EP-LCD

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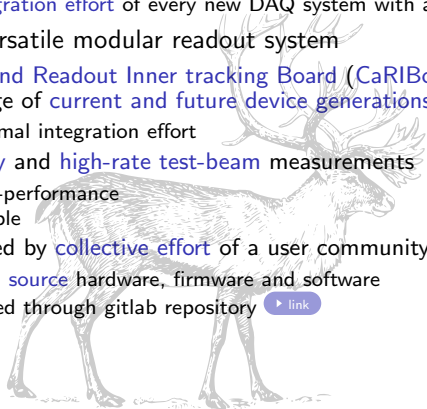
Outline

- 1 Motivation
- 2 Hardware
- 3 DAQ software
- 4 CLICpix2 use case

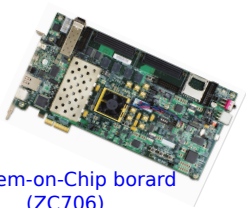


Motivation

- development of pixel detectors for future high-energy physics experiments
 - ▶ variety of DAQ systems
 - ★ chip characterisation requires **commissioning** and **debugging** of new hardware/firmware/software
 - ★ **not innovative** from functional point of view
 - ★ difficulty of **cross-compatibility**
 - ★ **integration effort** of every new DAQ system with a test-beam infrastructure
- solution: a versatile modular readout system
 - ▶ **Control and Readout Inner tracking Board (CaRIBou)**
 - ▶ wide range of **current and future device generations** support
 - ★ minimal integration effort
 - ▶ **laboratory and high-rate test-beam** measurements
 - ★ high-performance
 - ★ flexible
 - ▶ maintained by **collective effort** of a user community
 - ★ **open source** hardware, firmware and software
 - ★ shared through gitlab repository [▶ link](#)



CaRIBou as a multi-chip modular DAQ system



System-on-Chip board
(ZC706)



FMC cable
(optional)



interface board
(CaR)

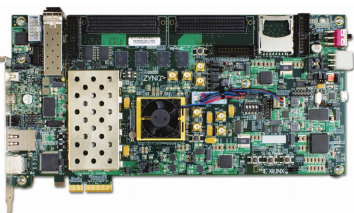


application specific
chipboard

Features:

- **CLICpix2/C3PD/FEI4/H35Demo/SOI-Cracow/Timepix3/...** support
 - ▶ set of chipboards with minimal functionality provided by users
- voltage regulators, ADCs, bias sources and clock generator are close to the chip on the directly connected interface CaR board
- **Zynq SoC** can be placed in a safe distance (~ 50 cm FMC cables) from the sensor assembly, to prevent radiation damage from sources or particle beams and facilitate mounting
- Zynq firmware and the interface CaR board developed by collective effort
 - ▶ collaboration under CaRIBOu project (Brookhaven National Lab, University of Geneva, CERN)

Commercial SoC ZC706 Evaluation Kit



- Zynq-7000 System-on-Chip (Z-7045)
- FMC HPC connector (8 GTX transceivers)
- FMC LPC connector (1 GTX transceiver)
- SFP+ connector
- availability
- cost effective and rapid solution for a small volume

Usage:

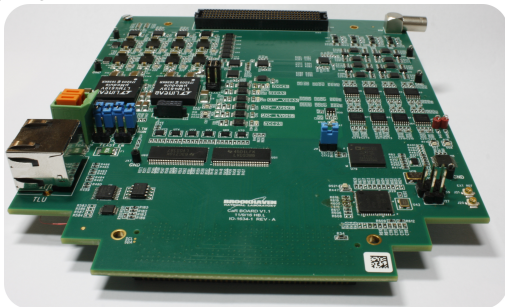
- the integrated dual core **ARM Cortex-A9 processor** runs **Linux OS** and the **actual DAQ software**
 - ▶ access through Secure Shell (*ssh*) connection (1Gbps Ethernet) or UART
- possibility of **prompt local software analysis** (data-quality monitoring, calibration, etc.)
- data pushed further through **1 Gbps** (RJ45) or **10 Gbps** Ethernet (SFP+)
 - ▶ possibility to use **other interfaces** of the evaluation kit (USB, SD card, PCIe) which are supported by the Linux kernel out of the box

Multi-chip CaR board v1.1 [▶ gitlab link](#)

- FMC mezzanine — FMC HPC Connector
- Chip Board Connector — Samtec SEAF 320 Pins
- 8 × general purpose power supplies

with monitoring capabilities

- ▶ Maximum current: 3 A
- ▶ Voltage range 0.8 — 3.6 V
- 32 × adjustable voltage output (0 — 4 V)
- 8 × current output (0 — 1 mA)
- 8 × voltage input (0 — 4 V)
- FEASTMP support
- 8 × full-duplex SERDES links
- ADC (16 channels, 65 MSPS/14-bit)
- 4 × injection pulser
- HV input
- I2C bus
- TLU RJ45 input (clock and trigger/shutter)
- general CMOS signals (10 × outputs, 14 × inputs) with adjustable voltage levels (0.8 - 3.6V)
- 17 × LVDS pairs — CML converters only on the specific chipboards
- output jitter attenuator/clock multiplier (SI5345)
 - ▶ Inputs: quartz, TLU, FMC, EXT (UMC)
 - ▶ Outputs: 3 × FMC (including GBT), 2 × SEAF, 1 × ADC
 - ▶ 0-delay mode

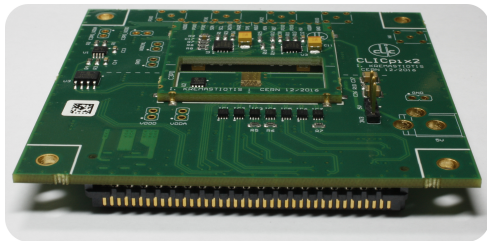


Suitable solution for various target chips:

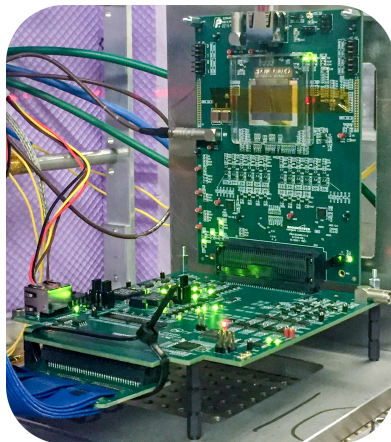
- support of many voltage levels, communication standards
- local measurement and monitor capabilities (ADCs)

Chipboards

- boards with **minimum functionality**
 - routing between SEAF connector and the chip under test
 - straightforward design
 - small production cost
 - specific buffers (LVDS-CML converters)
 - convenient test points



CLICpix2/C3PD chipboard



ATLAS FEI4/H35Demo chipboard mounted on CaR board

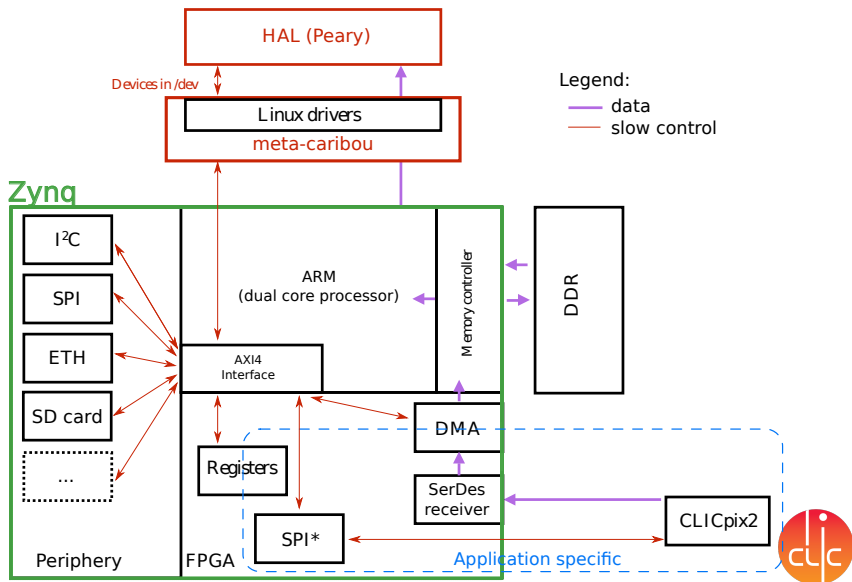
CaRIBou DAQ

CaRIBou DAQ consists of 3 parts shared through open access repositories:

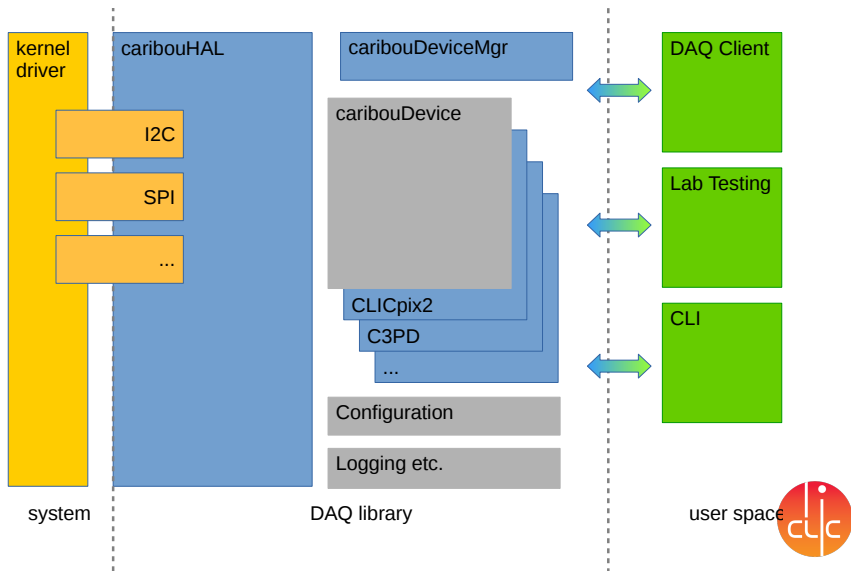
- **Peary** [▶ link](#) — software DAQ framework
- **Meta-caribou** [▶ link](#) — custom Linux distribution
- **Peary-firmware** [▶ link](#) — FPGA processing
 - ▶ universal CaR board unit
 - ▶ application specific unit
 - ★ library of sub-modules which can be ported between different applications



CaRIBou DAQ schematics



DAQ software framework for the CaRIBou DAQ System



DAQ software framework for the CaRIBou DAQ System

- control of the CaR board
 - ▶ user friendly [Hardware Abstraction Layer](#) (HAL)
 - ▶ unified way to access variety of hardware interfaces
- control of the chip
 - ▶ support of multiple devices in parallel (i.e.readout chip + sensor)
- device manager
 - ▶ [dynamic linking](#) of libraries based on device name stored in the configuration files
- [Command Line Interface \(CLI\)](#) support
- DAQ client support
 - ▶ integration with the top DAQ run control



Yocto layer customizing CaRIBou specific Linux distribution

CaRIBou customization:

- A console-only image with **full-featured Linux system** functionality installed
 - ▶ popular packages (python, ssh, gdb, etc.) pre-installed
- **Secondary Program Loader (SPL)**
 - ▶ loads FPGA firmware (bitfile from Peary-firmware)
 - ▶ set ARM CPUs in the desired state (Peary-firmware)
- integrated with fixed revision of Peary-firmware
 - ▶ resources automatically fetched by build process
- **CaR specific hardware description** (Device tree)
- SD image creation which can be raw copied
 - ▶ dedicated script (`/meta-caribou/scripts/preapre_sd.sh`)



full-featured Linux OS system

```
afiergol@adrian-laptop: ~  
afiergol@adrian-laptop:~$ ssh root@pclcd-zynq  
Last login: Thu May 18 14:36:31 2017 from 128.141.234.143  
root@caribou:~# uname -r  
4.6.0-xilinx-v2016.3  
root@caribou:~# python --version  
Python 2.7.12  
root@caribou:~# pearycli -c config.cfg  
[14:37:53.973] INFO: Welcome to pearyCLI.  
[14:37:53.974] INFO: Currently 0 devices configured.  
[14:37:53.974] INFO: To add new devices use the "add_device" command.  
# add_device CLICpix2  
[14:38:04.305] INFO: Creating new instance of device "CLICpix2".  
[14:38:04.305] QUIET: New Caribou device instance, version peary v0.5+24-g6dd100e  
[14:38:04.305] QUIET: Firmware version: 0x7aa2e557 (15/5/2017 14:21:23)  
[14:38:04.315] INFO: Appending instance to device list, device ID 0  
[14:38:04.315] INFO: Manager returned device ID 0.  
# init 0
```



- configuration of the System-on-Chip (SoC)
 - ▶ periphery
 - ▶ address space
 - ▶ clock frequencies
- design handled by [Xilinx IP Integrator](#)
 - ▶ autonomous blocks following [IP-XACT](#) standard
 - ▶ easy integration
- library of Vivado IPs (i.e. DMA, SPI, I2C, etc.)
 - ▶ [Linux device drivers](#) maintained by Xilinx community of users
- application specific blocks
 - ▶ provide access to the chip (i.e. CLICpix2)
 - ▶ [System Verilog](#) support
 - ▶ easily accessible from software through `/dev/mem` device
 - ▶ set of [custom sub-modules](#) (like SerDes receiver, custom SPI) already [available in the repository](#)
 - ★ software support examples
- Linux device tree and SPL generation
 - ▶ based on Hardware Description File (HDF)



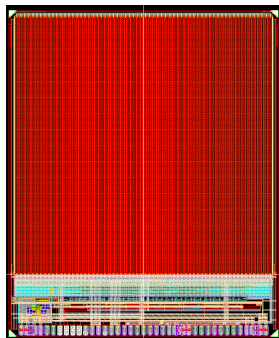
CLICpix2 readout chip specification

- 65 nm CMOS technology

- pixel matrix:

Matrix size [pixels]	128 × 128
Active area [mm^2]	3.2 × 3.2
ToT counter	5 bits
ToA counter	8 bits

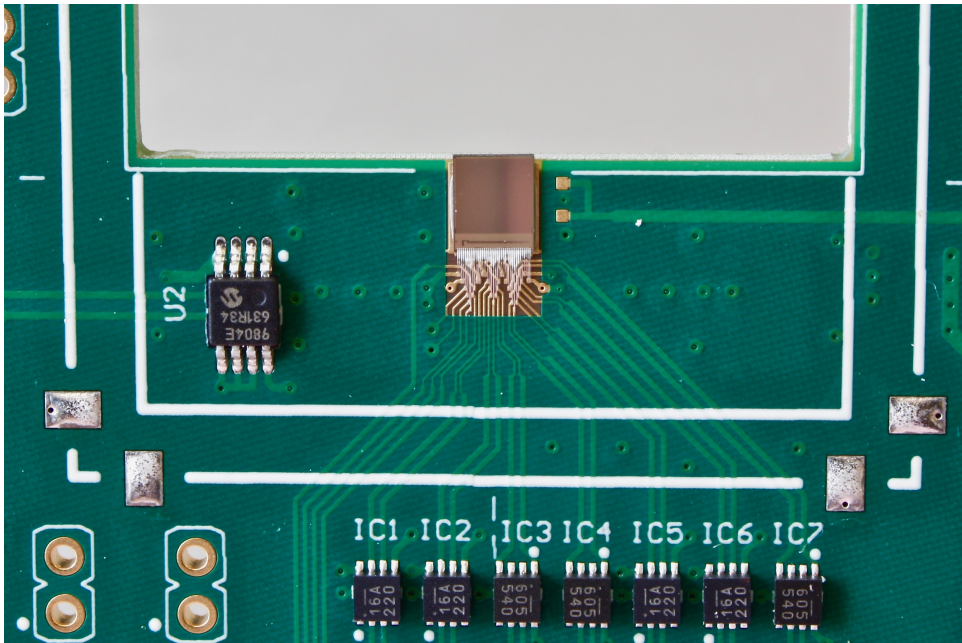
- readout protocol based on Ethernet-like 640 Mbps SerDes stream
- configuration over SPI protocol (100 MHz)
- data compression
- frame encoding
- test pulse
- power pulsing



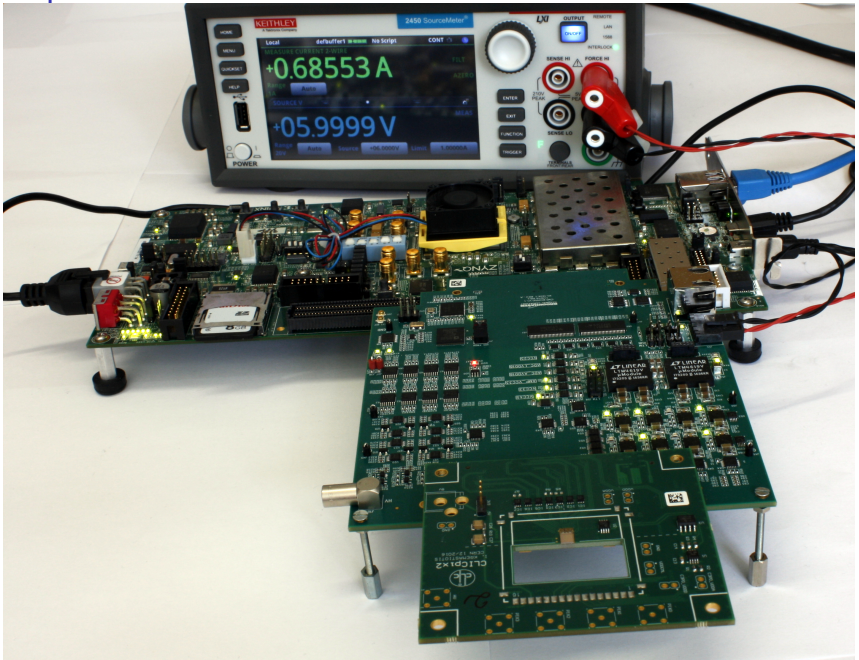
P. Valerio, E. Santin



CLICpix2 assembly

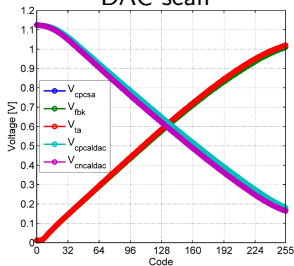


CLICpix2 in CaRIBou framework

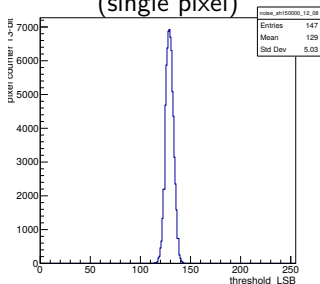


CLICpix2 commissioning using CaRIBou

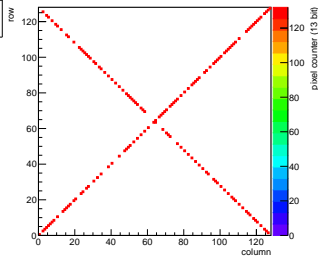
DAC scan



Threshold scan
(single pixel)



Matrix response



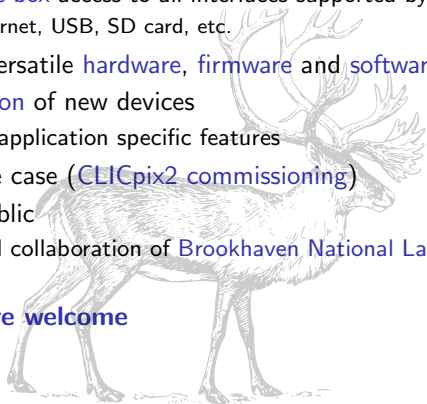
The measurements involved different features of the CaRIBou system:

- SerDes readout and software frame decoding
- chip configuration over SPI
- bias voltage and current source scans (DACs of the CaR board)
- local voltage measurements (ADCs of the CaR board)
- local clock generation using the CaR board resources
- adjustment and monitoring of power provided by the CaR board

Summary

The CaRIBou DAQ system:

- unique user experience of a regular **fully-functional Linux** terminal
- **rapid implementation**
- flexibility
 - ▶ can run locally user code written in **any language**
 - ▶ **out of the box** access to all interfaces supported by **Linux kernel**
 - ★ Ethernet, USB, SD card, etc.
- comes with versatile **hardware, firmware** and **software**
- **easy integration** of new devices
 - ▶ focus on application specific features
- successful use case (**CLICpix2 commissioning**)
- is open to public
 - ▶ successful collaboration of **Brookhaven National Lab, University of Geneva** and **CERN**
- **new users are welcome**





Thank you for your attention.

