Development of Radiation-Hard ASICs for the ATLAS Phase-1 Liquid Argon Calorimeter Readout Electronics Upgrade

Tim Andeen*, Jaroslav BAN, Nancy BISHOP, Gustaaf BROOIJMANS, Alex EMERMAN,Ines OCHOA, John PARSONS, William SIPPACH, Qiang WANG
* Now with UT Austin

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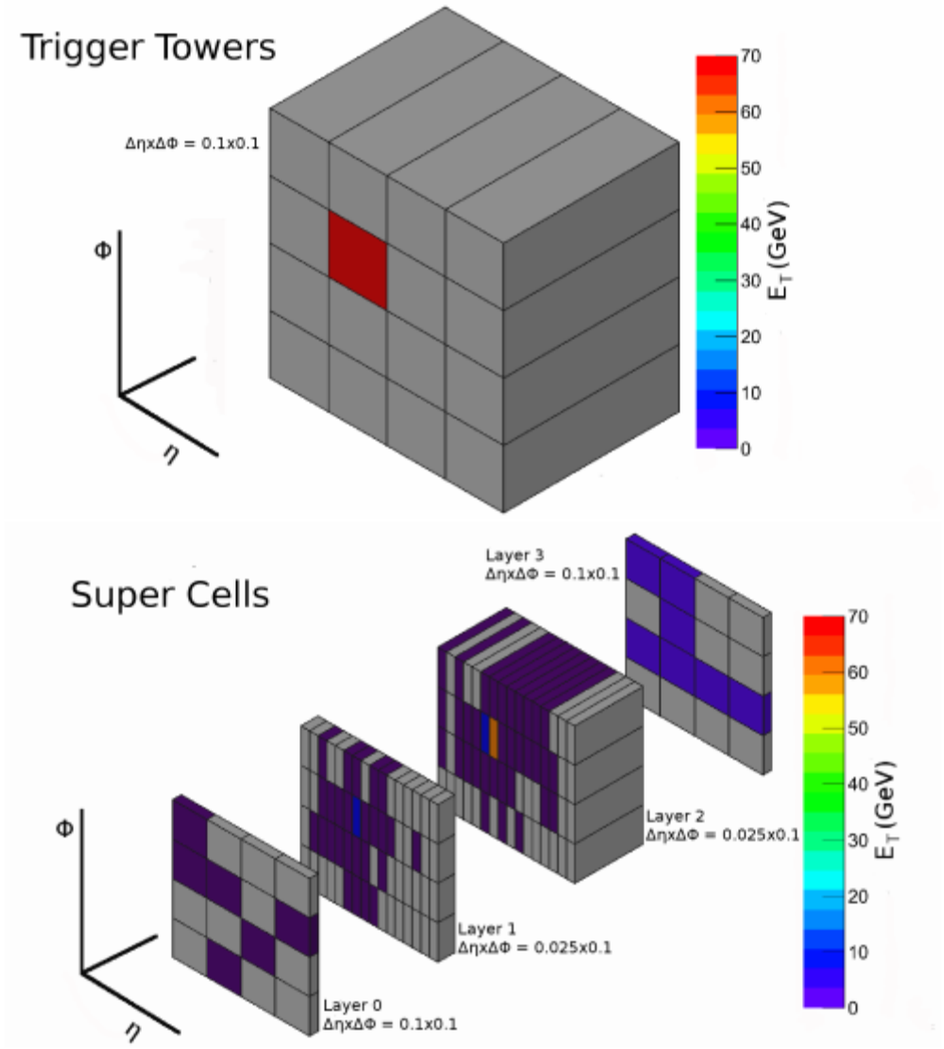
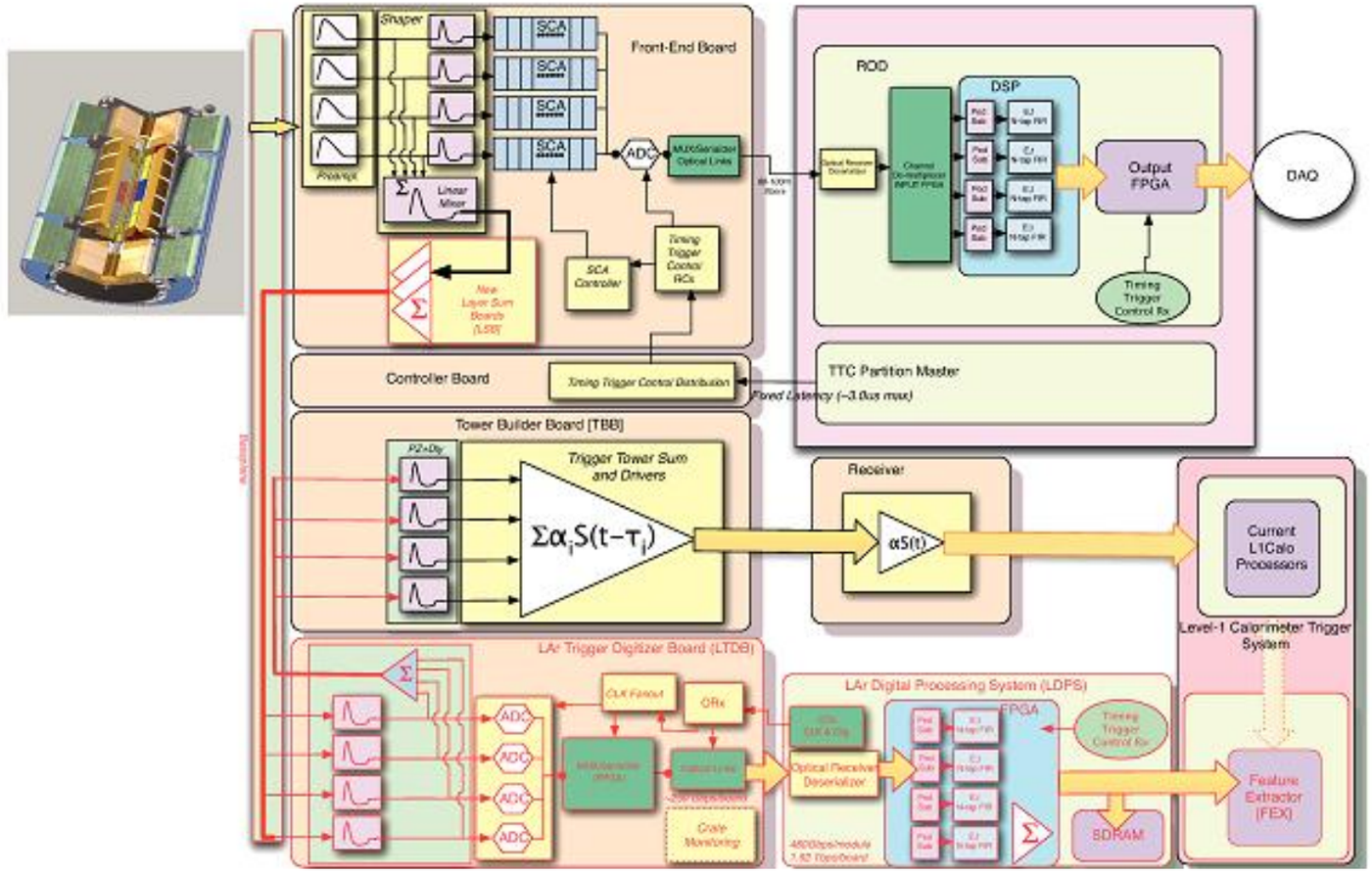
Introduction



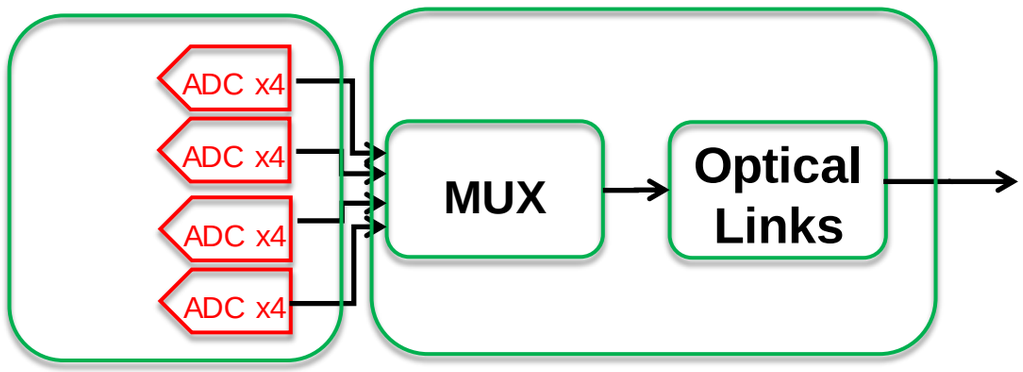
Simulation of energy deposition for a 70 GeV electron in the current trigger tower system (top) compared to the ne w super cell readout (bottom)



The Phase-I LAr electronics layout

Signal sampling

Data transmission off detector



Outline

- **Nevis ADC chip**

  A radiation-hard four-channel 12-bit 40 MS/s pipeline ADC

  - **Requirements**
  - **Development roadmap**
  - **Chip design**
  - **Performance test**
  - **Radiation test**

- **LArTDS chip**

  Multiplexes 16 channels of ADC data, then scrambles and serializes the data for transmission over optical links

- **Front-end readout electronic test**
- **Summary**

Nevis ADC

- **Requirements**
  - Signals must be continuously sampled and digitized at a frequency of 40 MHz
  - ADC power must be less than 145 mW/ch
  - Latency must be less than 200 ns
  - Must be radiation tolerant up to 100 kRad Total Ionizing Dose(TID) and test for SEU with a total fluency of 3.8 x 10^{12} h/cm^2
  - The energy measurement requires a dynamic range of approximately 12 bits to digitize energies from 32 MeV to 102 GeV for the front layer trigger cells and from 125 MeV to 400 GeV in the middle layer trigger cells

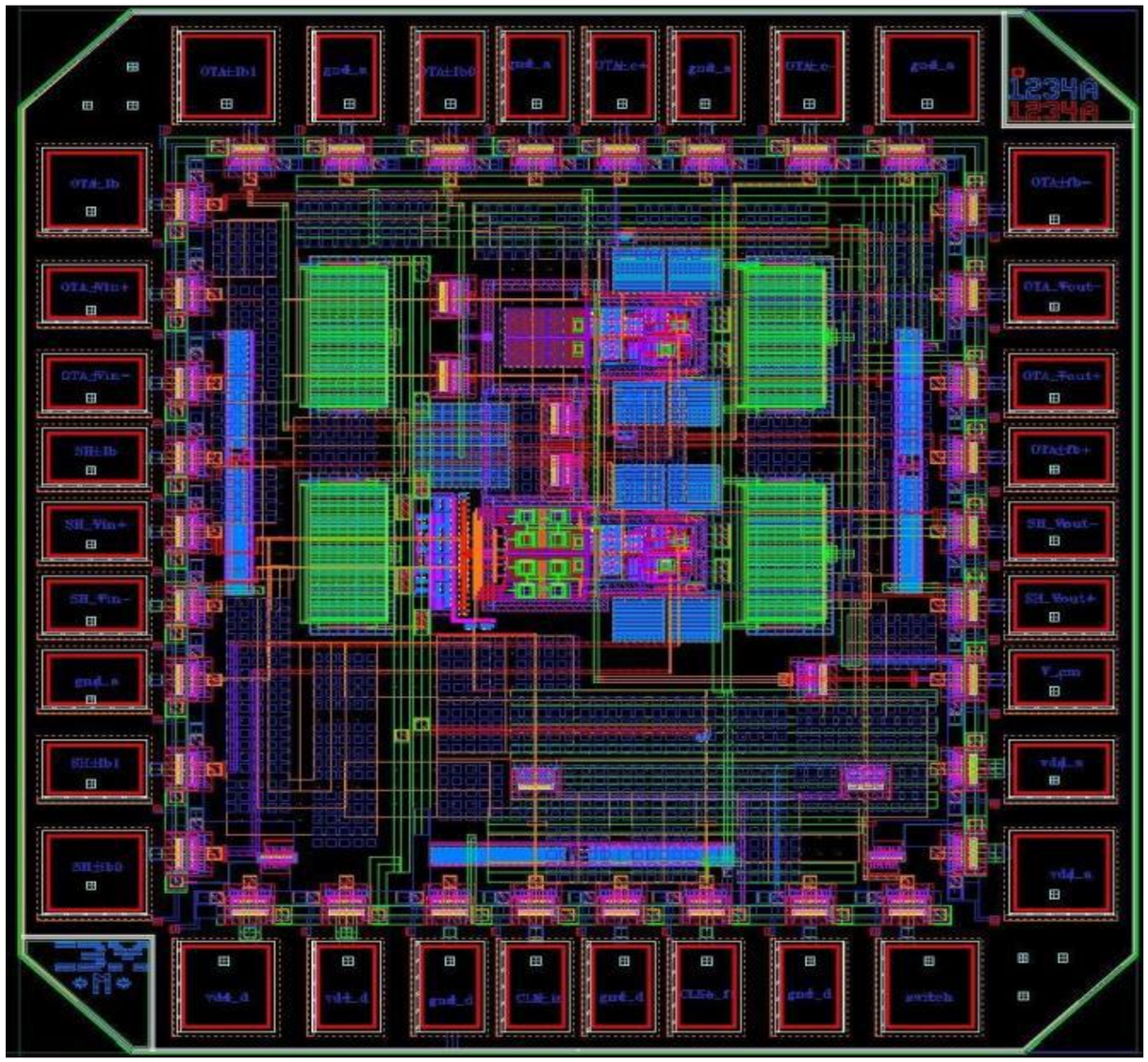
Combination of requirements on **speed**, **precision**, **low power** and particularly **radiation hardness** is not readily available commercially.

Nevis ADC development roadmap

The full ADC chip was developed following an approach of a roughly annual submissions of increasingly complete designs

Nevis09 Chip

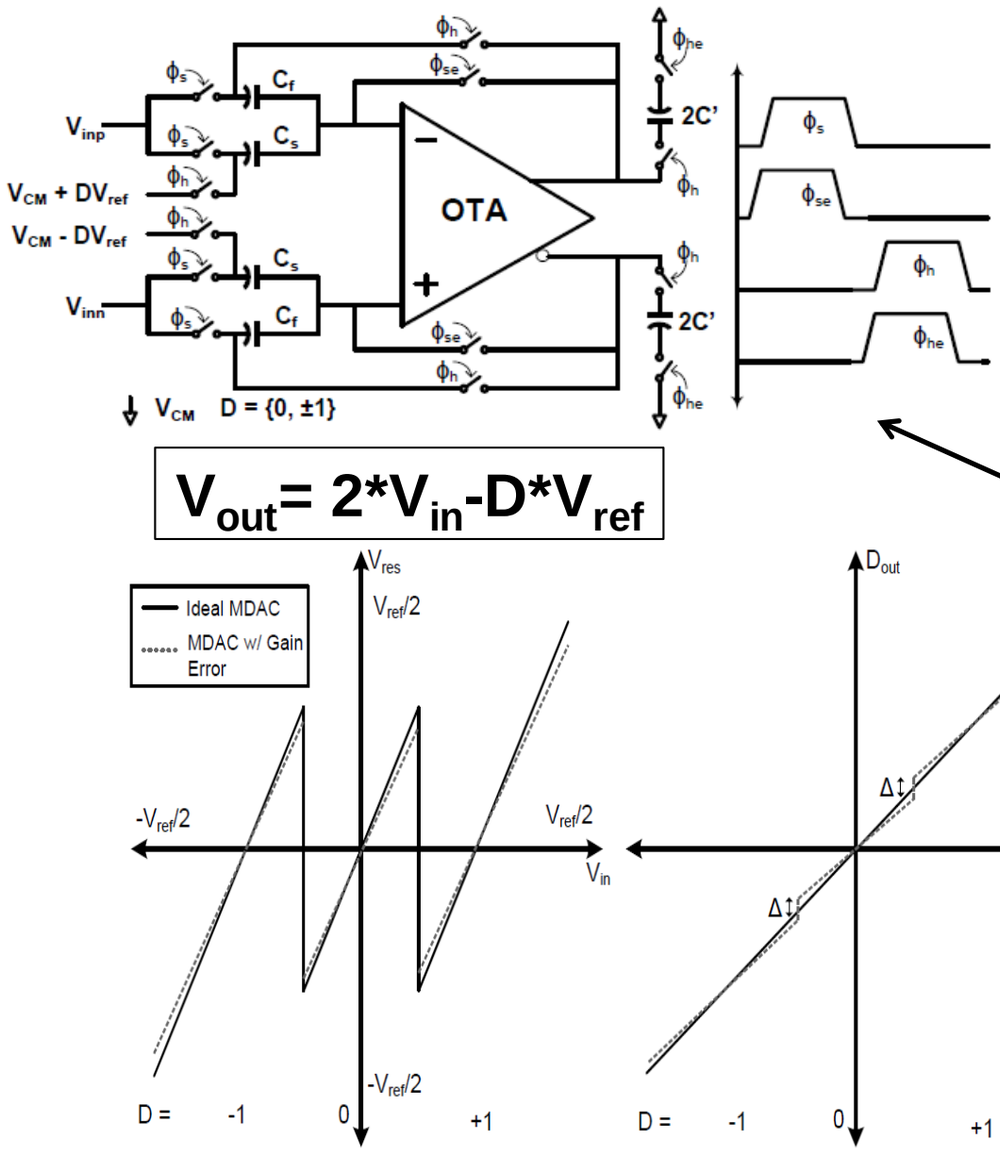
- Operational trans-conductance amplifier (OTA) circuit developed
  - DC gain of > 80 dB, UGB of >450MHz, power ~8mW, VDD=2.5V
- S/H circuit developed
- Confirmed understanding of the technology (IBM CMOS 8RF 130nm)



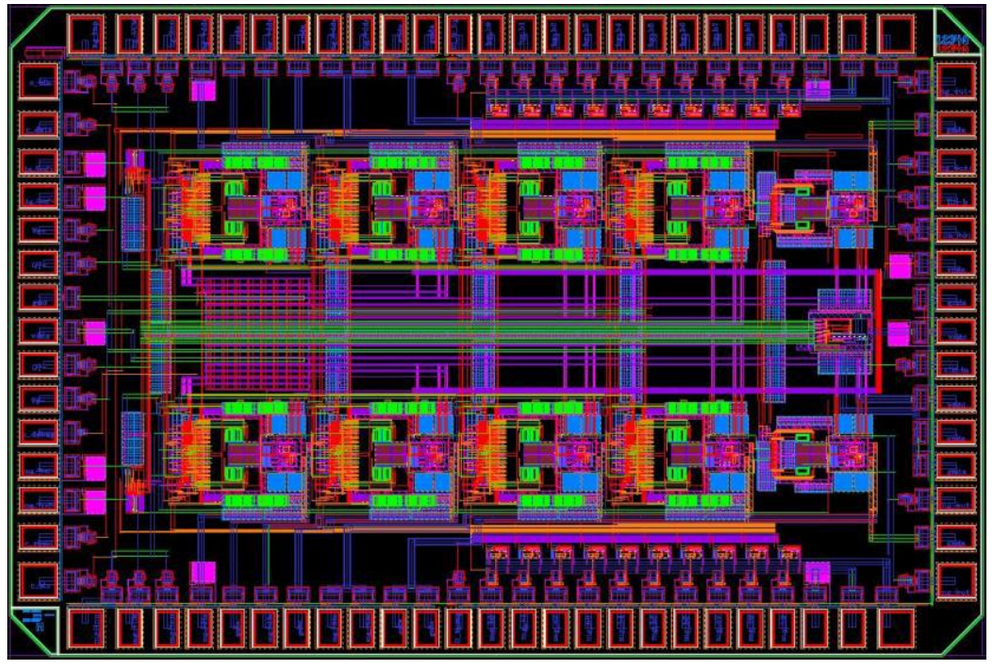
Nevis ADC development roadmap

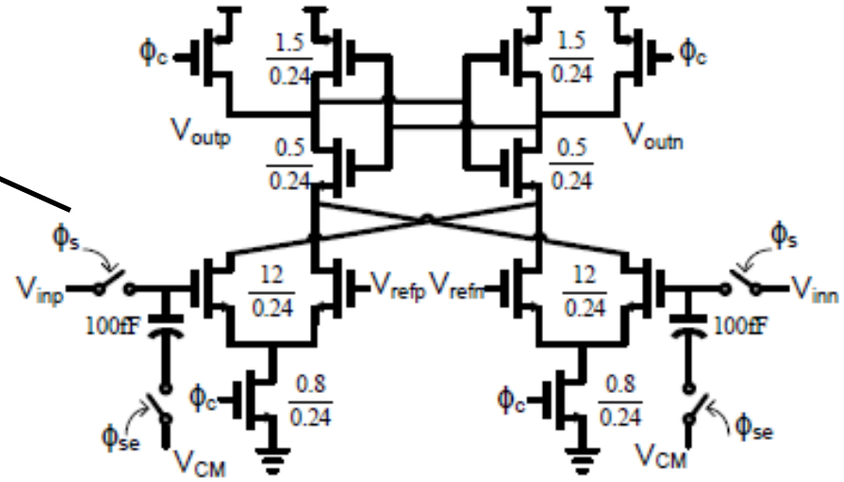
Nevis10 chip

- '1.5-bit' MDAC circuit with 12-bit performance developed



Input-output transfer function



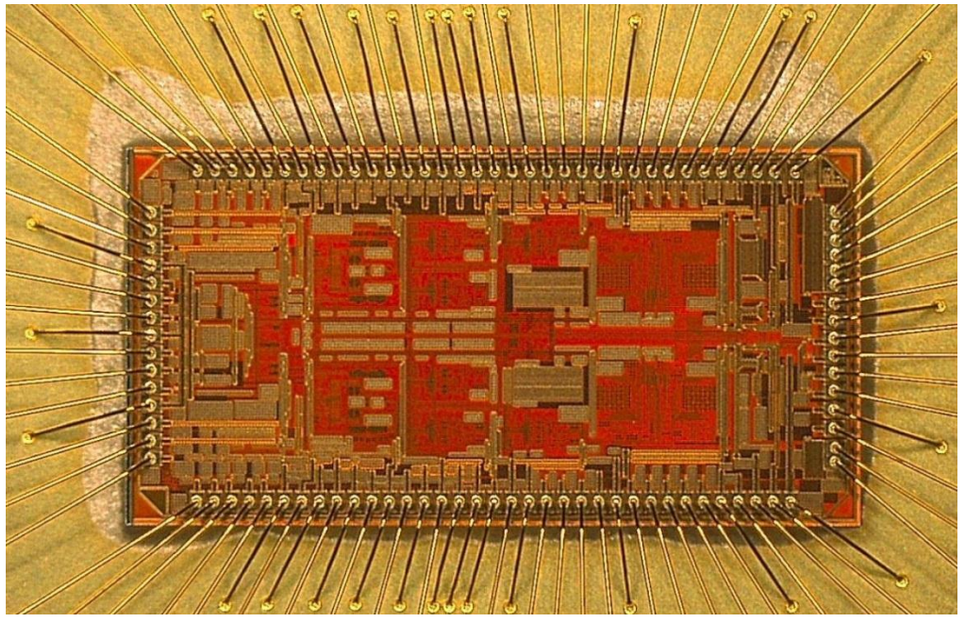


subADC

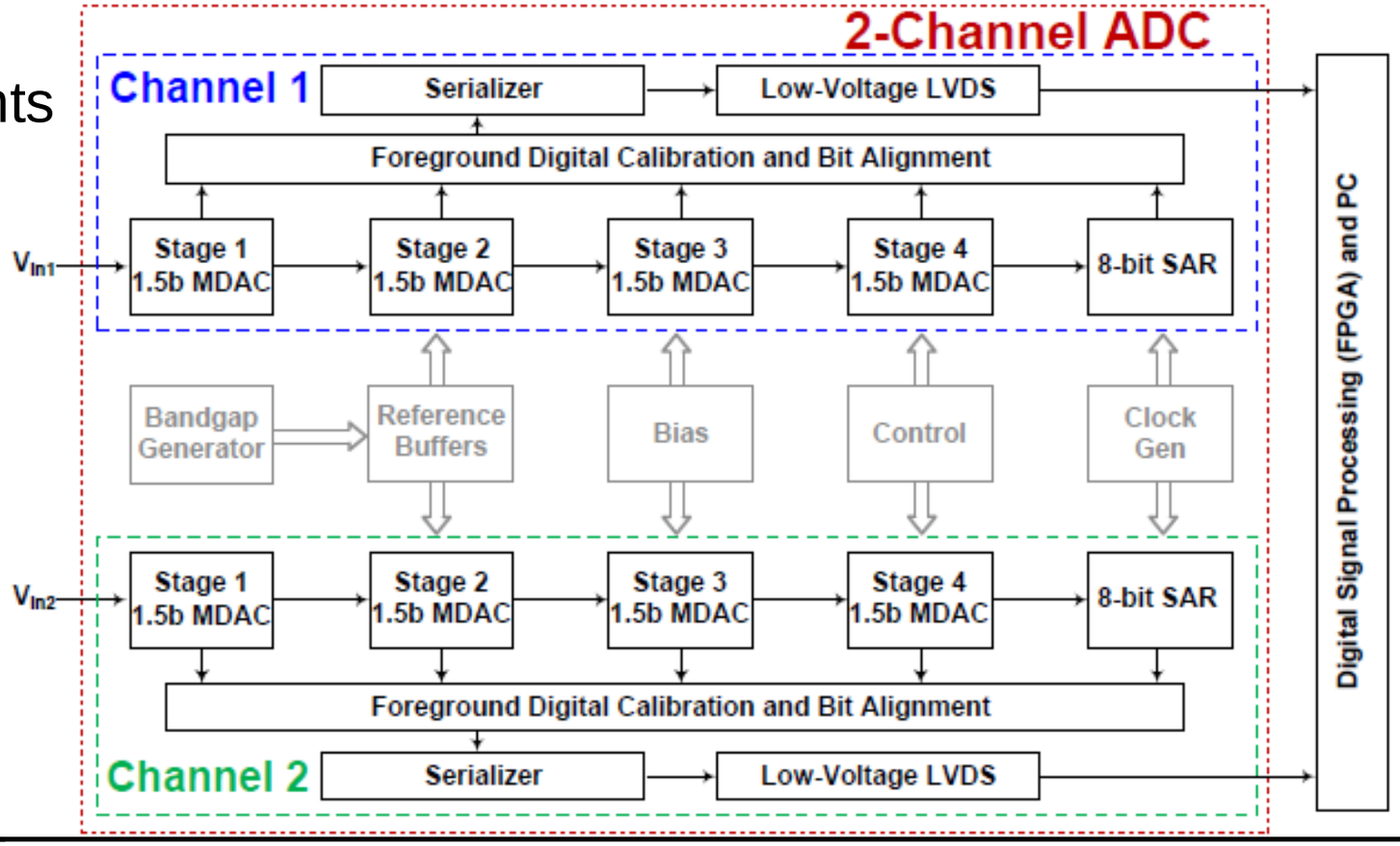
Some redundancy is included to eliminate the effect of subADC nonlinearity and interstage offset on overall linearity

Nevis ADC development roadmap

Nevis12 Chip: a big step toward the final design



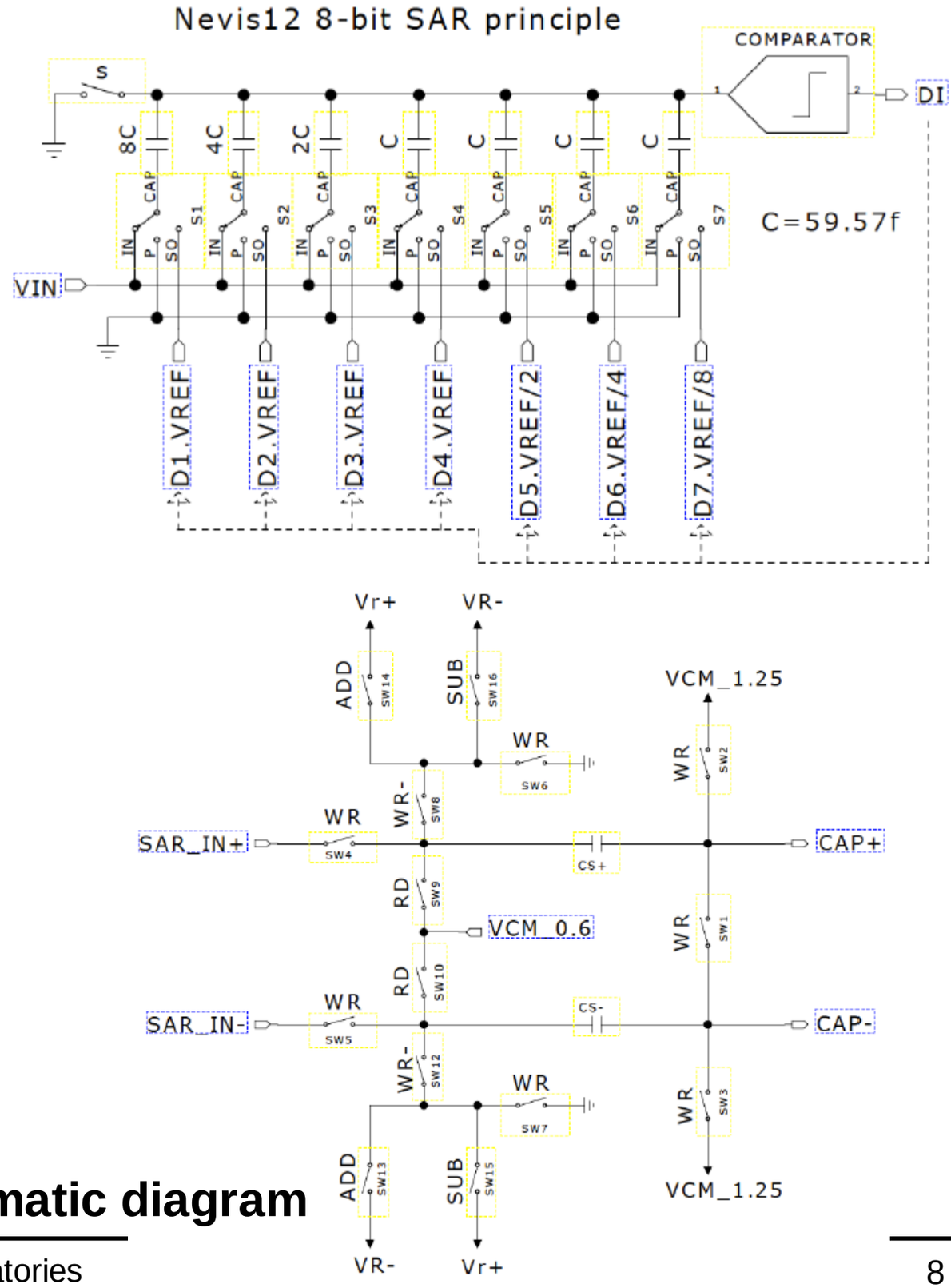
- 2 channels of 12 bit ADC, four 1.5b MDACs followed by 8 bit SAR unit
- Two clock system (640MHz and 40MHz, with no PLL on the chip)
- Output data serializer unit
- Digital data processing unit
  - Triple redundant calibration constants stored/used on chip
  - Digital correction on the chip
- 8 bit synchronous SAR unit
- Synchronous operation at 640 MHz



Nevis ADC development roadmap

Nevis12 Chip: a big step toward the final design

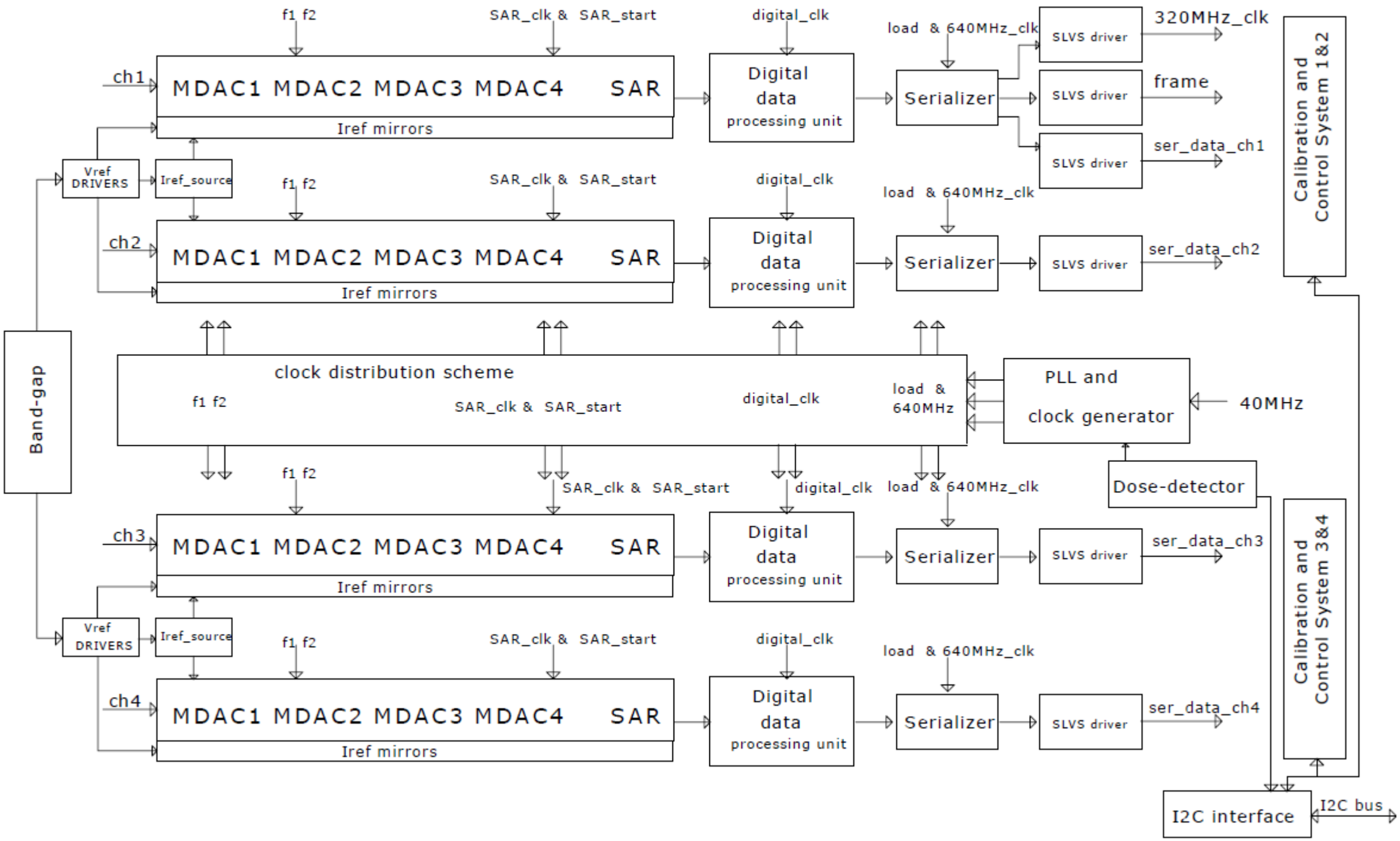
- **SAR Unit**
  - 8-bit synchronous SAR unit
  - Synchronous operation at 640 MHz
  - Very conservative approach
  - Total sampling capacitance of 1.072 pF
  - Power~3.8 mW
  - Control part: CERN digital library components



SAR switch schematic diagram

Nevis13 ADC—full function chip

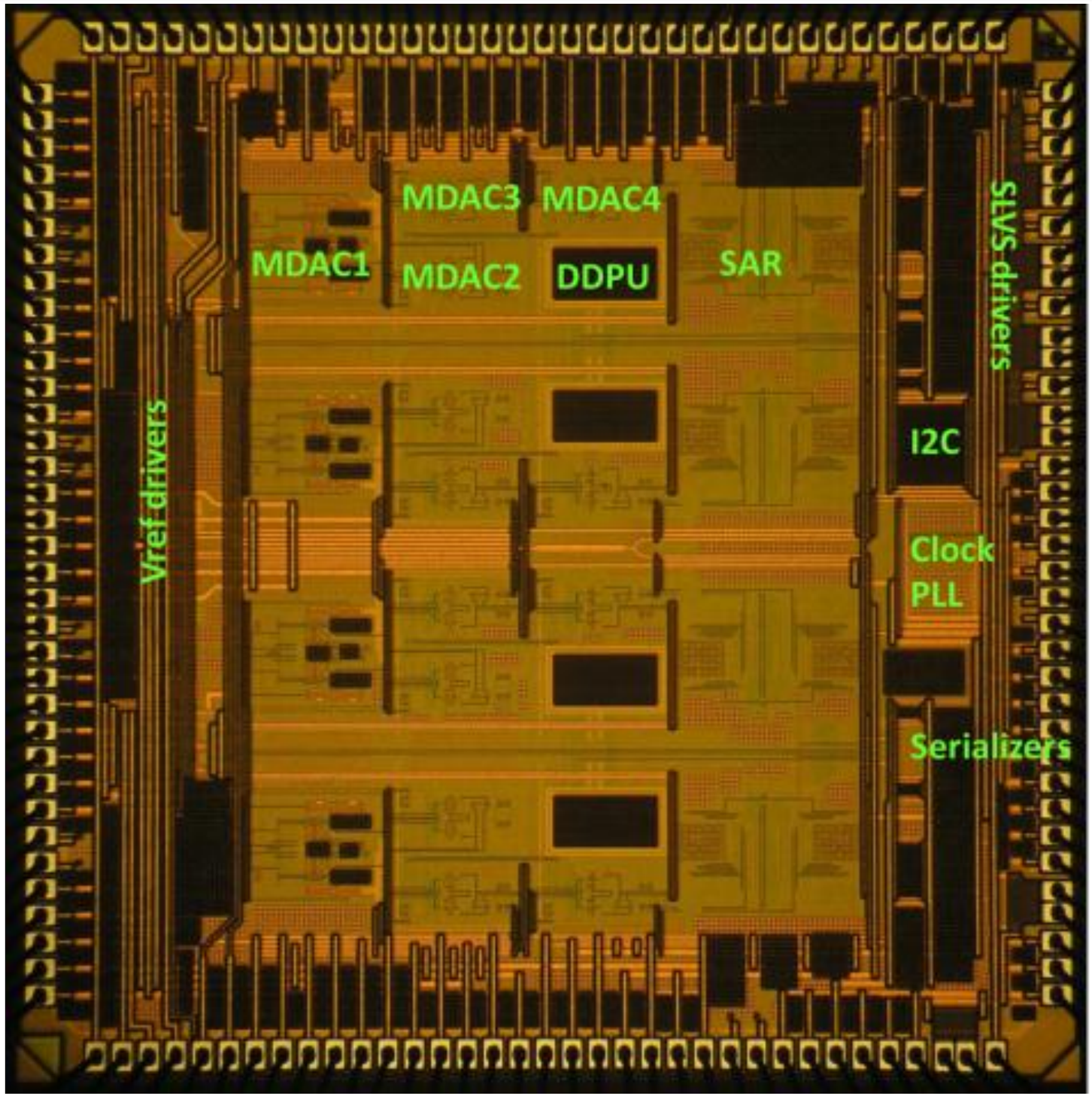
Nevis13 chip block diagram



Nevis13 ADC design

Chip layout

- 3.6 mm x 3.6 mm
- 120 die pins
- 48 GND down-bonds
- 72 pin QFN package

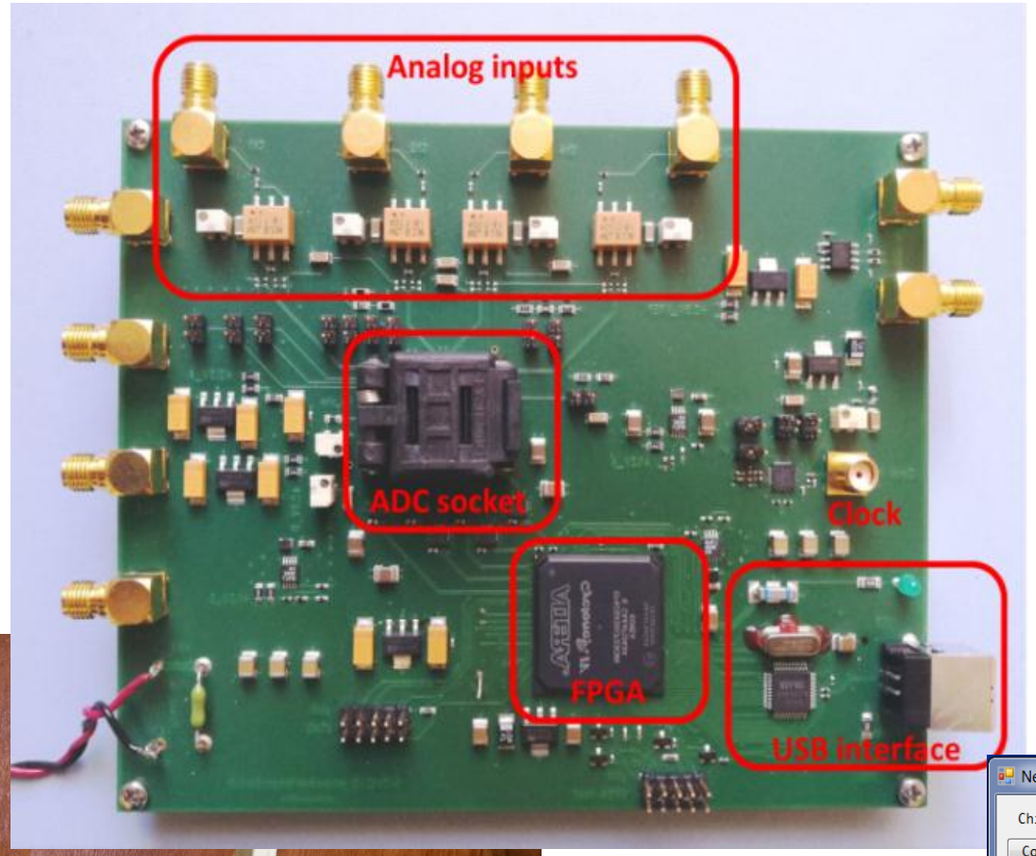


Nevis13 ADC design

Nevis 13 chip features

- 4 channels of 12bit ADC (4 MDACs and 8-bit SAR) 120 die pins
- Sampling information derived from the rising edge of differential input SLVS 40MHz clock
- Fast clock generated internally by PLL
- Differential signal input of 2.4V full scale with 1.25V common mode voltage
- Reference voltages available on the I/O pins
- Band-gap circuit designed at CERN
- Power supply voltages: 1.2V and 2.5V
- Conversion result available 87.5ns(+25 ns for serialized output) after sampling
- Data sent out serially using 320MHz DDR SLVS clock signaling
- Special frame signal marks MSB of shifted data
- Calibration constants computed outside and applied inside the chip
- I2C interface (1.2V signaling) allows to control all internal functions of the chip
- Power dissipation of ~43mW/channel (preliminary measurement on few chips)

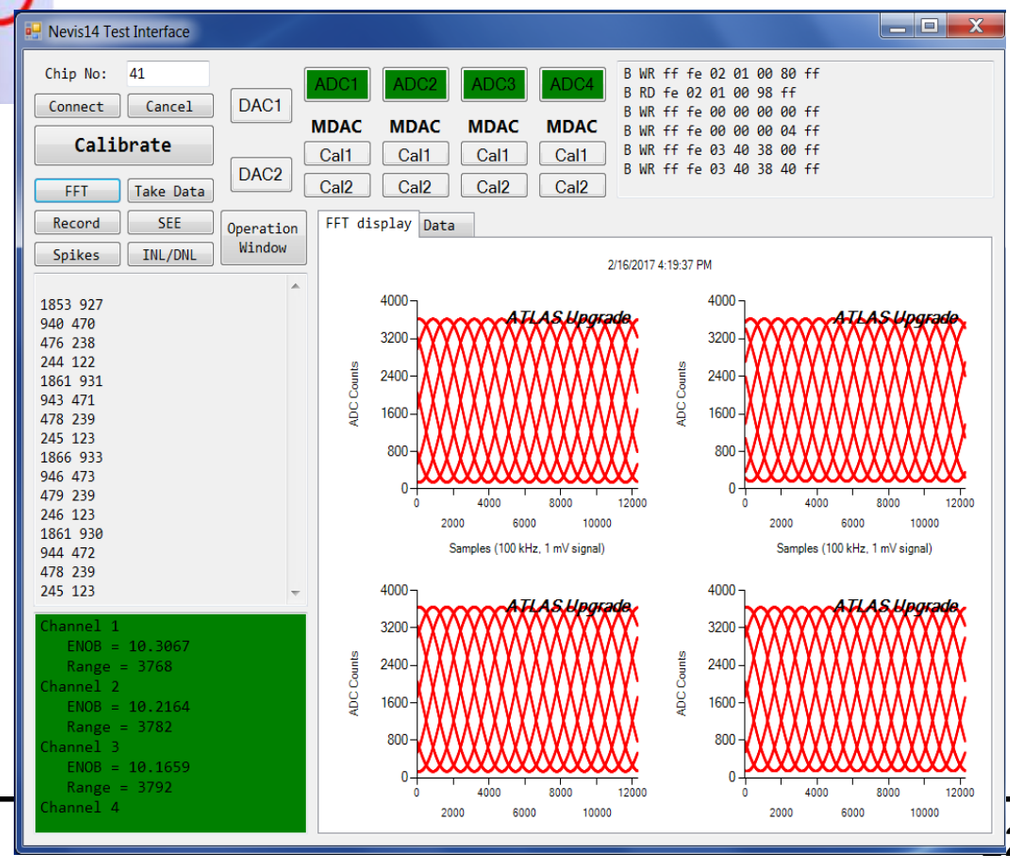
Nevis ADC test suite



ADC test socket board

ADC test setup

ADC test GUI program



Nevis ADC performance

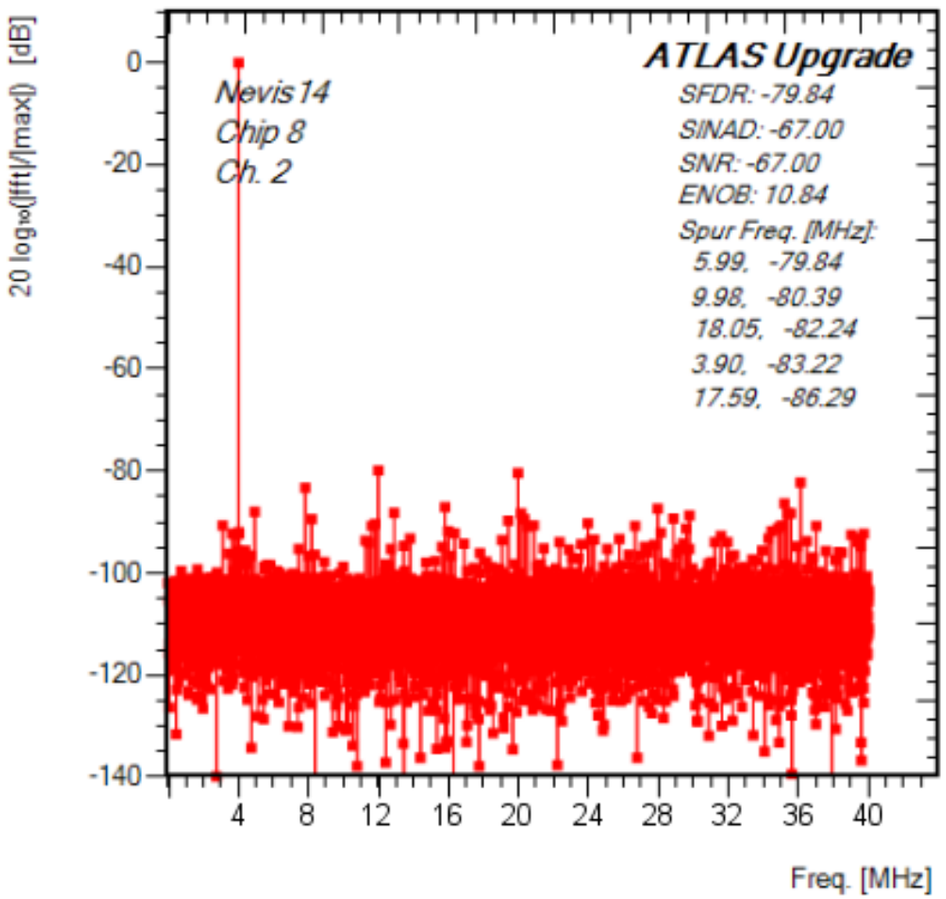
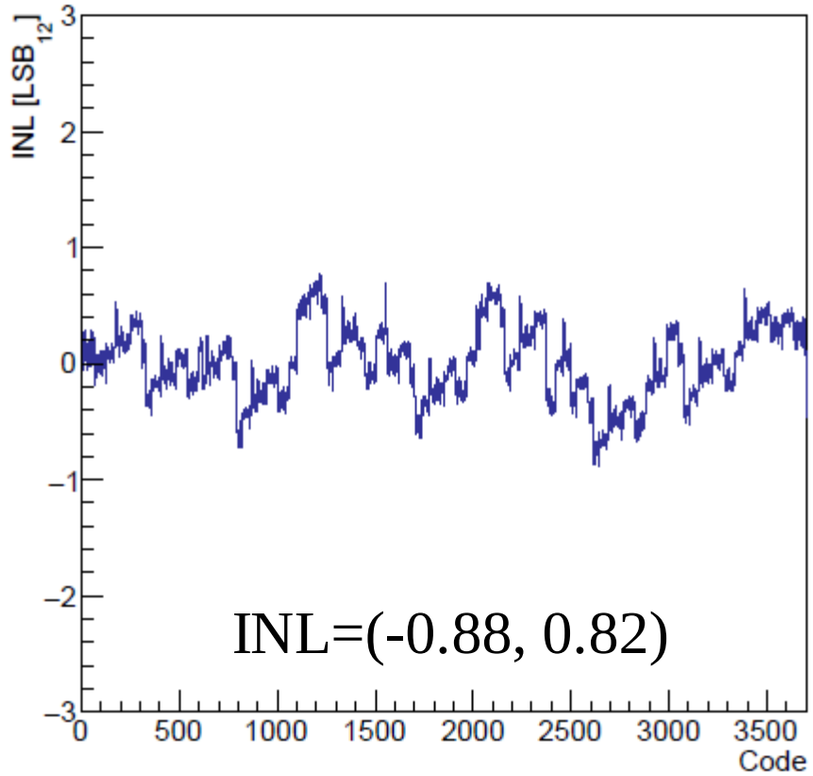
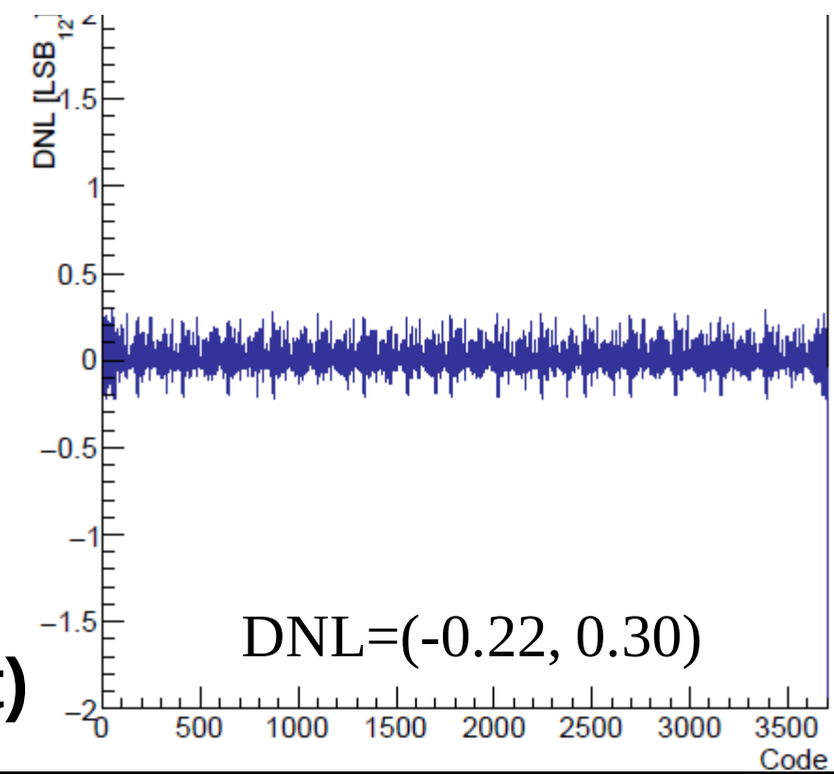


Fig. FFT with F_{in} =5.06 MHz sineware, F_s = 40 Msps





- **ENOB: 11 at 40 Msps**
- **INL: +0.82/-0.88**
- **DNL: +0.30/-0.22**
- **Power consumption: ~45 mW/ch**
- **Latency: 112.5 ns(signal in to last bit out)**

Nevis ADC radiation test

Fig. Long radiation tester board

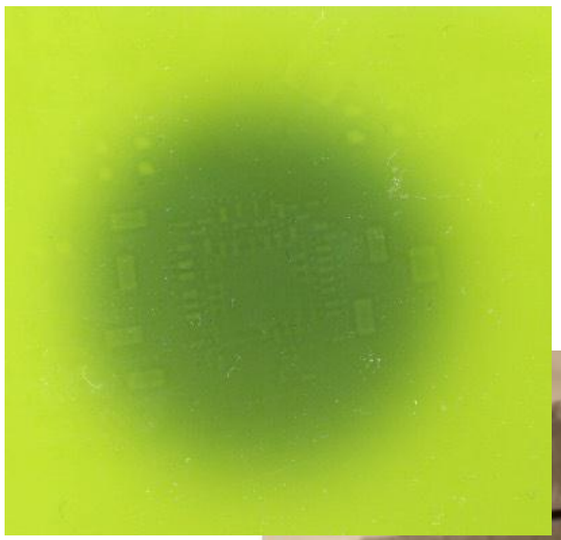


Fig. MGH proton therapy center 227 MeV proton beam

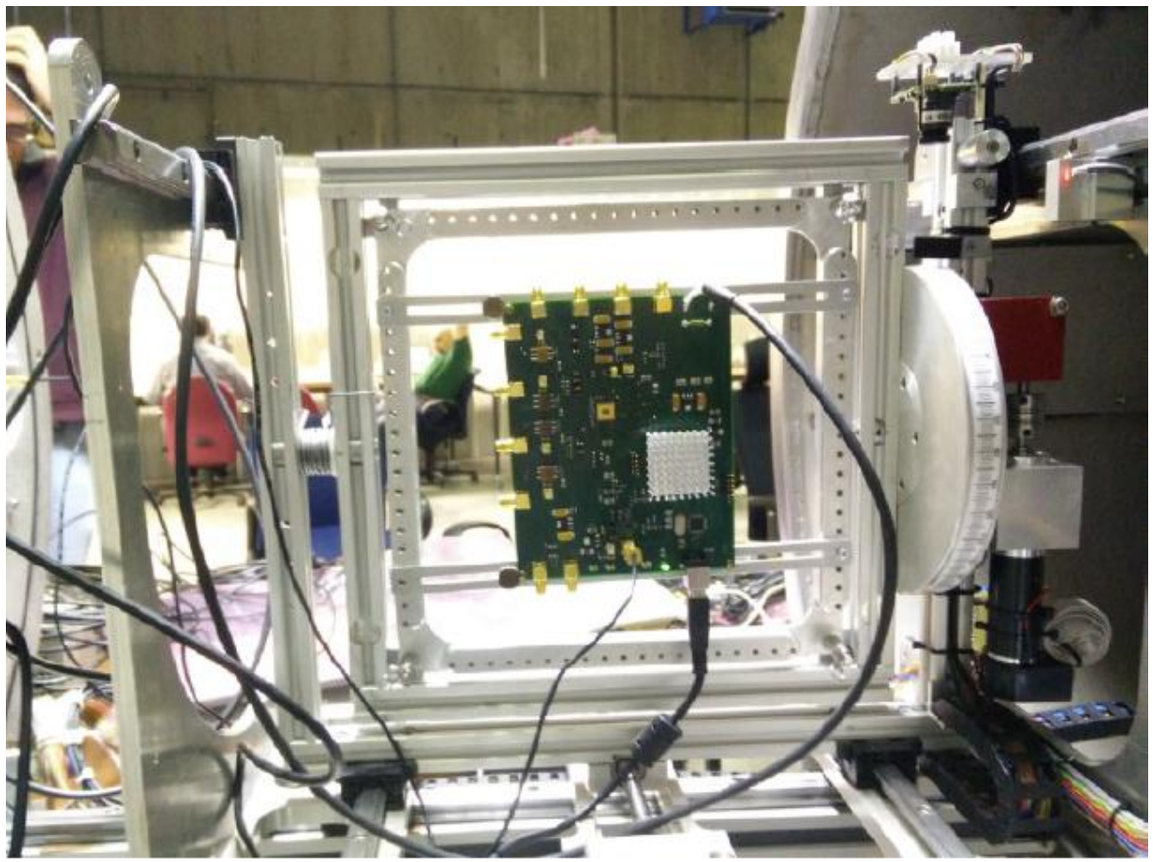


Fig. UC Louvain's cyclotron using heavy ions with open lid package

Nevis ADC radiation test--TID tolerance

- **Current**

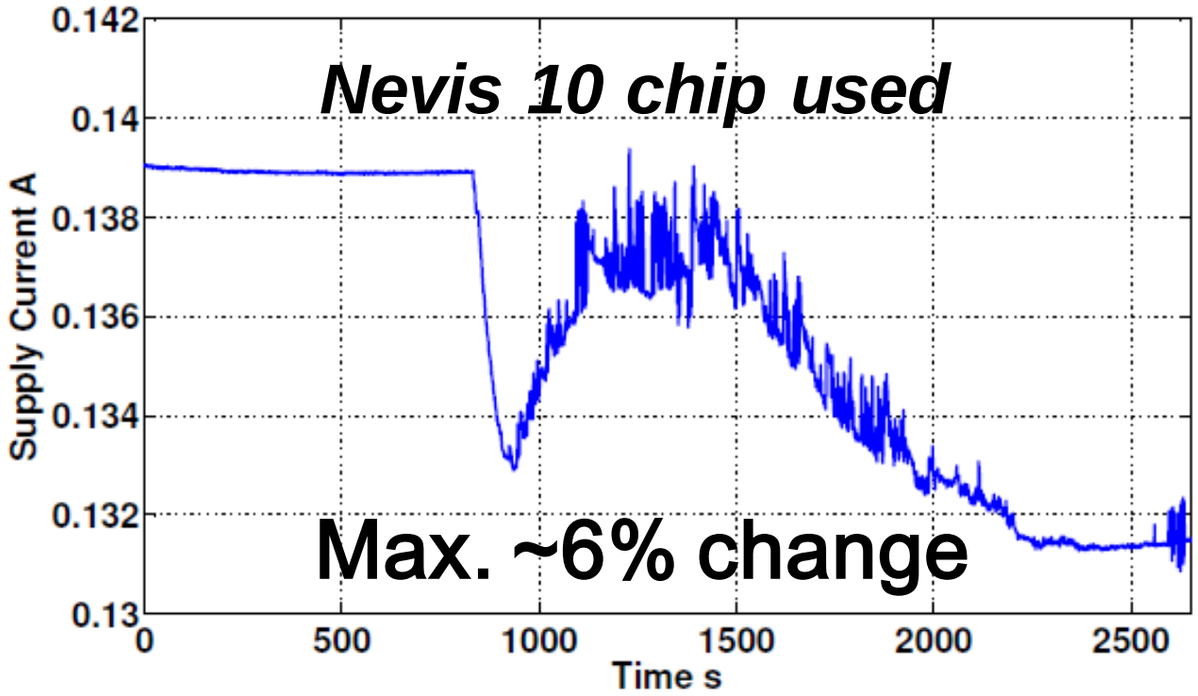


Fig. Current consumption change during irradiation. (2500 s horizontal scale corresponds to a dose of 5 Mrad)

- **Performance**

Nevis 12 chip

Chip Number	Dose [MRad]	SNDR [dBc] Pre/Post-Irradiation	SFDR [dBc] Pre/Post-Irradiation	ENOB Pre/Post-Irradiation
1	2	62.43/61.05	67.27/70.06	10.08/9.85
2	1	63.54/62.36	70.92/72.98	10.26/10.10

Table: Measurements of ADC performance before and immediately after irradiation in a 227 MeV proton beam at f_{in}=10 MHz

Nevis ADC radiation test--SEE cross-section

- Chip is powered with clock input but no input signal is applied
- Monitor ADC output data and register a **SEE**(Single-Event Effects) **event** when the data is off the baseline much bigger than noise level
- A SEFI(single-event functional interrupt) is detected when a constant ADC output is observed

SEE cross-sections:

- Chip is irradiated with a fluence rate of ~20-80 x 10^8 protons/cm^2/s
- No latch-up events(requiring power-cycling for restoring normal operation) were observed
- Cross-section for SEFI+ digital SEU(Single Event Upset) measured to be <10^{-12} cm^2/ch

Nevis 12 chip, 227 MeV proton

Chip Number	Rate [10^8 protons/cm^2/s]	Dose [kRad]	SEFI	SEU (Analog)	SEU (Digital)	SEE	Cross-section (w/ analog errors) [10^{-12} cm^2]
3	19.0	101	0	8	1	9	0.6 (5.7 ± 1.9)
3	76.0	283	0	41	2	43	0.6 (9.8 ± 1.5)
4	18.6	203	1	10	0	11	0.3 (3.5 ± 1.1)

Nevis 15 chip, 582 MeV, $^{58}Ni^{18+}$ beam

$^{58}Ni^{18+}$	SEU (Analog)	SEU (Digital)	SEFI	SEE	Cross-section (w/ analog errors) [cm^2]
Channel 1	59	3	1	63	6.76×10^{-7} (1.40×10^{-5})
Channel 2	75	4	1	80	9.01×10^{-7} (1.78×10^{-5})
Channel 3	32	2	1	35	4.50×10^{-7} (7.66×10^{-6})
Channel 4	61	1	1	63	2.25×10^{-7} (1.40×10^{-5})

Table: SEE+SEFI cross-section measurement

LArTDS

- **LArTDS ASIC**

  Multiplexes 16 channels of ADC data, then scrambles and serializes the data for transmission over two optical links each with a data transfer rate of 4.8 Gbps

- Based on MUX chip developed for Nevis ADC data multiplexing (key logic parts are triple redundant design) and high speed serializer developed by CERN(GBT) and U. Michigan(TDS)

- Backup for LOCx2

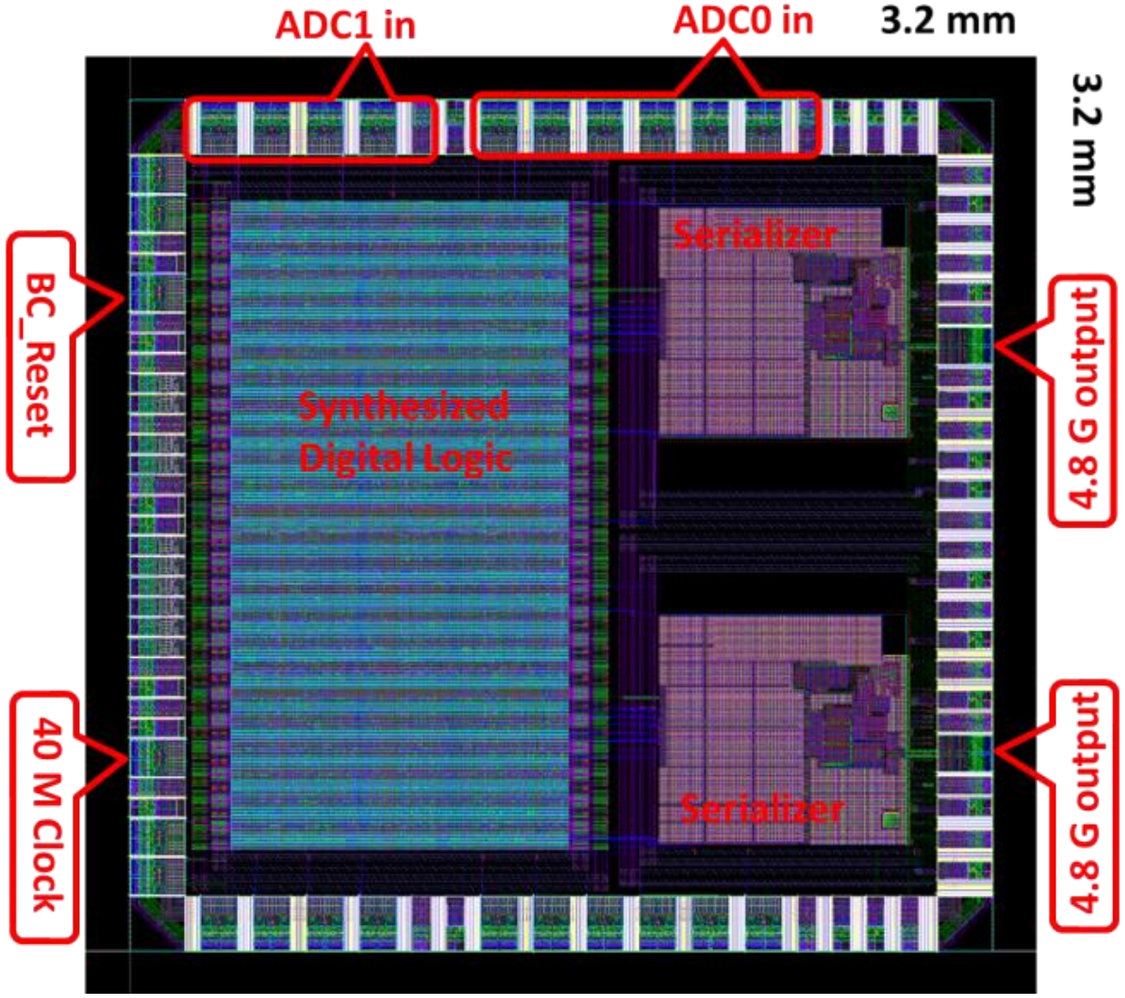


Fig. Chip layout

Fig. 120-bit package data format

header 1100	4 bit BC Flag	4 bit BCID ADC12	ADC 12 data 48 bits	4 bit BCID ADC34	ADC 34 data 48 bits	8 bit parity

LArTDS Test System

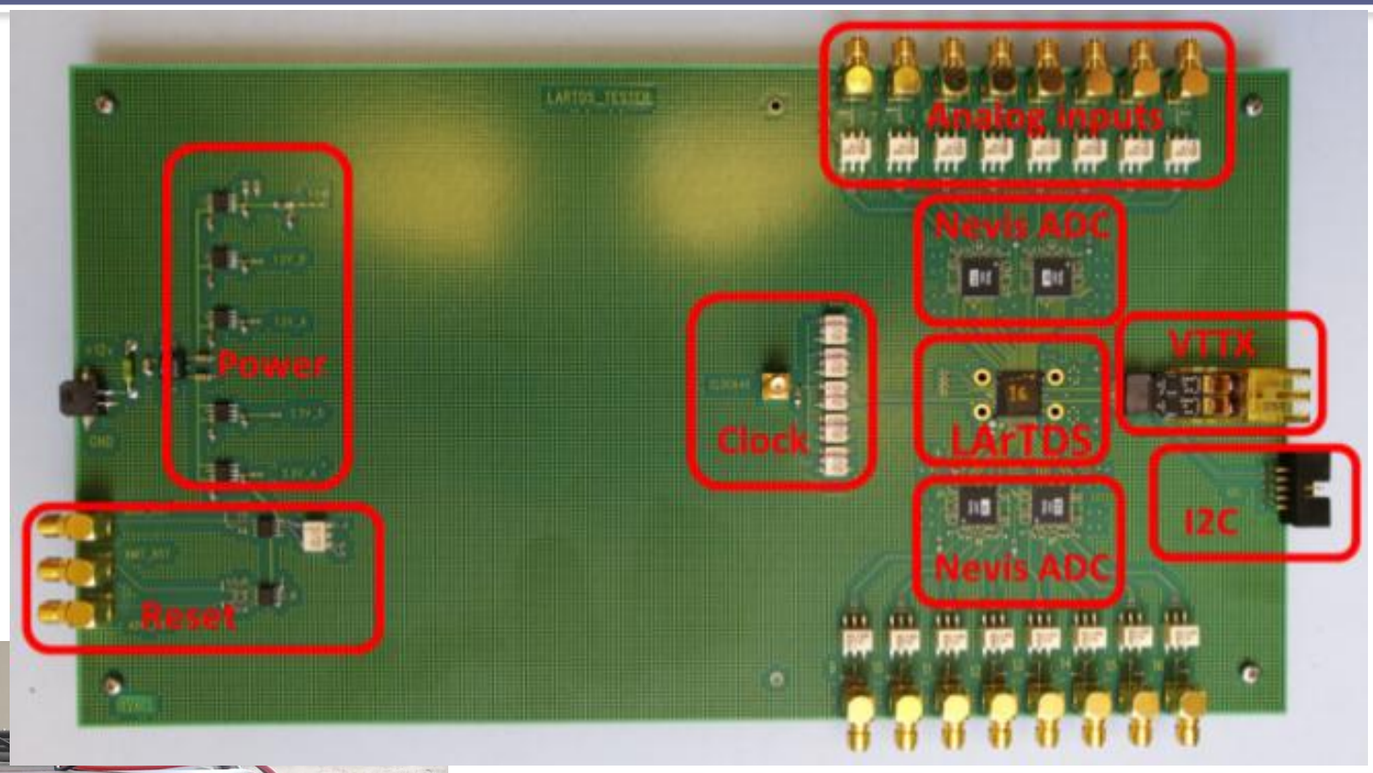


Fig. Tester board

Fig. Test setup

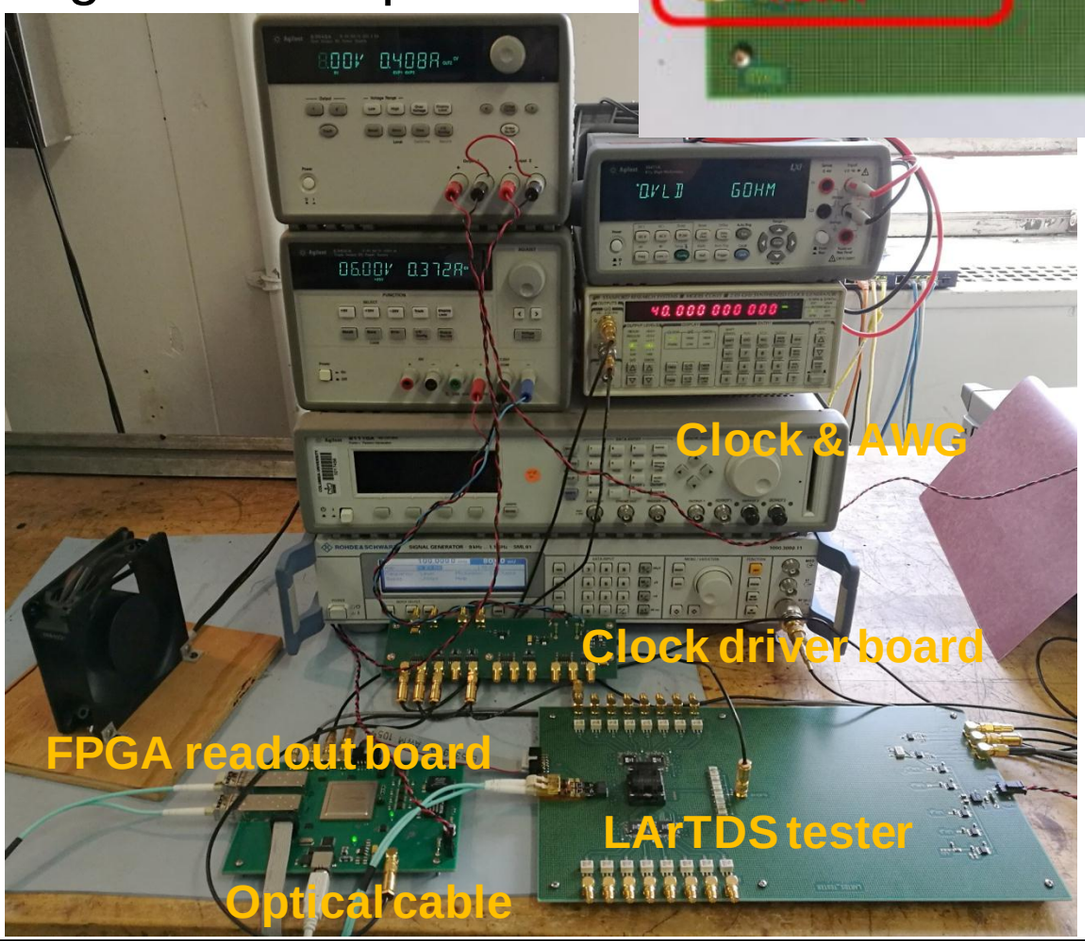


Fig. GUI program

Test Dataflow

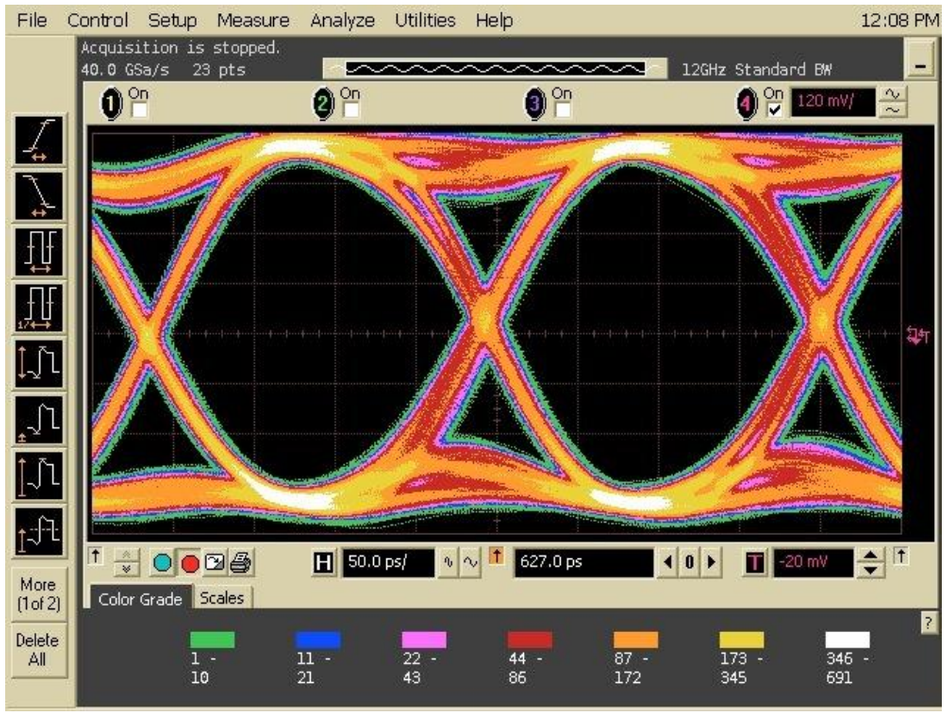


Fig. 4.8 Gbps serializer Eye diagram

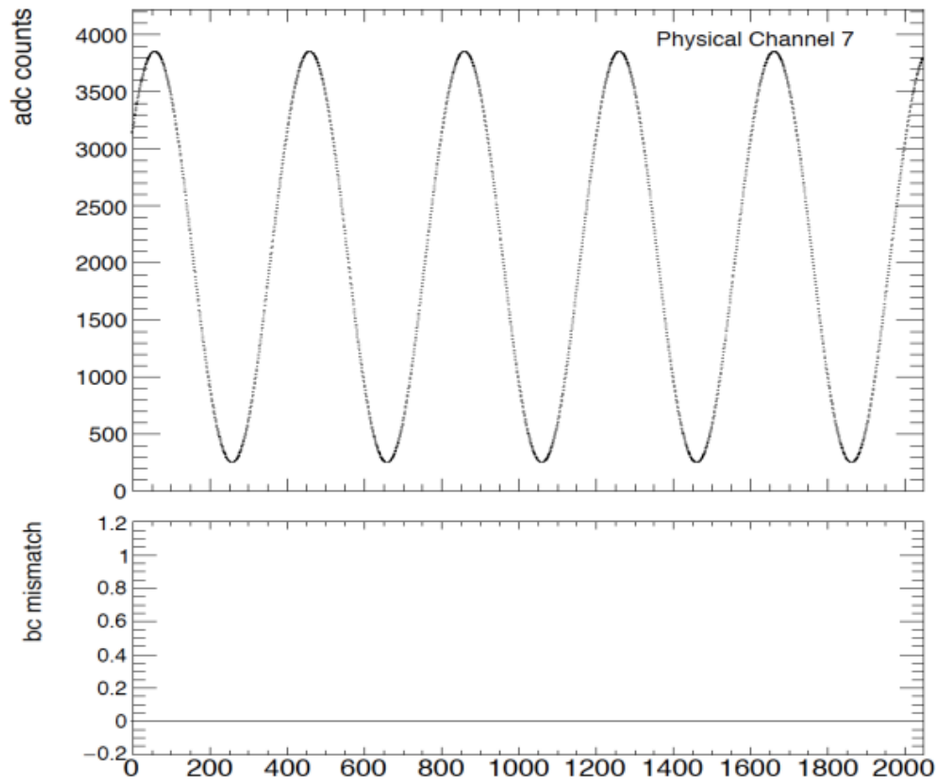


Fig. recovered sinewave data

- ❑ Nice eye diagram at 4.8 Gbps bit rate ✓
- ❑ Switch off scrambler and send all a's ✓
- ❑ Scrambler on, have all ADCs send test pattern data ✓
- ❑ Send sinewave into ADC, check output ✓
- ❑ Check phase between clock and data header ✓

Test Dataflow

- Bit error rate test
  - Set ADC in test pattern mode (const. output of 0xEF0)
  - LArTDS scrambles using PRBS
  - Descramble in FPGA, check for errors
    - Data pattern matched ✓
    - Parity bits matched ✓
    - BCID bits matched ✓

A 48 hours long term stability test shows the bit error rate is **below 1.2×10^{-15}** for both high speed serial channels

Summary

- **Nevis ADC: A mature design for phase-1 readout electronics upgrade**
  - Achieves an ENOB of 11 at 40 MS/s sampling rate
  - 112.5 ns latency(signal in to last serial bit out)
  - 45 mW/channel power consumption
  - No performance degradation after irradiation
- **LArTDS:**
  - Full functionality tested, works as designed
  - Bit error rate is below 1.2×10^{-15}
  - Radiation tolerance to be evaluated very soon