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# Capacitively Coupled Pixel Detectors: From design simulations to test beam

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An overview on the characterisation of aH35 HV-CMOS active pixel sensors for the ATLAS ITk. Capacitively Coupled Pixel Detectors (CCPDs) are only possible due to HV-CMOS sensors, where the high voltage (necessary to deplete the sensor) can be applied on CMOS circuits, allowing the sensor to be capacitively coupled to a read out ASIC, avoiding the expensive bump-bonds. An extensive work is done in the characterisation of this new sensor technology. TCAD simulations of the HV-CMOS pixel designs and TCT measurements on real devices is shown. In addition, automatised wafer probing measurements and the flip-chip, of the sensors with the readout chips, will be presented, and the FPGA-based read out system developed is introduced. Laboratory measurements, such as DAC scans and test-pulse calibration, will be shown. To conclude, test beam measurements done at CERN SPS and at Fermilab, using the UniGE FE-I4 Telescope, with non-irradiated and irradiated samples of the AMS-H18 CCPDv4 and H35 full-size demonstrator, will be shown and discussed.

## Summary

The work presented is done at CERN and at the University of Geneva on the ATLAS ITk framework. HV-CMOS sensors are being investigated and characterised to be used in CCPDs (Capacitively Coupled Pixel Detectors). CCPDs are possible due to the possibility of the application of high voltage on the substrate of CMOS chips. This depletes the substrate of the chip, making it sensitive to particle interactions. The CMOS chip amplifies the signal generated by the particle and makes it possible to capacitively transfer the signal, through a layer of glue, to the read out ASIC. This avoids the use of bump bonds, making cheaper to build larger pixel detectors. The work presented involves TCAD simulations of the sensor chip design with TCT measurements on real devices. At the university's clean room, the sensor wafer is probed in order to use good sensors in the assembly with the FE-I4 read out ASIC. The flip-chip is done at the University of Geneva as well and pattern recognition is used to precisely align the chips together. A FPGA-based read out system was developed for the CCPD assemblies. Laboratory measurements, such as DAC scans and test pulse calibration, are performed with controlled environment. Finally, multiple test beam campaigns are done, gradually increasing the irradiation dose on the devices under test, in order to measure the performance of the chip, and results are presented from beam tests at CERN SPS (2016) and Fermilab (2017).

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