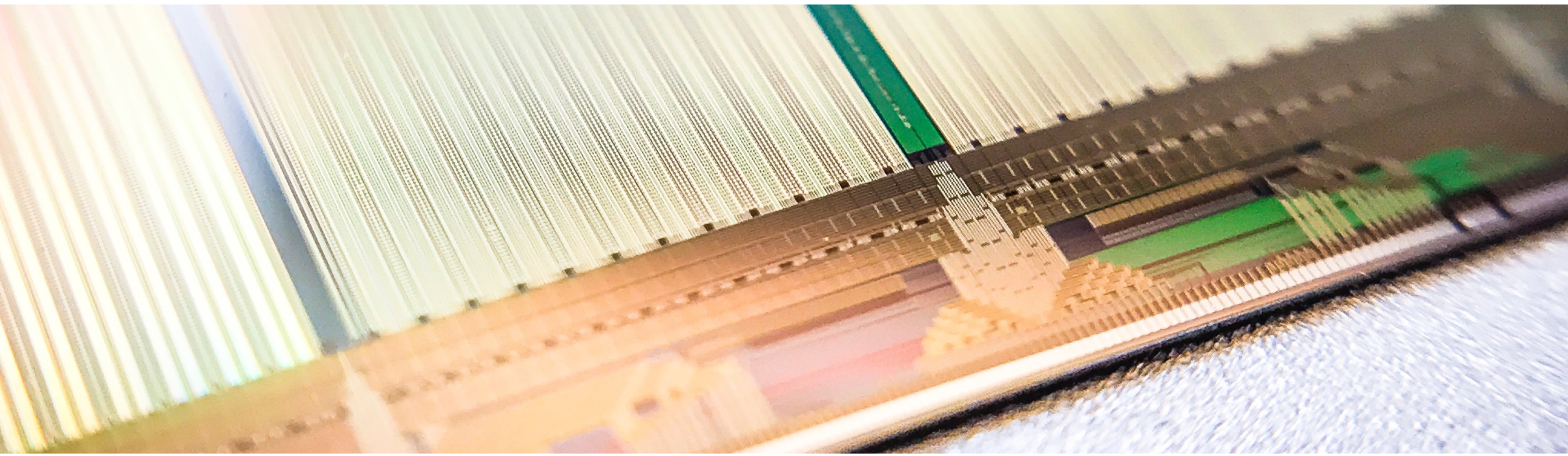
# HV-CMOS Active Pixel Sensors

## CCPDs: From design simulations to testbeam

R&D for the ITk ATLAS HL-LHC Upgrade



H35DEMO 100 µm thick

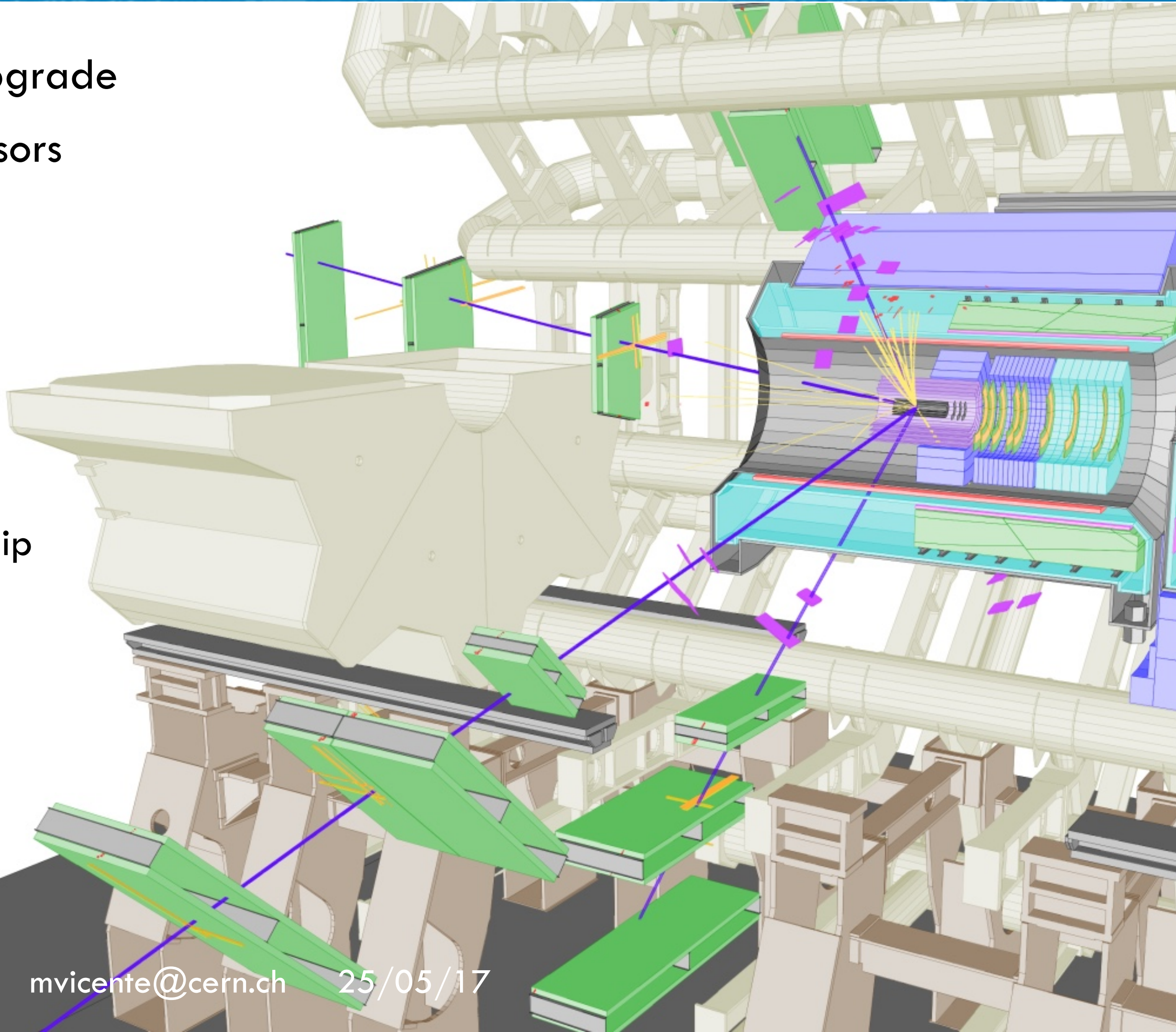
TIPP2017 – R4(5)
25/05/2017

**Mateus Vicente (UniGE/CERN)**
**on behalf of the ATLAS HV-CMOS UniGE collaboration**

# Talk outline



- The ATLAS Inner Tracker Upgrade
- HV-CMOS Active Pixel Sensors
  - HV-CMOS sensor concept
    - H35DEMO CCPD
  - TCAD simulations
  - TCT measurements
- Assembling
  - Wafer probing and flip-chip
- Caribou DAQ system
- Characterization
  - Testbeam measurements
- Summary and Conclusions

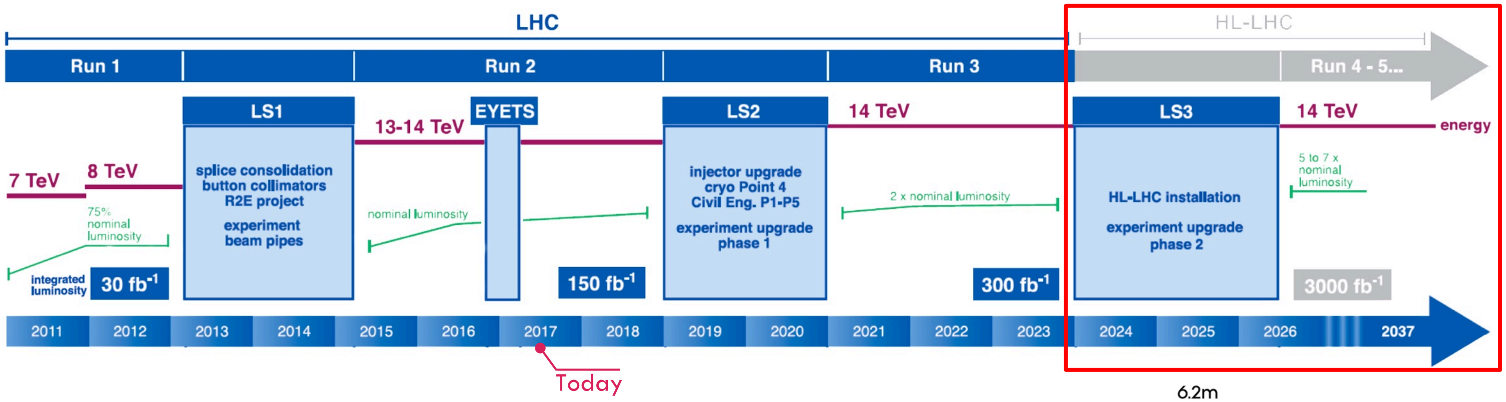


# ATLAS Inner Tracker

## All-silicon tracker upgrade



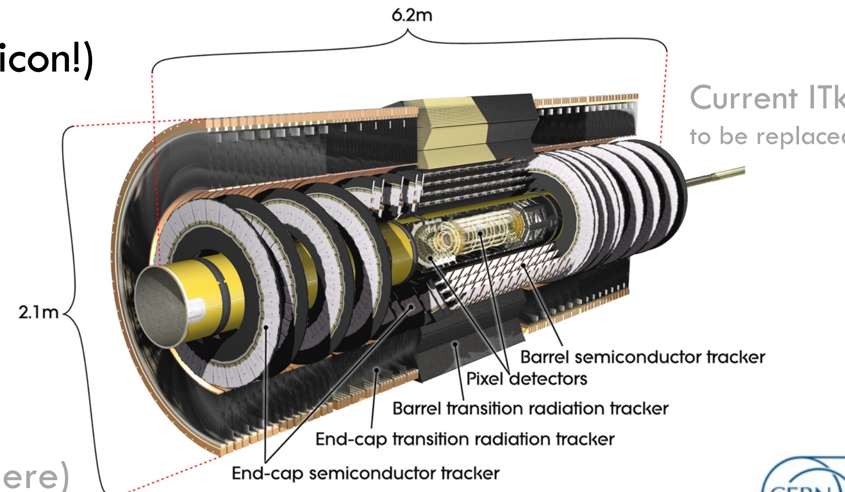
- Luminosity upgrade on LHC to improve measurements and searches




- New all-silicon inner tracking (~**200m²** of silicon!)
- Candidate for some detector layers:

New **HV-CMOS** Active Pixel Sensors

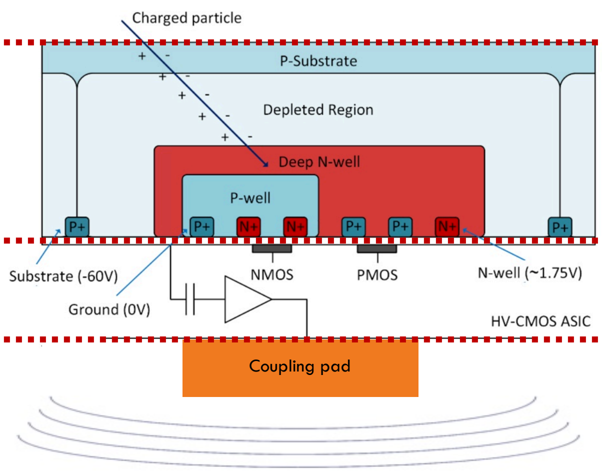
- Commercial process ➔ **Low cost**
- Capacitively Coupled Pixel Detector (**CCPD**)
  - Bump-bonds are changed by glue
- HV-CMOS Monolithic Detectors (not covered here)

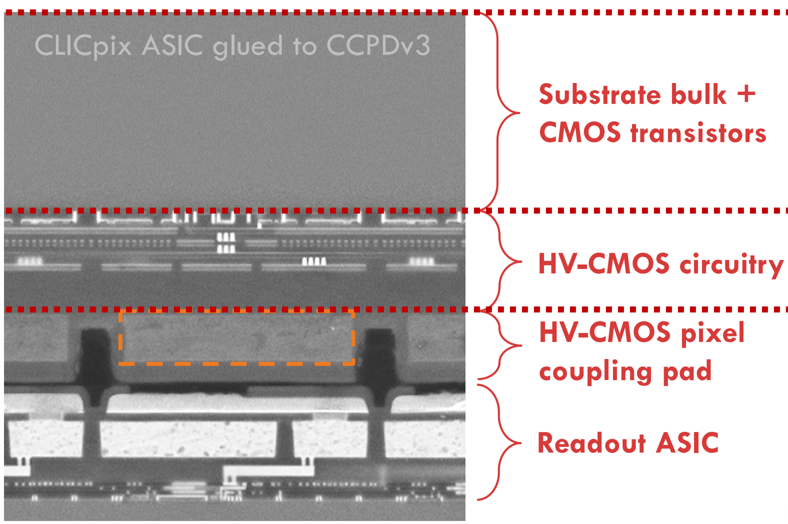


# ATLAS Inner Tracker
## HV-CMOS CCPDs



- New **HV-CMOS** technology being investigated
  - **H**igh **V**oltage can be applied on silicon sensor **bulk** (for **fast charge collection** like on planar sensors) where the the transistors of a readout **CMOS circuitry** is also implanted
    - **CMOS** transistors **shielded from bulk HV** by **Deep N-well implant** (sensor **collecting diode**)
    - The **signal** generated by a particle in the sensor bulk is already **processed in the sensor**
      - **Amplification** of the signal to cope with a **capacitive coupling** between sensor and readout chip



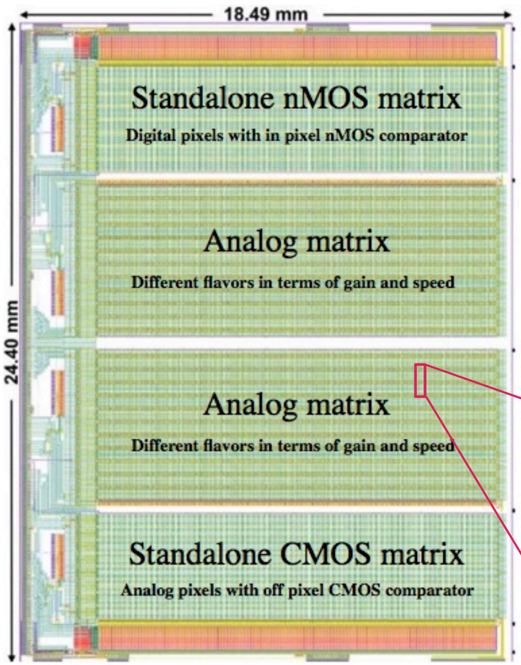
# HV-CMOS H35DEMO Pixel Sensor

## General description

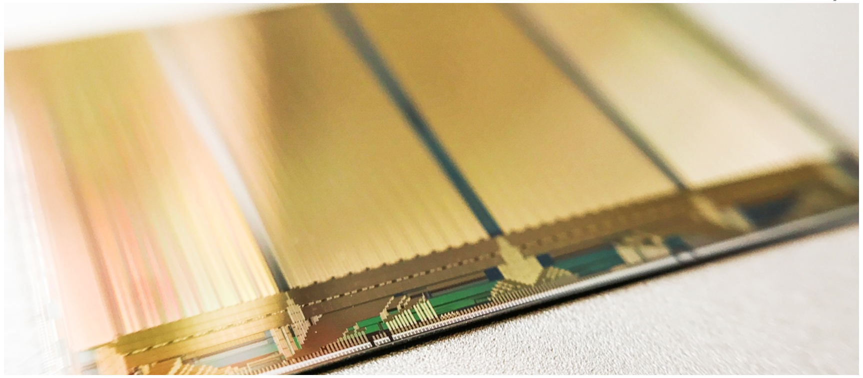


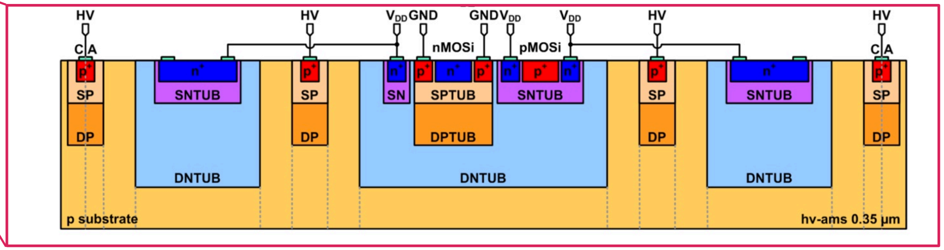
- Demonstrator Pixel Sensor chip implemented in a **350 nm HV-CMOS** process
  - Pixel pitch of **50x250 µm** (matching FE-I4 readout chip foot print)
  - **Different** pixels and **readout types** with differences in the **electronic circuits**
    - All pixels flavors has the **same implants structure**

Design: R. Casanova (IFAE), I. Peric (KIT) and E.Vilella (Uni. Liverpool)




H35DEMO chip





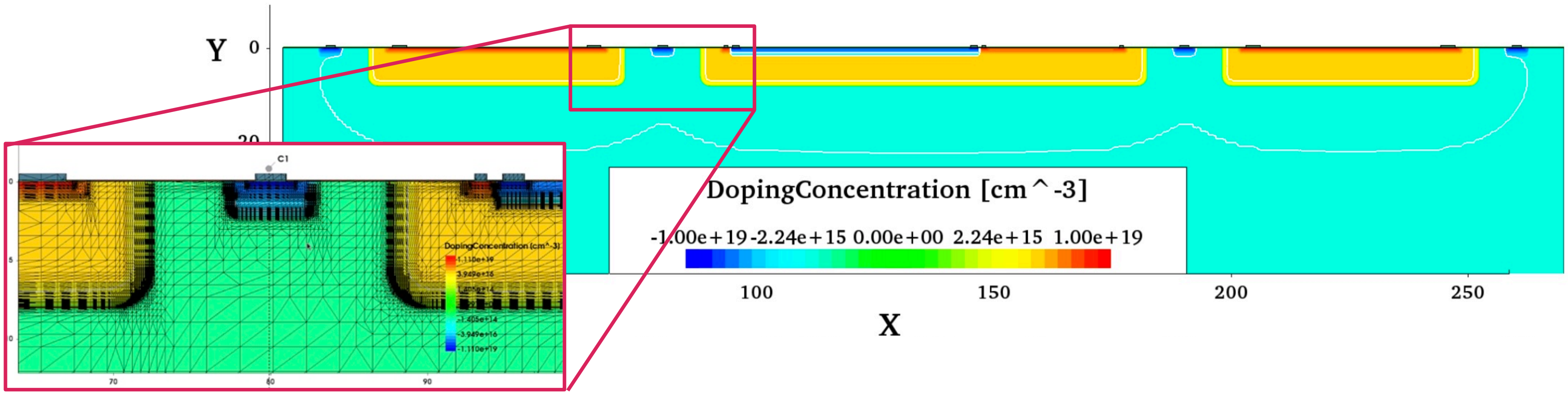

Pixel cross section schematic

# HV-CMOS H35DEMO Pixel Sensor

## TCAD simulations



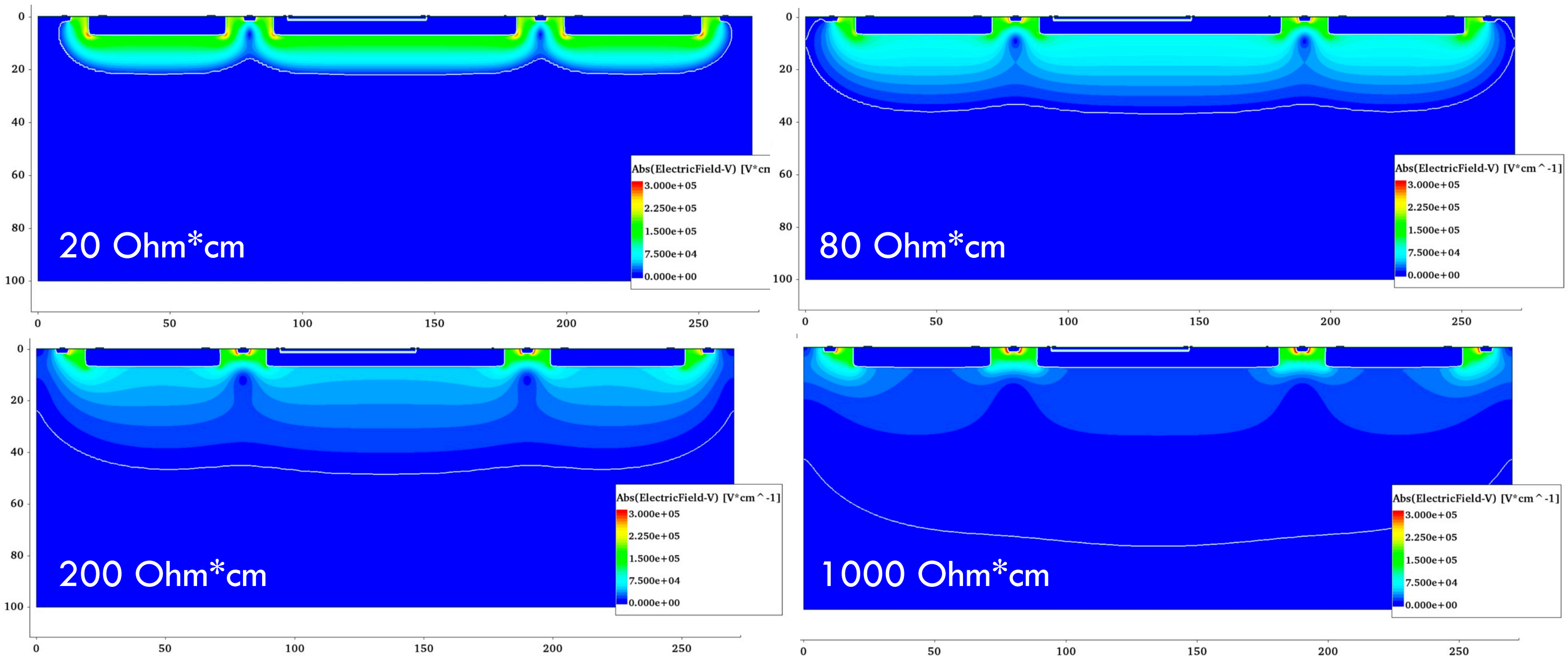
- **TCAD simulations** to analyse design of the pixel implants and circuit transistors
  - Different **wafer resistivities** available from the foundry
    - **20, 80, 200** and **1000** Ohm*cm
  - Difference between devices **biased** from the **top** and from the **back**
  - Study of sensor **general features and behavior**
    - Leakage current; charge collection (from drift and/or difusion); signal evolution; etc…



# HV-CMOS H35DEMO Pixel Sensor

## TCAD simulations – Different resistivities

- Comparison of the electric field between 20, 80, 200 and 1000 Ohm*cm



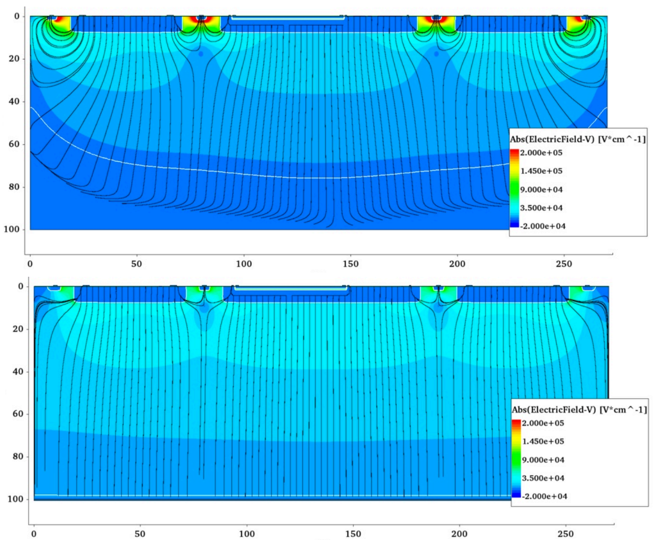

  - While lower resistivities has higher electric field close to the collection diode, higher resistivities leads to larger depletion zone

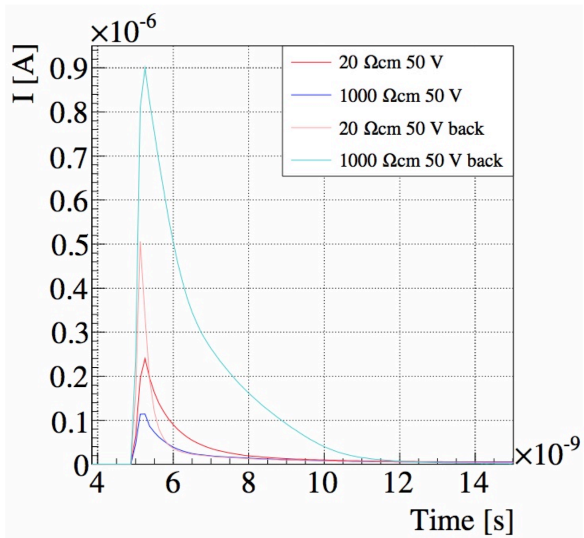
# HV-CMOS H35DEMO Pixel Sensor

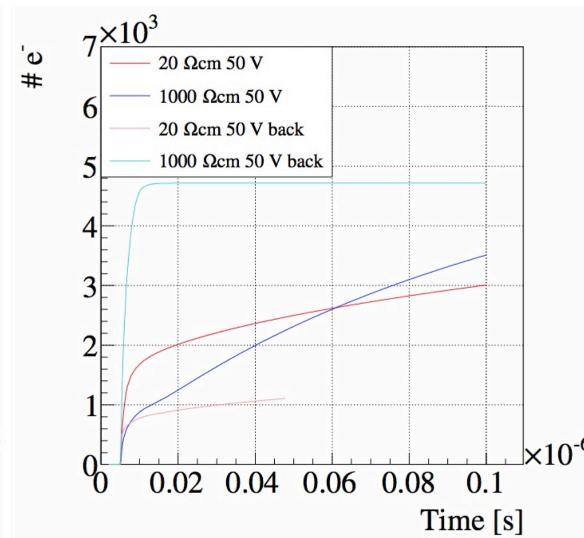
## TCAD simulations – Different biasing



- Possibility to process the devices back side, allowing to bias the sensor from the back plane (opposite to the collection diode)
  - Visible effect on electric field intensity and charge collection efficiency
    - **Larger depletion** zone for the same bias voltage
    - Combined with higher substrate resistivity can lead to **faster** and **higher charge collection**



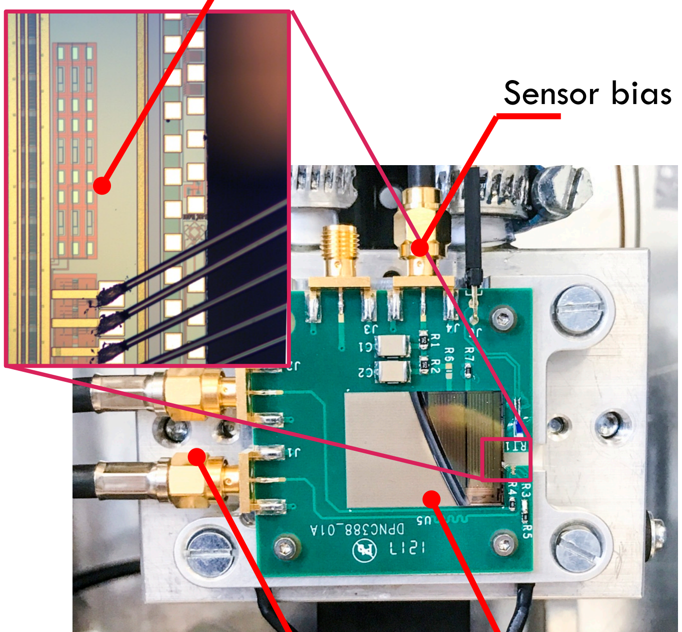



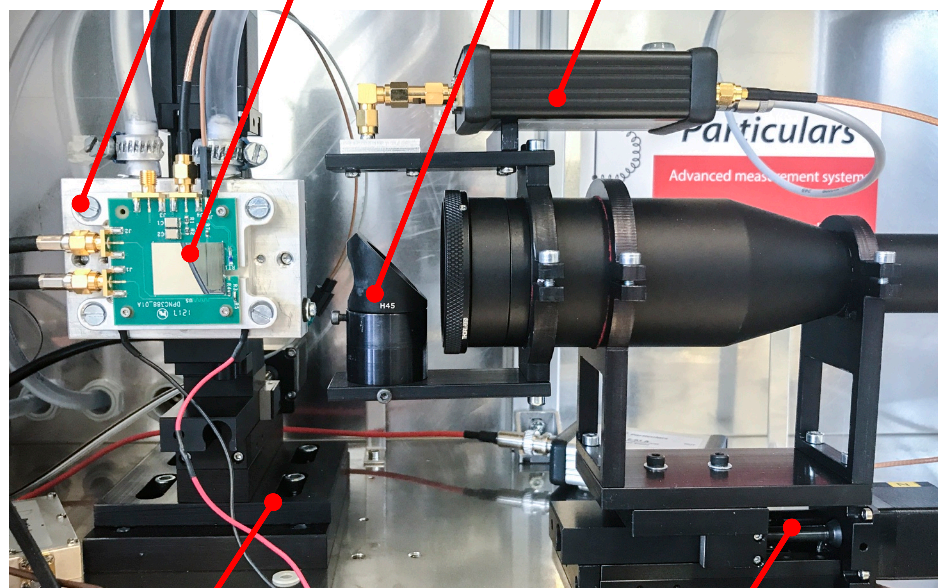



# HV-CMOS H35DEMO Pixel Sensor

## TCT measurements – Setup

- Red (**660 nm**) and infrared (**1060 nm**) laser for **top** and **edge TCT** measurements



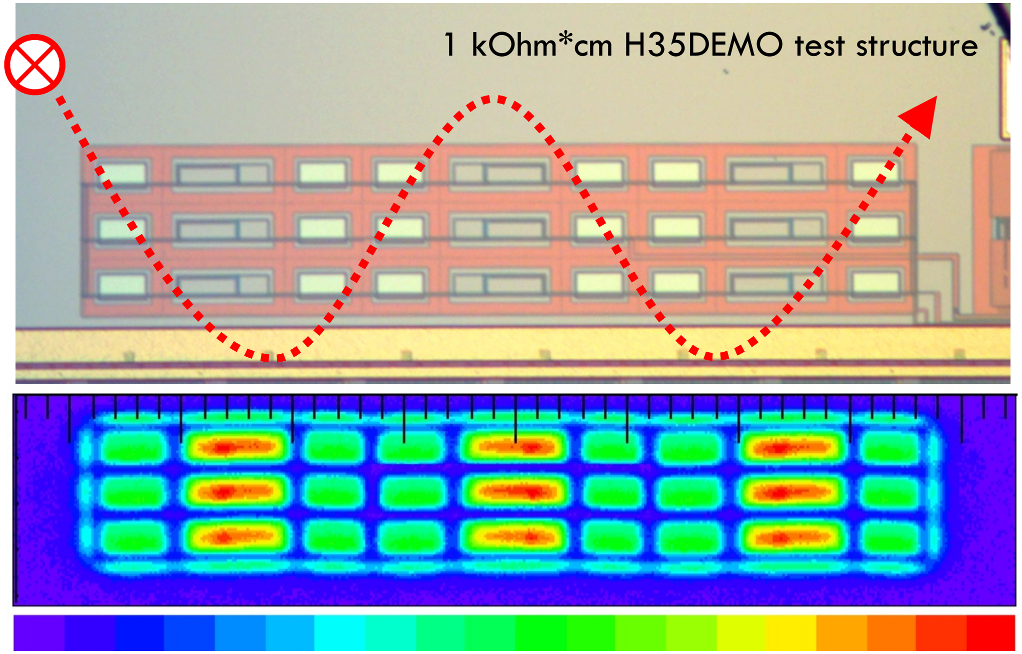
# HV-CMOS H35DEMO Pixel Sensor

## TCT measurements – Top surface scan



- Scan over the surface with a 1064 nm laser
  - Record of **each current pulse** generated by the laser hit on each position
  - Penetration depth of **~1 mm**
  - Clear visibility of pixel collection diodes

1064 nm laser

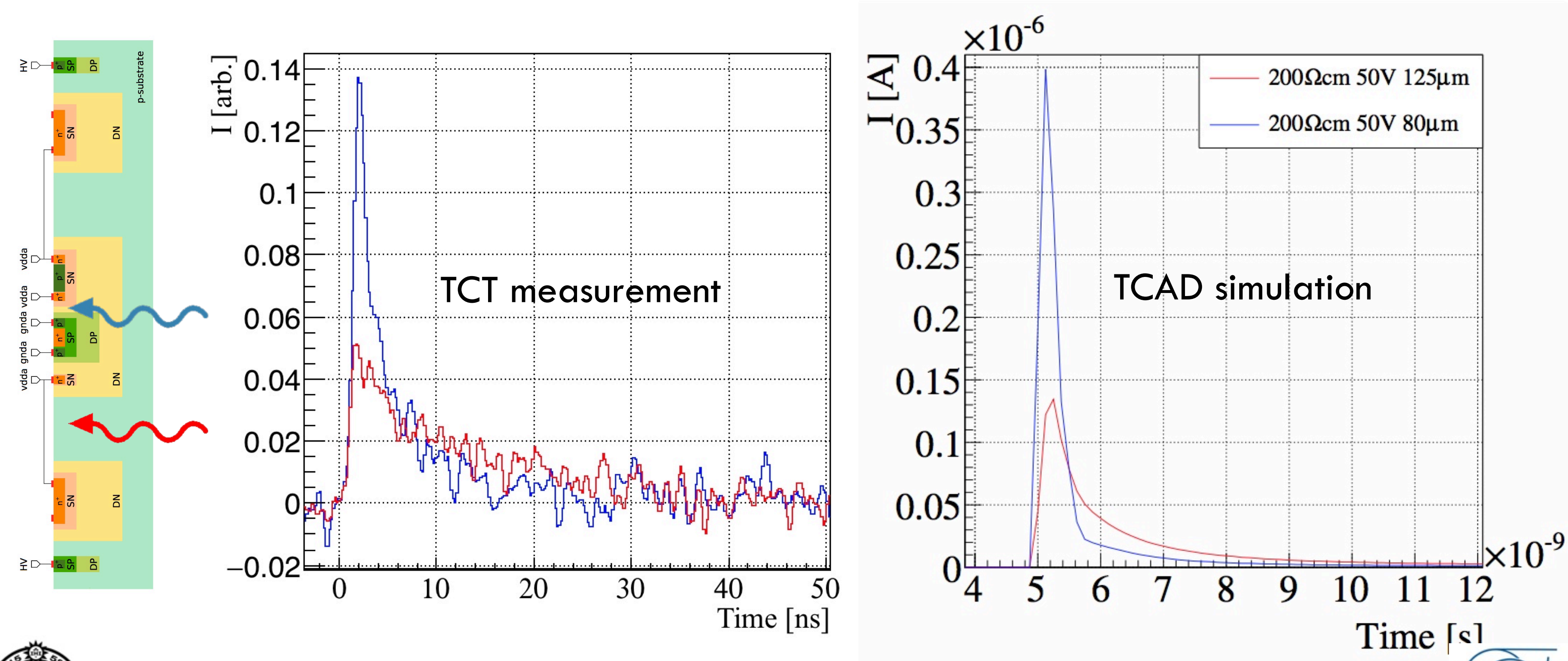


# HV-CMOS H35DEMO Pixel Sensor

## TCT measurements – Top surface scan



- Charge collection (efficiency) within one pixel in a 200 Ohm*cm sample
  - Laser beam focused on the middle of the pixel middle diode *VS* between pixel collection diodes

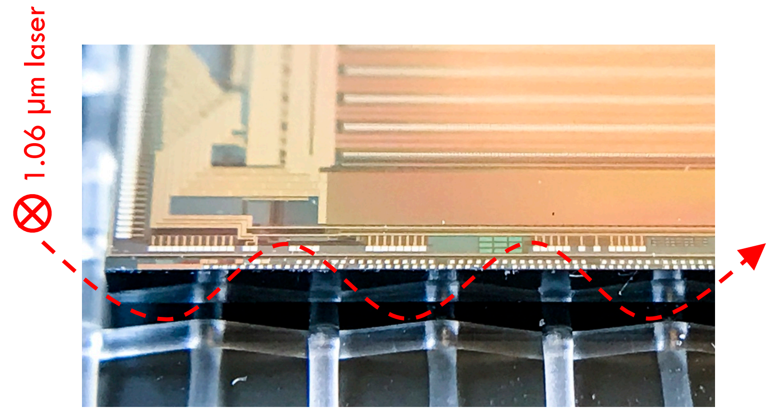


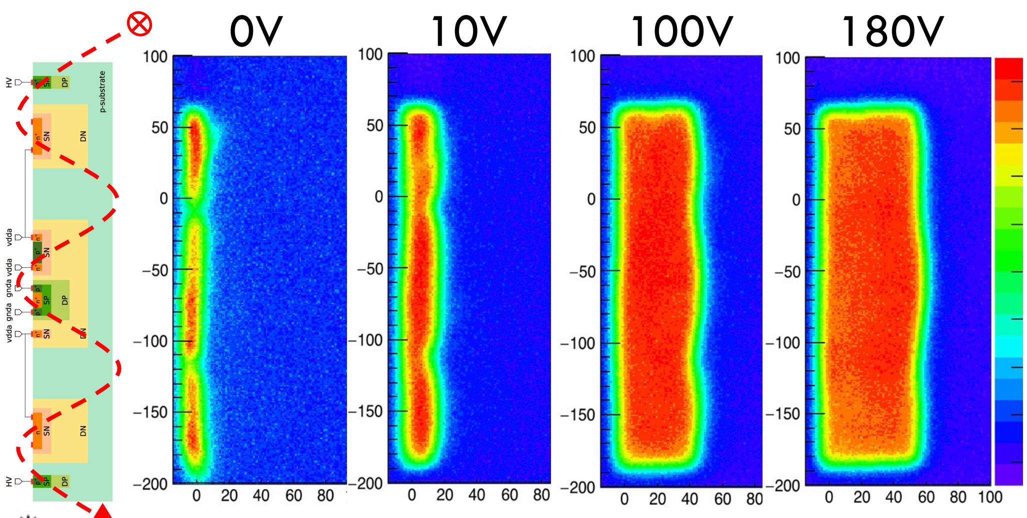
# HV-CMOS H35DEMO Pixel Sensor

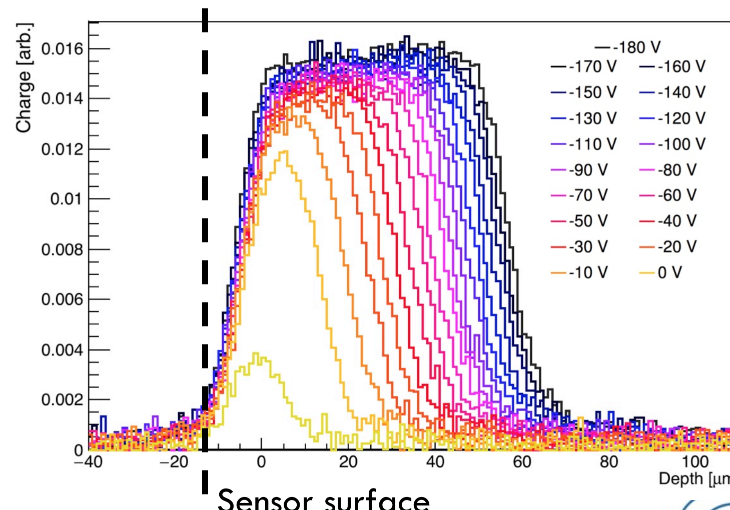
## Edge TCT measurements – Edge surface scan



- **Edge laser scans** on the device allows to simulate different bulk depth interactions (infrared laser)
  - Hits inside the depletion zone will create a faster charge collection (and a higher collection within a small integration time)
  - Voltage scans shows how the depletion zone grows



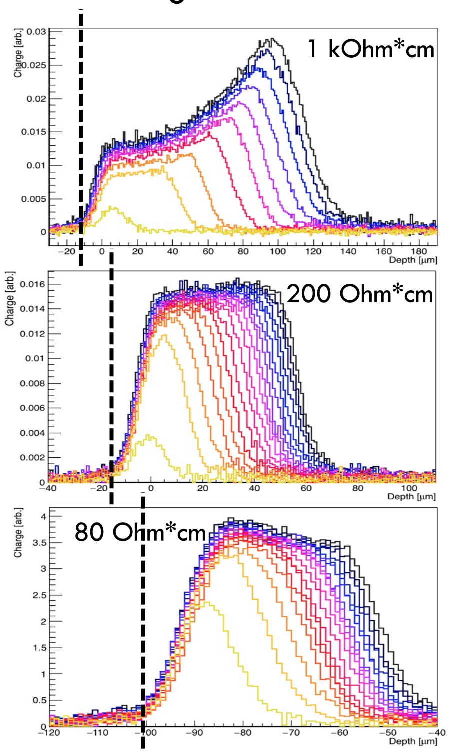



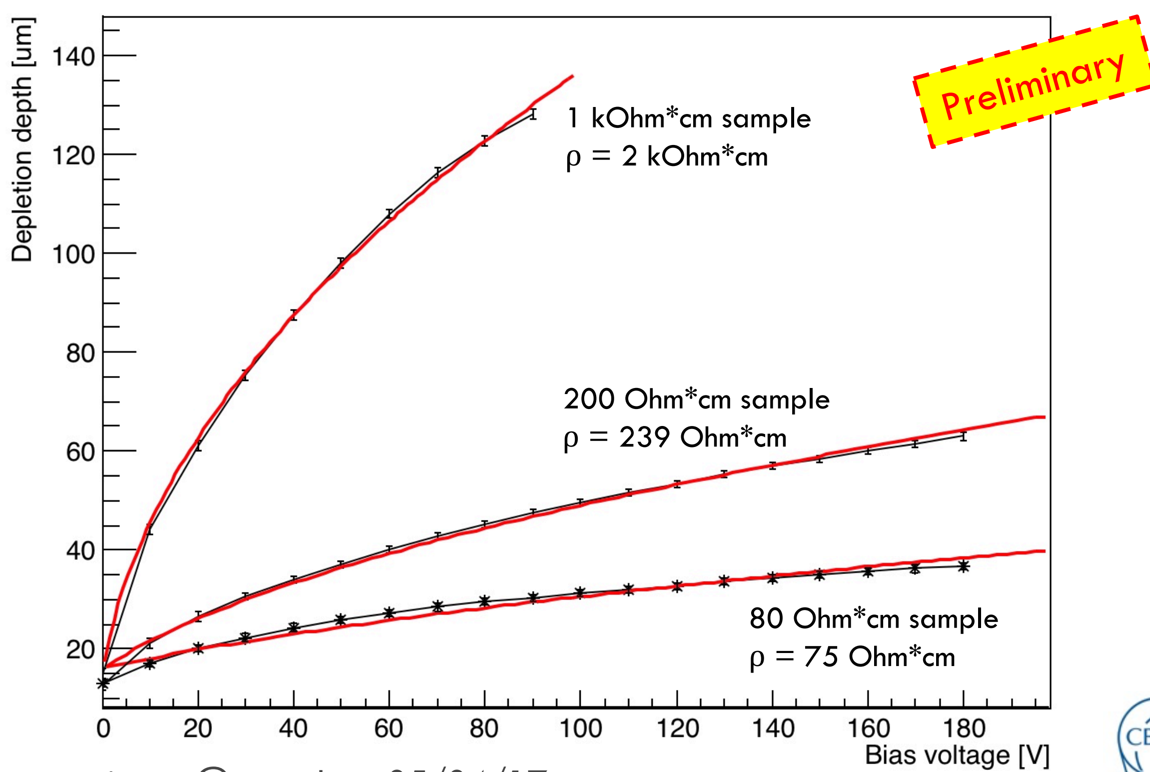
# HV-CMOS H35DEMO Pixel Sensor

## eTCT measurements – Depletion depth *VS* Bias



- **Depletion depth** of sensors with **different resistivities**
  - Depletion depth fit with $d = 0.3 \cdot \sqrt{\rho \cdot (V_B + V_{bi})}$
    - Agreement with **TCAD** simulations **under verification**




mvicente@cern.ch 

# Detector assembly
## @ UniGE Clean Room

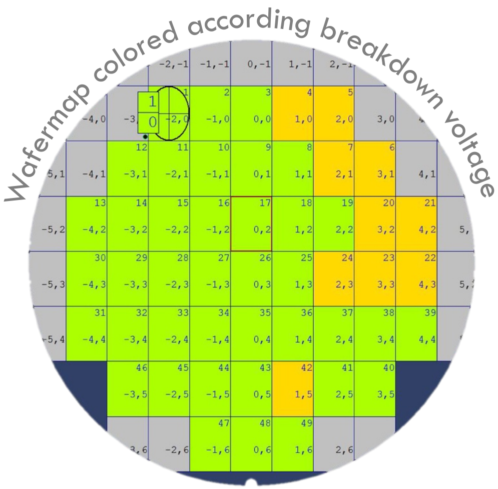


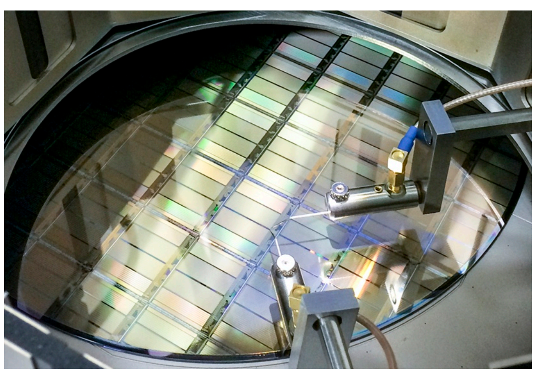
# H35DEMO wafer probing

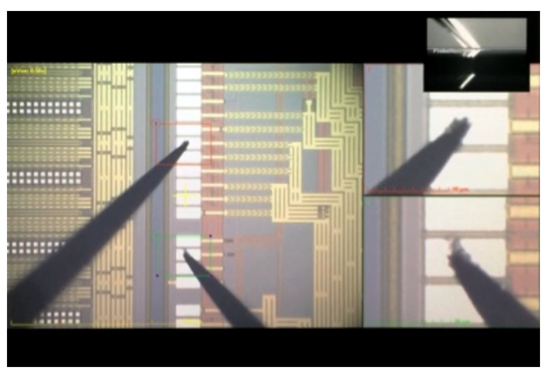
## HV-CMOS IVs

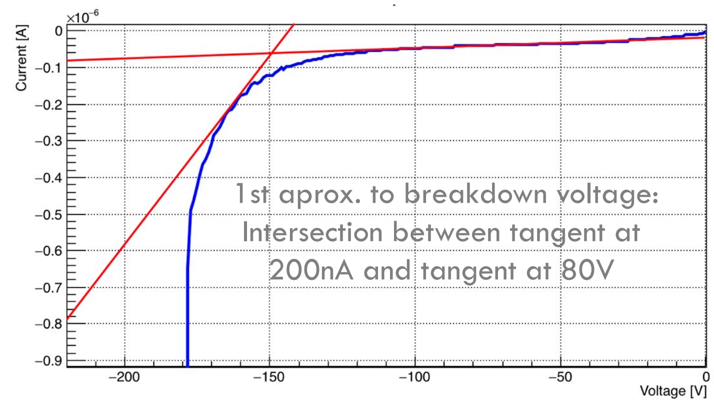


- **Semi-automated** operation wafer prober
  - Thermal Chucks from **-60°C** to 300°C
  - XYZ Resolution: **0.2 µm**
  - **Auto XYZ** and **theta correction** for sub-micron stepping
  - **Automatic** die size measurement and **wafer mapping tool**
- Programable tests over full wafer
  - Current *vs* Voltage on each (sub)die automatically **(~50 devices/hour)**





H35DEMO wafer with probes positioned


Probes positioned on HV pads

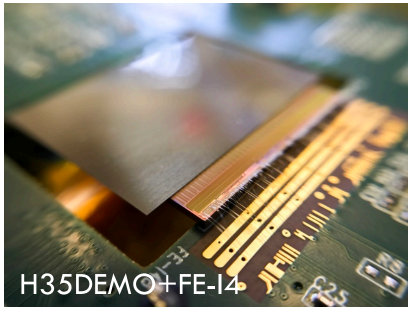


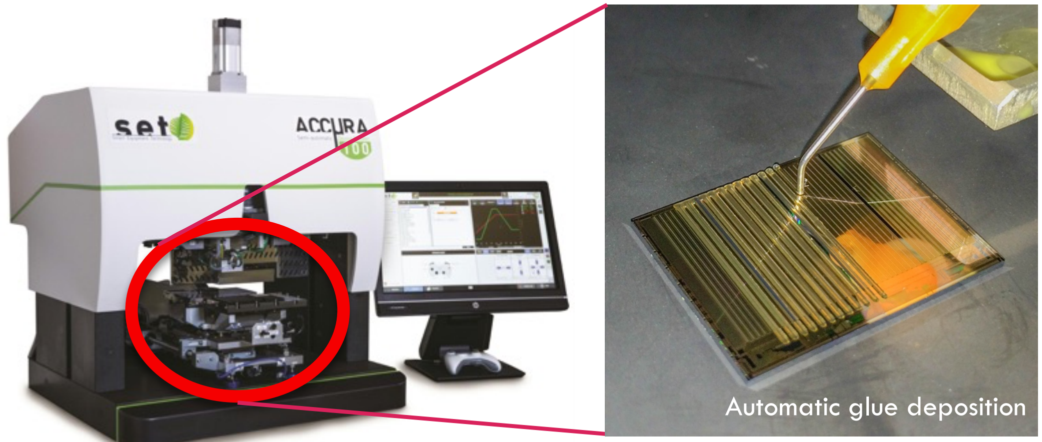
# Flip-chip for CCPDs

## H35DEMO + FE-I4

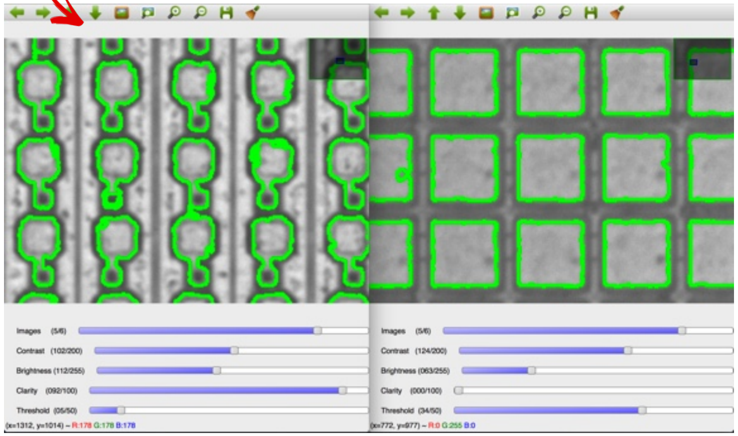


- Heating up to **400 degC** and force applied by bonding arm up to **100 kgf**
  - H35DEMO+FE-I4: **100 degC** (for **6 min**) and **5N bonding force**
    - **Automatic** glue (**Araldite 2011 epoxy resin**) **deposition** on H35DEMO
- Post bonding accuracy **~1 µm** achieved
  - < 0.5 µm (theoretically)
  - **PixelShop** pattern-recognition program to guide alignment




Set Accura 100



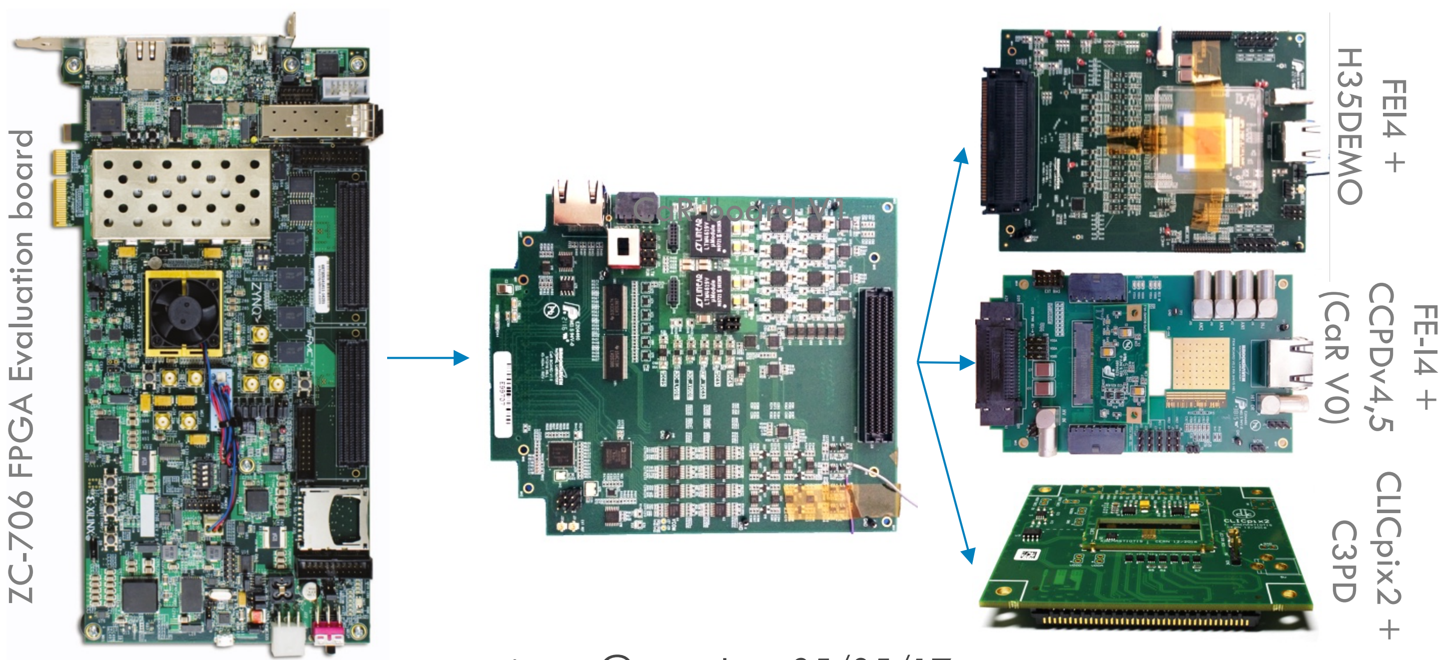
CLICpix (left) and CCPDv3 (right) pixel pads

# CaRIBOu System

## HV-CMOS DAQ – GITLAB LINK



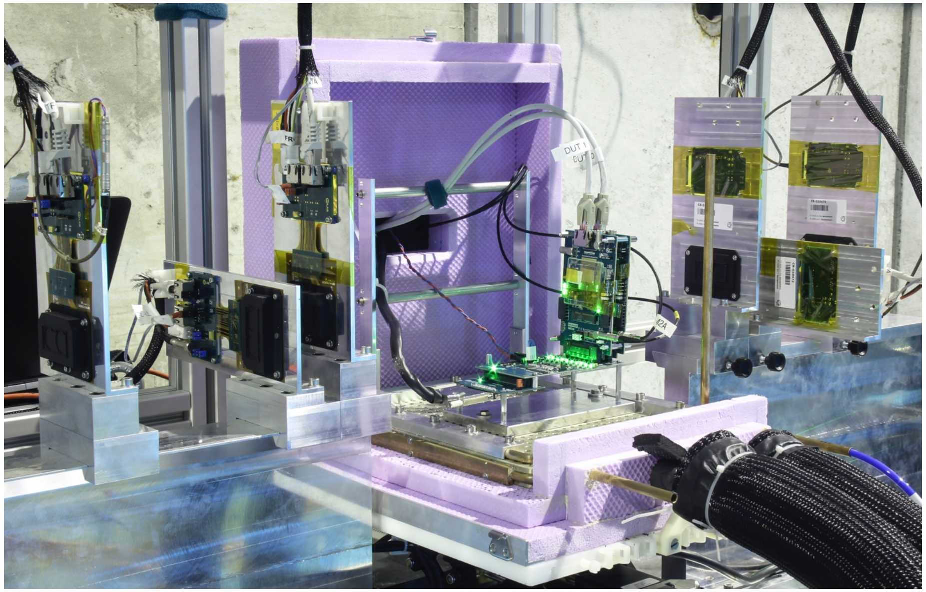
- A **FPGA based modular** readout system for silicon detectors
  - Developed at **BNL** with collaboration from **UNIGE** and **CERN** for **ATLAS** and **CLIC**
  - **Modular architecture** allows for integration of **new readout chips and sensors**
    - Adrian's talk (CERN): http://indico.ihep.ac.cn/event/6387/session/38/contribution/24
    - Hongbin's talk (BNL): http://indico.ihep.ac.cn/event/6387/session/52/contribution/260



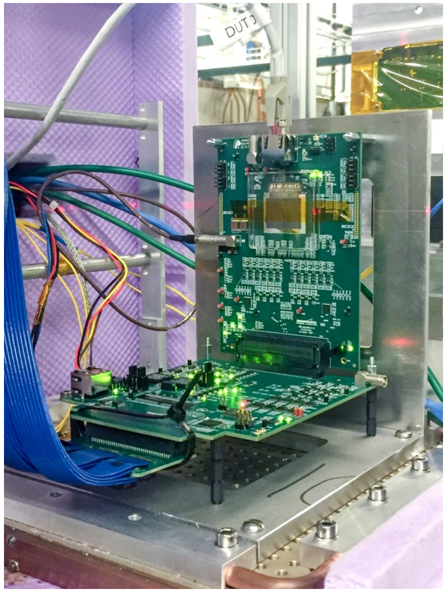
# Testbeam results

## The FE-I4 UniGE Particle Telescope

- **FE-I4b** based telescope
  - ”Permanently” installed at **CERN SPS H8** testbeam hall
  - 6 planes of double FE-I4b modules (HSIO/RCE redout) (+ 2 Mimosa26 planes being installed)
    - Current: **8x12 μm.** With Mimosa26 planes: **2-3 μm**
  - Cold DUT box (down to **-20 degC** @ DUT)



FE-I4b UniGE telescope with CaR board V0.1 and 2x CCPDv4 as DUT



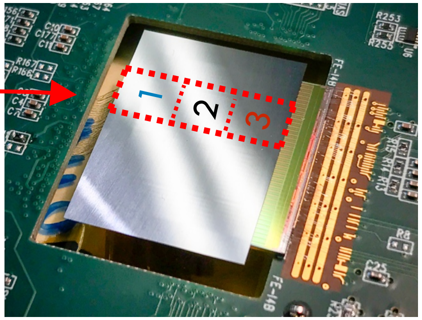
CaR board V1 with FE-I4|H35DEMO sample

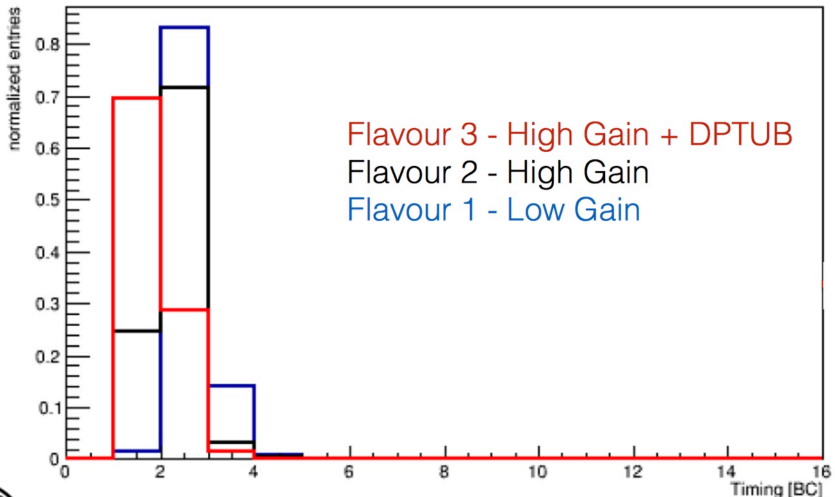
# H35DEMO Testbeam results

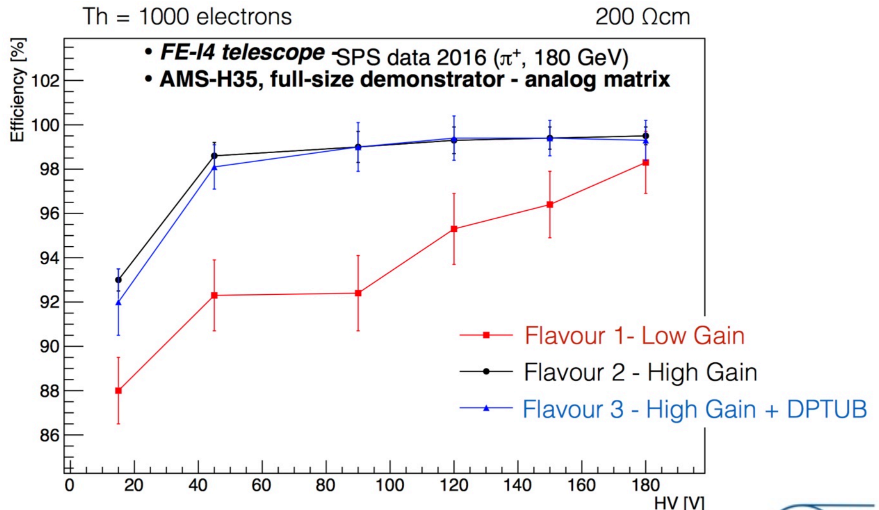
## CERN SPS - Nov 2016



- 200 Ohm*cm H35DEMO Analog Matrix 1 studied
  - **Caribou H35DEMO 01** sample
  - CERN SPS **180 GeV pions** beam
  - 1000 e⁻ FE-I4 threshold
  - **99% of collected charge within 50 ns** (left plot)
  - **99% efficiency for bias voltages > 90V** (right plot)



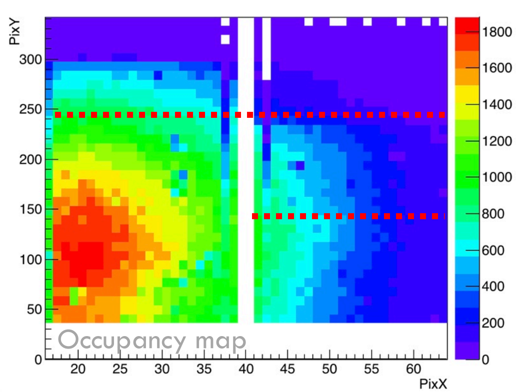
# H35DEMO Testbeam results

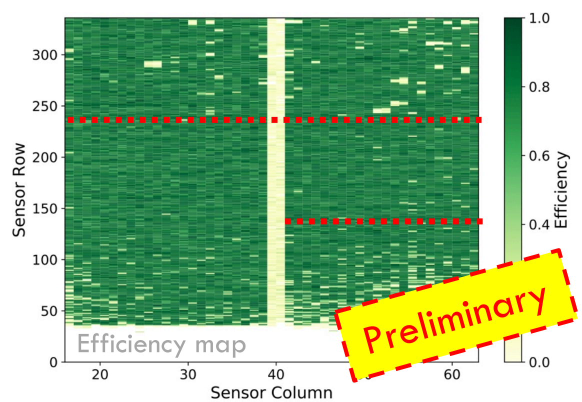
## Fermilab TestBeam Facility – 2017

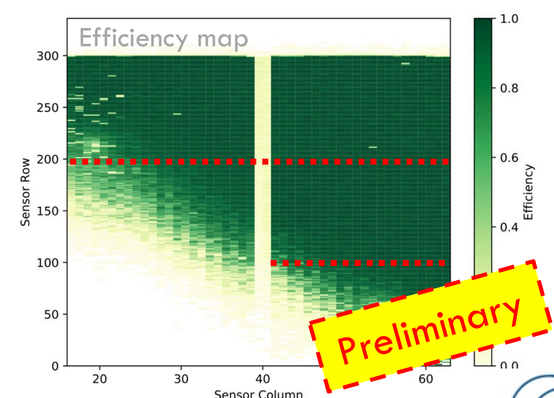


- Testbeam campaign at **FTBF** – IL/USA
  - **120 GeV protons** beam
  - Samples with **4** different **resistivities**
    - + voltage and threshold scans
- **Preliminary results!**
  - **High efficiency** for all 3 pixel types in both analog matrices
    - Some samples with **non uniformity** in the **efficiency**
      - Cross-section measurements shows a chip gap variation of ~7µm

**Thanks for our friends at Fermilab and Argonne!**



# Conclusions

## and overview



- ATLAS inner tracker detector will be upgraded for the LHC high lumni upgrade
  - **New all-silicon inner tracker** ➔ large area of silicon ➔ $$$
- **HV-CMOS** based sensor/readout chip is a candidate for the new detectors
  - **H35DEMO** HV-CMOS detector demonstrator chip
- **TCAD simulations** are done to evaluate sensor performance
  - **Top and edge TCT measurements** are done in order to verify achieved performance
  - **Agreement** between simulation and measurements is **satisfactory**
  - Results indicates **better performance** on sensors with **higher bulk resistivities** and **back biased** devices
- **Assembly** of HV-CMOS sensor with readout ASIC
  - **H35DEMO Wafer IV scan** ensures a good production **yield** and saves **time/money**
  - **H35DEMO + FE-I4b flip-chip** gluing using Araldite 2011 **Epoxy Resin** ➔ cheaper production
- **Testbeam results** using the **CARIBOU** DAQ system
  - First sample tested at SPS indicates **high efficiency** (~99%) with **99% of the charge** collected in **50 ns**
  - **Fermilab** testbeam **data** is still **under analysis. Good efficiency** on pixel matrix is **already observed**

# Future

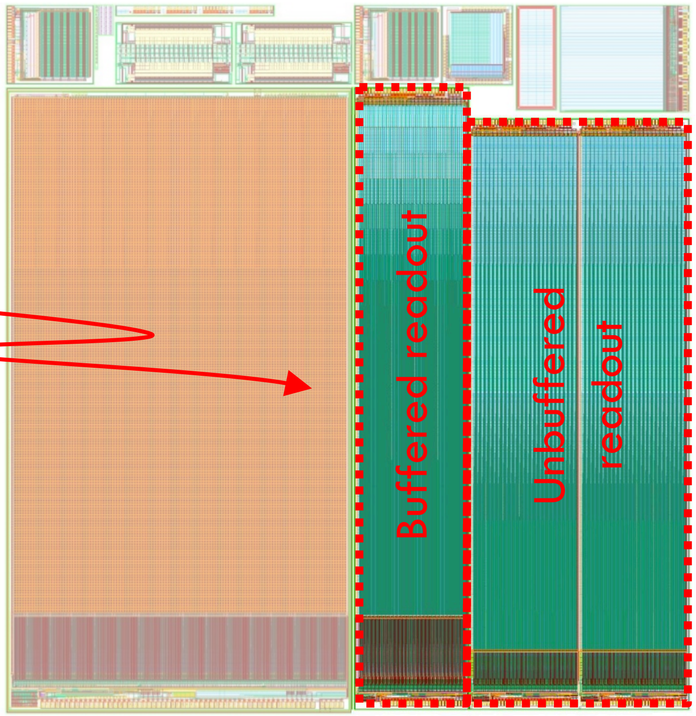
## and next steps



- Further tests on capacitively couples pixel **(irradiated)** devices
  - Cheaper implementation for larger areas by not using bump-bonds
  - **Pixel sizes < bump-bonds pitch restriction**
- Investigation on **MAPS** (monolithic detectors)
  - **Standalone** readout matrices of **H35DEMO**
    - Before and after irradiation
  - New **180nm** CMOS **demonstrator AtlasPix** chip
    - Previous **180nm prototype** results:

Before irradiation https://aps.arxiv.org/pdf/1603.07798.pdf

After irradiation https://arxiv.org/pdf/1611.02669v1.pdf




- Stay tuned for new results =)

谢谢

**Thank you**

# BACKUP

# H35DEMO
## Analog pixel flavors



### Analog Matrix 1

CSA uses a folded-cascode with an nMOS transistor as input device without gain boosting
> less noise, better radiation tolerance, increased power consumption

| Flavour 1 | Flavour 2 |
|---|---|
| use linear transistors | use enclosed layout transistors |

### Analog Matrix 2

CSA uses a folded-cascode with a pMOS transistor as input device

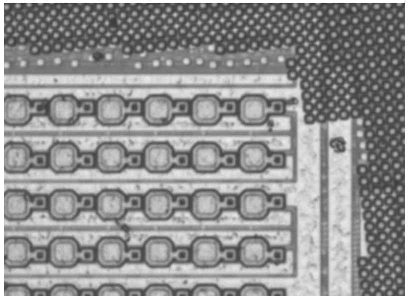
| Flavour 3 | Flavour 2 | Flavour 1 |
|---|---|---|
| with DPTUB for HV<br>High Gain | without DPTUB for HV<br>High Gain | without DPTUB for HV<br>Low Gain |

# Flip-chip at UniGE

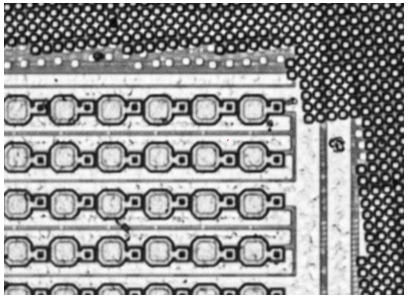
## CLICpix + CCPDv3 with PixelShop

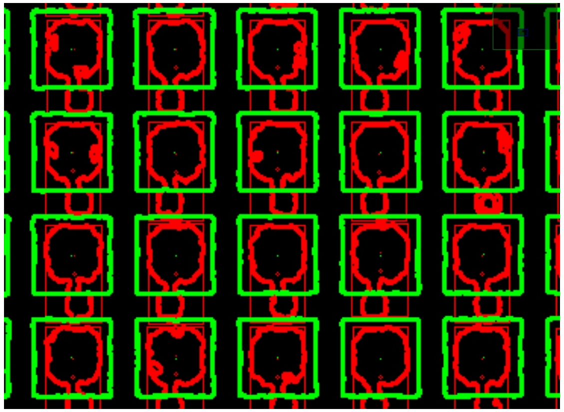
- PixelShop
  - Pictures from flip-chip digital cameras
    - 2 cameras with field of view of 900x700um
      - 0.37 um/pixel
  - C++ and OpenCV framework
    - Enhance pictures contrast for better contour finding
    - Calculate offset between contour geometric center

CLICpix original picure



CLICpix edited picure

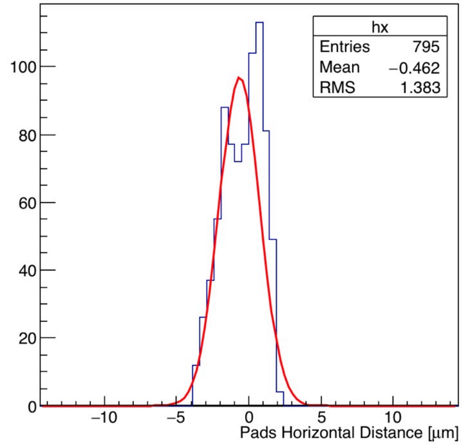




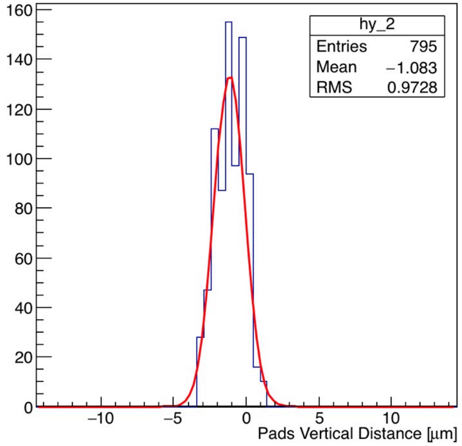
Pixel pads contours

CLICpix and CCPDv3

Horizontal pads offset




Vertical pads offset



# CaRIBOu System

## CaR board ressources



- 8 × general purpose power supplies with monitoring capabilities
- 32 × adjustable voltage output (0 — 4 V)
- 8 × current output (0 — 1 mA)
- 8 × voltage input (0 — 4 V)
- ADC (16 channels, 65 MSPS/14-bit)
- 4 × injection pulser
- I2C bus
- TLU RJ45 input (clock and trigger/shutter)
- general CMOS signals (10 × outputs, 14 × inputs)
  - with adjustable voltage levels (0.8 - 3.6V)
- 17 × LVDS pairs

FE-I4 + H35DEMO @ Fermilab 2017