CMOS pixel development for the ATLAS experiment at HL-LHC

Branislav Ristić
on behalf of the ATLAS CMOS Pixel Collaboration

TIPP 2017
2017/05/25

Outline

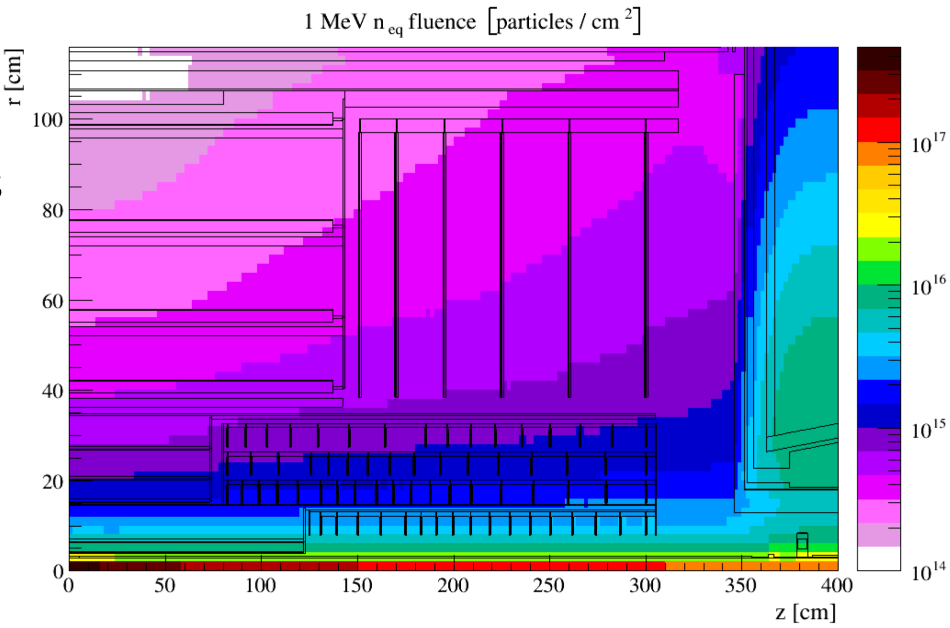
- The ATLAS Phase II Inner Tracker Upgrade
- CMOS Pixel Sensors
  - Concepts and Prototypes
- Results from Capacitively Coupled Devices
- Monolithic Modules
  - Current Monolithic Developments
- Summary

ATLAS Phase II Inner Tracker Upgrade

- LHC Phase II Upgrade in 2025:
  - 10 x increase of luminosity
  - Harsh radiation environment
  - → Up to 10^{16} neq/cm², 1Grad for inner layers
  - ~MHz/mm² hit occupancy

→ All silicon Inner Tracker covering ~200m²

- ! Cost effectiveness
- ! Power consumption
- ! Speed



CMOS Pixel Sensors

- Industry standard processes
  - Commercially available by variety of foundries in large volumes
  - Low cost per area, wafer thinning quite standard
- Cheap hybridisation: Gluing instead of bump bonding

  …or none at all → Monolithic sensors

The ATLAS CMOS Pixel Collaboration

KIT Karlsruher Institut für Technologie

University of Liverpool

CERN

Berkeley Lab

University of Oxford

Universität Heidelberg Zukunft seit 1386

universität bonn

University of Glasgow

u^b Universität Bern
AEC Albert Einstein Center for Fundamental Physics

Université de Genève Faculté des Sciences

Brookhaven National Laboratory

Bergische Universität Wuppertal

IFAE

Irfu - CEA Saclay
Institut de recherche sur les lois fondamentales de l'Univers

Lancaster University

INFN Istituto Nazionale di Fisica Nucleare

SLAC National Accelerator Laboratory

Institut "Jožef Stefan" Ljubljana, Slovenija

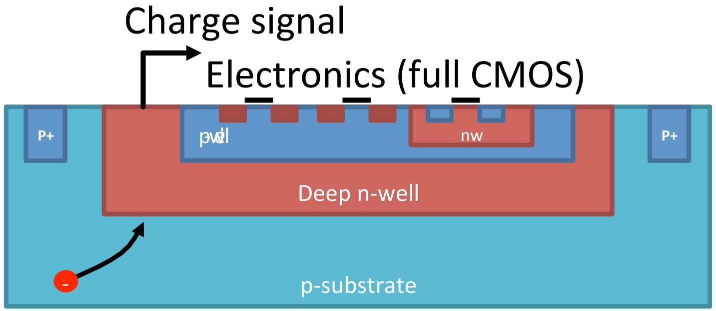
Centre de Physique des Particules de Marseille CPPM

Depleted CMOS Pixel Sensors

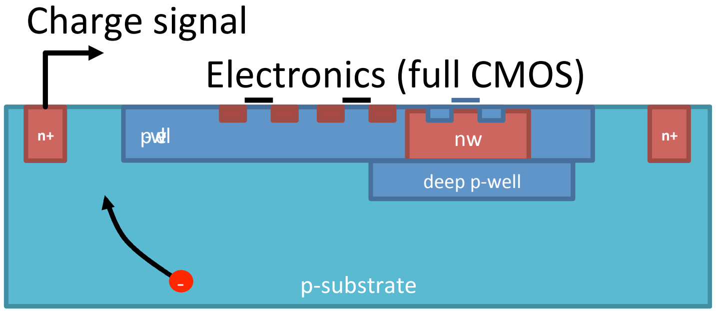
- Basic principle: High Voltage biased diode and LV electronics on top
  - Deep buried well: Collecting diode and/or shield for LV electronics
- Process parameters
  - Substrate resistivity: O(100)Ωcm (HVCMOS) to kΩcm (HRCMOS)
  - Additional shielding wells, epi layer, backside processing

$$d \propto \sqrt{\rho V}$$

- Large fill factor electrode
  - Uniform field, short drift distances
  - Large sensor capacitance
    → Noise, timing, power

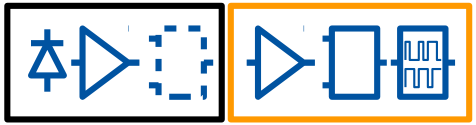


- Small fill factor electrode
  - Small sensor capacitance
    → low power and high speed
  - Potentially less radiation hard due to long drift distances



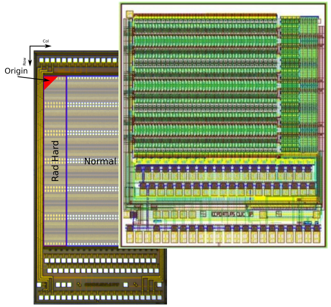
T. Hemperek, Pixel2016

Concepts and Prototypes

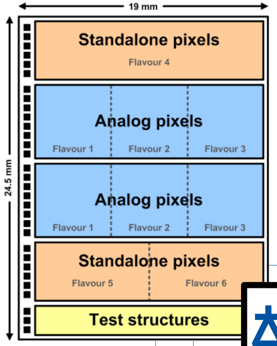


Active hybrid

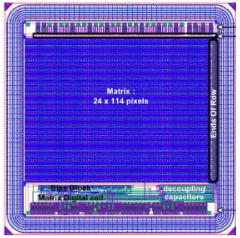
AMS



- HVCMOS 180nm process
- 6 small prototype generations
- Full size demonstrator in 350nm process

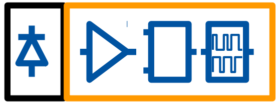


LFoundry



- 150nm HRCMOS process on 2kΩcm substrate
- CCPD_LF: initial prototype
- LF-CPIX: Large demonstrator adapted to FE-I4 readout

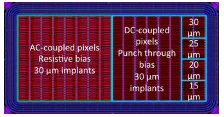
Also investigated: Global Foundry, ESPROS, Toshiba, STM, IBM, XFAB

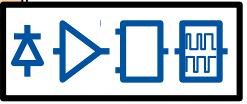


Passive hybrid

LF 150nm

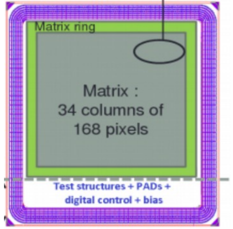
- 2kΩcm
- AC/DC coupling

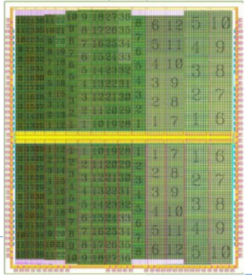




Monolithic readout

MONOPIX
MALTA
ATLASPIX
→ later



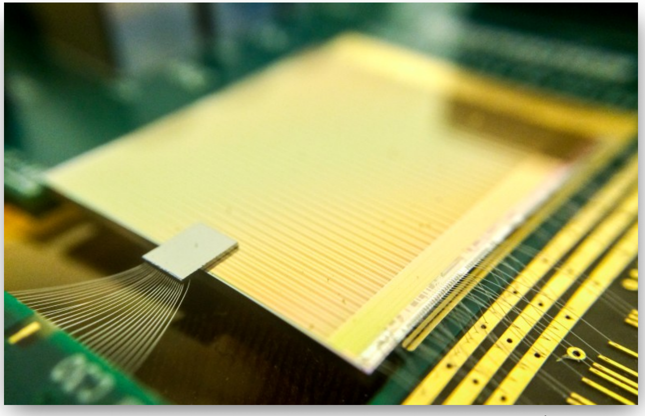


TowerJazz Investigator

- 180nm 1kΩcm epi layer
- 3T source follower readout

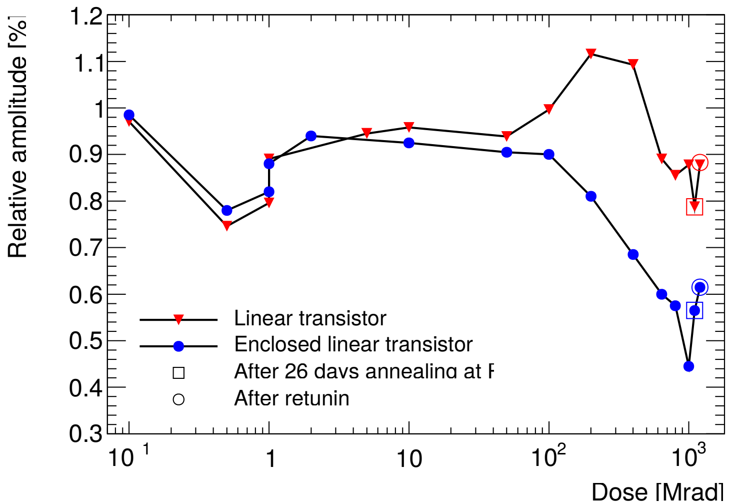
AMS H18 CCPDs

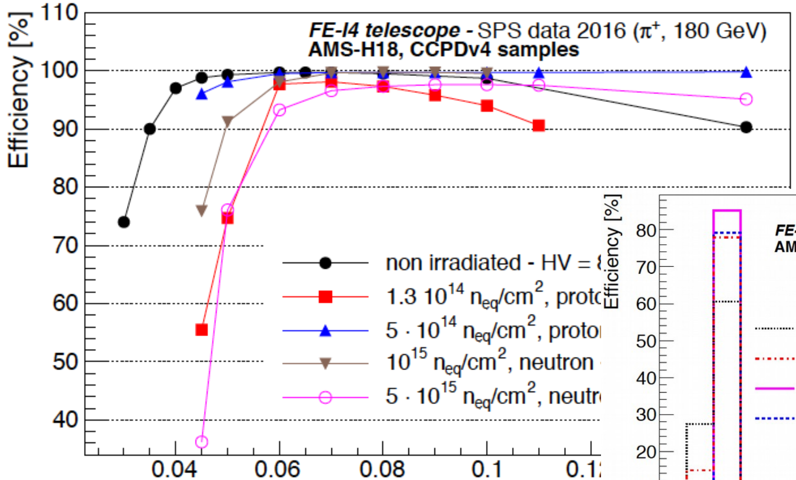
- 180nm HV-CMOS process on **~10-100Ωcm p-type** substrate
- Irradiated up to **$2x10^{16}$ n_{eq}/cm^2** and **1Grad TID**
- Efficiency of **>99%** measured after **$1x10^{15}$ n_{eq}/cm^2**

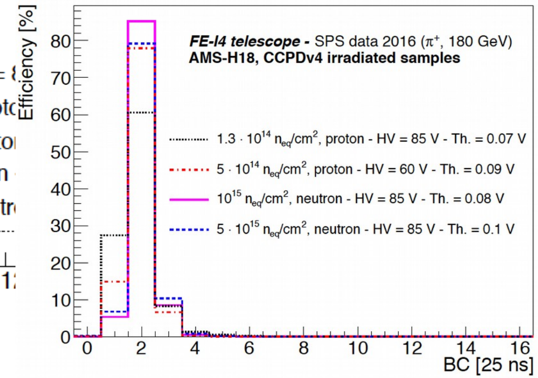


M. Vicente

→ More today by Mateus Vicente

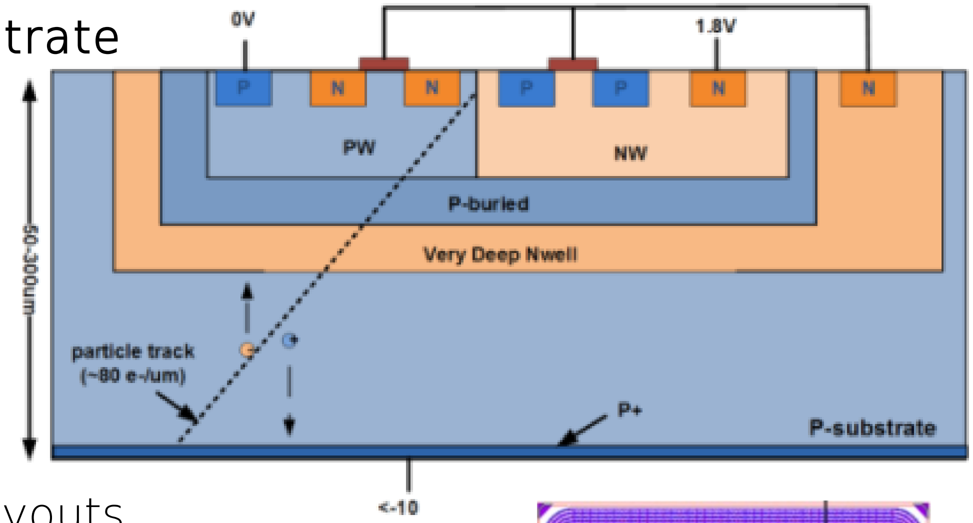


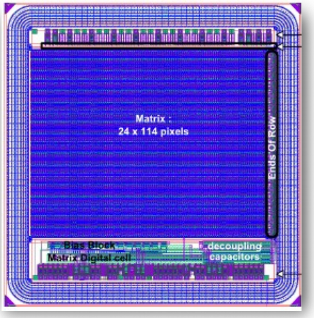


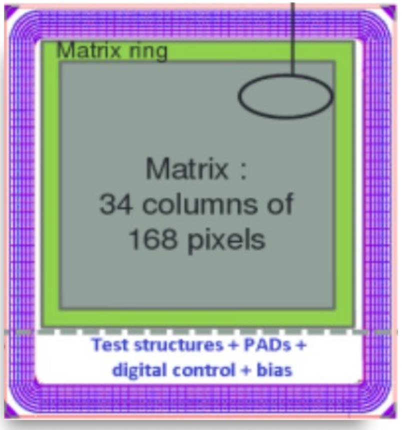


LFoundry 150nm CCPDs

- 150 nm process on high resistive substrate
  - Full CMOS possible
  - Implant customizations possible
  - Backside processing
- CCPD_LF (FE-I4 type)
  - Pixel size: 33um x 125 μm²
  - Chip size: 5 mm x 5 mm (24 x 114 pix)
  - Different amplifier designs/transistor layouts
  - Irradiated up to **50Mrad** and **10^{15} n_{eq}/cm^2**
- LF-CPIX (Demonstrator chip, FE-I4 type)
  - Improved discriminator and guard ring design
  - Pixel size: 250 x 50 μm²
  - Chip Size: 10 x 9.5 mm² (34 x 168 pix)
  - Thinned to 100 and 200μm with backside electrode

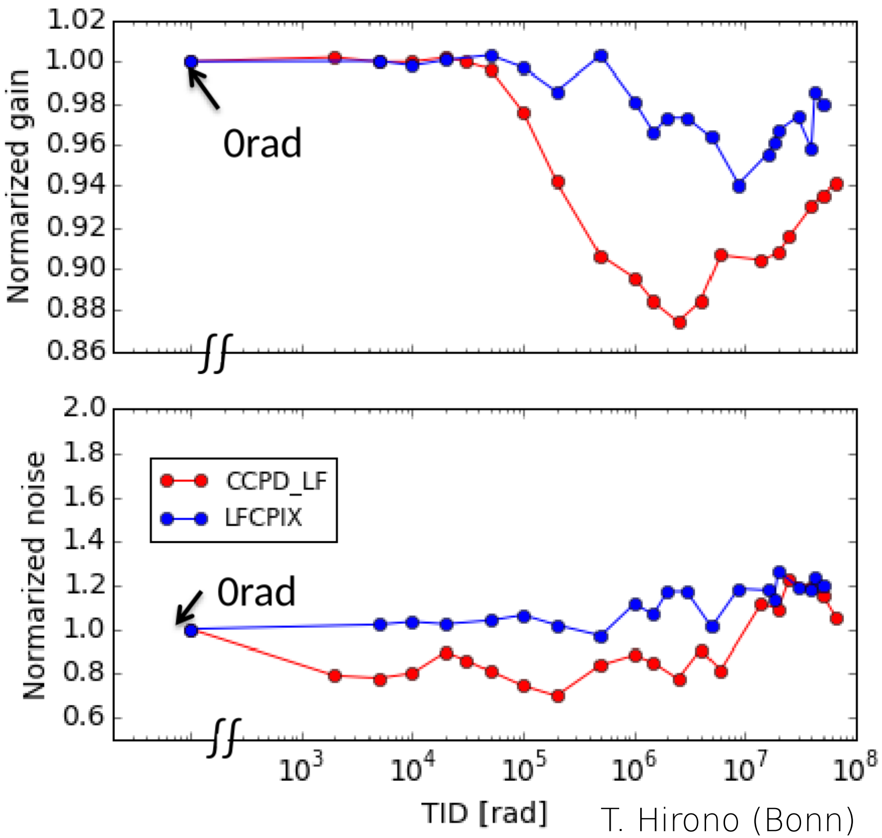






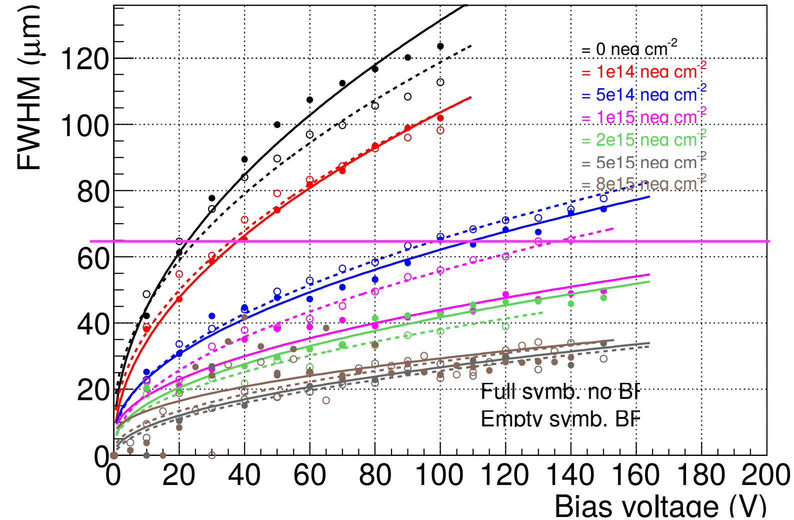
LFoundry 150nm CCPDs | Results

- X-Ray irradiation and test pulse injection up to 50Mrad

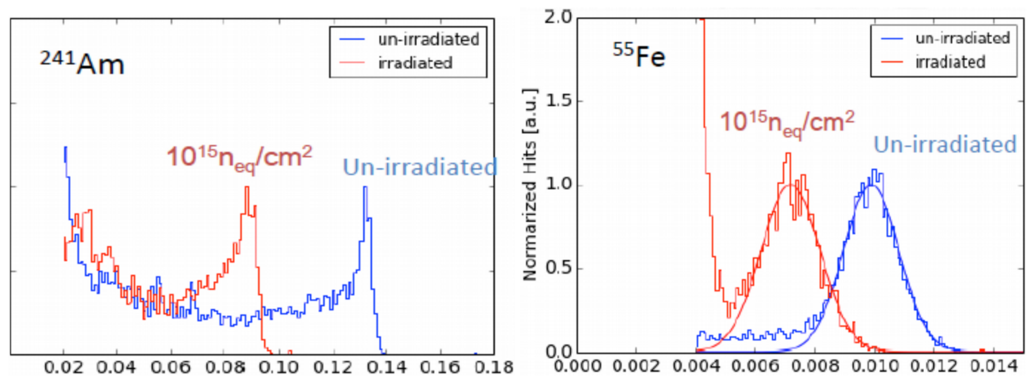


T. Hirono (Bonn)

- Neutron irradiation up to $5x10^{15}$ n_{eq}/cm^2



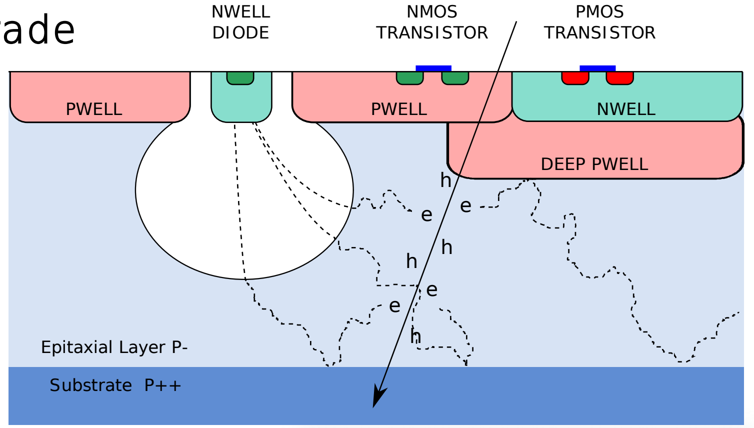
I. Mandic et al.
JINST 12 P02021

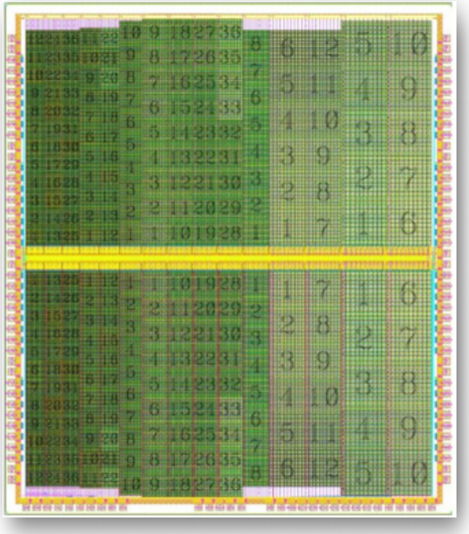


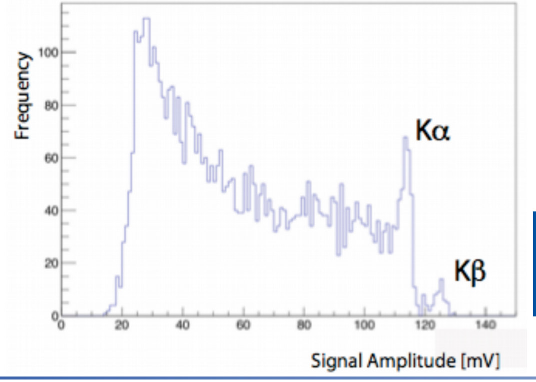
The TowerJazz 180nm Investigator

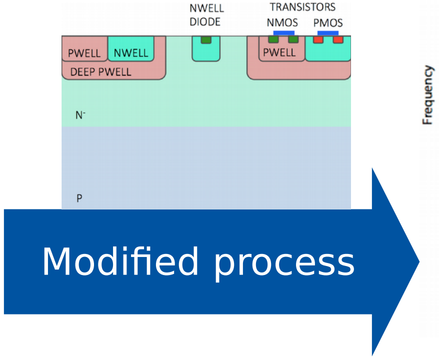
- Originally R&D for the ALPIDE chip for the ALICE Upgrade
- Epitaxial layer on high resistive substrate
- Separate, small collecting diode
  → Small capacitance
  → Higher gain and speed, potentially low power
- Charge collection difficult far from n-well, especially after irradiation

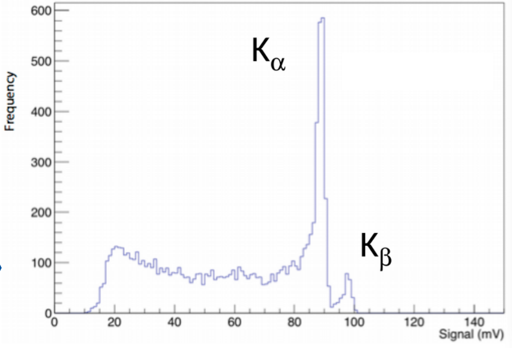
  → Process modification adding planar n-type layer
- Investigator prototype implements various electrode parameters (spacing, size)
- 3 transistor readout cell



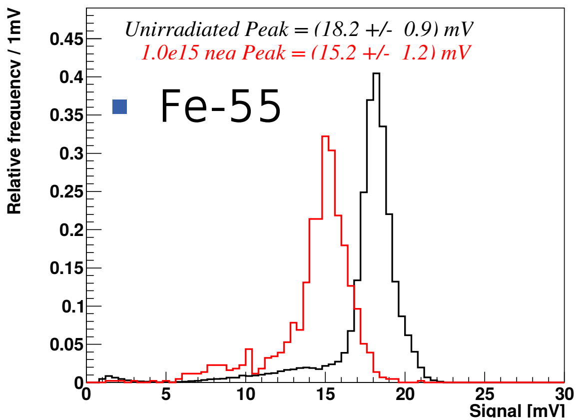


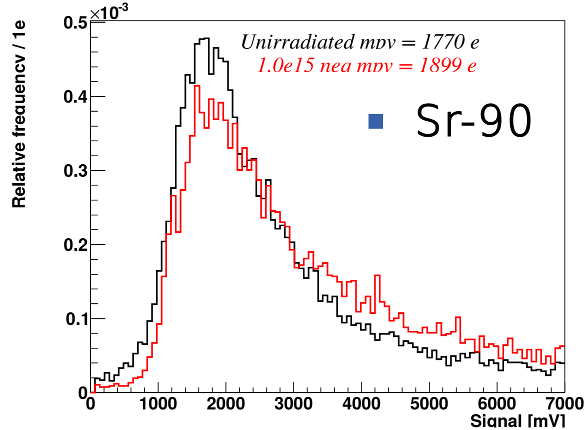


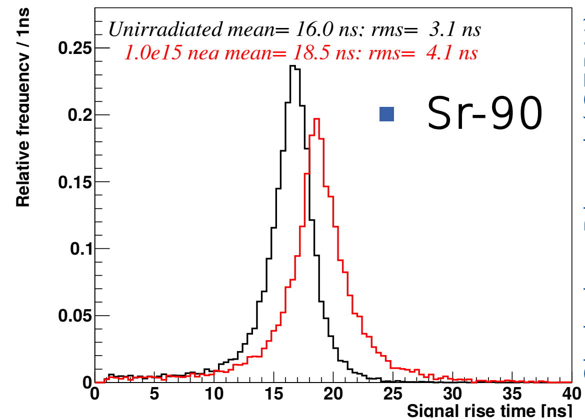




The TowerJazz 180nm Investigator

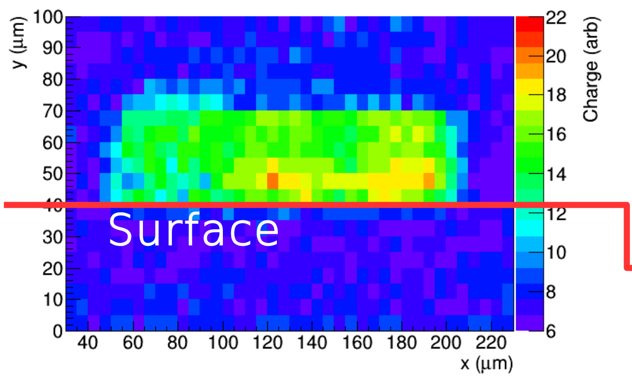






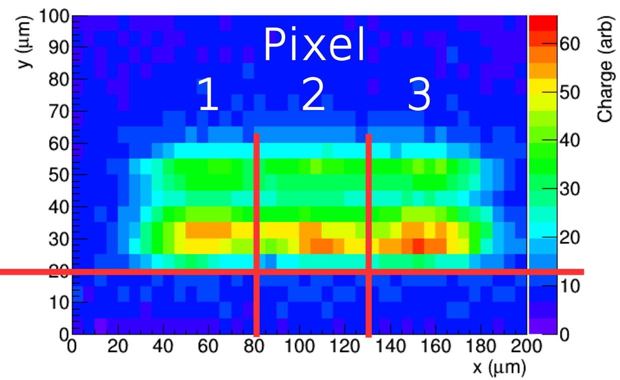
Christian Riegel (CERN)
doi:10.1088/1748-0221/12/01/C01015

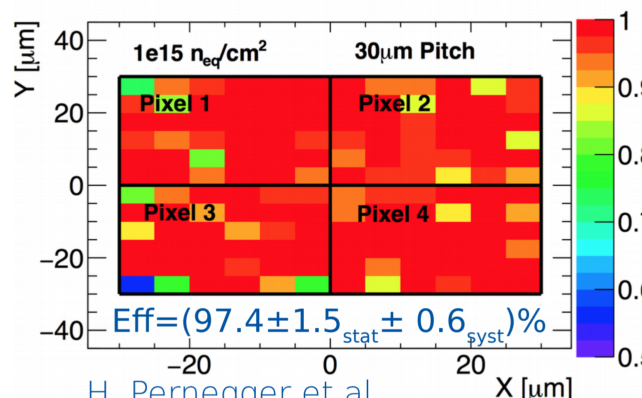
- Unirradiated



B. Hiti (Ljubljana)

- $1\times10^{15}\ n_{eq}/cm^2$



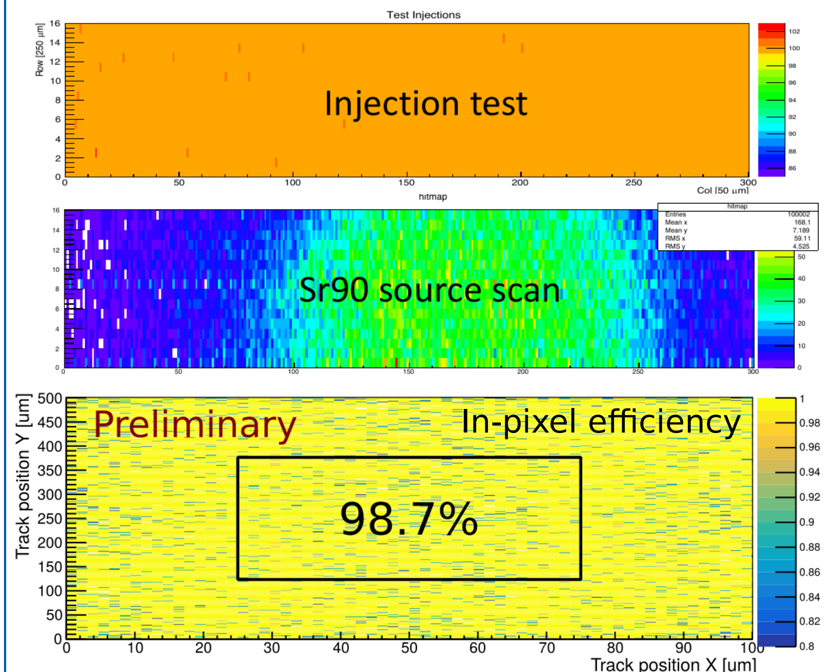


H. Pernegger et al.
Under review by JINST

Depleted Monolithic Sensors for ITk

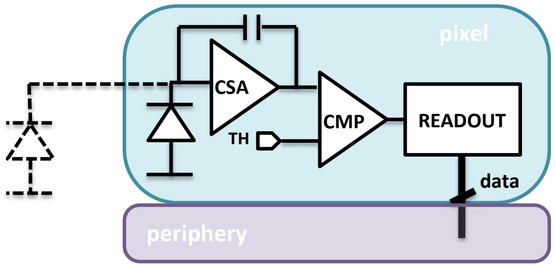
- Advantages
  - **No hybridization** (Cost effective, simple assembly)
  - Low **material budget** (chips thinned down to depletion thickness)
  - As **radiation hard** as hybrid modules
- Challenges
  - Power consumption
    (input capacitance, digital logic)
  - Isolation from digital crosstalk and noise
  - Pixel size (depending on readout scheme)
- First results with monolithic parts of the **AMS H35DEMO** and lots of experience from Mu3e Collaboration

→ **Extensive development effort in ATLAS**

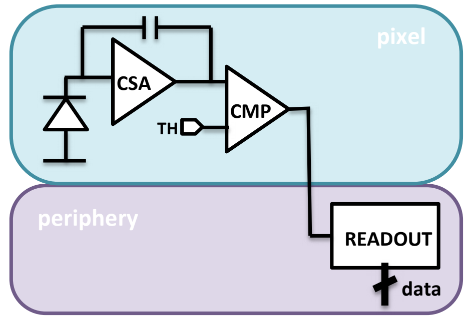


S. Terzo et al.
arXiv:1705.05146

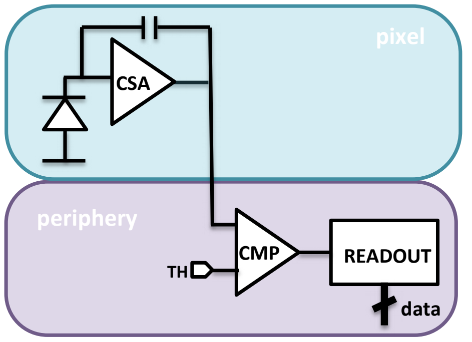
Monolithic Readout Concepts



- Small inactive periphery
- Buffer in Matrix
- Digital activity in matrix



- Smaller pixel size possible
- No clock to the matrix
- 1 – 1 routing



- Less digital crosstalk
- Complex routing of analogue signals
  - Signal integrity
- Large inactive periphery

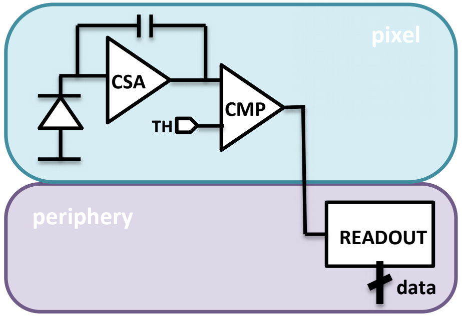
Column drain architecture

- Token traverses column, triggering R/O
- Hit buffering (ToT or LE/TE timestamps)
- Synchronous readout of buffers

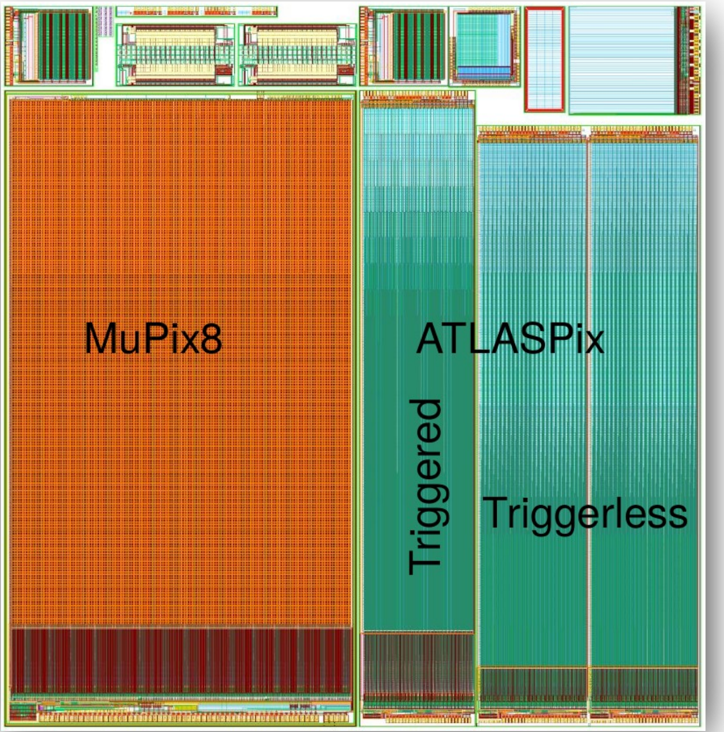
Asynchronous hit to periphery

- Comparator output (directly) to periphery
- Buffering and time-stamp at periphery
- 1 – 1 connection or pixel bus and delay

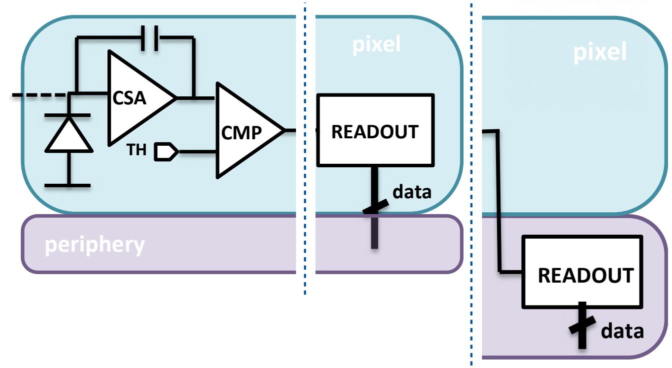
AMS aH18 ATLASPIX



- Joint submission with the Mupix8 Chip
- Pixel sizes 40µm x 130µm and 50µm x 60µm
- Amplifier and Discriminator in pixel cells
- Triggered matrix
  - 16 pixels connected to four readout buffer cells
  - 8-bit wide Parallel Pixel To Buffer (PPTB) bus
  - FE-I4 like latency based readout
  - Fast, but can be ambiguous
- Triggerless matrix
  - Each front end connected directly to a corresponding digital cell in the periphery
  - Continuous polling for new hits
  - Simple and small front end to periphery bus

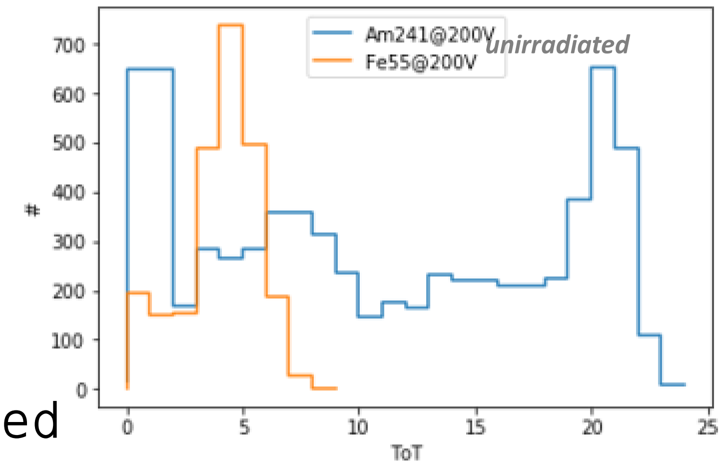


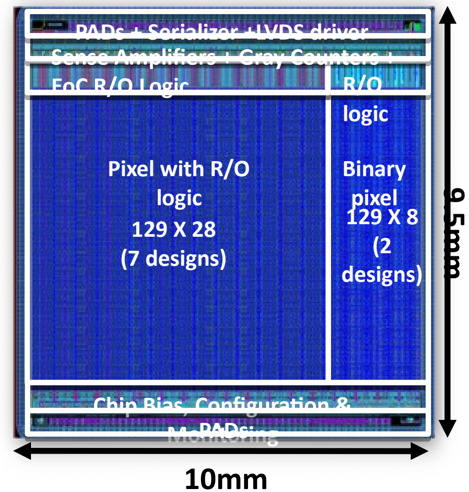
LFoundry Monopix



- ~10 x 10 mm² with 50 x 250 µm² pixels
- Each pixel: hit address and 8bit leading edge + trailing edge timestamp
- Column Drain Readout: Two approaches
- Readout in pixel
  - Simple bus, complex pixel
- Only CSA and comparator in pixel
  - Simpler pixel, 1-1 routing to periphery
- Nine pixel flavors implemented
- Pre-radiation sensor breakdown of above 250V

Single pixel spectra (full digital readout)



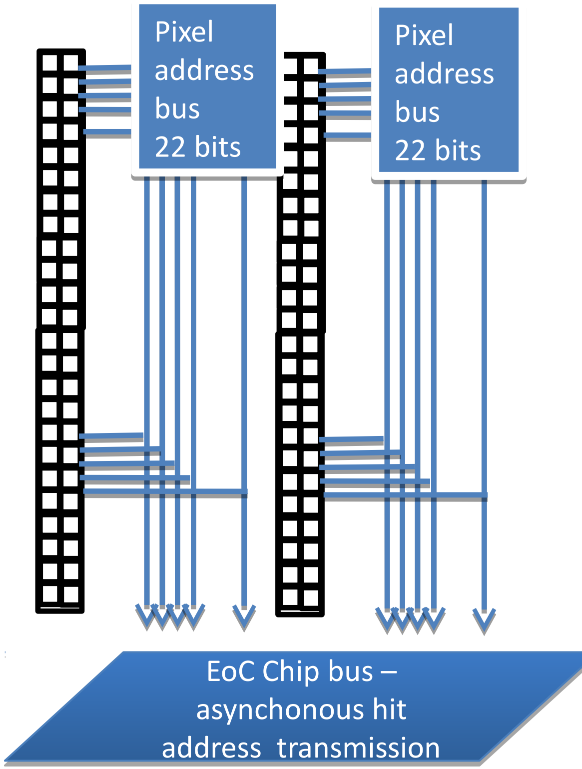


T. Wang et al 2017 JINST 12 C01039

- Further LF prototypes: COOL, LF2, ALPHA (ATLASPIX like)

TowerJazz 180nm MALTA

- Active area 18 x 18 mm² with 36.4 x 36.4 µm² pixels, separate collecting diode
- Novel concept for triggerless readout
- All hits are asynchronously transmitted over high-speed bus to EOC logic
  - Each pixel: CSA + Discriminator + Flip-flop
  - Matrix divided in double columns and pixel groups
  - Hit info (pixel group + hit pattern) sent via DC bus to periphery
- 40bit chip bus to LVDS/CMOS output
  - Daisy chains of chips possible
- No clock distribution over active matrix (power and cross-talk)
- External BCID clock for synchronisation and charge measurement
  - Analog measurement through time difference to leading edge
- Bias current 200nA to 500nA can be used to adjust TW range



- Same periphery, but Column Drain Readout and ToT in pixel cell → TJ Monopix

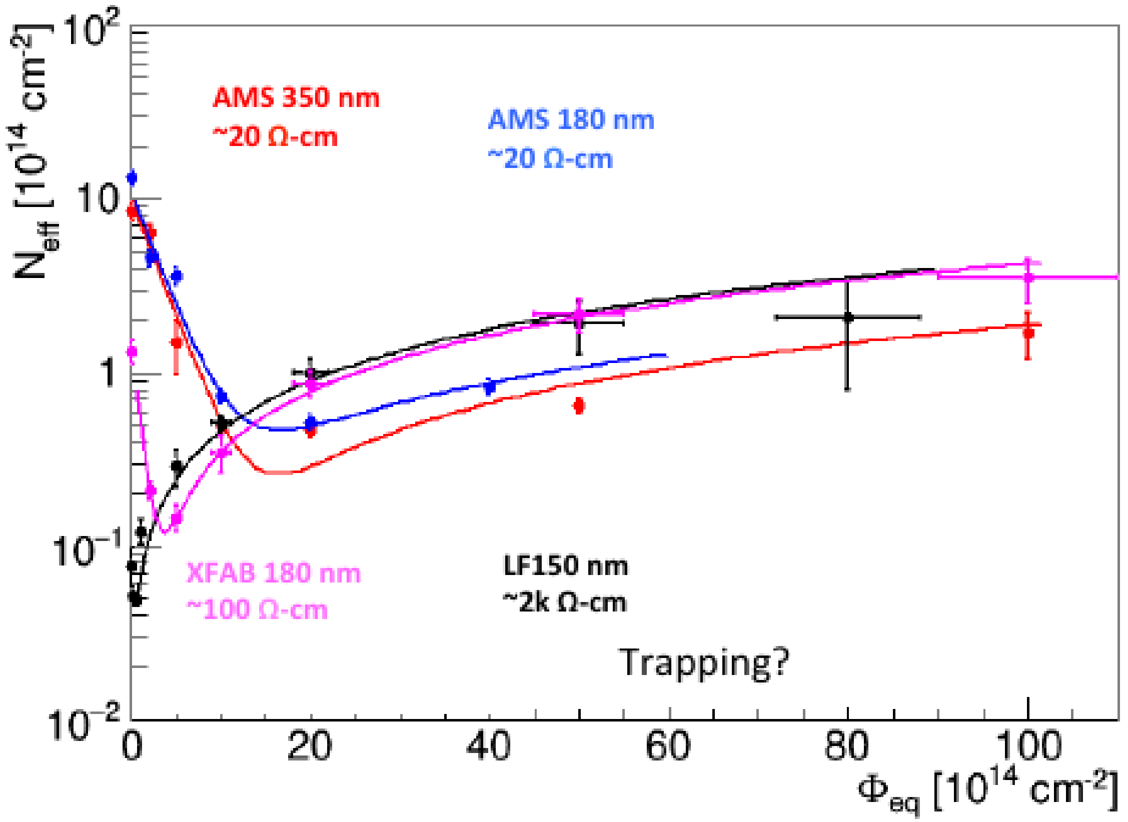
Summary

- Huge momentum for a monolithic solution for ATLAS ITk
- Extensive characterization of CCPD prototypes
  - Irradiation up to 1Grad and 10^{16} n_{eq}/cm^2
  - Efficiency in testbeam experiments: >99%
  - Constant improvements to hit timing
- Suitable candidate for outer pixel layers
  - Material budget, power consumption, production/assembly costs
  - Several prototypes in AMS, Lfoundry, TowerJazz technology in design and/or production
  - Several/novel read out and pixel schemes
  - Characterization till end of the year
- Common design early next year

Backup

Substrates after irradiation

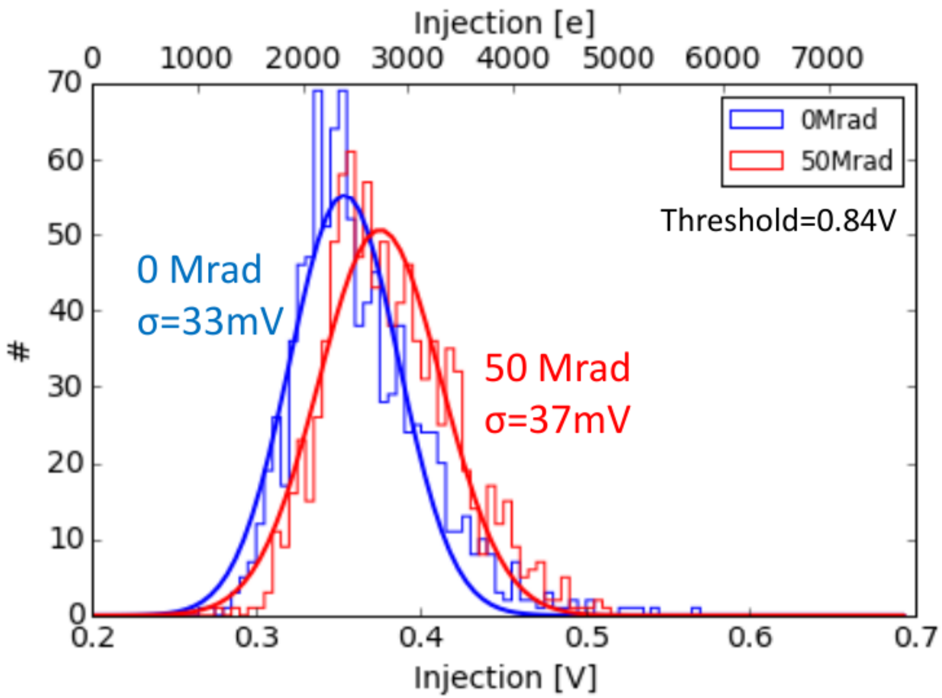
- Behaviour similar after 10^{15} n_{eq}/cm^2
- Dip around $2x10^{14}$ n_{eq}/cm^2 for low resistivity substrates has to be accounted for in electronics

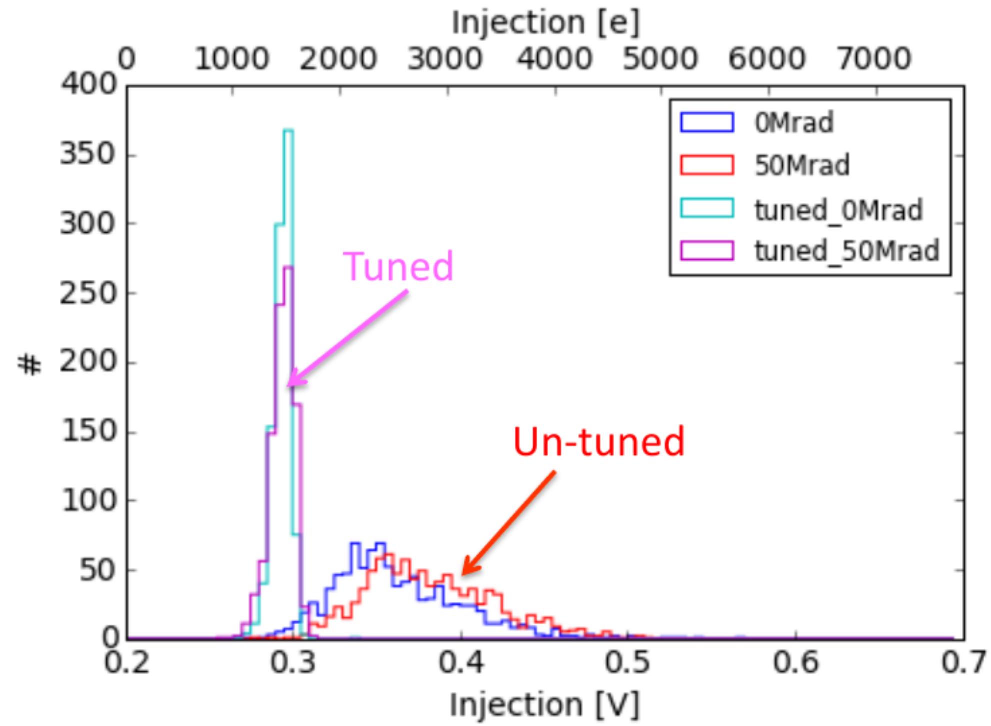


Igor Mandić, Jožef Stefan Institute, Ljubljana Slovenia
11th "Trento" Workshop, February, Paris, 2016

LF-CPIX Threshold Behaviour

- Sensor remains well tunable with similar noise behaviour after 50Mrad





T. Hirono, AUW2017, CERN

TowerJazz Investigator Readout