Development of Trigger and Readout Electronics for the ATLAS New Small Wheel Detector Upgrade

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on behalf of
the ATLAS Muon Collaboration

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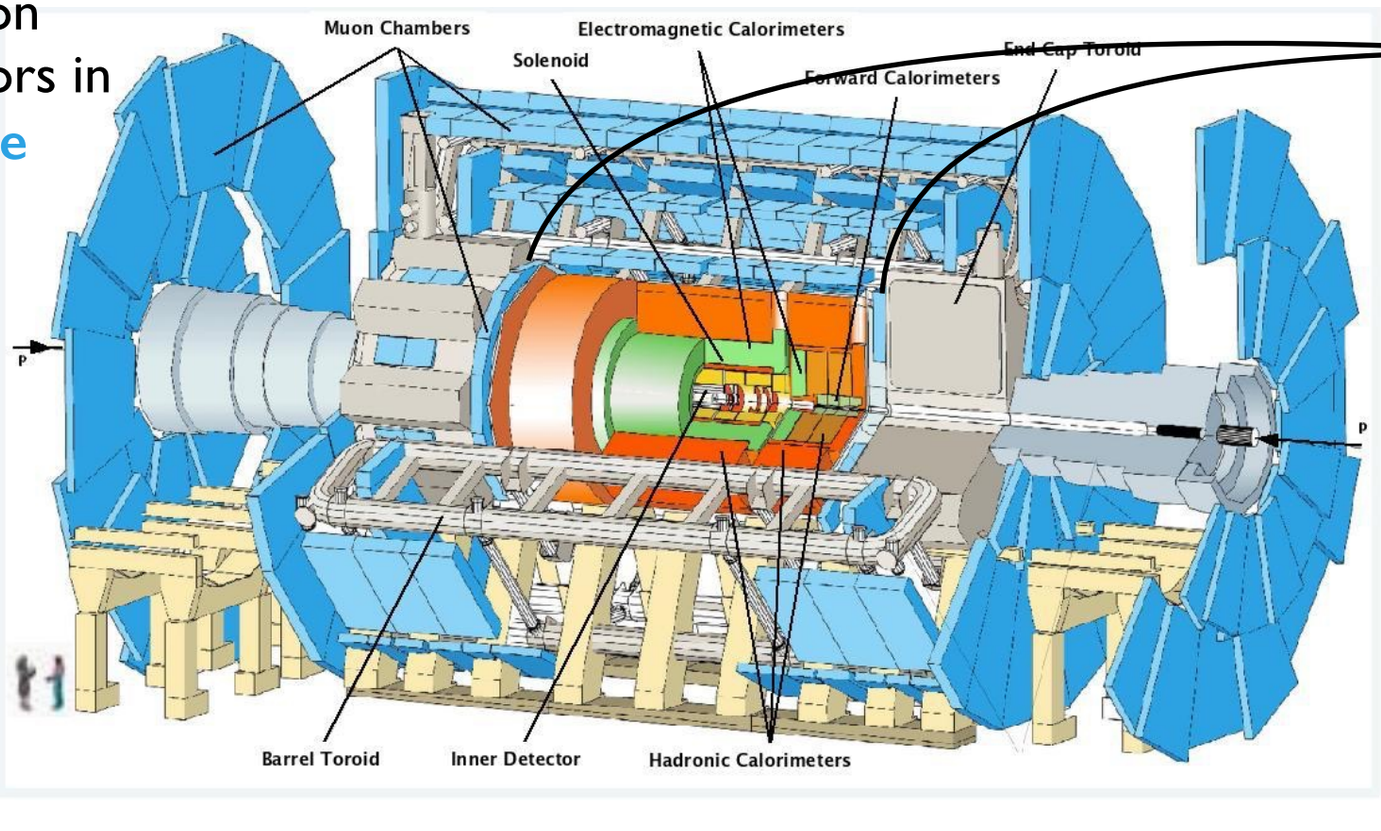
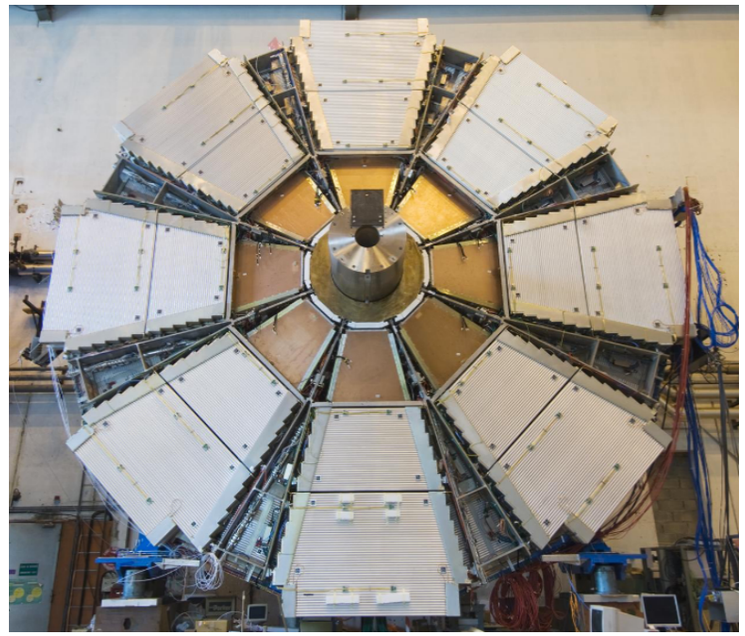
Outline

- Introduction to the New Small Wheel (**NSW**)
  - What does it address?
  - What is it?
- NSW data paths and their electronics
  - Precision data
  - Trigger data
- What we have achieved so far
  - Integration efforts
  - On-going & current tests

Introduction — Why the NSW?

muon detectors in **blue**





~10 meters

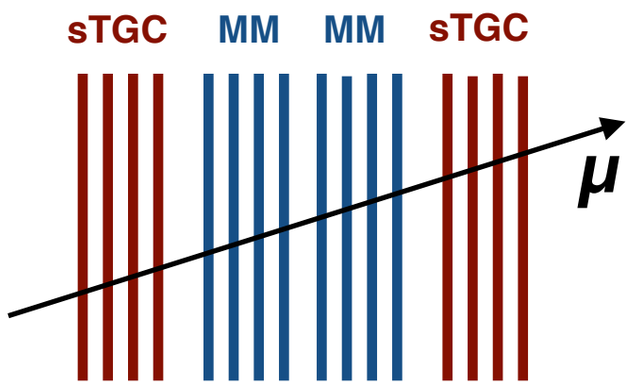
current "Small Wheels" (**SW**) of the ATLAS detector

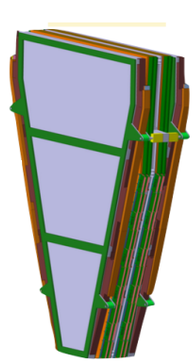
- In **2021** LHC reaches design energy 14 TeV and increases collision intensity $\mathcal{L}$=2x10^{34}/cm^2/s, giving 55-80 interactions per *p-p* bunch collision
- In **2027** LHC moves to High Luminosity LHC (HL-LHC) phase and increases collision intensity to $\mathcal{L}$=5-7x10^{34}/cm^2/s, giving **140-200 interactions per *p-p* bunch collision**
- Neither the current SW *detectors* nor *electronics* will be able to cope with the changes

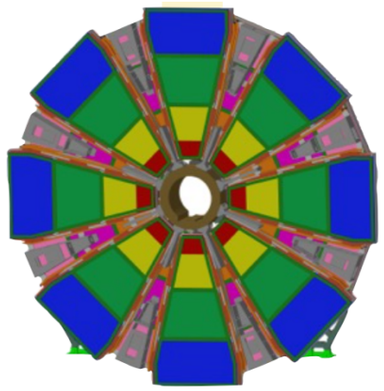
➡ In 2019 the NSW will replace the current SW so that ATLAS will be able to maintain its **low p_T thresholds** for single muons and its excellent **tracking capabilities** throughout the HL-LHC regime

Introduction — What is the NSW?

- Two, *new* gaseous detector technologies:
  1. Resistive-strip Micro Mesh Gaseous Structure (MicroMegas, **MM**)
  2. Small-strip Thin Gap Chambers (**sTGC**)







~10 meters

system redundancy ensures efficient running over the next ~20 years, while having very limited access!

Both provide muon **triggering and precision tracking**

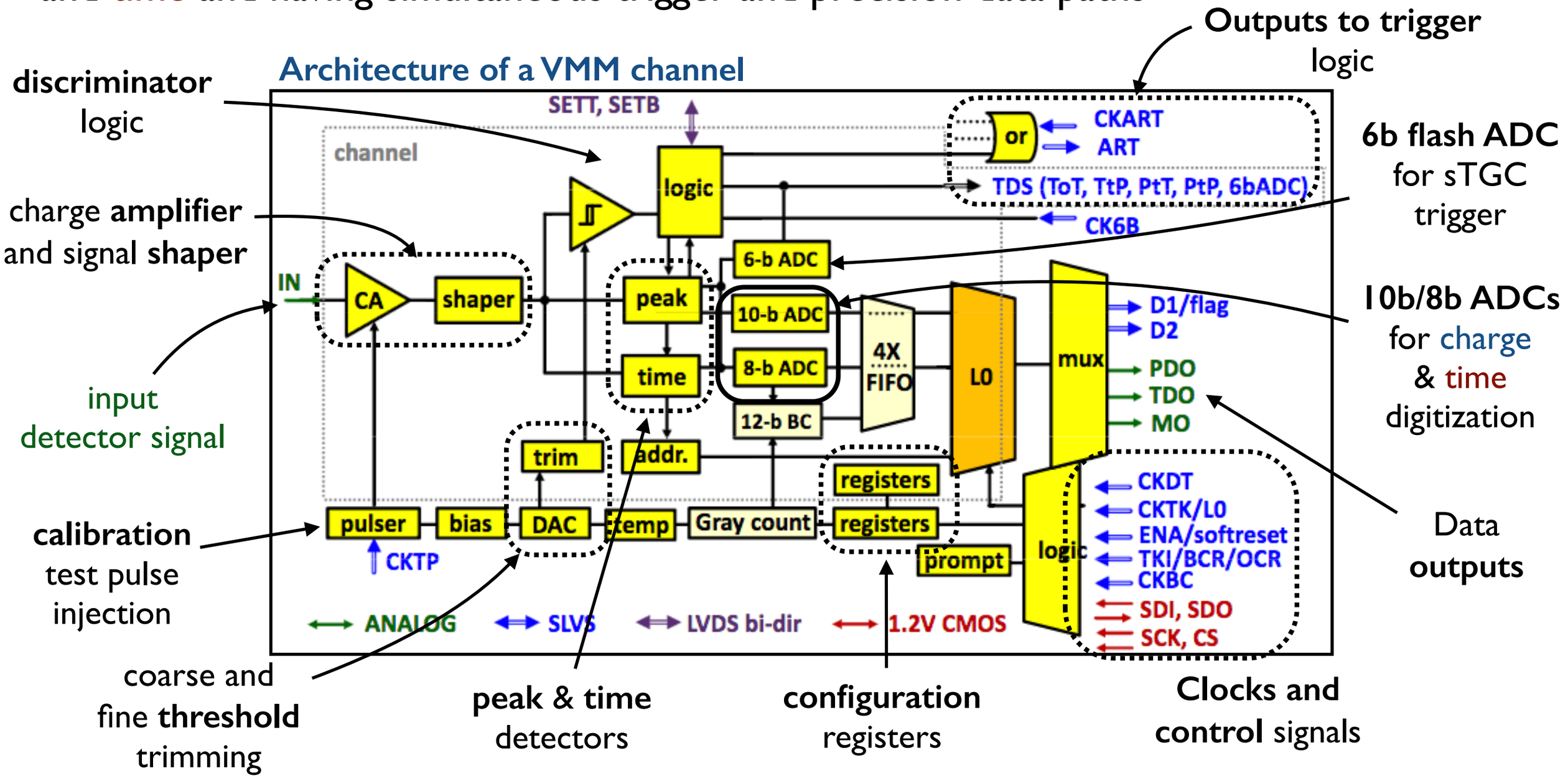
Each have **independent trigger and data paths**

- A 4-ASIC family has been developed for the NSW:
  1. **VMM**: front-end chip for MM and sTGC, precision data collection and fast trigger data signals
  2. **ROC**: "**R**eadout **c**ontroller", buffering and aggregating of precision data from VMM
  3. **TDS**: "**T**rigger **D**ata **S**erializer", prepares sTGC trigger data
  4. **ART**: "**A**ddress in **R**eal **T**ime" ASIC, prepares MM trigger data

➡ The fast NSW front-end electronics will achieve the **1MHz readout rate** required for the LHC upgrades while maintaining excellent muon triggering & reconstruction

VMM ASIC

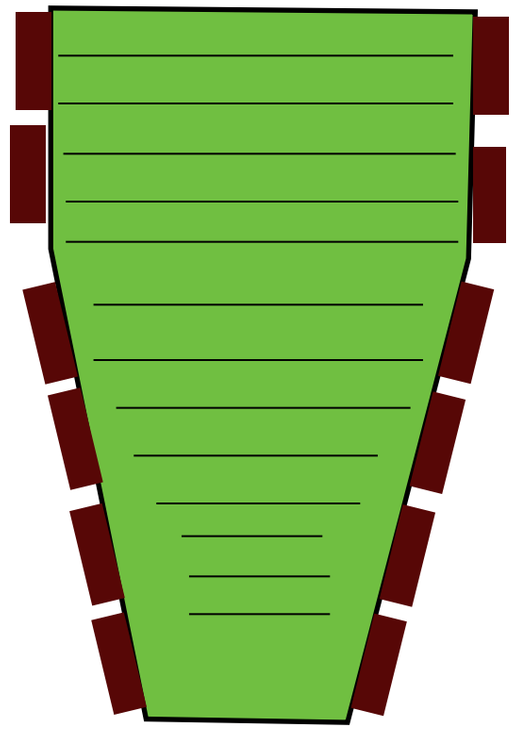
- The VMM is the central front-end digital ASIC of the NSW **used on both sTGC and MM**
- **64-channels** interface directly with the detectors' signaling elements, measuring charge and time and having simultaneous trigger and precision data paths

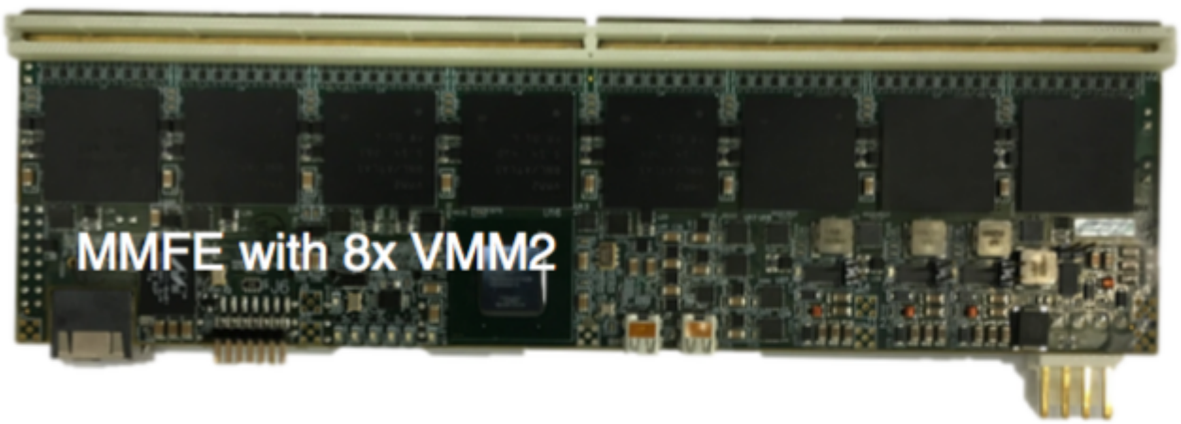


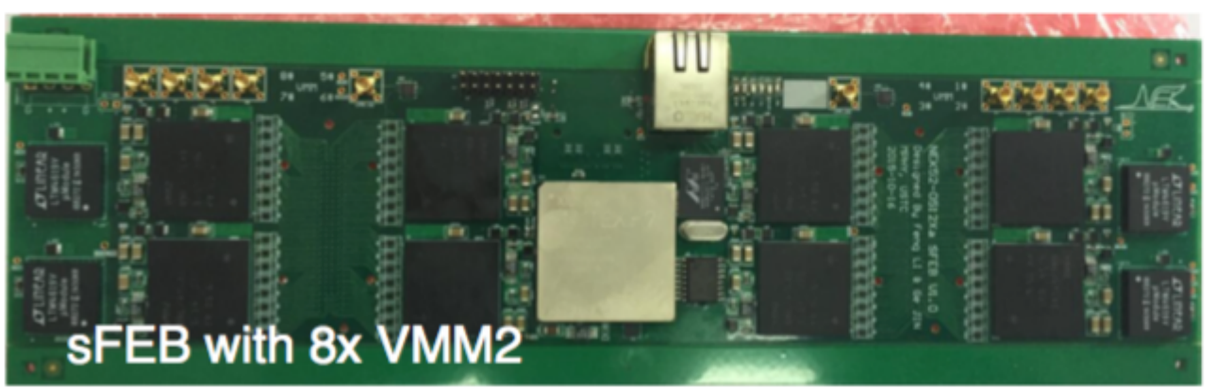
512 Mb/s (8b/10b) output capability, giving a max **5MHz hit rate per channel**

NSW Readout

- **MM**
  - ~2M readout channels
  - VMMs housed on front-end board (FEB) MMFE8
- **sTGC**
  - ~350k readout channels
  - VMMs housed on sFEB (“strips”) and pFEB (“pads” & wires)
- FEBs are on the edges of the detectors
- ~5-6000 total FEBs on the NSW (4096 MMFE8, 768 s/pFEB)

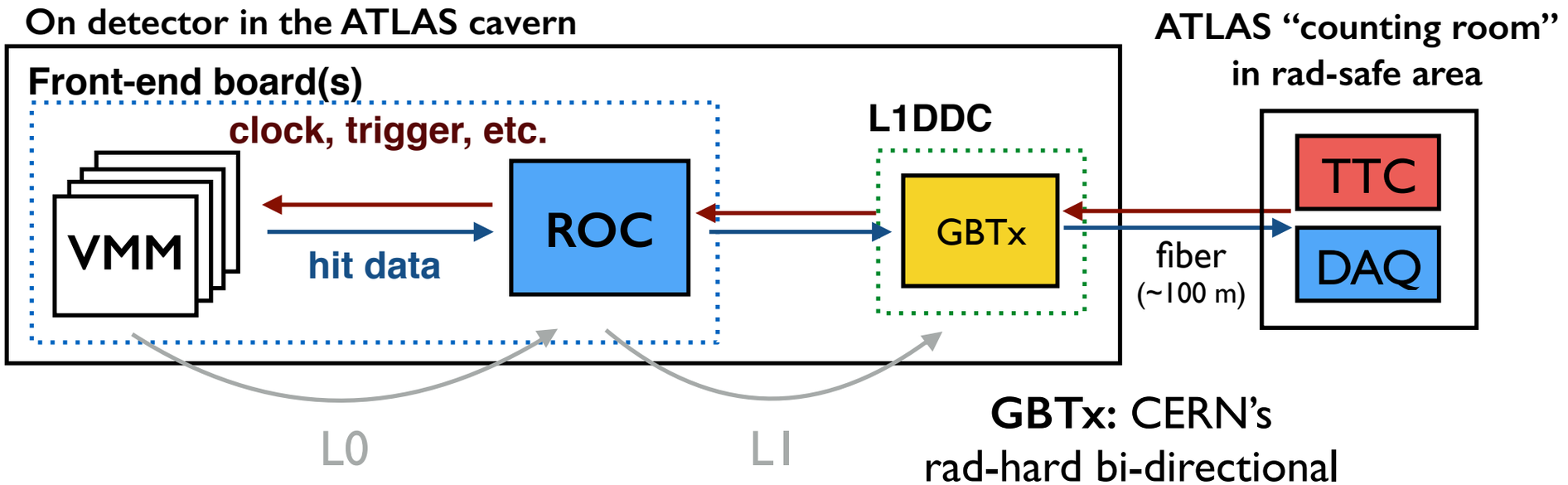






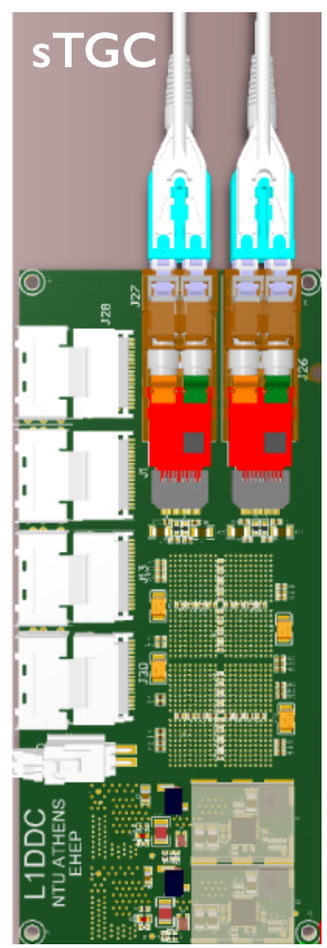
NSW Readout

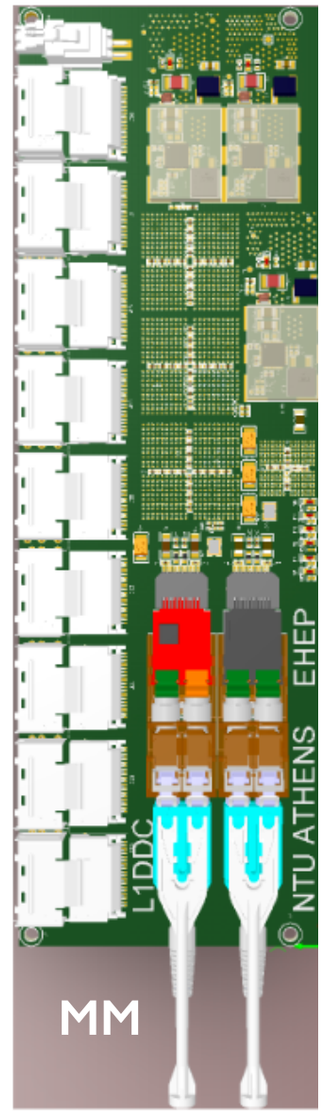
- Timing, trigger, & control (TTC) signals are distributed by the ATLAS **TDAQ** network and propagated via optical fiber to the L1DCC ("**L**evel **1** **D**ata **D**river **C**ard")
- The L1DDC distributes TTC to the **ROC ASIC** on multiple front-end boards, which distributes the TTC to multiple VMMs
- Upon a trigger VMMs sends event data to the ROC which buffers and tags the data with the trigger information
- ROC sends this data to the L1DDC, which sends this via optical fiber to the ATLAS DAQ network to be included in the full event reconstruction / HLT



GBTx: CERN's rad-hard bi-directional optical link (de)serializer ASIC

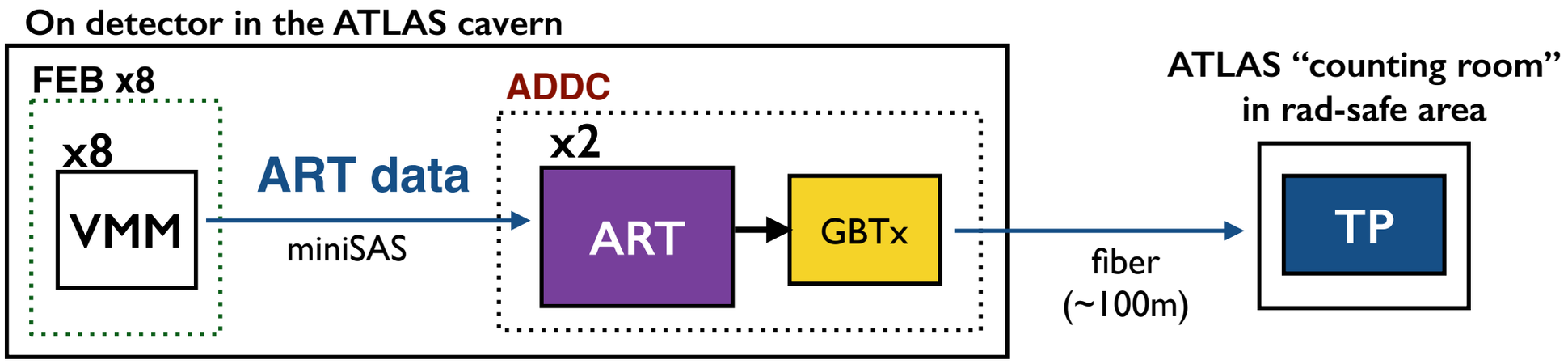
L1DDCs





NSW Trigger Paths — MicroMegas

- Fine strip granularity of MM (450*μm* strip pitch) allows the MM trigger to take an "**A**ddress in **R**eal **T**ime" (**ART**) approach:
  - Each VMM sends the address (channel #) of **only its first hit in each proton-proton collision** to an **ART ASIC** located on a so-called "**A**rt **D**ata **D**river **C**ard" (**ADDC**) located on-detector
    - Reduces data rate by a factor of 64
  - The ART ASIC chooses ***at most 8*** addresses from 32 VMMs to send to the MM Trigger Processor (**TP**)
- Reduces data rate by a factor of at least 4



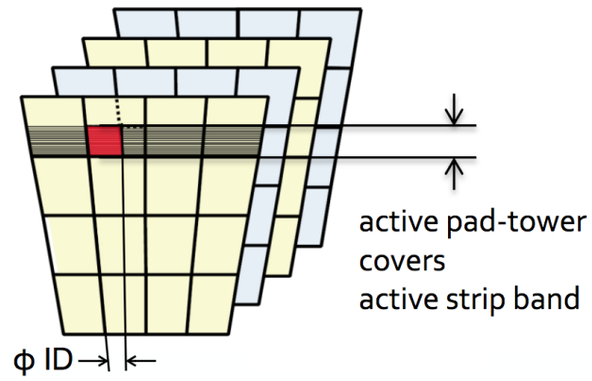
NSW Trigger Paths — sTGC

- sTGC trigger path follows two-steps

1. Pad coincidence

1.1. VMMs on sTGC pads (~1300 per layer) send fast signals to the **pad TDS** which forwards this to the **Pad Trigger**

1.2. Pad Trigger finds 3-of-4 layer coincidences between pads

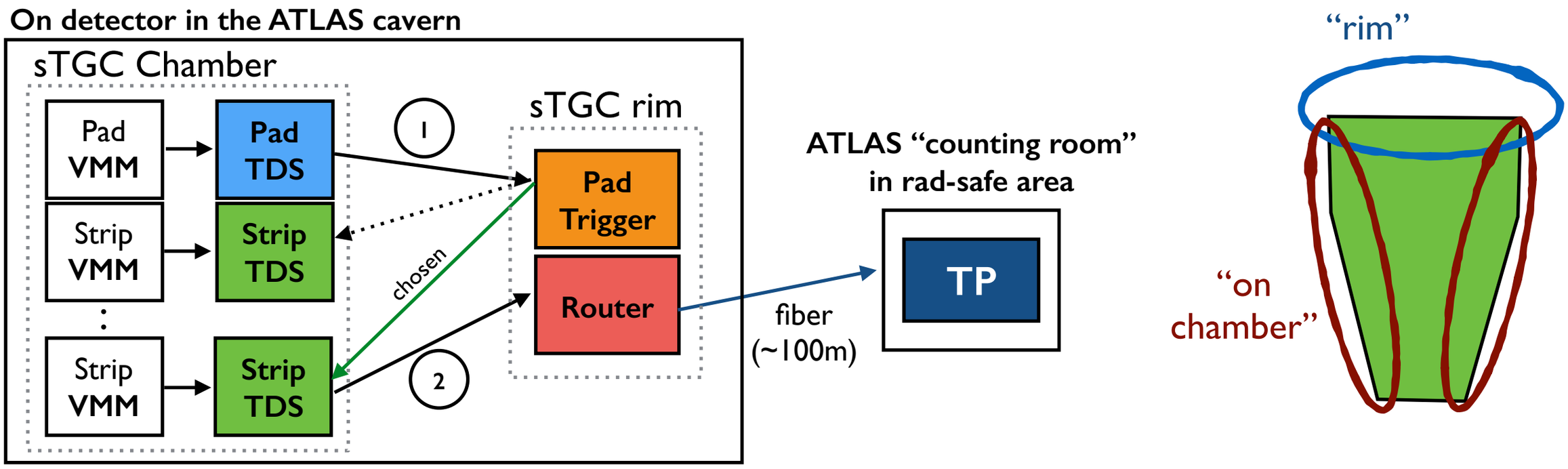


2. Selecting & Sending Strip Charges

2.1. **Strip TDS** collects fast strip charge data from VMM

2.2. Pad Trigger finds the strip TDS whose strips lie beneath the coincident pads

2.3. This strip TDS sends its *3-5* strip charges to the **Router** which forwards the data to the sTGC TP

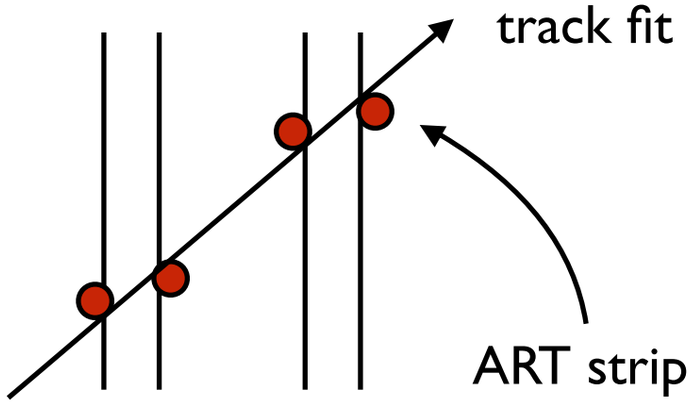


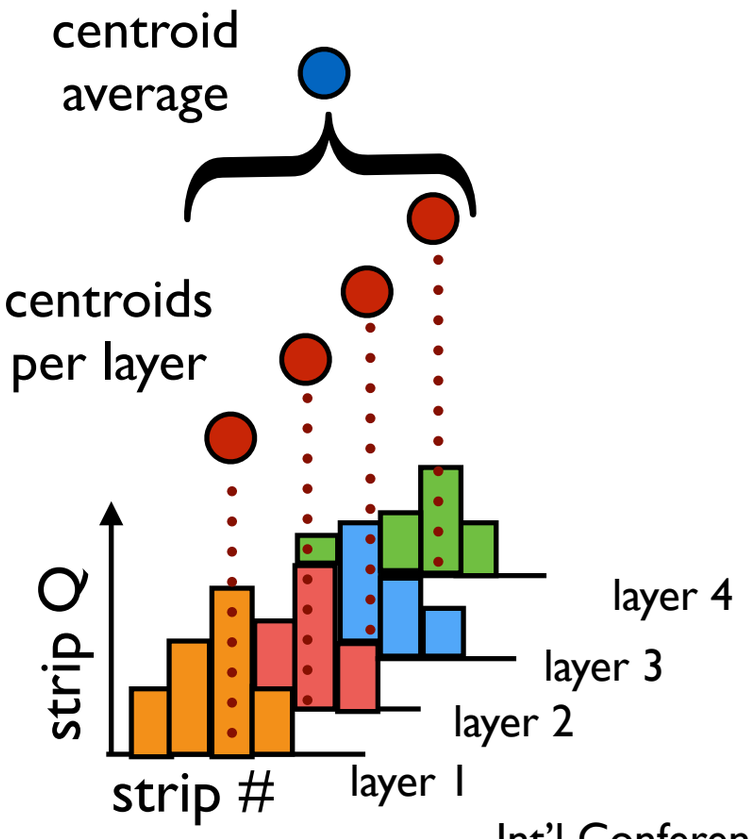
NSW Trigger Algorithm

Not only are the MM and sTGC trigger data *sent independently* to the TP but their *algorithms are run independently* on separate FPGAs

MM Algorithm

- FPGA deserializes the ART data (strip locations) to categorize each hit into a given slope (a projective line from the proton-proton interaction)
- Performs "track fit" across MM layers using these filtered-by-slope hits (*space points*)



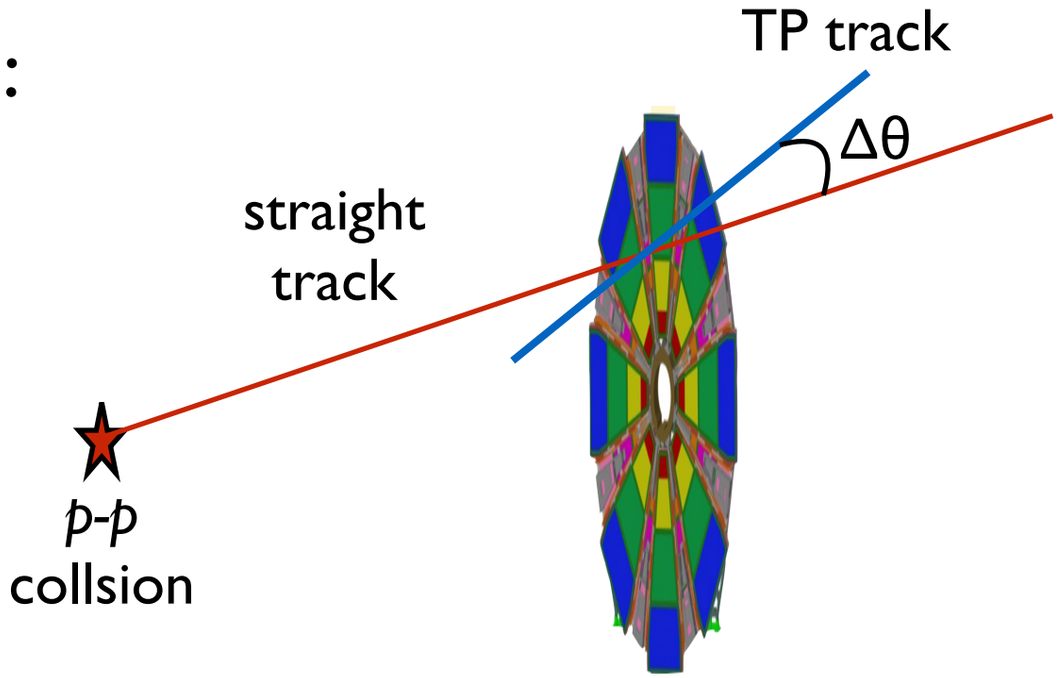


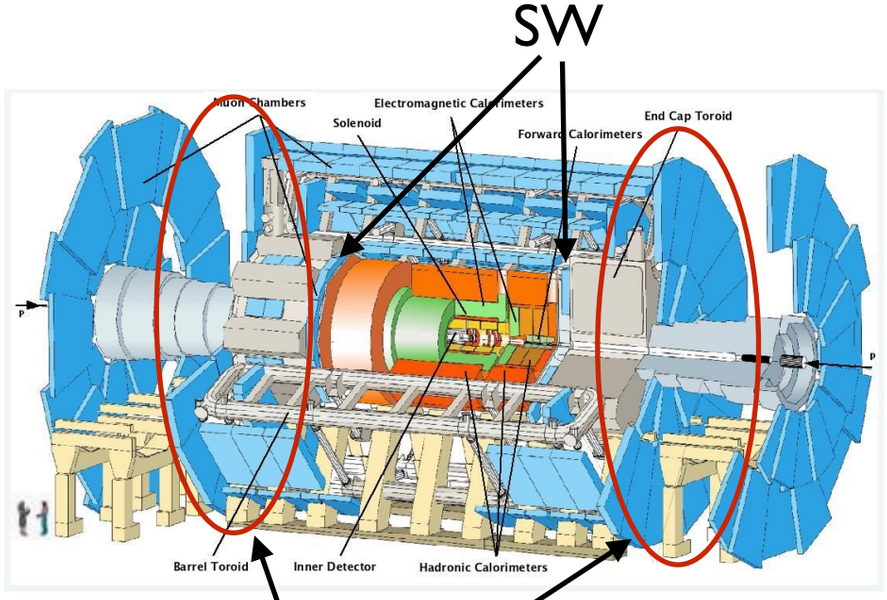
sTGC Algorithm

- FPGA uses strip charges to find centroid position (charge-weighted position) on each sTGC layer
- Averages centroids to make space points to perform "track fit" across sTGC

NSW Trigger Algorithm

- MM & sTGC track segments are merged:
  - Remove common segments to avoid duplicate triggers
  - Impose quality criteria on segments
  - **Calculate Δθ of the segment w.r.t. to straight-line-track from *p-p* collision**



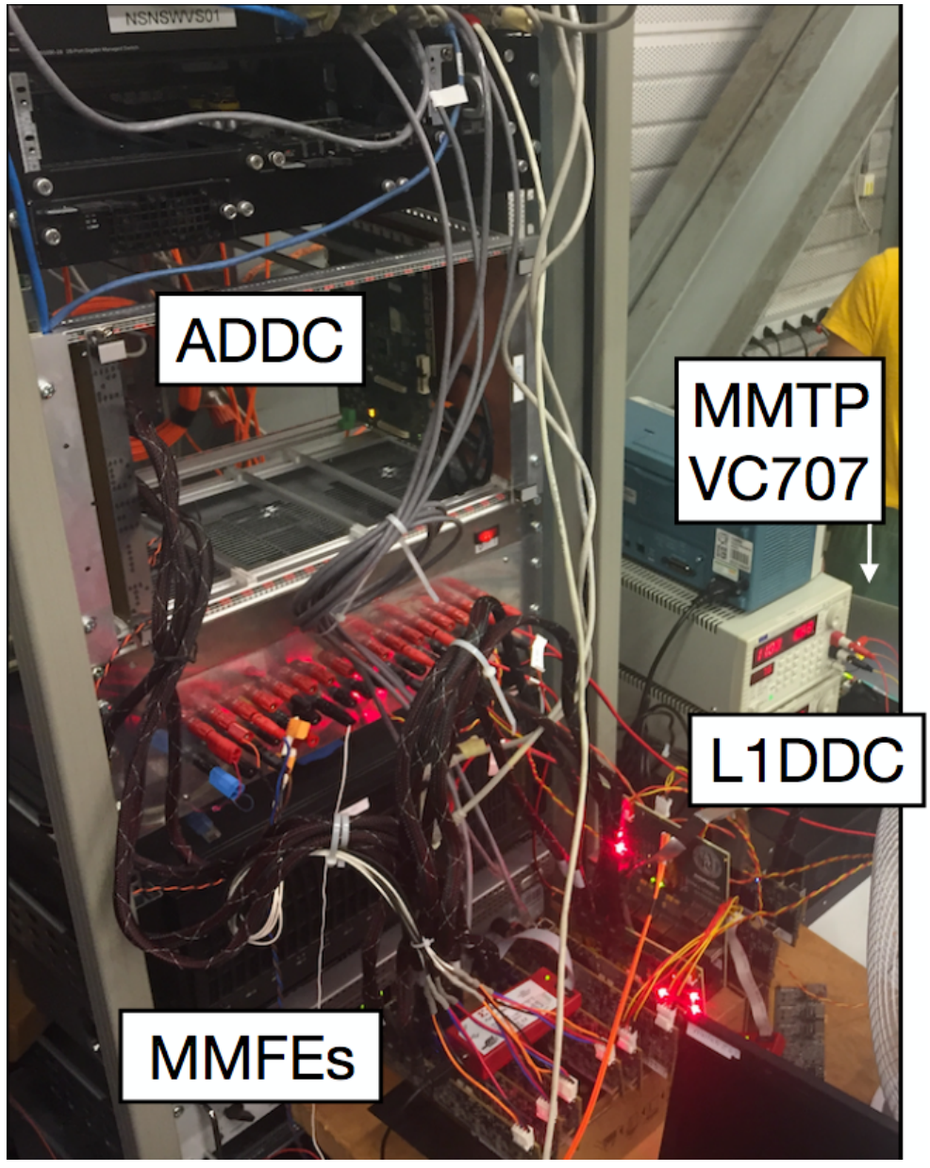


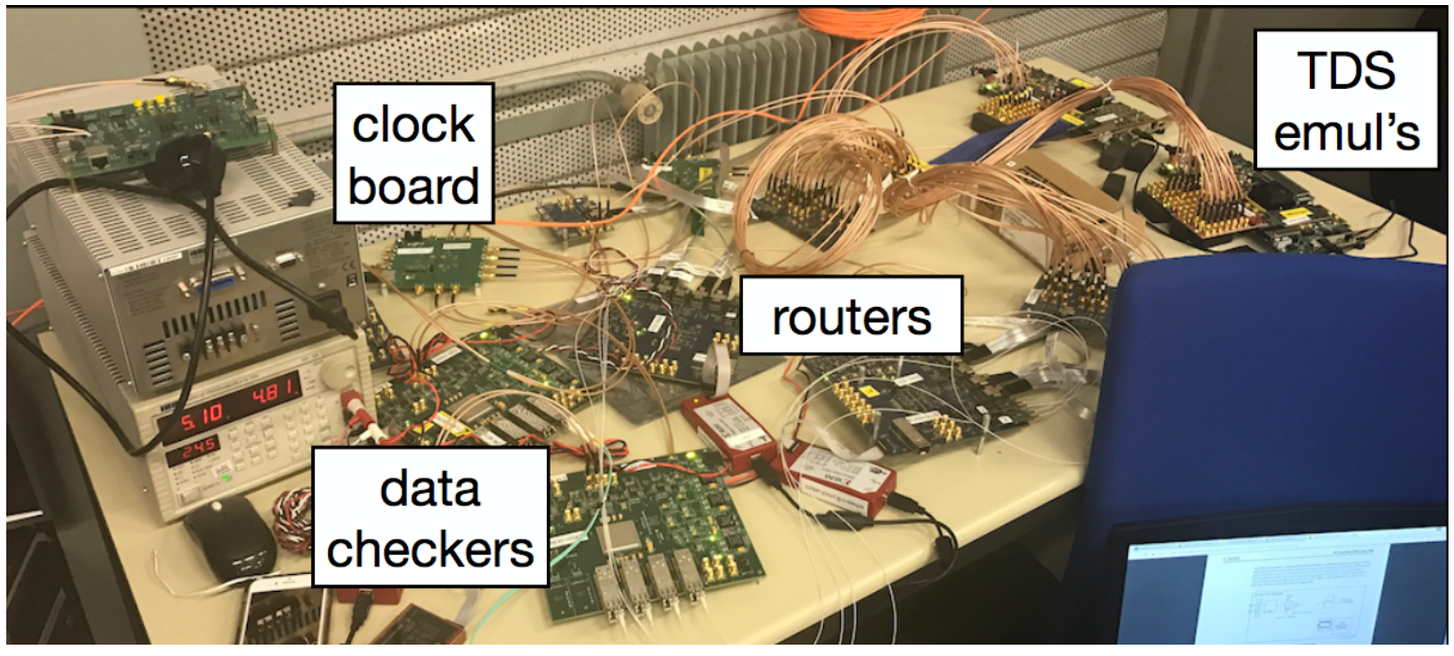
confirm trigger candidates in "Big Wheels"

- These muon candidates are sent to the Big Wheel Sector Logic to confirm muon candidates found there
- 1016 ns latency from initial *p-p* collision to NSW TP sending out the segments (35% due to transit time in optical fiber)

Integration and Status

- We are converging on having electronics data & trigger paths ready for NSW installation in 2019
- Periodic "Integrations" to put together and test the full trigger and readout chain
- Most recent Integration:
  - Successful test of MM trigger path, with fake tracks "fitted" by the MM TP firmware
  - LHC clock successfully propagated from ATLAS TTC system to the L1DDC to the FEB with VMMs
- Sending of TDS trigger data to the sTGC Router board

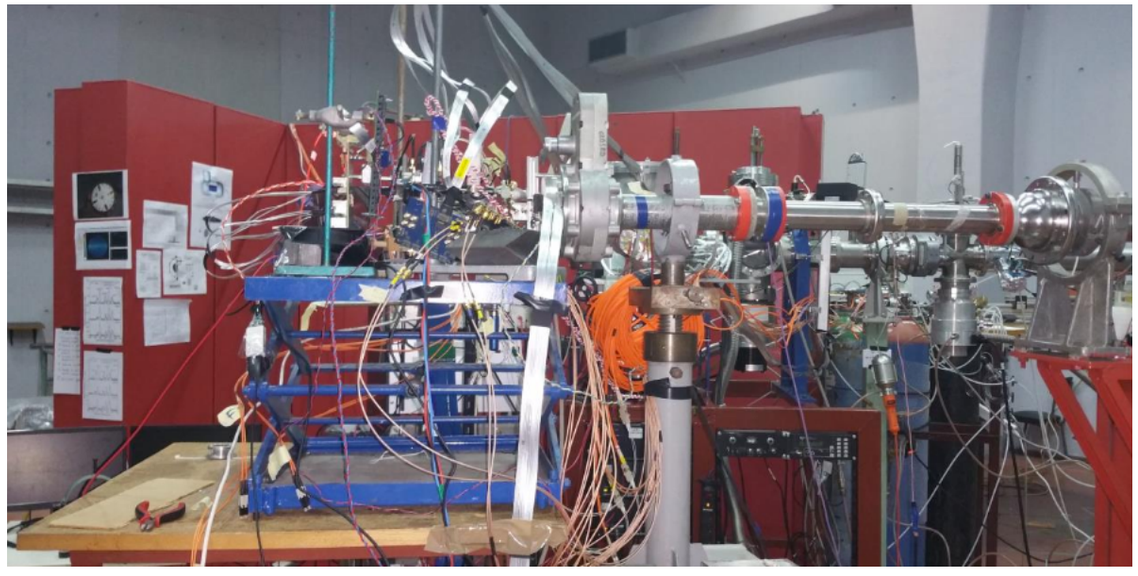




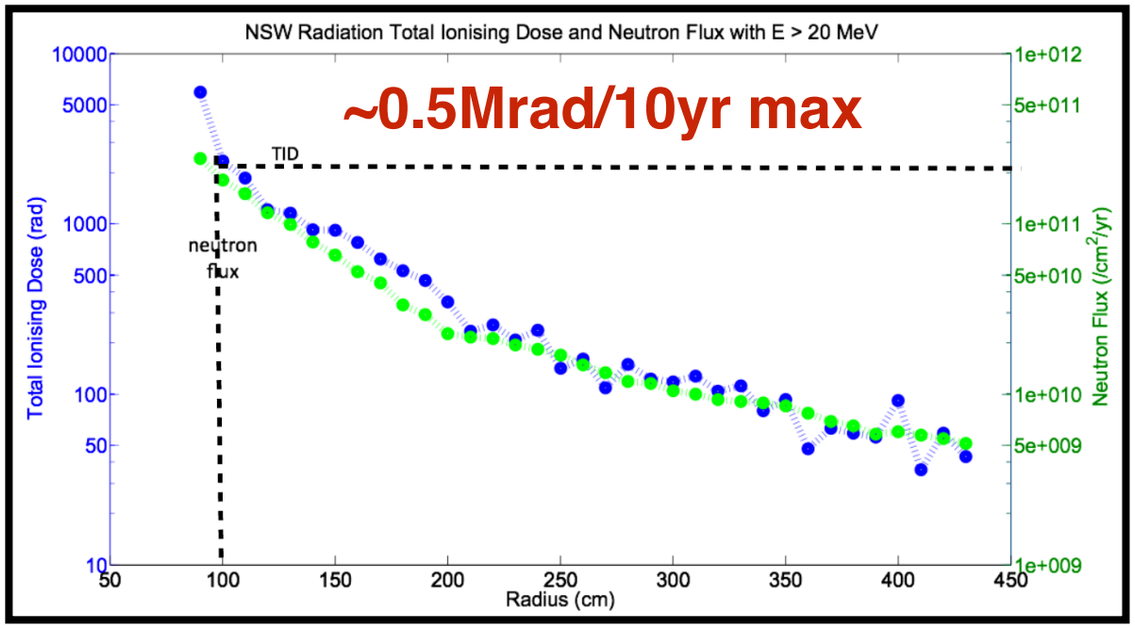
We are getting ready for the next Integration period in July!

Integration and Status

- Final review to qualify NSW ASICs for mass production and use in ATLAS is in progress
  - Recently performed 1week irradiation of the FEE in a neutron beam facility in Athens to test SEU robustness
  - VMM, ART, ADDC, L1DDC saw no configuration or data corruption with *n* fluxes reaching those of ATLAS' yearly flux at the inner radius (nearest the beam pipe)



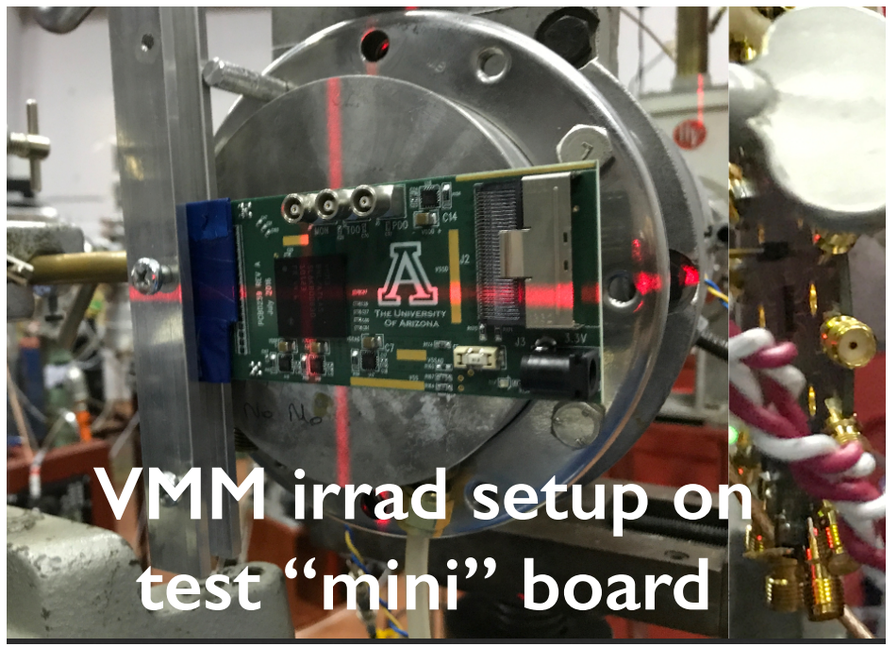
20 & 24 MeV neutrons



ART ~7e11

VMM ~2e11
ADDC ~7e10

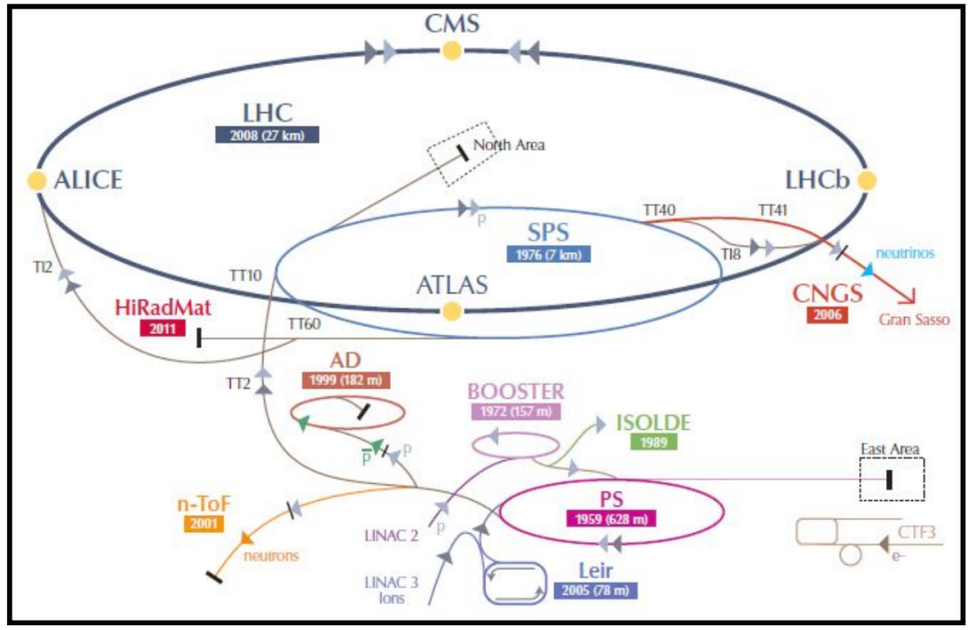
L1DDC ~6e9



The plan is for all ASICs to go into production later this summer

Integration and Status

- The next few weeks we will be holding a test beam campaign in CERN's North Area of the SPS
- **Goals:**
  - Test external triggering & readout of latest version of VMM in the high intensity environment
  - Measure VMM timing resolution on-detector
    - **μTPC mode of MM**
  - Charge measurements of sTGC
    - **Tail attenuation** of large Q sTGC signals
  - Validation of FEB on **large scale modules**



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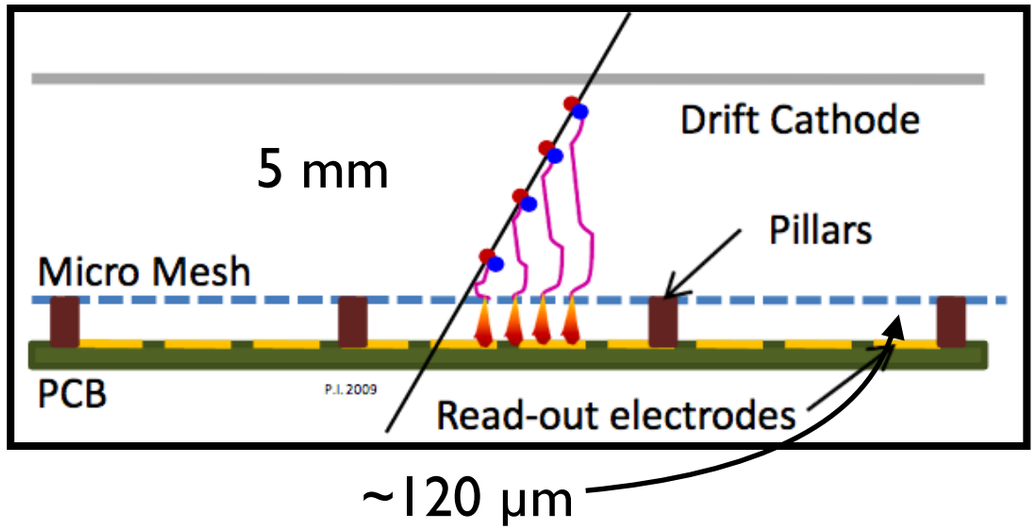

Conclusion

- Introduced the New Small Wheel Upgrade of the ATLAS experiment at CERN
- Outlined the front end electronics that will enable the NSW DAQ and trigger paths to operate efficiently at a readout rate of 1MHz
  - Detailed the family of custom ASICs and front-end boards
  - Illustrated NSW readout, trigger paths & algorithms
- Briefly outlined NSW electronics' current and on-going tests and integration efforts

We are progressing well and will continue to ramp up as the full ASIC production and testing begins this summer!

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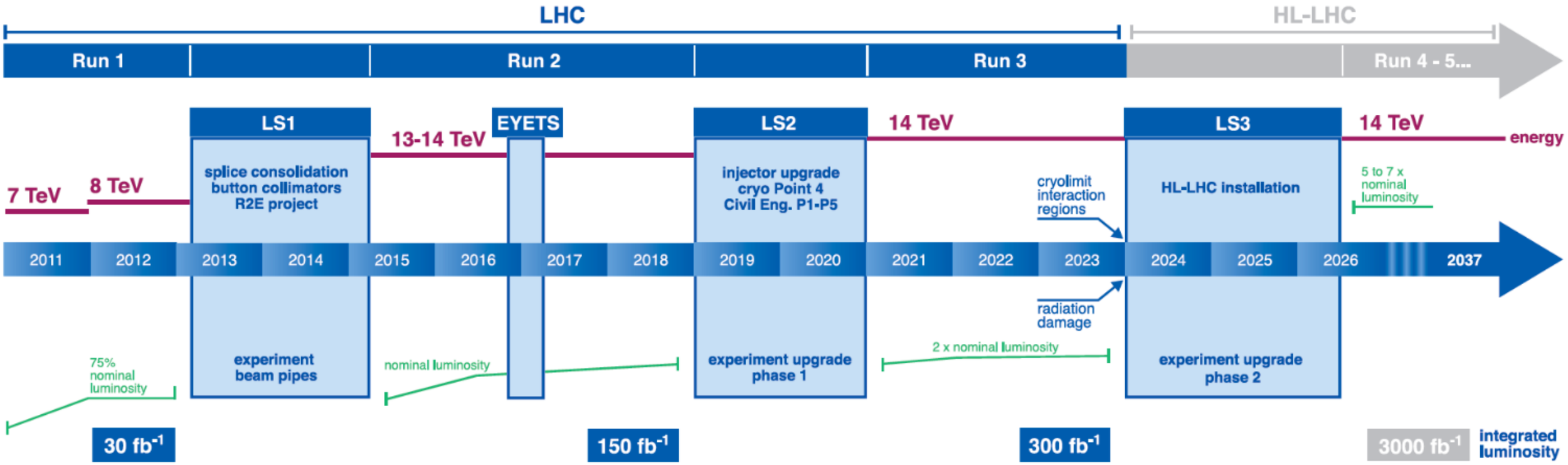
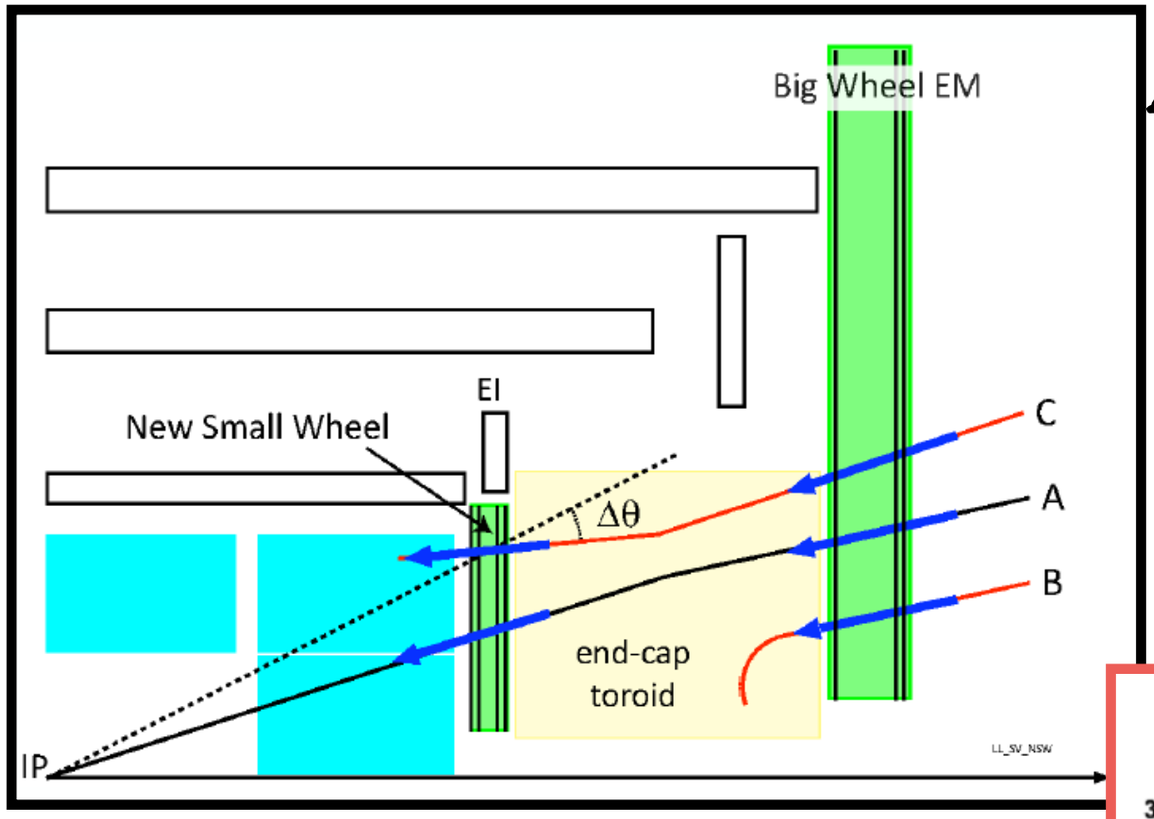
Thank You!

additional

LHC & Upgrade Timeline

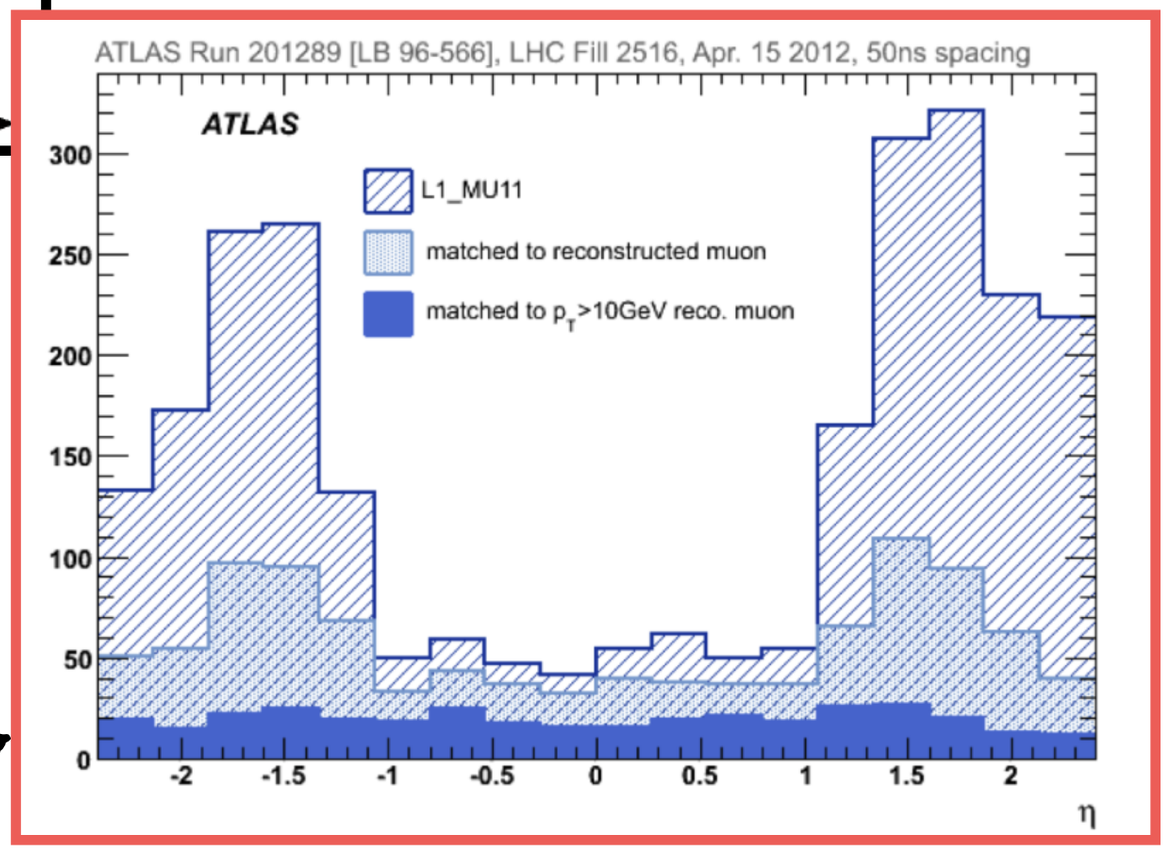


Trigger Concept



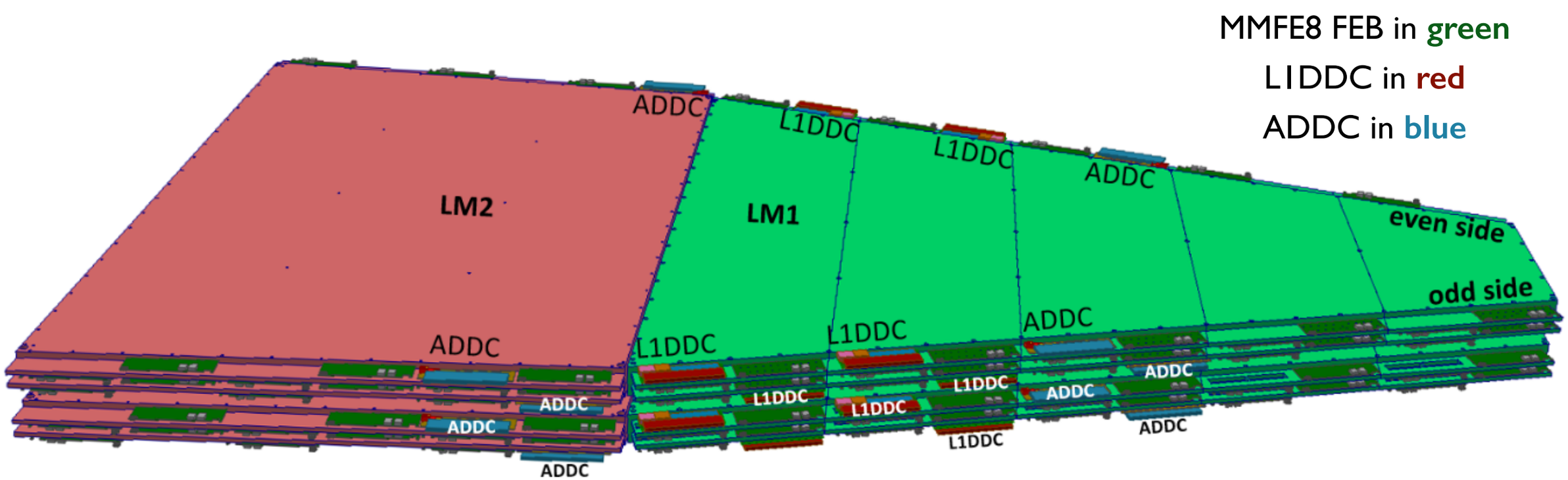
should only trigger on track "**A**"

majority of muon L1 trigger bandwidth due to *fake* muons in the end-cap region with current SW

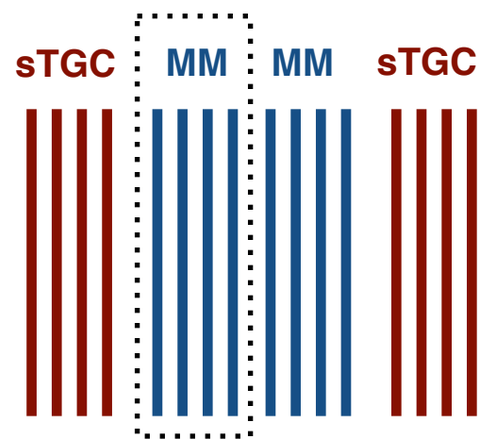


What it Looks Like

Now that we have detailed the front-end electronics, here is an example of 4-layers (a *quadruplet*) of MM with the front end boards for readout and trigger along the edges of the detector



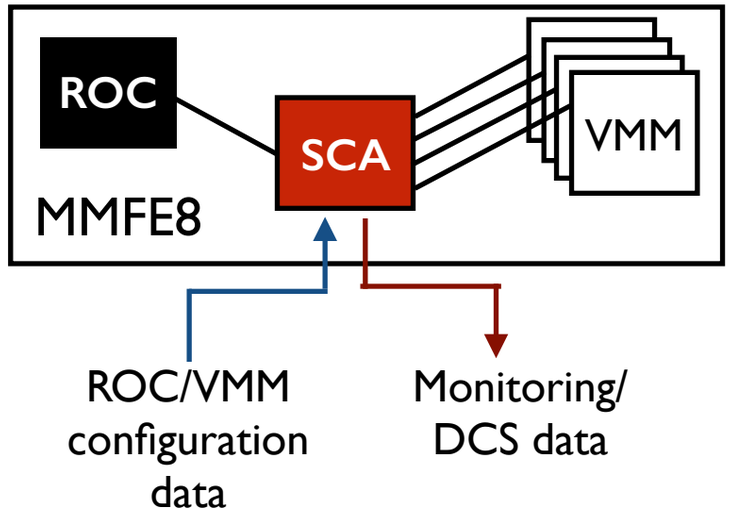
L1DDC & ADDC placed centrally to equalize the cable length (cables not shown)



Configuring and Monitoring the FE Electronics

The front-end boards (MMFE8, s/pFEB, L1DDC) are also host to the so-called Slow Control Adapter ASIC (**SCA**)*

The SCA is responsible for receiving and propagating **configuration** commands to the ASICs on each of the front-end boards, e.g. sending the VMM configuration



The SCA also samples ADCs and various sensors on the FEBs for **monitoring** and detector-control purposes

*Non-NSW specific, developed by ATLAS detector controls group