First Prototype of the Muon Frontend Control Electronics for the LHCb Upgrade: Hardware Realization and Test

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Abstract. The muon detector plays a key role in the trigger of the LHCb experiment at CERN. The upgrade of its electronics is required in order to be compliant with the new 40 MHz readout system, designed to cope with future LHC runs between five and ten times the initial design luminosity. The framework of the Service Board System upgrade aims to replace the system in charge of monitoring and tuning the 120'000 readout channels of the muon chambers. The aim is to provide a more reliable, flexible and fast means of control migrating from the actual distributed local control to a centralized architecture based on a custom high-speed serial link and a remote software controller. In this paper, we present in details the new Service Board System hardware prototypes from the initial architectural description to board connections, highlighting the main functionalities of the designed devices with preliminary test results.

Keywords: LHCb, muon, Service Board System, upgrade

1 Background of the System upgrade

1.1 LHCb upgrade

In the future, the performances of the Large Hadron Collider at the European Center for Nuclear Research will increase in terms of luminosity and energy produced by the particle collisions compared to the initial design parameters. This requires an upgrade of many crucial parts of the experiments. The LHCb readout electronics has been completely redesigned [1] to cope with the new values. It is vital that all the Front-End (FE) and the Back-End (BE) systems in the sub-detectors comply with a common set of specifications related to the new readout scheme and control [2] based on the GBT-link [3].

1.2 Muon Detector upgrade

The LHCb muon On-Detector electronics is based on the CARDIAC boards that host one DIALOG [4] and two CARIOCA [5] chips. At the moment the control and monitor system of this electronics, the so-called Service Board System (SBS), bases on a local

network of microcontrollers that independently communicate with a central supervisor [6]. To comply with the new common LHCb read out architecture this infrastructure was redesigned at system level while the On-Detector electronics was left unchanged. Taking advantages of the high-speed serial link specifically designed for application under radiation, a centralized remote server has the whole control of the CARDIAC chipset. This significantly increases the flexibility and reliability of the system as well as the communication speed. The integration of the GBT link in the actual Service Board facility, next to the muon stations, requires the new Service Board System (nSBS) architecture [7] hardware development. This paper presents the new Pulse Distribution Module (nPDM), the new Service Board (nSB) and the new Custom Backplane (nCB) first prototypes release (rev.01), focusing on the most important sections of the design process with additional early test results.

2 Hardware Design Description

2.1 Interfacing the ECS serial streams

A core item of the design (see a quick system overview in **Errore. L'origine riferimento non è stata trovata.**) is the interface between the GBT-SCA [7] chip and the custom bidirectional serial link of the DIALOG slow control. The entire proposed implementation relies on this section. This link comply with standard I2C-Bus protocol at electrical level, thus the I2C-Bus peripheral of the GBT-SCA drives the channel. A custom translator, which resides in the nSB on-board FPGA, merges the protocols at physical layer. The FPGA also generates the pulses used by the DIALOG chips for other tuning purposes. Thus, using an FPGA provides a solution for both control and communication of the muon On-Detector electronics, compliant with the novel LHCb Read-Out architecture. A Finite-State-Machine translates and map the I2C data frame in to the custom bi-direction serial link. This link uses LVDS standard at the physical layer, thus integrated multi-standard differential drivers are preferred. The Microsemi IGLOO2®, a flash based FPGA built on 65 nm process that gives extremely comfortable performance in radiation environment [7], provides different resources that satisfies the needs. It incorporates also M-LVDS drivers, used to fan out of Timing and Fast Controls (TFC) signals delivered by the nPDM to the whole crate, excluding the need of additional components in the design and installed on the boards.

On nPDM, the GBTx extracts TFC signals from the high-speed optical link. The IGLOO2 on the nPDM generates the signals used by the FPGA(s) on the nSB(s) to produce the dedicated pulses used during tuning of the different readout channels. Due to the aim of the information carried by these signals all the traces are routed with phase control constraints in order to minimize the skew, on both the nPDM and the nSB. The realized wiring satisfies the requirements given in [7] adding as well a certain grade of flexibility to reduce the complexity of the required logic.

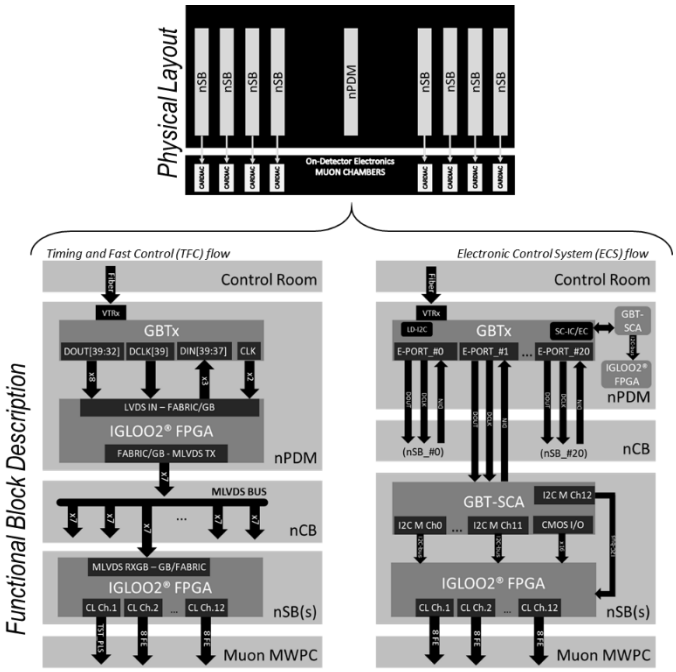

Fig. 1. Quick Physical and Functional overview of the new Service Board System.

2.2 E-link distribution

The use of the SLVS standard at physical level of the e-link [7] requires the study of compatibility of e-port with standard LVDS transceivers present on the IGLOO2. We proved that the communication works but we do not have any information regarding the degradation of the noise margin and the Bit Error Rate. A full characterization might be advantageous in the future and it is in the purpose of the prototype realization.

The distribution of the GBT link across the new Service Board Crate required as well the design of a new Custom Backplane (nCB). In order to save the mechanical infrastructure and to reduce the time required to replace the components during the commissioning step, the mechanical design bases on the VME standard reference. Through the backplane routes 20 serial e-link from the GBTx to the GBT-SCA [7] on the nSB boards. Three differential pairs compose them, allowing a synchronous point-to-point full-duplex communication between the two devices. In this configuration, it carries slow control information (ECS path). Specific special timing-driven constraints drives the routing of these lanes, in order to keep a low skew between data output and clock. This is vital for proper operation of the e-link driver on the GBT-SCA.

2.3 Additional features

Due to the particular application, the design includes special hardware recovery functionalities. A back-up I2C-Bus equips the nSBS crate. It connects all the boards and can be used in case of e-link failure (e.g. GBT-SCA malfunctioning). This provides redundancy to the crate control link. Soft and hard reset are predisposed for all the chips allowing different grade of recovery from critical situations. In addition, the logic is able to cut one single power rail at time, performing delimited power cycles. The access to the reset and power cycle functionalities can be either local or remote (i.e. either another board or the server can send the recovery command). This can be useful in case the primary power cycle link do not respond.

3 Early test results

3.1 I2C-Bus bridge

A very first release of the I2C protocol converter (the I2C-Bus bridge) implemented in the prototype of the nSB and on a preliminary evaluation set up proved the possibility to establish a stable communication between the muon On-Detector electronics and a commercial I2C driver (see **Fig. 2**). Repeating the same test at CERN on the muon detector, established a successful continuous communication for more than 13 hours, exchanging about 1,2GB of data with zero errors. This is equal to 480 write and read operation on all the 160'000 configurable registers of the system. Finally, additional test proved that the communication is stable and successful as well using the GBT link and the GBT-SCA chip (at that moment available on their evaluation board only).

Fig. 2. Screenshot of two successful I2C transaction (W and R) between a commercial I2C driver (SCL/SDA) and the muon On-Detector Electronics custom serial link (SCNx/SDNx/SDBn).

This very early series of tests also demonstrate that the developed digital translator speeds-up the data exchange from the actual 100 kbps to 1 Mbps, reducing the access time to the DIALOG register by a factor of 10. These translators have separate FSM(s) that run independently and act On-The-Fly. Distributing the data load of one e-link on 12 drivers allows the GBT link to control all the serial channel of the new Service Board simultaneously.

3.2 SLVS serial channels

Characterizing Standard DIN 41612 connectors proved the possibility of use them with differential SLVS-400 (Scalable Low-Voltage Signaling) used at the physical layer of the e-link protocol. **Fig. 3** shows the eye-diagram taken at 80Mbps (a) and at 400Mbps (b). The test uses an evaluation trace of a length comparable with those present on the designed nCB board (with similar stack-up and PCB FR4 dielectric). The results shows no significant attenuation of the amplitude of the signal and acceptable level of jitter and distortion.

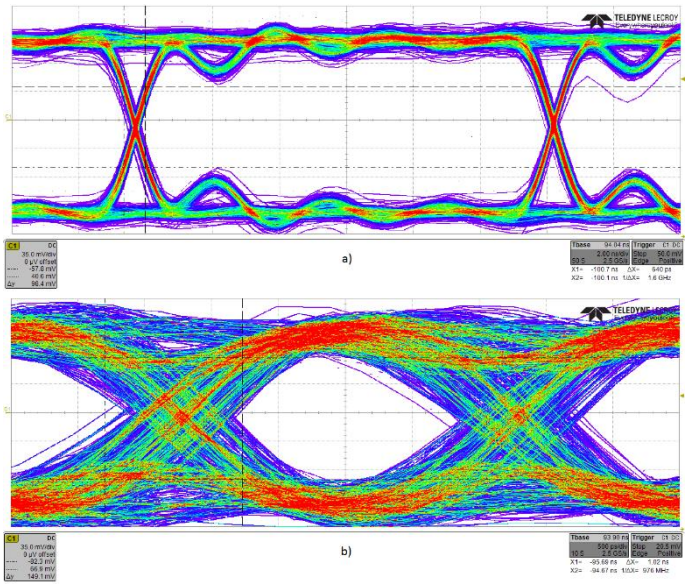

Fig. 3. Eye-Pattern taken with SLVS-400 compliant pseudo-random sequence at 80 Mbps in a) and 400 Mbps in b). The channel include two male DIN 41612 mated with the two female soldered on the PCB board.

4 Conclusions

4.1 Summary

The increased flexibility and independence of every single muon Control Channel associated with the higher data transfer rate allows the development of new algorithms for fine noise measurements at any moment, without changing any part in the new Service Board crate. When the whole facility will be ready and equipped more tests and a full characterization will take place. Anyway, for what concerns the design of the new Service Board System prototype these results are a proof-of-concept that in fact motivated the production of a limited number of preliminary boards (see **Fig. 4** and **Fig. 5**).

Fig. 4. The new Pulse Distribution Module (nPDM) prototype rev.01, produced in March 2017

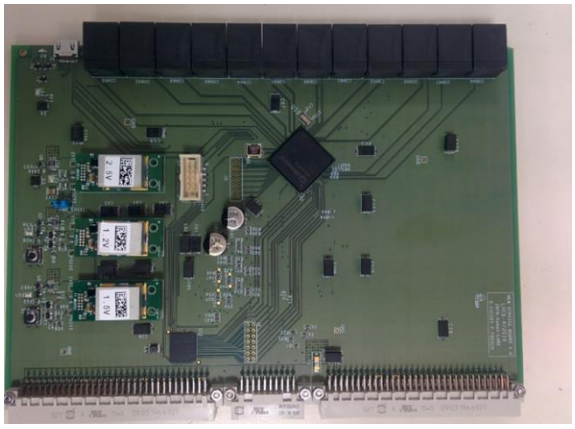

Fig. 5. The new Service Board (nSB) prototype rev.01, produced in July 2016

4.2 Acknowledgements

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