First Prototype of the muon Frontend Control Electronics for the LHCb upgrade

Hardware realization and test

V. Bocci, G. Chiodi, P. Fresch et al.

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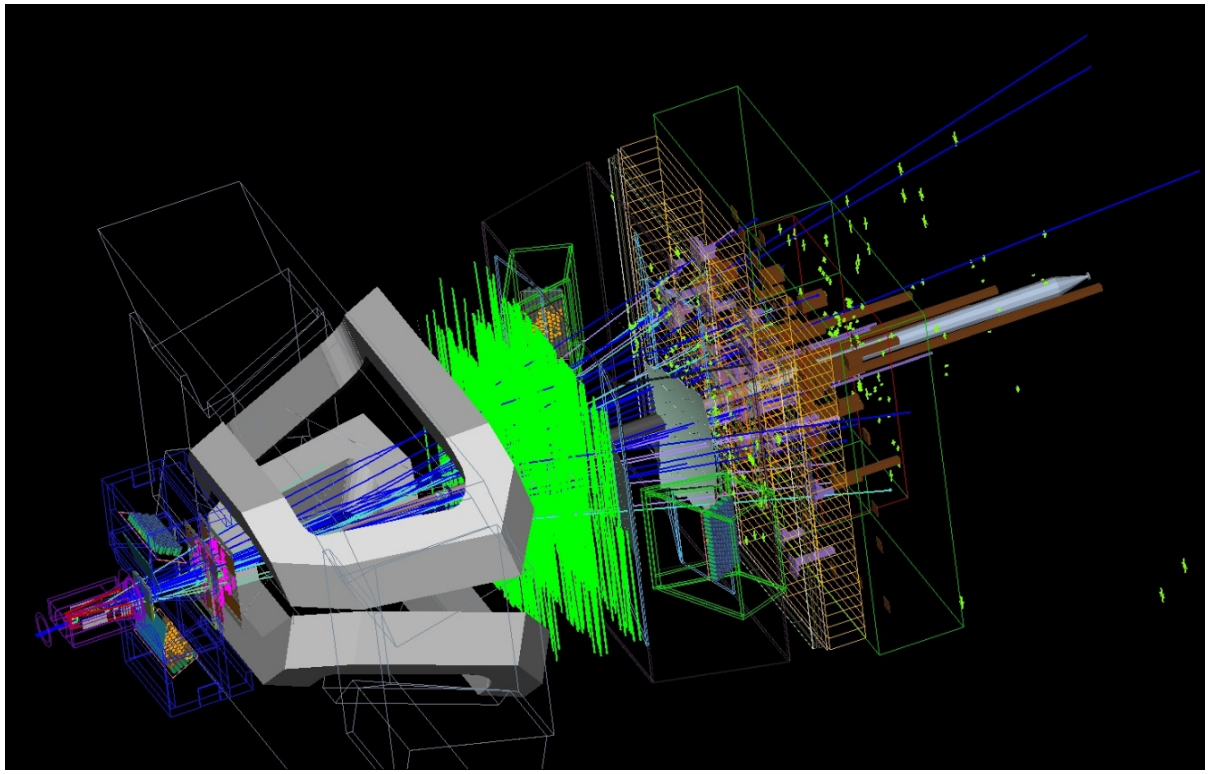
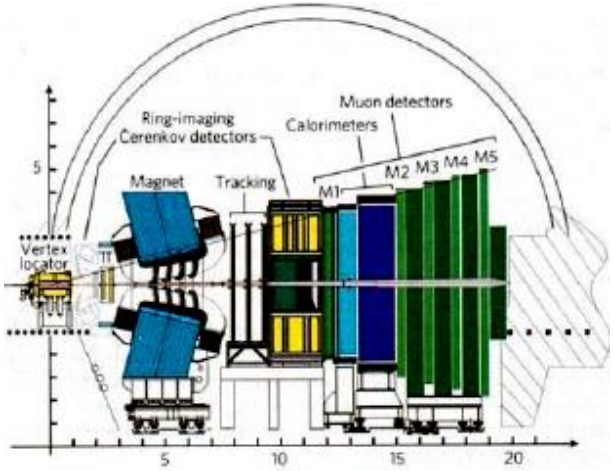
Introduction and Background

The muon detector plays a key role for the particle identification of the upgraded LHCb Experiment at CERN



In the upgrade configuration, it comprises 4 stations of MWPC (Multi-Wire Prop. Chamb.) alternated with 4 iron walls

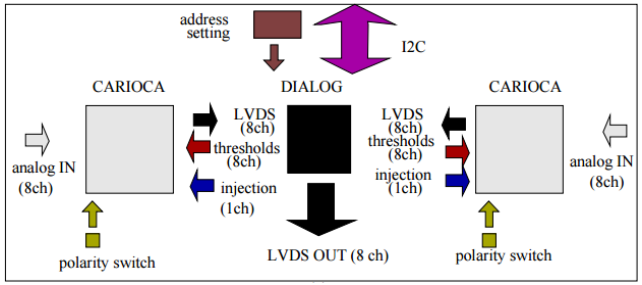


A total amount of 1104 MWPC's are installed in the detector through M1 to M5

Introduction and Background

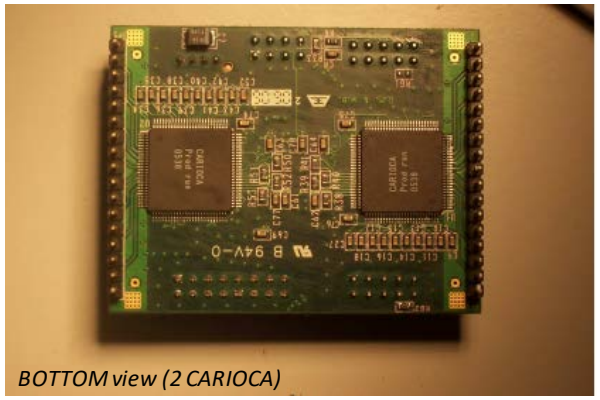
On MWPC the Readout is managed by two CARIOCA chips...

CARDIAC board, hosts 2 CARIOCA and 1 DIALOG

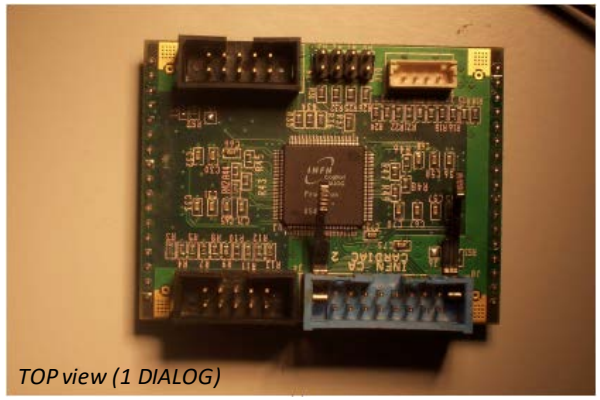


...and one DIALOG chip, which also transmits the data out (LVDS OUT)

CARDIAC board



BOTTOM view (2 CARIOCA)



TOP view (1 DIALOG)

Each MWPC is equipped with 4 CARDIAC, forming ~100k analog channels

Long cables with different lengths are required to cover the whole detector

The CARIOCA's ASD (Amplifier Shaper Discriminator) threshold are selectable

Optimal performance against variability of MWPC parameters

Threshold and timing equalization settings are available in the DIALOG using the custom I2C-LVDS port

LHCb Readout and Control System Upgrade (muon)

"The LHCb experiment has proposed an upgrade towards a full 40 MHz readout system in order to run at between five and ten times the initial design luminosity

The various electronics sub-systems will need to be upgraded. It is vital that all the Systems in the sub-detectors comply with a common set of specifications, based on the GBT optical link"

The SOL40 board distributes Timing and Fast Controls (TFC) and Electronic Control System (ECS) messages (packed in the GBT frame)

The CARDIAC boards and the MWPC's will be left unchanged during the upgrade

An interface between the optical link and the legacy FEE control link (I2C-LVDS) is required

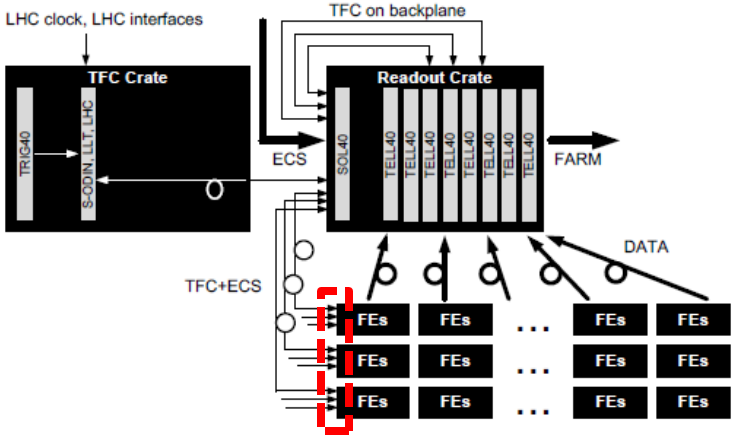


Figure 3: Physical architecture of a partition of the upgraded readout system

LHCb Readout and Control System Upgrade (muon)

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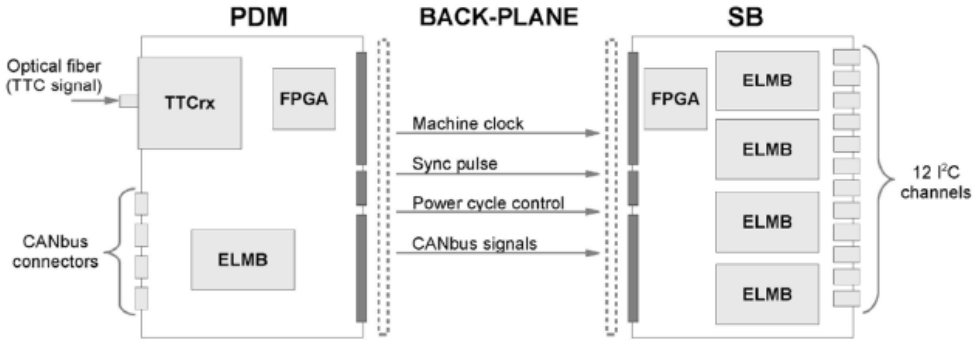
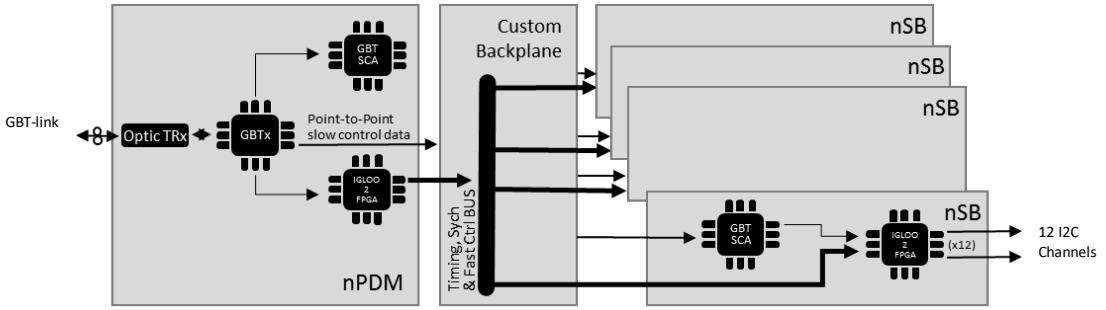
The various electronics sub-systems will need to be upgraded. It is vital that all the Systems in the sub-detectors comply with a common set of specifications"

The framework of the Service Board System Upgrade is aimed to develop a new control infrastructure to interface the SOL40 board (Control Room) with the CARDIAC boards (DIALOG configuration registers)



Present Service Board System Architecture

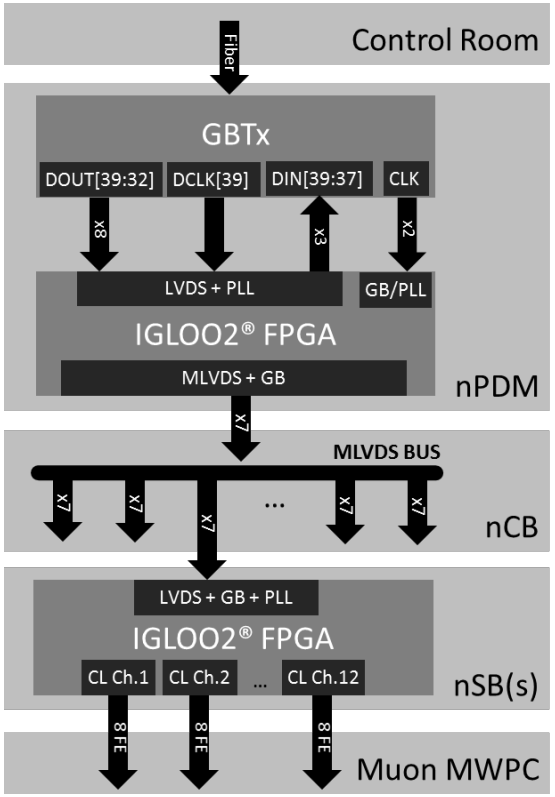


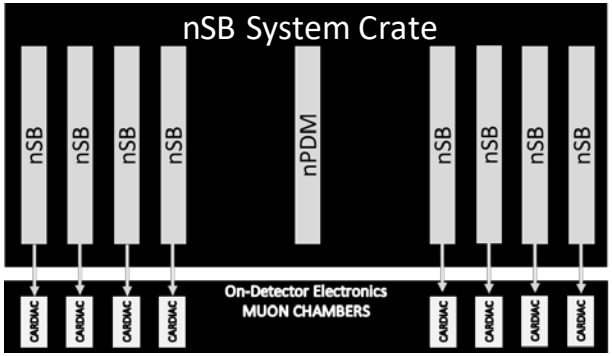
Upgraded Service Board System Architecture

new Service Board System Architecture (with GBT-link)

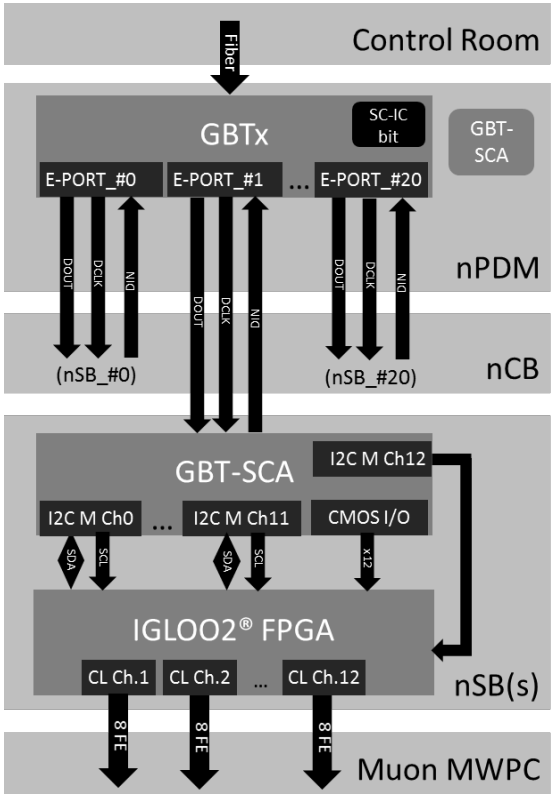
The new electronic will be allocated in the actual muon tower that host the rack with the electronic boards

Timing and Fast Control flow





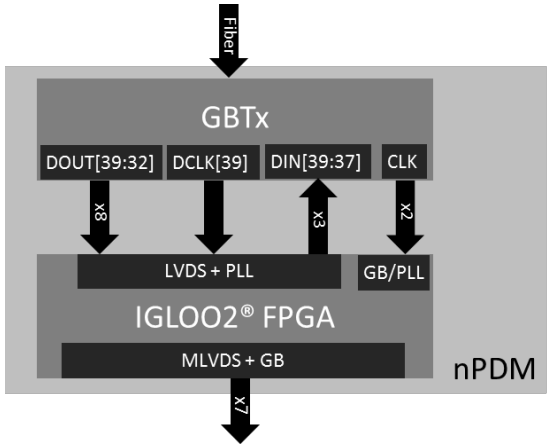
Electronic Control System flow



This has required the design of a new Pulse Distribution Module, new Service Board and a new Custom Backplane that fits in the VME 6U crate

new Service Board System Architecture (with GBT-link)

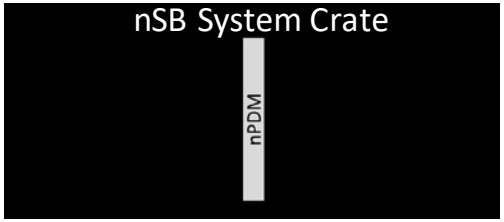
Timing and Fast Control flow



8 (+2) SLVS channels deliver the Timing and Fast Control signals to the FPGA

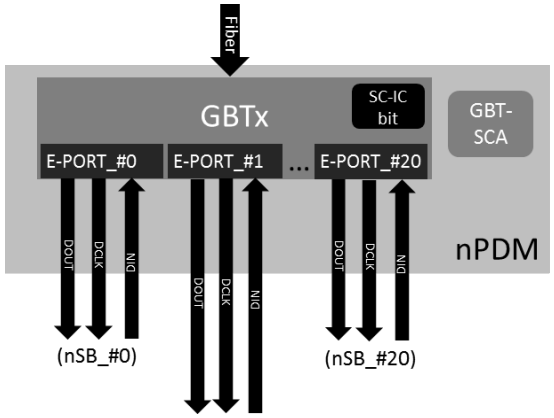
7 MLVDS I/O drivers broadcast a sub-set of them to all the nSB in the crate

The new Pulse Distribution module is the master board of the crate. It receives data from the Control Room through a 150m-long optical fiber



All the boards are connected through the new Custom Backplane

Electronic Control System flow



The Electronic Control System data flow in 20 (+1) point-to-point full-duplex e-links.

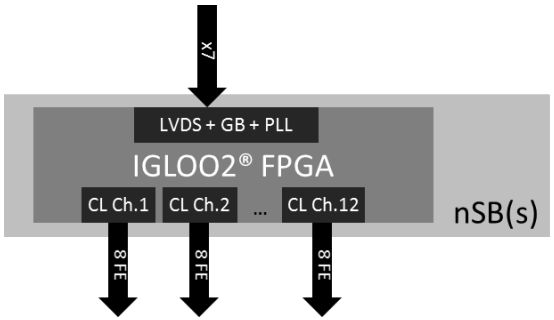
Each nSB has one dedicated e-link @ 80 Mbps

new Service Board System Architecture (with GBT-link)

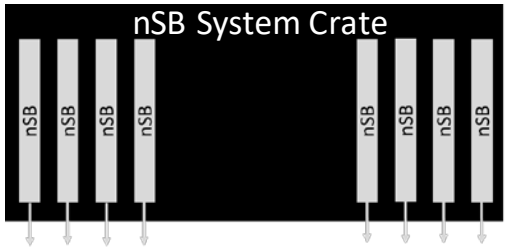
The new Service Board is the slave board of the system. It receives data from the nPDM

Timing and Fast Control flow

The Timing and Fast Control signals are elaborated and fanned-out on 12 independent channels

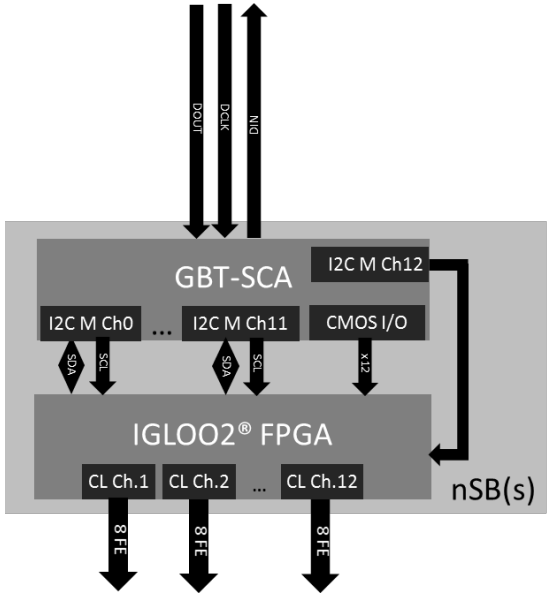


12 FPGA LVDS I/O drivers used to CARDIAC



Electronic Control System flow

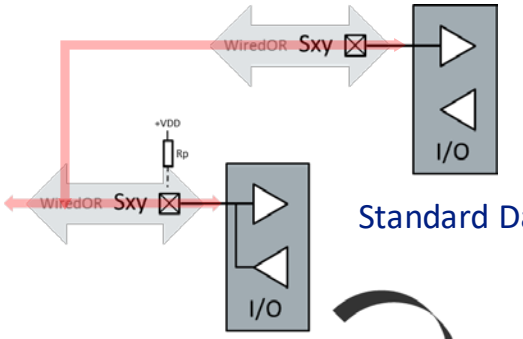
The e-link from nPDM is connected to the GBT-SCA



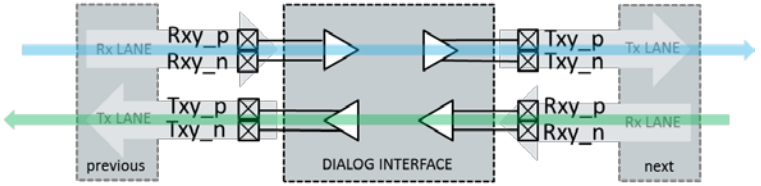
The I2C-bus interfaces are used to communicate with the DIALOG's bus. But the two protocols differs at physical layer...

The new Service Board (nSB)

First critical point is the interface between the GBT-SCA chip and the custom bidirectional serial link of the CARDIAC's slow control. This protocol differs from the I2C-bus in the physical layer

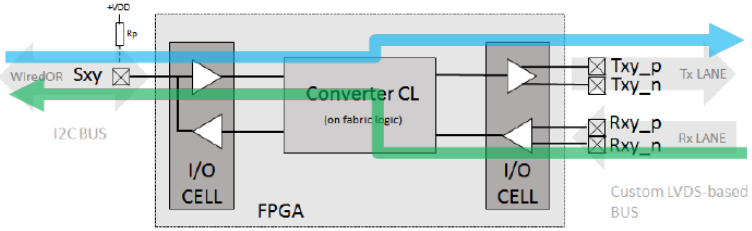


Standard Data Interface for I2C-bus



DIALOG's Data Interface (custom I2C-LVDS)

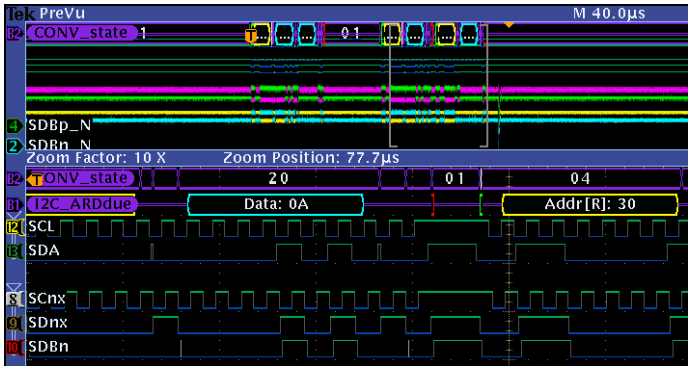
Our solution is a Custom I2C-to-I2C_LVDS On-the-Fly Converter implemented in a dedicated FPGA:



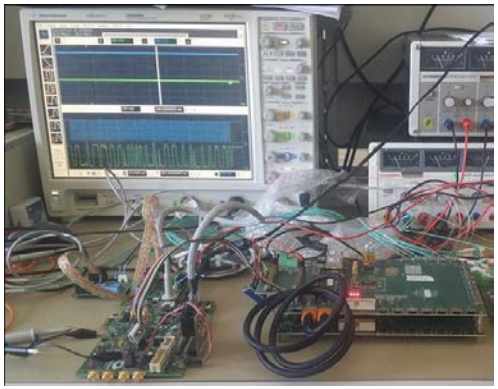
The new Service Board (nSB)

The custom I2C-LVDS on 12 Channels requires 36 differential I/O's

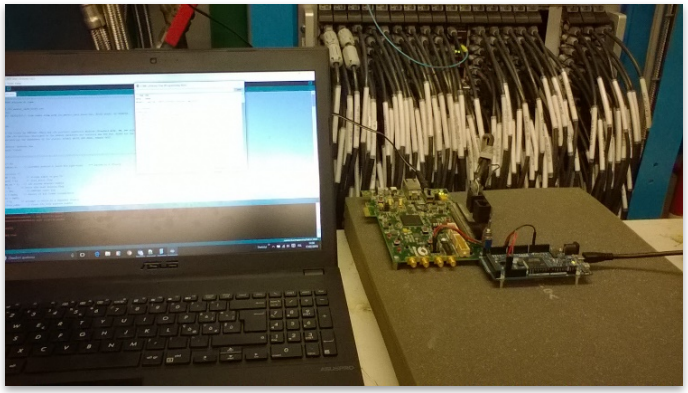
The Microsemi IGLOO2® Flash-based FPGA do not require any additional part and is less prune to SEU errors compared with other technologies



The Custom Converter evaluation prototype tested in two different real scenario:



GBT-link Evaluation kit (VLDB+miniDAQ) (CERN)



LHCb muon detector (LHCb cavern – CERN)

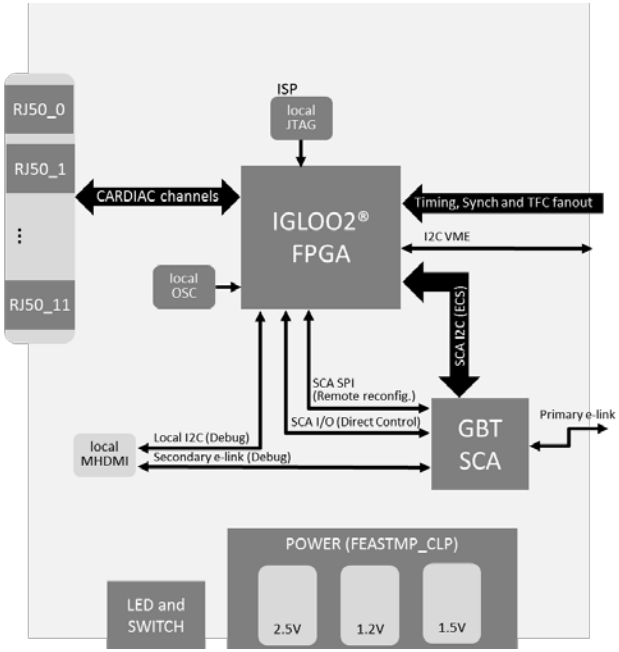
```
I2C Scanner
Scanning...
I2C device found at address 0x30  <- OK
I2C device found at address 0x31  <- OK
I2C device found at address 0x32  <- OK
I2C device found at address 0x33  <- OK
I2C device found at address 0x34  <- OK
I2C device found at address 0x35  <- OK
done


Move the switch to start the test!


Communication with slave @ address:  30
started @(us):  2747538

ended @(us):  53354617
# of W&R attempts: 100000000   NACK_couter: 0 0
Comm_err counter: 0
```

The obtained positive results…

The new Service Board (nSB)

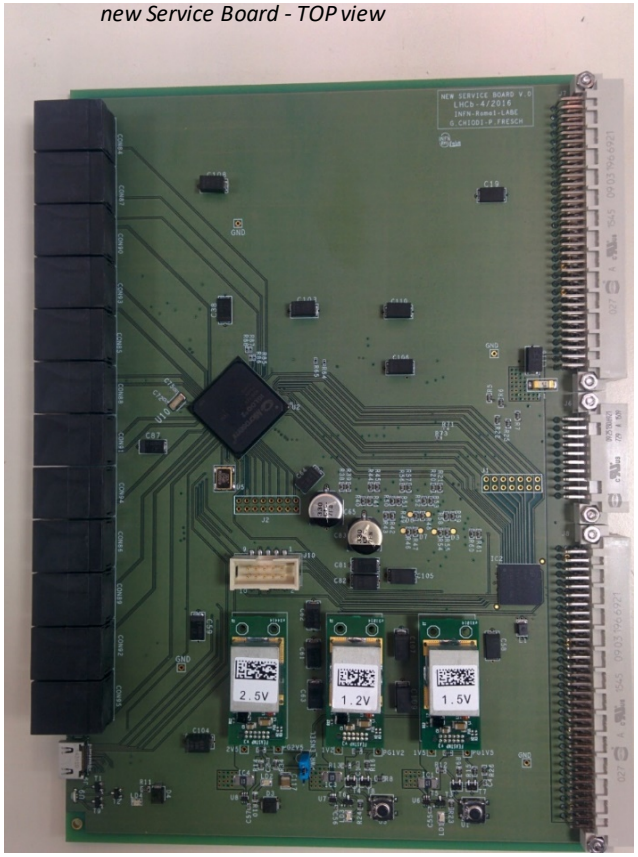
…motivated the realization of the nSB rev01 prototype

nSB Functional Blocks

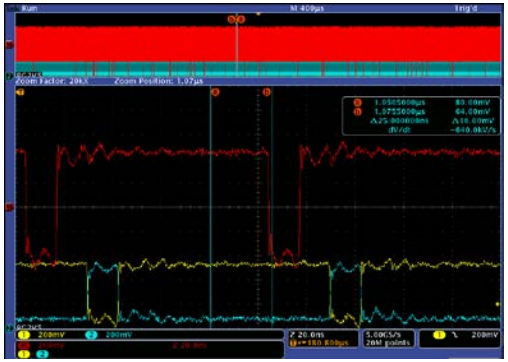


nSB REV01 Prototype

new Service Board - TOP view



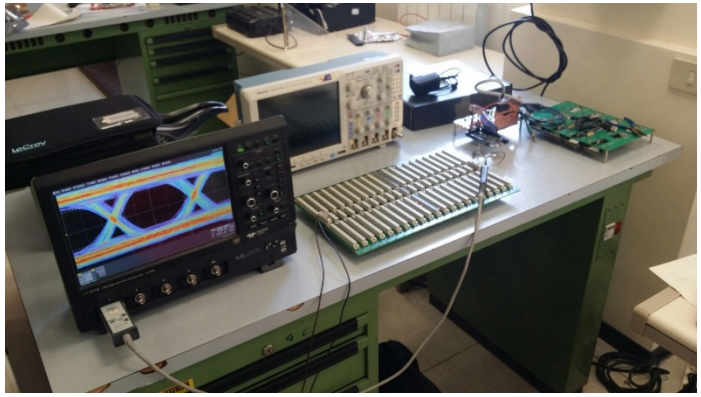
Debugging…

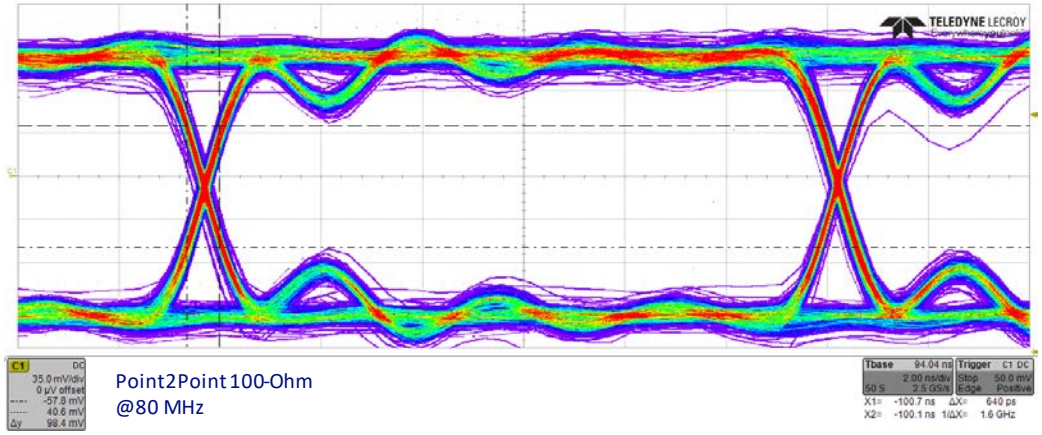


The new Custom Backplane (nCB)

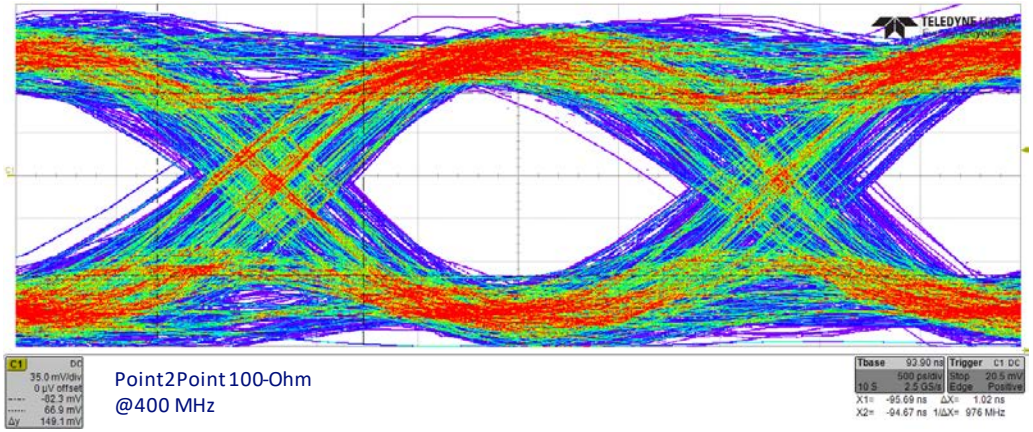
Second critical point is the routing of the e-link through two VME DIN 41612 96-pin connector…

… a spare part of the present system has been modified and tested to prove the signal integrity





Point2Point 100-Ohm
@80 MHz

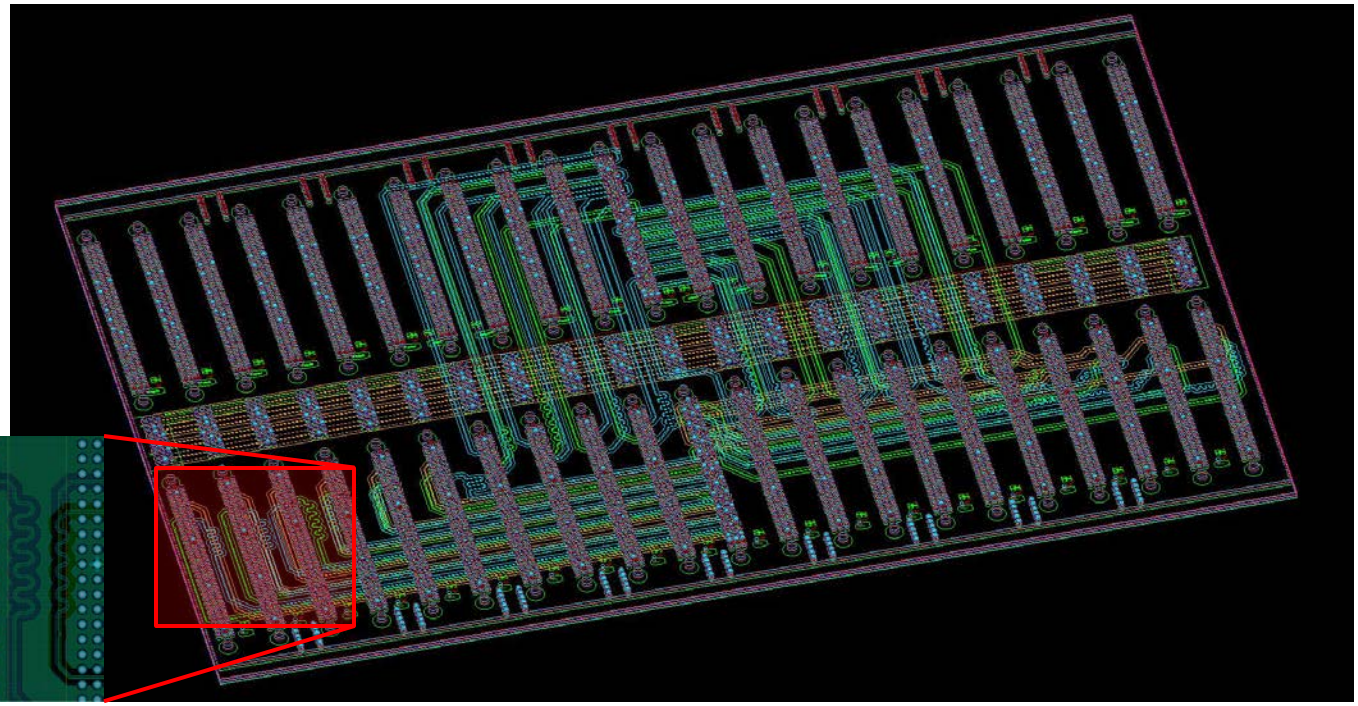


Point2Point 100-Ohm
@400 MHz

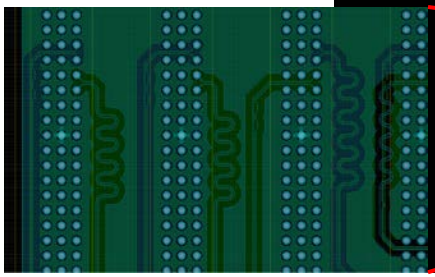
The new Custom Backplane (nCB)

Through the backplane 20 serial e-link (SLVS) are routed from the GBTx to the GBT-SCA chips on the nSB boards…

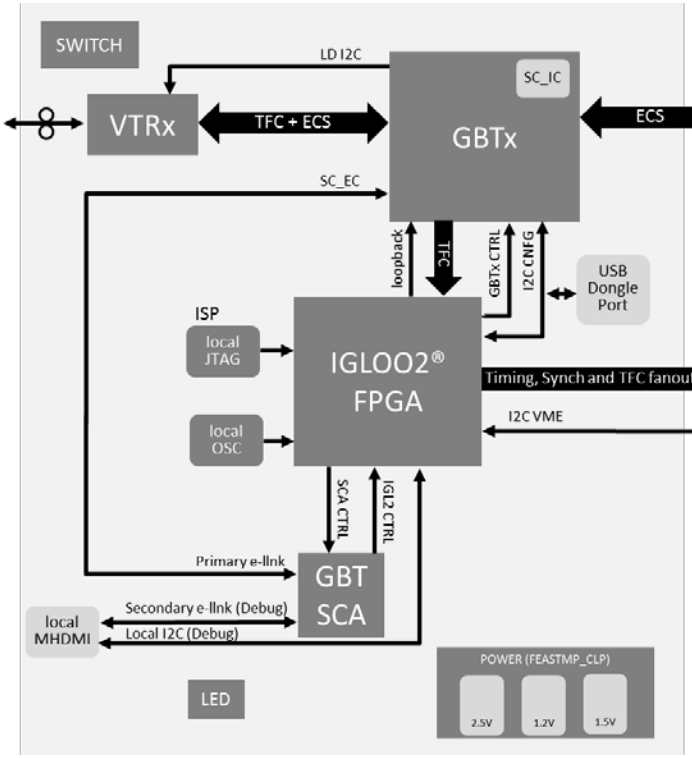
…and up to 7 MLVDS-bus broadcast the Timing and Fast Control signals



Phase adjustmet of the elink lanes



The new Pulse Distribution Module (nPDM)



After manual routing of:

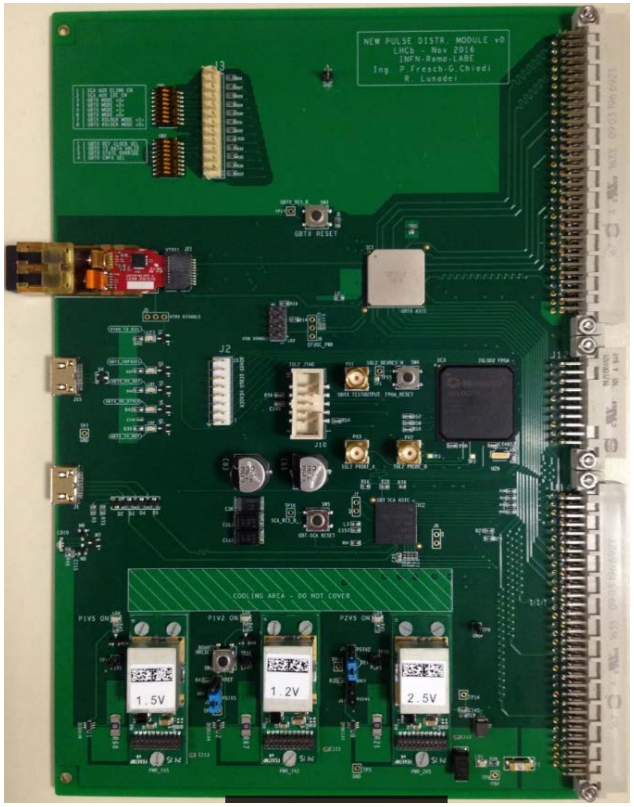
60 differential pairs with controlled phase…

… a 4.2 Gbps serial link…

… additional 7 differential pairs in MLVDS “fashion”…

We produced the first prototype of the nPDM!

new Pulse Distribution Module - TOP view

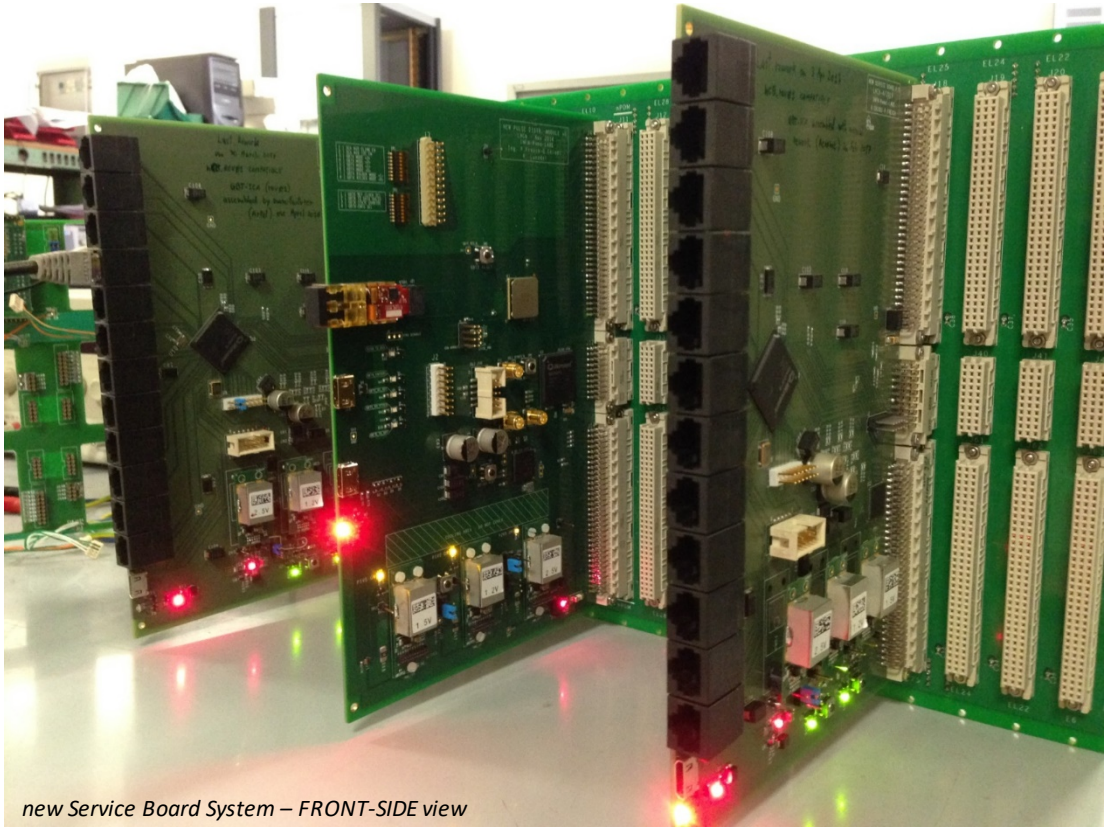


Conclusions

Basic test of board functionalities completed on nSB REV01

Few errors detected and corrected

The nSB is able to communicate with DIALOG



new Service Board System – FRONT-SIDE view

Complete FPGA code release is under working, including debug and test functionalities

Characterization and performance study will be possible

Radiation test are planned

Full system validation test is required

Thank you

for your attention!