MiniDAQ1

A COMPACT DATA ACQUISITION SYSTEM FOR GBT READOUT OVER 10G ETHERNET
Overview

- LHCb upgrade
- Optical frontend readout
- Slow control implementation
- Fast control implementation
- DAQ & Ethernet implementation
- Transition to MiniDAQ2 and final architecture
The LHCb experiment

One of the 4 major experiments at the Large Hadron Collider under the French-Swiss border.

Single arm forward spectrometer for accurate measure of B meson decays. A collaboration between 69 universities and laboratories from 16 countries. In operation since 2009.
LHCb Run 3 upgrade

- Remove L0 hardware trigger
  - L0 saturation at high luminosity
- Send full event rate to HLT
  - 1 MHz → 40 MHz
- Higher event size
  - 50 KB → 100 KB
- Zero suppression on frontends
- New readout electronics
- Frontend readout over new protocols

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LS 2 | Run 3 | LS 3

LHCb Run 2 Trigger Diagram
- 40 MHz bunch crossing rate
- L0 Hardware Trigger: 1 MHz readout, high $E_T/P_T$ signatures
  - 450 kHz $h^2$
  - 400 kHz $\mu/\mu$
  - 150 kHz $e/\gamma$

LHCb Run 3 Trigger Diagram
- 30 MHz inelastic event rate (full rate event building)
  - Software High Level Trigger
  - Full event reconstruction, inclusive and exclusive kinematic/ geometric selections
  - Buffer events to disk, perform online detector calibration and alignment

12.5 kHz (0.6 GB/s) to storage

2-5 GB/s to storage
Optical frontend readout

Versatile link
Rad-hard receiver and transmitter for multi-mode and single-mode fibers

GBTX
- Rad-hard optical link interface chip
- Flexible frontend topology through configurable serial “E-links”
- GBT mode (data links or control links)
  - RS FEC, 3.36 Gb/s
- WideBus mode (data links only)
  - No FEC, 4.48 Gb/s

VELO frontend
- GWT (Vertex Locator data links only)
  - Velopix, 5.12 Gb/s

VTRx (duplex) + 2 VTTx (simplex) on a frontend board
MiniDAQ1 hardware

AMC40 mezzanine + AMCTP carrier

- **AMC40**
  - Stratix5 FPGA
  - 3 MiniPOD AFBR-811VxyZ (Tx)
  - 3 MiniPOD AFBR-821VxyZ (Rx)
  - Up to 24 GBT/WB/GWT
  - Up to 12 10GBASE-R Ethernet

- **AMCTP**
  - Local 40/80 MHz oscillator
  - External clock input
  - COM Express Module
  - PCI Express x1 to FPGA
  - GbE to LAN
MiniDAQ1 firmware

- **SOL40/SODIN**
  - Highly configurable for each FE topology
  - Bidirectional commands and monitoring

- **TELL40**
  - Highly configurable for each FE protocol
  - Synchronize with frontend BXID
  - Align data between links
  - Assign global EVID
  - Aggregate BXID data as “fragments”
  - Front-end specific data processing (optional)

- **ECS**
  - Control system access from AMCTP

24 GBT + SODIN + SOL40 + TELL40 + ETH ≈ 85% FPGA logic
Slow control

GBT-SCA

- Rad-hard ASIC for slow control functions over GBT

MiniDAQ1

- SCA protocols implemented
  - ADC
  - I2C
  - GPIO
  - SPI
  - JTAG

- Remote programming flash-based FPGAs through GBT-SCA
  - Xilinx Kintex7
  - Microsemi SmartFusion2 and IGLOO2
Fast commands

**SODIN**
- Regulate throughput from readout boards
- Distribute timing and synchronous commands
  - Front-end reset
  - Synchronization
  - Header only
  - Non-Zero Suppressed
  - Calibration
  - Random/orbit trigger
  - ...and more

**SOL40**
- Fan-out fast commands to TELL40 and to FE
- Distribute ECS configuration to FE
- Receive ECS monitoring from FE

In MiniDAQ1, SODIN+SOL40+TELL40 coexist in one same board
Control system

**WinCC-OA**
- Device description (Run-time DB)
- Device access (DIM, OPC, drivers...)
- Alarm handling
- Archiving, logging, scripting, trending
- Access control
- User interface

**SMI++**
- Abstract behavior modeling (FSM)
- Automation and recovery

**GbtServ**
- Interface between SCADA and FPGA

**Writer**
- Interface between SCADA and storage
10GBASE-R readout

- Multiple UDP streams
  - Raw data, TELL40 data, SODIN data
- Reformat stream to a more efficient format for transmission
- Simple round-robin scheduling between available network links
  - Keep TELL40 and SODIN data for a same event on the same link
- Bidirectional protocol stack
  - UDP, ARP, ICMP
- Links are always point-to-point
  - Optional event building done in PC
- ChelsioT420-CR
  - WireDirect driver for line-rate throughput
Readout software

DIM integration with control system
- Publish status updates
- Receive commands and configuration

Output to disk
- Retain event fragments for offline analysis

Output to monitoring
- Best-effort sampling for online data quality

Event builder
- Prototype implementation to merge fragment streams from multiple sources
Scaling out

It is possible to scale the readout system by chaining multiple MiniDAQ1s

Control system
- Just instantiate multiple FSM trees

Master board
- Local oscillator provides common reference
- Local SODIN provides central synchronization
- Local front-end generator provides data

Slave board(s)
- Recover clock from master link
- Use recovered clock for TELL40 links

Readout
- Store one separate file per source
- Compare EVID and BXID sequence
Some test setups

- Sub-detector groups are actively using MiniDAQ1 to develop the new frontends
- MiniDAQ1 continues to be maintained and will also be used to stress-test MiniDAQ2
MiniDAQ2 hardware (PCle40)

- PCI express add-in card
  - Full-length, full-height

- Arria10 FPGA
  - 2x resources as Stratix5
  - 24 links: 85% on S5 to 46% on A10

- High-density optical IO
  - Up to 48 bidirectional links

- PCle Gen3.0 interface to Event Builder
  - Custom 100 Gb/s DMA engine

- Design has been validated
  - Full board self-test

- Initial production started

- Collaboration institutes have started to receive first devices
Transition to MiniDAQ2

Aim to make the change transparent:

**Hardware**
- Everything changed (FPGA, Clock tree...)

**Firmware**
- New Low-Level Interface
- Fronted side stays the same
- Backend side replaced by PCIe

**Software**
- GbtServ unchanged
- Control system & panels compatible
- Stream and buffer API adapted to DMA
- Writer output format unchanged
- Interface to monitoring and presenter unchanged
Final architecture

Custom electronics

Common board for all TFC/ECS/DAQ

COTS hardware

Detector front-end electronics

Event Builders (PC + readout board)

UX85B

Clock & fast commands

throttle from PCIe40s

Event Builder network

6 x 100 Gbit/s

online storage

Event Filter Farm
1000 – 4000 nodes

subfarm switch

subfarm switch

x500

6 x 100 Gbit/s
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