

The Intelligent FPGA Data Acquisition Framework

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The Intelligent FPGA Data Acquisition Framework (IFDAQ)

is used for the development of the data acquisition systems.

It provides a collection of IPcores needed to built entire data acquisition systems starting from a very simple stand-alone Time-to-Digital-Converter module to a large-scale DAQ including time distribution, slow control, data concentrators and event builders.

The IPcore library consists of SERDES-based TDC with a resolution depending on the FPGA type (229 ps for the Artix7-1 speedgrade, 100 ps for the Virtex6-2 speedgrade), an ADC interface including data processing ([pedestal] determination, signal detection and time extraction using digital constant fraction discrimination), a Unified Communication Framework (UCF), an event builder, and a slow control core.

The UCF is an inter-FPGA communication protocol for high-speed serial interfaces. It provides up to 64 different communication channels via a single serial link. One channel is reserved for timing and trigger information, the other channels can be used for slow control interfaces and data transmission. All channels are bidirectional and share link bandwidth according to assigned priority. The timing channel distributes messages with fixed and deterministic latency in one direction. From this point of view the protocol implementation is asymmetrical. The framework supports point-to-point and star-like 1:n topologies. The star-like topology can be used for front-ends with low data rates and pure time-distribution systems. In this topology, the master broadcasts information according to assigned priority, the slaves communicate in a time-sharing manner to the master.

The first applications of the IFDAQ is the upgrade of the drift detectors of the COMPASS experiment at CERN, the straw detectors of the drift chambers of the NA64 experiment at CERN, and the read-out for the Belle II pixel detector at KEK in Japan.

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