

TIPP 2017

# Design of a Data Acquisition Module Based on PXI for Waveform Digitization

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Beijing International Convention Center

University of Science and Technology of China





# Outline

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Waveform digitization in physics experiment

Description of the module

Performance of the system

Summary and Prospect



# Waveform digitization

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- **SCA**
  - Switch Capacitor Arrays
  - High resolution ADC
- **Experiments**
  - ANTARES
  - AMANDA
  - H.E.S.S-II
  - MAGIC-II
  - Etc.
- **ADC**
  - High speed & high resolution ADC
- **Experiments**
  - DANCE
  - TAC
  - GTAF
  - Darkside
  - LUX
  - XENON
  - *PANDAX IV*
  - Etc.



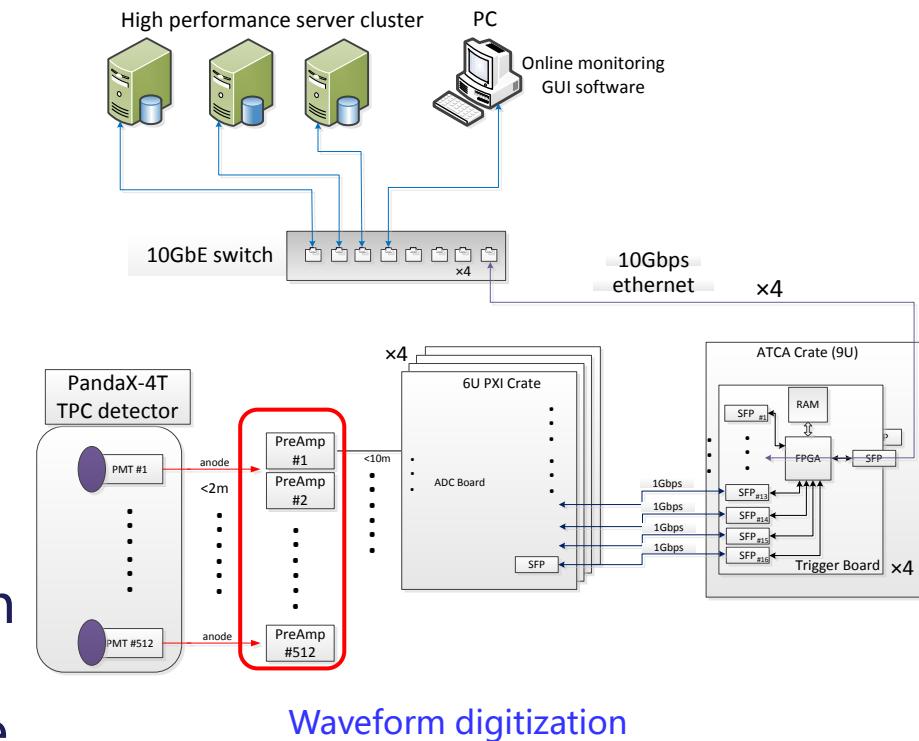
# PandaX-4T

- **Particle and Astrophysical Xenon Experiments**

- China Jinping underground laboratory
- Dark matter direction detection
- 4-ton Double phase Xenon TPC

- **Principle verification**

- Waveform digitization
- Trigger mode
- Data buffer & storage



# Scheme of the module



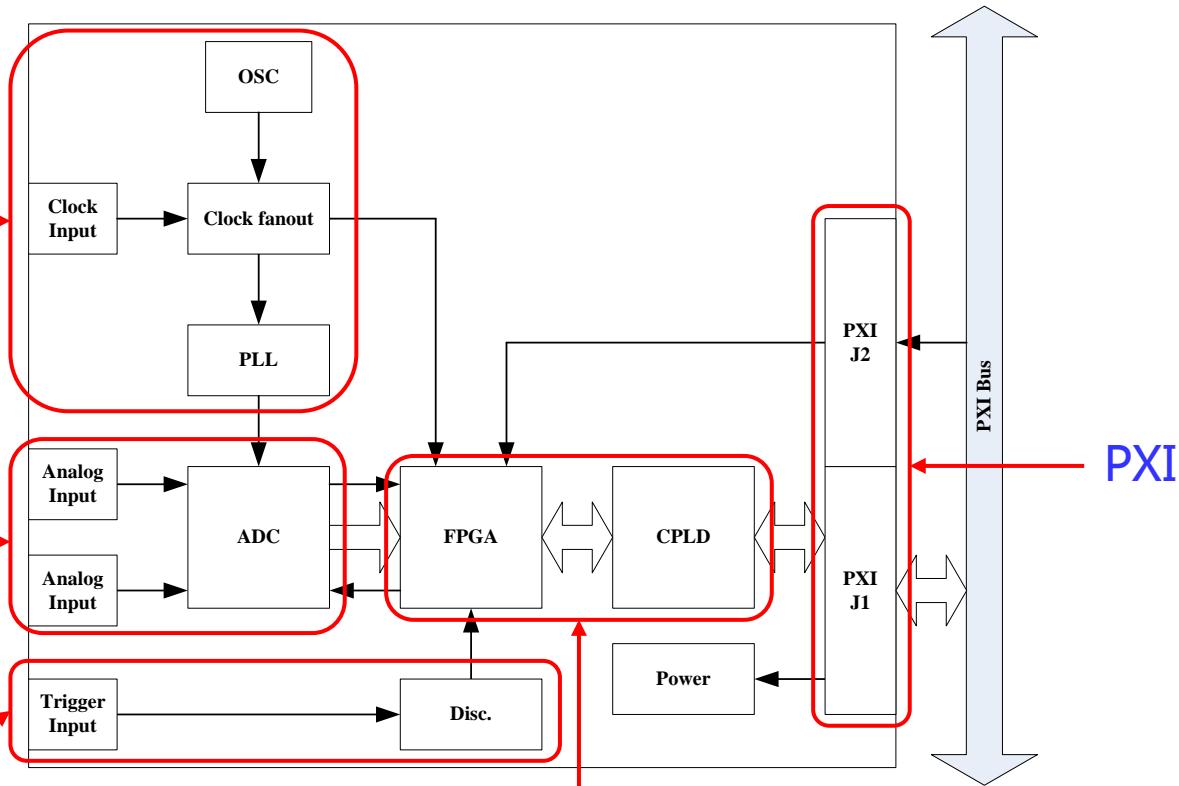
Clock system

ADC

External trigger

Interface & controller

PXI





# ADC & EPLD

- **ADC12D1800**

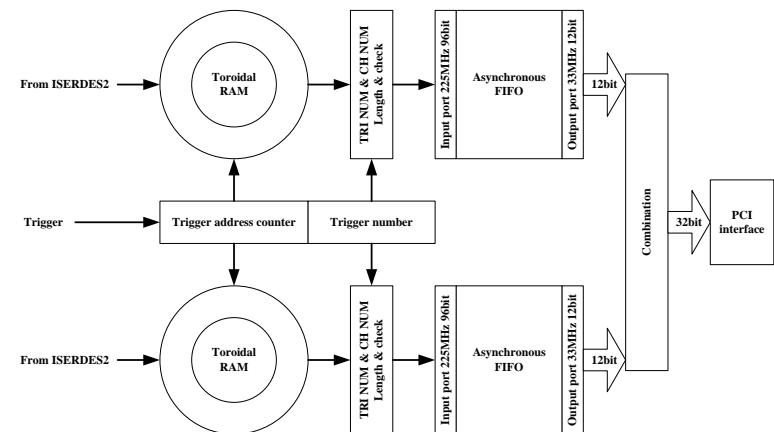
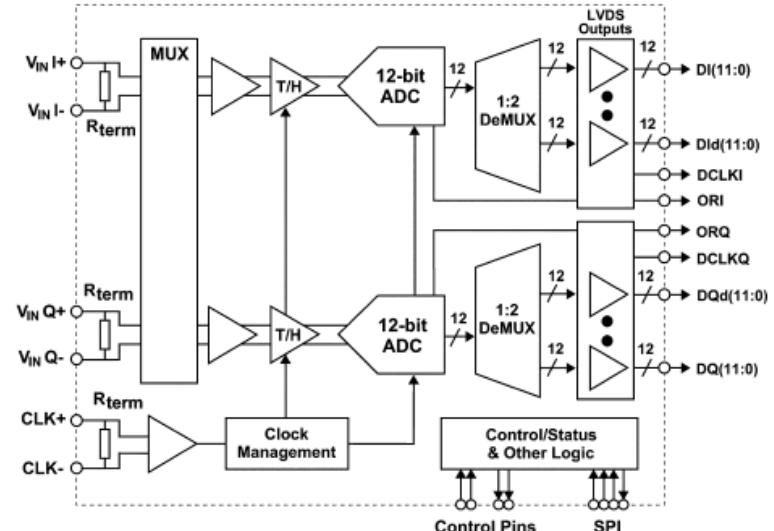
- TI co.
- folding interpolating
- 2 ch.
- 12 bits
- Up to 1.8 GSPS

- **Artix7**

- Config, control & status
- Buffer & storage
- Find triggered data
  - -100us to  $+\infty$

- **MAX II**

- PXI interface
- Module reuse
- DMA transfer





# Clock & trigger

- **Clock**

- Local or external

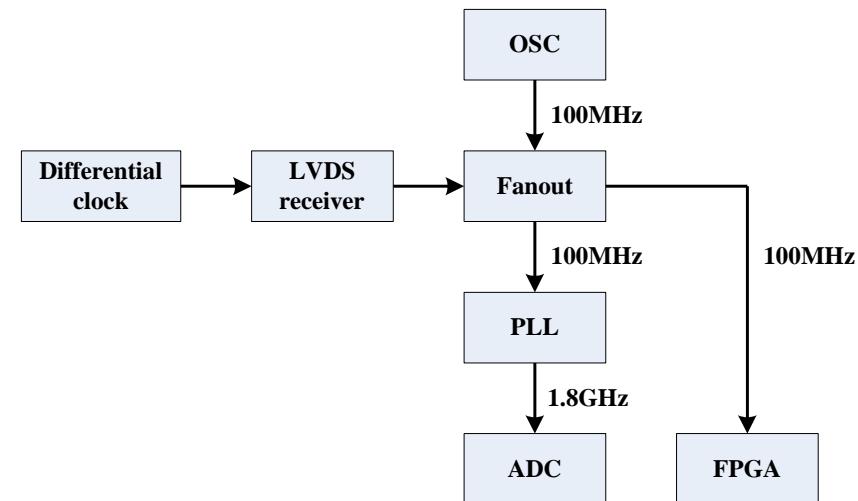
$$SNR = -20 \log(2\pi f_{in} t_{jitter})$$

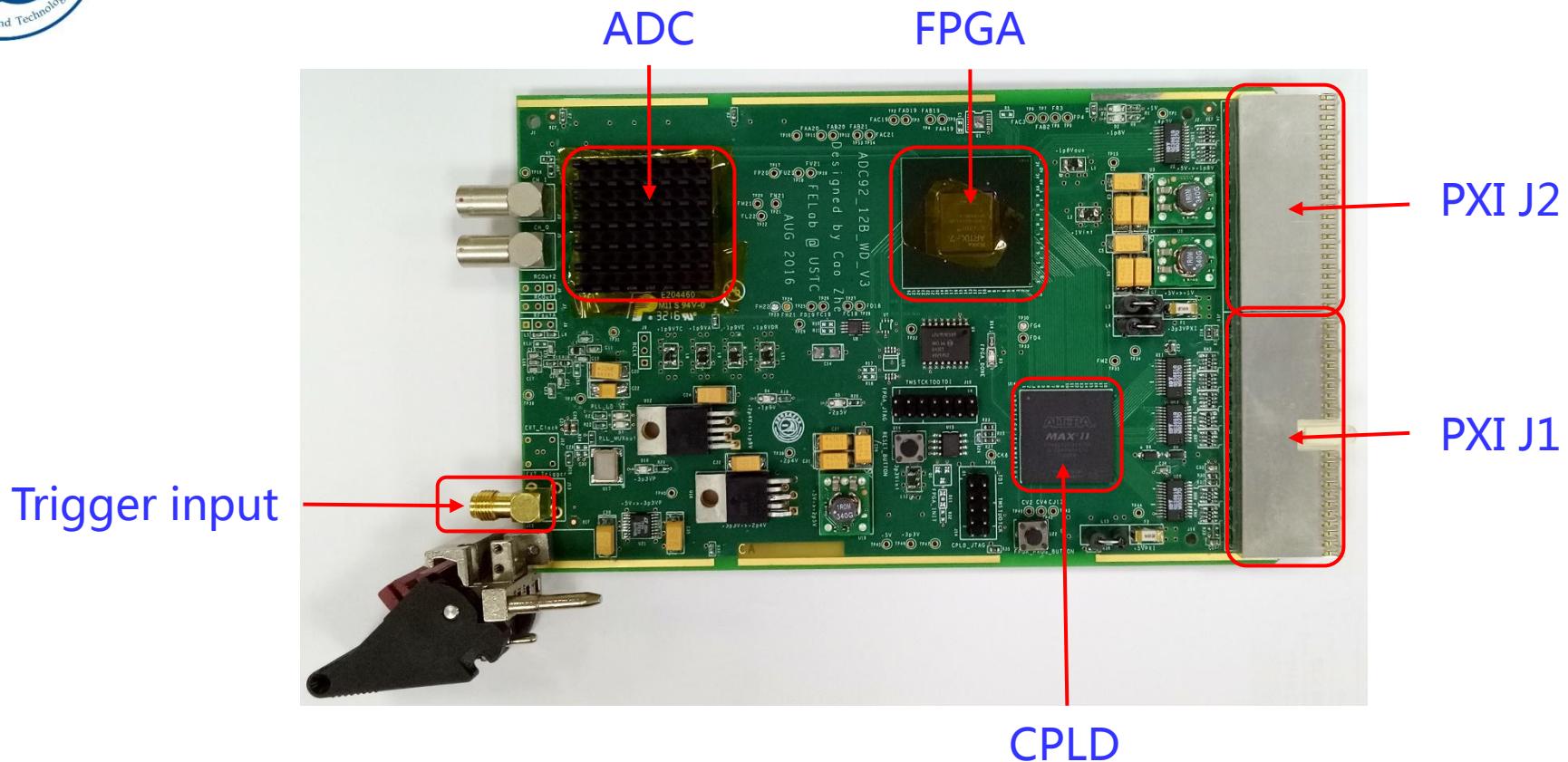
- PLL

- Low frequency to high frequency
- RMS jitter=139fs

- **Trigger**

- External
  - Discriminator
- Internal
  - Star trigger from slot2
- Self
  - Software

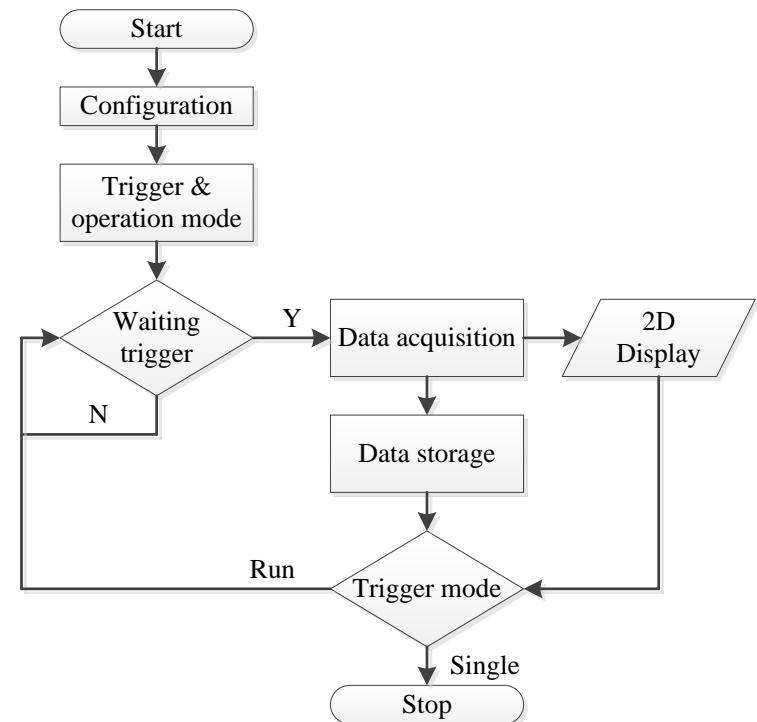




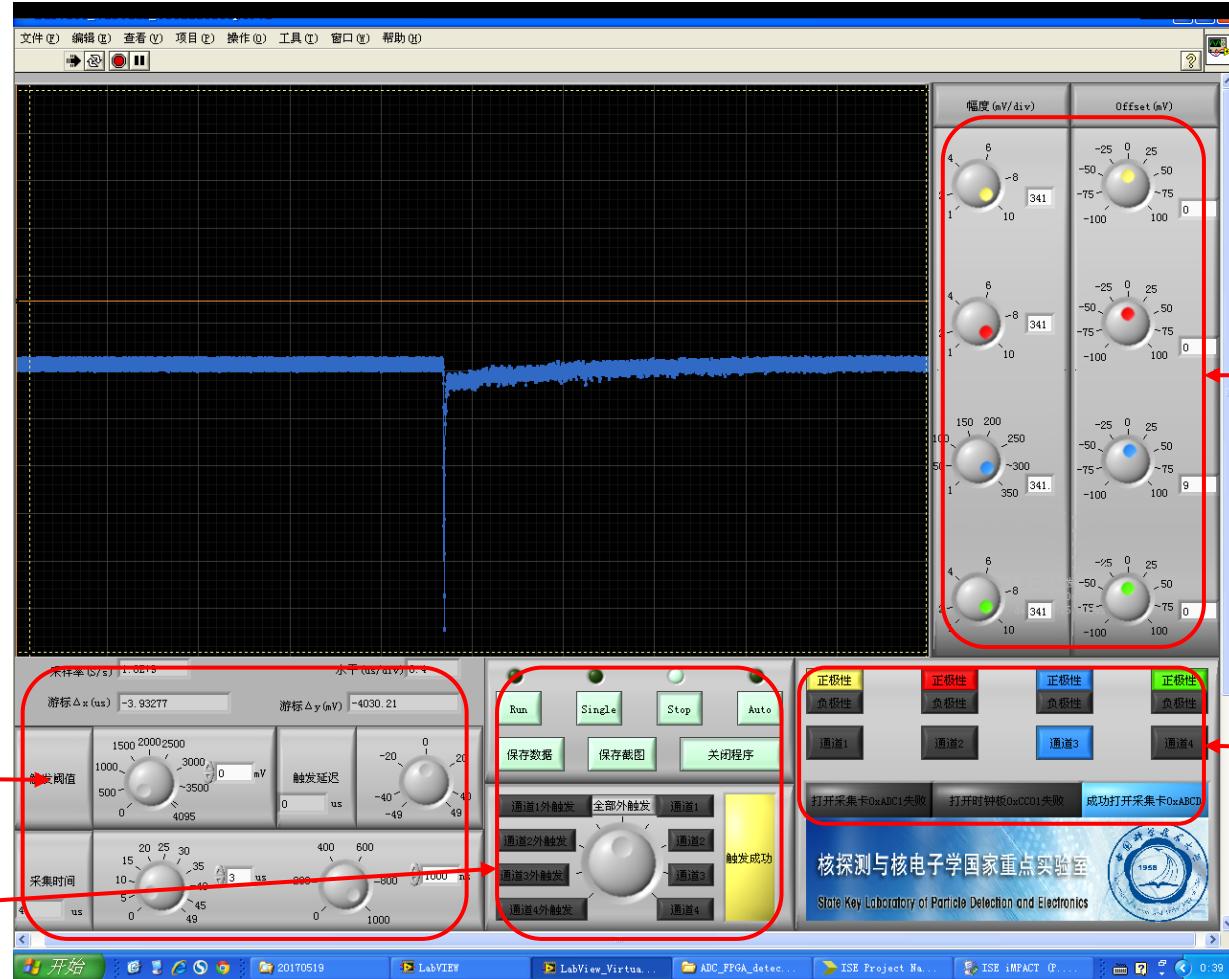


# Virtual instrumentation

- Benefit of test, measurement, automation
  - Powerful application software
  - Cost-effective hardware
- LabVIEW
  - Configuration: ADC, PLL, FPGA
  - Channel: up to 4 ch.
  - Trigger: external or channel, trigger level, trigger delay
  - Operation mode: run, single
  - Sample depth (horizontal): up to 50 us
  - Display (vertical): amplitude, offset



# GUI



Trigger config

2017-5-25

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Horizontal set

Channel config



# System test

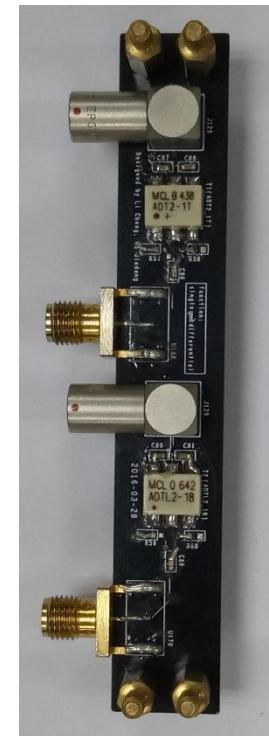
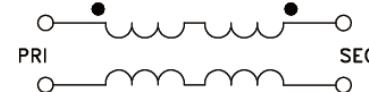
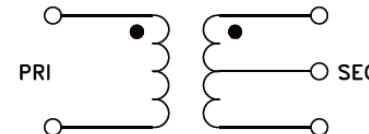
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- **Performance test**
  - Frequency response
  - ENOB
- **Detector test**
  - BaF<sub>2</sub> with PMT
- **Test equipment**
  - PXI platform
    - Adlink PXIS-3320 with controller: 15-slot, 6U
  - Oscilloscope
    - Lecroy 715Zi: 20GSPS, 8bits, 1.5GHz
    - Lecroy HDO6104: 2.5GSPS, 12bits, 1GHz
  - Vector signal generator
    - R&S SMA100A: 9kHz~6GHz
  - Bandpass filter
    - A series of filter from 2.4MHz~798MHz

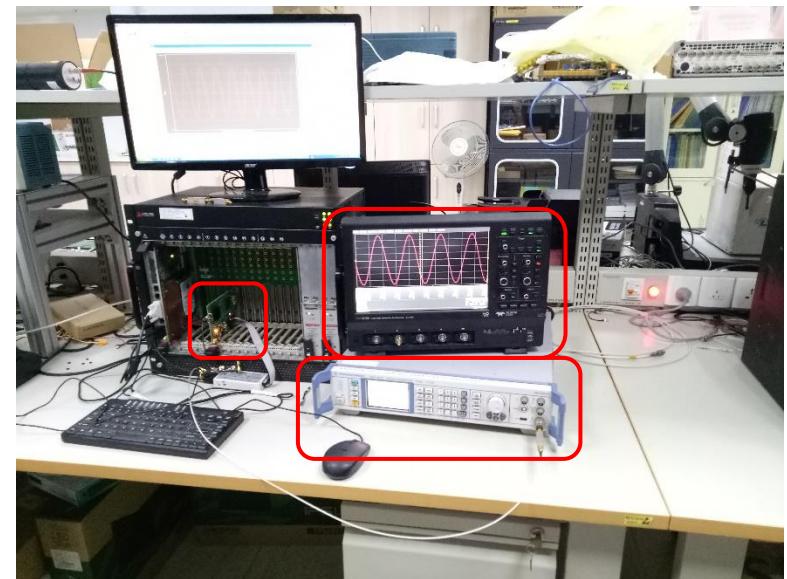
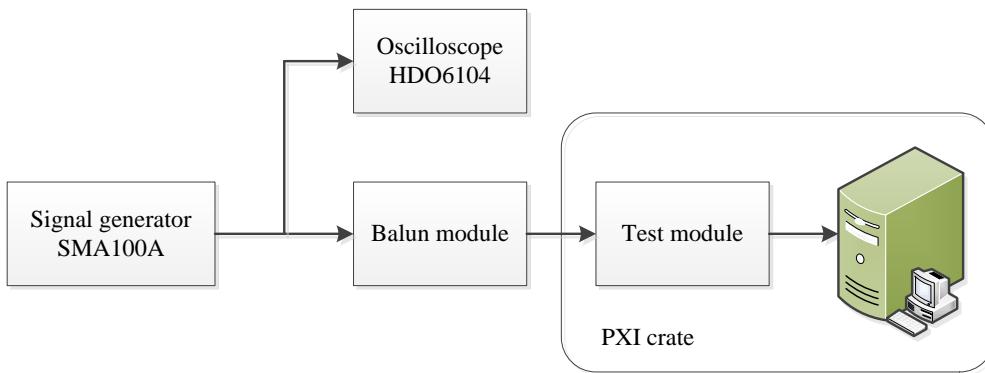


# Balun module for test

- Single end to differential
  - From generator or detector to module
- **ADT2-1T**
  - Conventional
  - Insertion loss: 0.4~450MHz@3dB
- **ADTL-18**
  - Transmission line
  - Insertion loss: 30~1800MHz@3dB

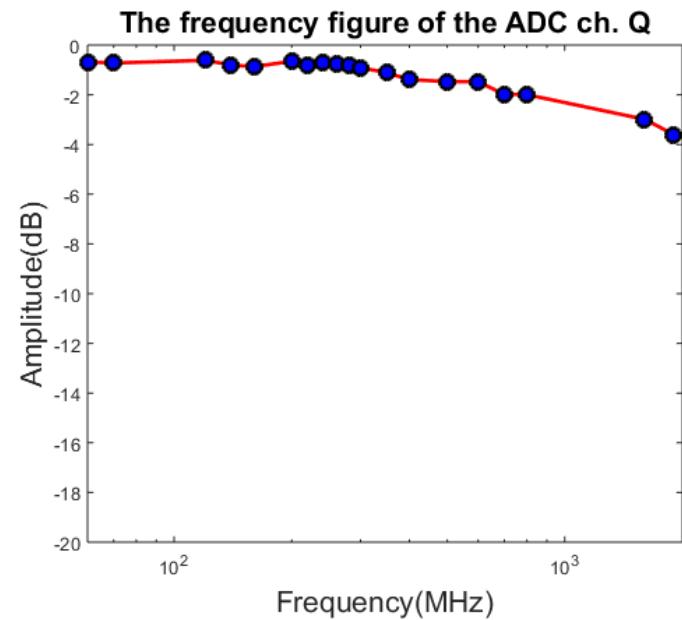
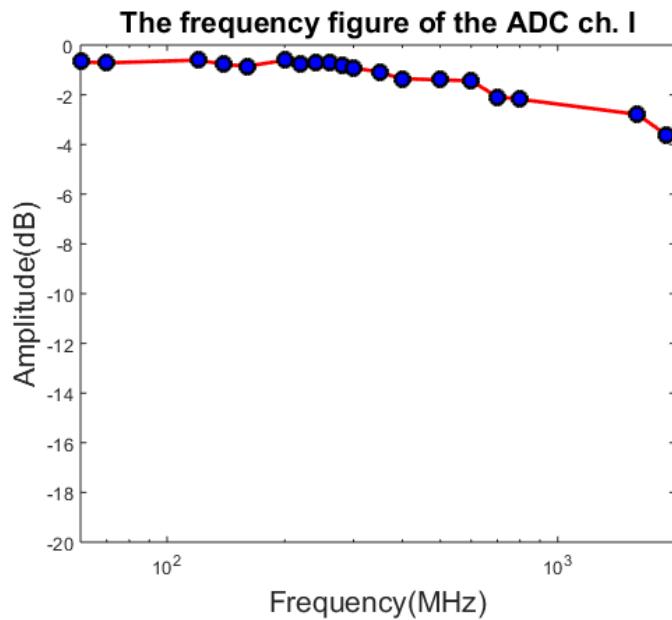


# Frequency response test





# Result@1.8GSPS



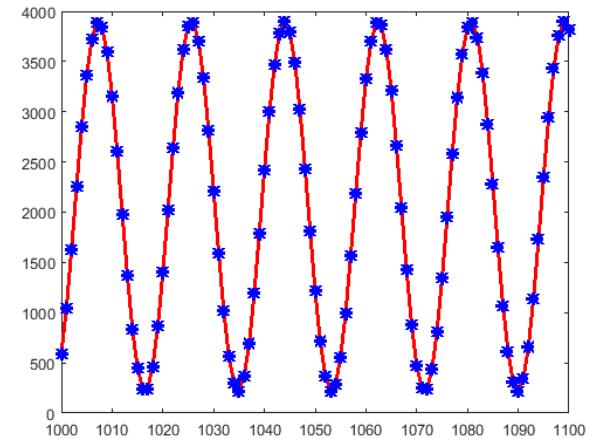
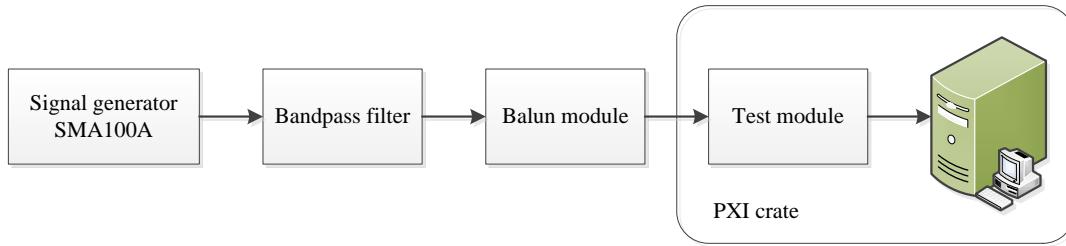


# ENOB test

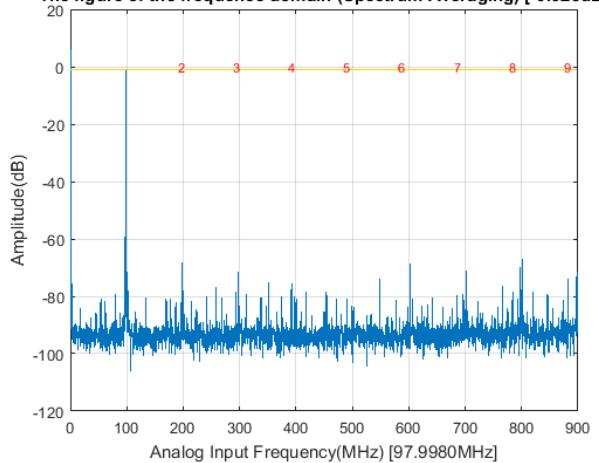
$$SINAD = 20\lg \frac{RMS_{signal}}{RMS_{(noise+distortion)}}$$

$$ENOB = \frac{SINAD - 1.76 \text{ dB}}{6.02}$$

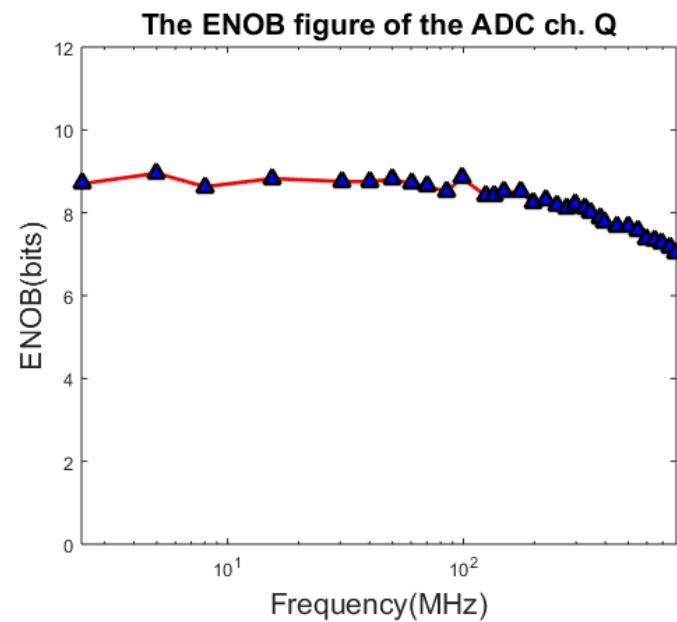
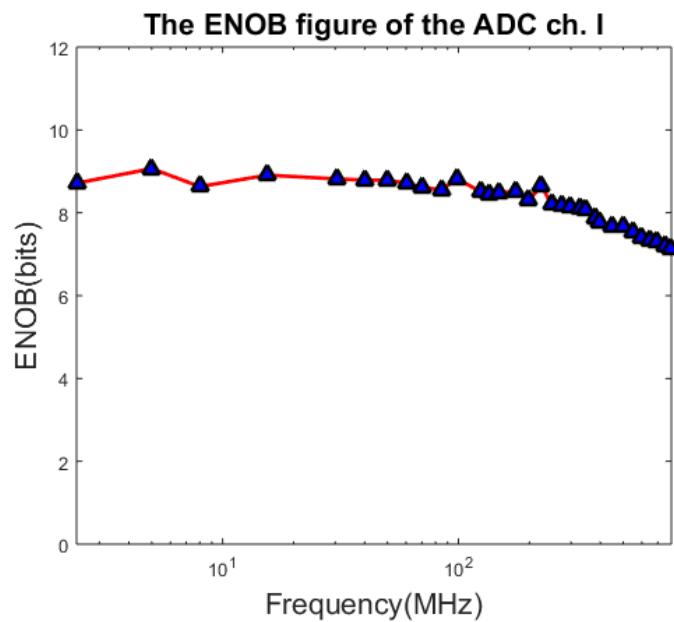
- IEEE STD 1241-2000



The figure of the frequency domain (Spectrum Averaging) [-0.923dB]

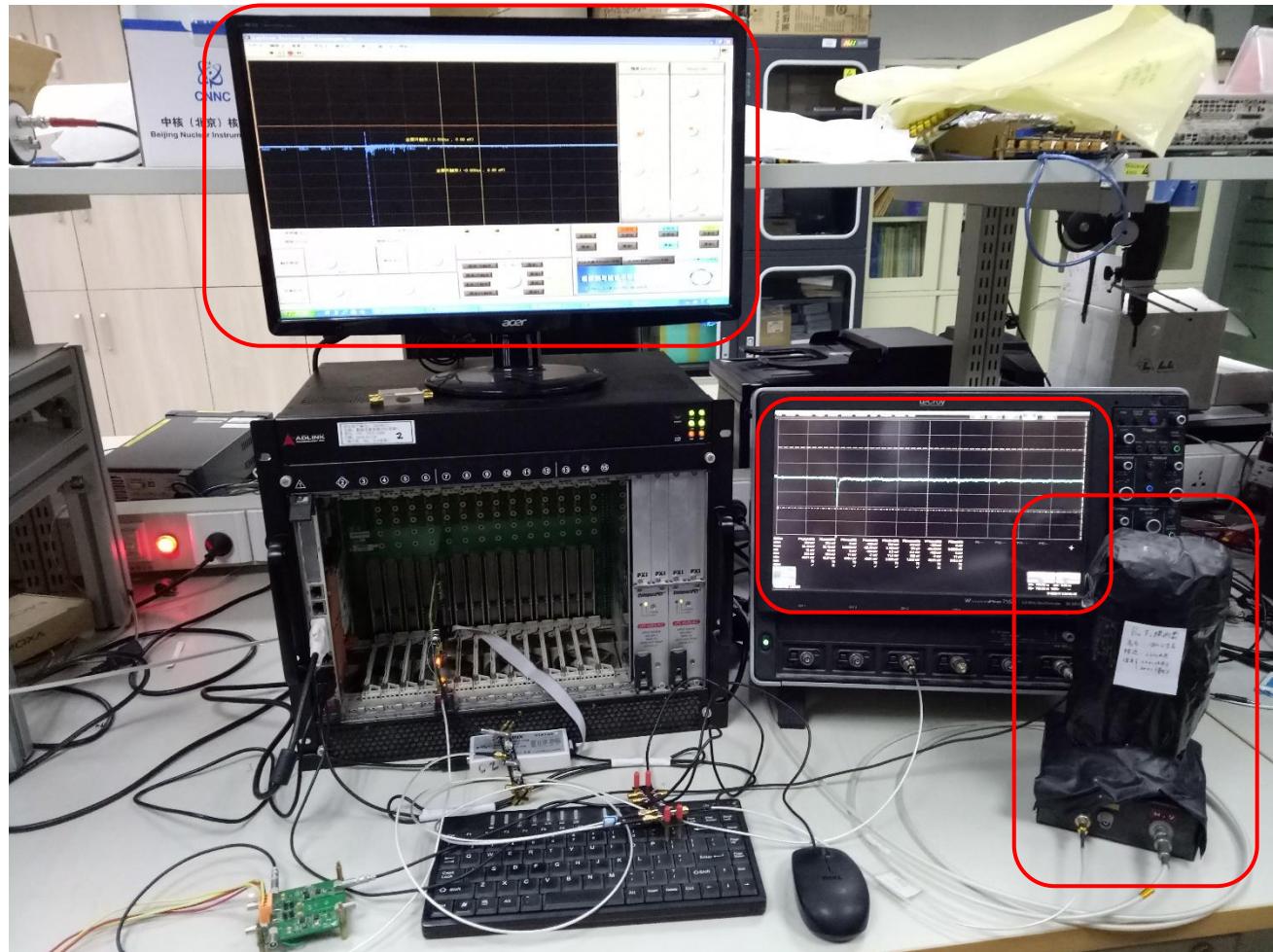


# Result@1.8GSPS



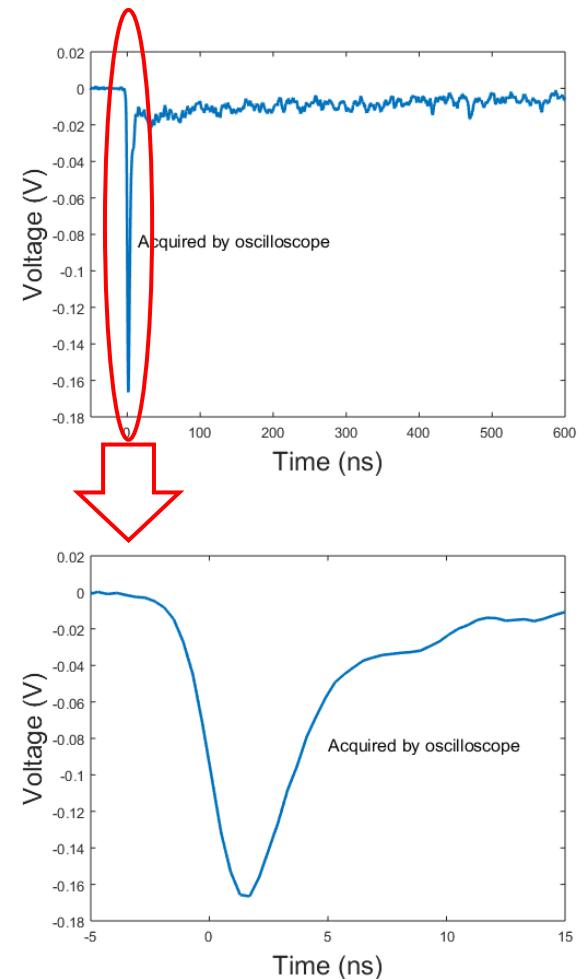
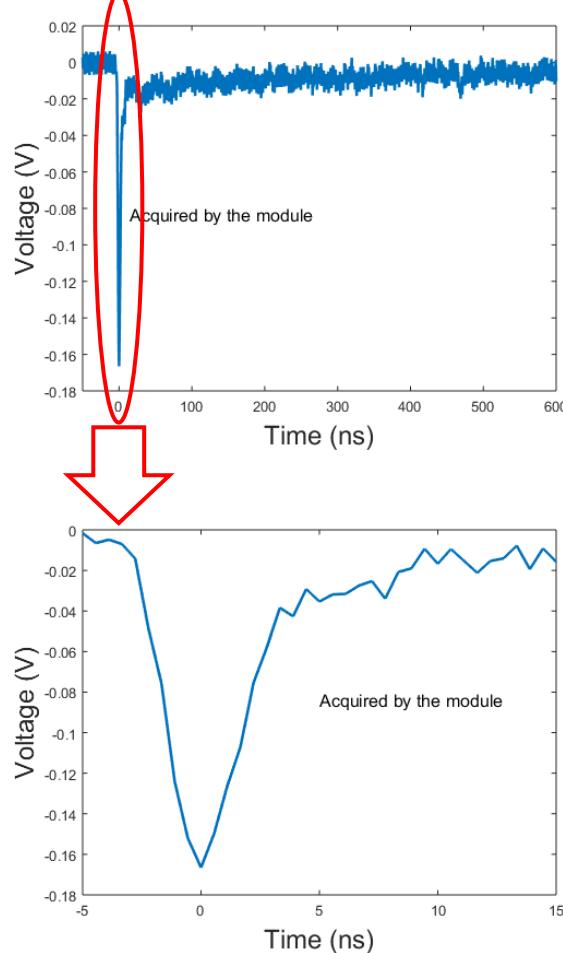


# BaF<sub>2</sub> with PMT





# Result vs. oscilloscope





# Next & Acknowledgment

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- **Next**

- Test with TPC
- Extract T & Q
- Improve data transmission bandwidth

- **Supported by**

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# MAHALO!