Contribution ID: **22** Type: **oral**

An SOI pixel sensor with in-pixel binary counters

Thursday, 25 May 2017 14:00 (18 minutes)

Results from an SOI pixel sensor with in-pixel binary counters are reported. It's been well known that the transition of output pattern within each counter would induce considerably large spurious signal on the nearby charge collection electrodes, which interferes with the detection of real signals. Among the various remedies investigated, Double-SOI process proved to be an effective cure thanks to the advancement in semi-conductor industry. The design concept of CPIXTEG3b, in particular the usage of the shiedling layer enabled by Double-SOI is covered in this talk. S-curve measurement reveals ENC around 60e- and sigma of threshold distribution less than 20 e-. The pixel array has demonstrated an excellent feature of zero noise with a low threshold around 800e-. The depletion of sensor and inefficiency at the square boundary of pixel have been studied using a synchrotron X-ray beam. The depletion depth reaches 130um under -100V bias. Charge sharing at the edge of two adjacent pixels can be corrected by properly setting the threshold, while at the corner where 4 pixels adjoin specific comparison logic is needed to cope with it. The success of CPIXTEG3b brings about a promising prospect for applications such as photon counting for the synchrotron light source and charged particle tracking for future e+e- collider.

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Session Classification: R4-Semiconductor detectors(6)

Track Classification: Semiconductor detectors