A Service-Oriented Platform for Embedded Monitoring Systems in the Belle II experiment

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Overview

- uSOP: a **Service-Oriented Platform** for embedded applications
- Hardware
- Software
- uSOP at work: monitoring complex detectors
  - Belle2, Beast2 @ KEK
- Conclusions
uSOP

- **uP-based, Service-Oriented Platform** for embedded applications
- Strongly oriented to SPI, I2C, JTAG, UART, with isolated power for peripherals and sensors
- Fully managed remotely
- 3U Eurocard native form factor, expandable
- Derived-from and compatible-with BeagleBone Black open-source project

The uSOP board

- Running Linux OS (Debian) – porting armv7l
- Full support for compilers and applications
- Kernels: major releases available – 3.x and 4.x
uSOP – uP and utilities

4 GB Flash eMMC

10/100 Ethernet

USB host

uSD

10/100 Ethernet (controls and management only. See next slide)

512 MB DDR3 RAM

5V, 500mA (typ)

Sitara AM3358

4 GB Flash eMMC

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Sitara AM3358

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Remote Management

1) LAN access to Sitara processor

2) LAN for board management

- Remote control over IP for:
  - uP Reset
  - Boot mode
  - Power on/off
- UART over IP:
  - Console
  - Bootloader

- Based on the latest version of Lantronix Xport-Pro
- µP Freescale MCF5208, MMU-less architecture, 8MB RAM, 16MB Flash
- SoC running uCLinux with a full cross-compiled SDK
uSOP – Peripherals/Intf

16 x GPIO
- Timer
- PWM
- Event Capture
- PRU

2 x RS232 (*)
- JTAG (*)

4 x 12 bit AIN (**)
+ 2 on-board power monitoring

2 x SPI (*)
2 x I2C (*)

- = fully isolated, 5V-12V supply
- ** = buffered
ΔΣ ADC – LTC2499 noise floor

- **uSOP bench test with LTC2499:**
  - ΔΣ ADC, 24 bit
  - I²C, powered by uSOP isolated supply
  - $V_{\text{in}} = 0\,\text{V}$, Input shorted to local ground
  - ~5 Hz sampling rate
  - 50 Hz filter
  - $V_{\text{ref}}$: 5V
  - Read-out by EPICS IOC
  - GUI by CSS/BOY

Source: linear.com
MONITORING IN BELLE II EXPERIMENT
The Belle2 EndCap at rest: monitoring during upgrade

- Minimal, stand-alone monitoring system at the EndCap ECL test station
- 4 sectors over 32 monitored to control the conditioning system (T, Rh)
- Up-time ≈ 2 year
- Data available via both EPICS and cloud
The T-Rh Controller board (LTC2983)

- Dual channel architecture, custom designed for the endcap readout
- each controller reads out two forward sectors (3x T, 1x Rh probes powered by uSOP) with galvanic isolation

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T-Rh Controller

- 20 UNIVERSAL INPUTS ALLOW COMMON HW SHARING FOR DIFFERENT SENSOR TYPES
- BUFFERED INPUTS ALLOW EXTERNAL PROTECTION AND FILTERING WITHOUT DROOP ERRORS
- 24-BIT ADCs AND 10PPM REFERENCE ENABLE BENCHTOP ACCURACY MEASUREMENTS
- ROTATABLE CURRENT SOURCES ELIMINATE THERMOCOUPLE EFFECTS IN RESISTIVE MEASUREMENTS
- STANDARD COEFFICIENTS STORED IN ROM ELIMINATE LOOKUP TABLES
- CUSTOM COEFFICIENTS STORED IN RAM ACCOMMODATE CUSTOM SENSORS
- BUILT-IN LINEARIZATION AND FAULTS ALLEVIATE CODING AND HOST PROCESSOR RESOURCES
- SPI INTERFACE PROVIDES CONVENIENT DEVICE CONFIGURATION AND SENSOR READOUT IN ºC OR ºF

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We have programmed the on-chip uP to perform a 3-cycle measurement and processing:
- (a) Inject current in Rsense and probe $\Delta V$ across thermistor
- (b) Set the current to obtain $\Delta V \sim 1$V (best ADC performance, low self-heating)
- (c) Invert $\Delta V$ polarity and take a second measurement, to cancel parasitic thermocouple effect by averaging
• 3 Hz read out speed achievable with good signal integrity up to 40m cable length
• Double exponential decays: full discharge in $O(1s)$
• BEAST2 (phase 1) is a detector that has taken data at SuperKEKB Interaction Point, to study beam background (see Miroslav Gabriel talk)
• uSOP has been used to monitor T and Rh of the 18 BEAST2 crystals (LYSO, CsI, CsI(Tl)). Data available via EPICS and cloud display (Beebotte)
• uSOP used also to monitor upset in FPGA exposed to beam background (see Raffale Giordano talk)
ECL backward installation

- ECL backward installed in January 2017
- uSOP monitoring connected
The ECL EndCap monitoring system

- The final monitoring system has been installed at KEK during 2016
- Forward and Backward ECL:
  - 2112 CsI(Tl) crystals, 32 sectors
  - T and Rh monitor, 128 analog channels (96 thermistors + 32 Rh probes)
- Features:
  - 3-wire read-out to cancel the 40m cable stray resistance
  - Stray thermocouple effects cancellation
  - 4 uSOP boards, 8 T controllers with 24 bit ADCs for each endcap
  - 6U, 12HP form factor, shielded
  - Selective ground scheme to avoid loops
  - Read-out and controls via network
EPICS Experimental Physics and Industrial Control System

- EPICS (http://www.aps.anl.gov/epics/) is a set of Open Source software tools, libraries and applications developed collaboratively and used worldwide to create distributed soft real-time control systems for scientific instruments such as a particle accelerators, telescopes and other large scientific experiments.

- On uSOP:
  - Straightforward compilation on ARM
  - Variety of EPICS extensions available on board:
    - ALH (ALarm Handler)
    - PV gateway
    - Asyn
    - StreamDevice
    - Autosave
  - IOCs for:
    - Linear LTC2499 (I2C)
    - Linear LTC2983 (SPI)
    - Sitara ADC (parallel)
Displaying variables

Grafana metrics dashboards

Temperature

Humidity

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uSOP performance monitoring

Network monitoring: return time trip

CPU usage display monitoring

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What’s next

• **Forward endcap and Slow control integration**
  – Cabling of forward wheel (starting from August)
  – Graphical user interface based on CSS
  – Integration with the EPICS archiver

• **Going plus...**
  – Texas instruments has released the 1.5 GHz dual-core Cortex A15 Sitara AM5728
  – On this uP, we started design of a new platform with FPGA and dual high-speed ADC: uSOP+
  – Beyond monitoring: DSP, hardware processing, high speed links,...

• **uSOP Rad-tolerance tests**
  – TID degradation studies and SEE induced error (cooperation with ESA people)
  – *System hangs* analysis as function of irradiation level
  – Different OS footprints to evaluate the impact on failure rate
Conclusions

- uSOP has been intensively tested at KEK, starting from Apr. 2015
- Stable and reliable LINUX platform, with uptime ≈ 2 years
- Hardware controllers for all most common serial busses
- Fully (re)configurable and managed remotely (from brick to fully functional)
- Designed to work as a stand-alone unit, yet easy to deploy in complex control infrastructures
- EPICS compliant, IOCs developed for all the needed DAQ units
BACKUP
Data publishing architecture
Cortex A Cores (32bit)

<table>
<thead>
<tr>
<th>ARMv7-A</th>
<th>Cortex-A7&lt;sup&gt;[24]&lt;/sup&gt;</th>
<th>Application profile, ARM / Thumb / Thumb-2 / DSP / VFPv4-D16 FPU / NEON / Jazelle RCT and DBX, 1–4 cores / optional MPCore, snoop control unit (SCU), generic interrupt controller (GIC), accelerator coherence port (ACP)</th>
<th>4–64 KB / 4–64 KB L1, MMU + TrustZone</th>
<th>1.57 DMIPS/MHz per core</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cortex-A7&lt;sup&gt;[24]&lt;/sup&gt;</td>
<td>Application profile, ARM / Thumb / Thumb-2 / DSP / VFPv4-D16 FPU / NEON / Jazelle RCT and DBX / Hardware virtualization, in-order execution, superscalar, 1–4 SMP cores, MPCore, Large Physical Address Extensions (LPAE), snoop control unit (SCU), generic interrupt controller (GIC), ACP, architecture and feature set are identical to A15, 8–10 stage pipeline, low-power design&lt;sup&gt;[25]&lt;/sup&gt;</td>
<td>8–64 KB / 8–64 KB L1, 0–1 MB L2, MMU + TrustZone</td>
<td>1.9 DMIPS/MHz per core</td>
<td></td>
</tr>
<tr>
<td>Cortex-A5&lt;sup&gt;[27]&lt;/sup&gt;</td>
<td>Application profile, ARM / Thumb / Thumb-2 / VFPv3 FPU / NEON / Jazelle RCT and DAC, 13-stage superscalar pipeline</td>
<td>16–32 KB / 16–32 KB L1, 0–1 MB L2 opt ECC, MMU + TrustZone</td>
<td>Up to 2000 (2.0 DMIPS/MHz in speed from 000 MHz to greater than 1 GHz)</td>
<td></td>
</tr>
<tr>
<td>Cortex-A9&lt;sup&gt;[27]&lt;/sup&gt;</td>
<td>Application profile, ARM / Thumb-2 / DSP / Optional VFPv3 FPU / Optional NEON / Jazelle RCT and DBX, out-of-order speculative issue superscalar, 1–4 SMP cores, MPCore, snoop control unit (SCU), generic interrupt controller (GIC), accelerator coherence port (ACP)</td>
<td>16–64 KB / 16–64 KB L1, 0–8 MB L2 opt parity, MMU + TrustZone</td>
<td>2.5 DMIPS/MHz per core, 10,000 DMIPS @ 2 GHz on Performance Optimized TSMC 40G (dual-core)</td>
<td></td>
</tr>
<tr>
<td>Cortex-A12&lt;sup&gt;[23]&lt;/sup&gt;</td>
<td>Application profile, ARM / Thumb-2 / DSP / VFPv4 FPU / NEON / Hardware virtualization, out-of-order speculative issue superscalar, 1–4 SMP cores, Large Physical Address Extensions (LPAE), snoop control unit (SCU), generic interrupt controller (GIC), accelerator coherence port (ACP)</td>
<td>32–64 KB / 32 KB L1, 256 KB–8 MB L2</td>
<td>3.0 DMIPS/Hz per core</td>
<td></td>
</tr>
<tr>
<td>Cortex-A15&lt;sup&gt;[25]&lt;/sup&gt;</td>
<td>Application profile, ARM / Thumb / Thumb-2 / DSP / VFPv4 FPU / NEON / Integer divide / fused MAC / Jazelle RCT / hardware virtualization, out-of-order speculative issue superscalar, 1–4 SMP cores, MPCore, Large Physical Address Extensions (LPAE), snoop control unit (SCU), generic Interrupt controller (GIC), ACP, 15-24 stage pipeline&lt;sup&gt;[25]&lt;/sup&gt;</td>
<td>32 KB w/parity / 32 KB w/ECC L1, 0–4 MB L2, L2 has ECC, MMU + TrustZone</td>
<td>At least 3.5 DMIPS/Hz per core (up to 4.01 DMIPS/Hz depending on implementation)&lt;sup&gt;[20]&lt;/sup&gt;</td>
<td></td>
</tr>
<tr>
<td>Cortex-A17</td>
<td>Application profile, ARM / Thumb / Thumb-2 / DSP / VFPv4 FPU / NEON / Integer divide / fused MAC / Jazelle RCT / hardware virtualization, out-of-order speculative issue superscalar, 1–4 SMP cores, MPCore, Large Physical Address Extensions (LPAE), snoop control unit (SCU), generic Interrupt controller (GIC), ACP</td>
<td></td>
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<tr>
<td>ARMv8-A</td>
<td>Cortex-A3&lt;sup&gt;[21]&lt;/sup&gt;</td>
<td>Application profile, AArch64, NEON advanced SIMD</td>
<td>8–64 KB w/optional parity / 8–64 KB w/optional ECC L1 per core, 128 KB–1 MB L2 w/optional ECC shared</td>
<td></td>
</tr>
</tbody>
</table>
3-WIRE READOUT

3-WIRE SENSOR w/DUAL MATCHED CURRENT EXCITATION. CONVERTS WITH A SINGLE DIFFERENTIAL MEASUREMENT. ADSELF-COMPENSATES FOR MATCHED +/- LEAD RESISTANCES.
Beaglebone Black

BeagleBone Black Development Board

(Key Document)
- BeagleBone Black Quick Start Guide (external link)
- BeagleBone Black System Reference Manual (external link)
- View All Technical Documents (6)

Description
BeagleBone Black is a low-cost, open source, community-supported development platform for ARM® Cortex™-A8 processor developers and hobbyists. Boot Linux in under 10 seconds and get started on Sitara™ AM335x ARM Cortex-A8 processor development in less than 5 minutes with just a single USB cable.

BeagleBone Black ships with the Debian GNU/Linux™ in onboard FLASH to start evaluation and development. Many other Linux distributions and operating systems are also supported on BeagleBone Black including:
- Ubuntu
- Android
- Fedora

BeagleBone Black’s capabilities can be extended using plug-in boards called “capses” that can be plugged into BeagleBone Black’s two 40-pin dual-row expansion headers. Capses are available for VGA, LCD, motor control, prototyping, battery power and other functionality. More information.

Visit the BeagleBone Black Support Community
AM5728 Sitara™ Processors
Silicon Revision 2.0

1 Device Overview

1.1 Features

- Three Video Input Port (VIP) Modules
- General-Purpose Memory Controller (GPMC)
- Enhanced Direct Memory Access (EDMA) Controller
- 2-Port Gigabit Ethernet (GMAC)
- Sixteen 32-Bit General-Purpose Timers
- 32-Bit MPU Watchdog Timer
- Five Inter-Integrated Circuit (IIC) Ports
- HDC™/I-Wire® Interface
- Ten Configurable UART/I2C/I2R Modules
- Four Multichannel Serial Peripheral Interfaces (MCSPis)
- Quad SPI Interface (QSPI)
- SATA Gen2 Interface
- Multichannel Audio Serial Port (MCASP)
- SuperSpeed USB 3.0 Dual-Role Device
- High-Speed USB 2.0 Dual-Role Device
- PCIe Express® 2.0 Subsystems With Two 5-Gbps Lanes
  - One 2-lane Gen2-Compliant Port
  - or Two 1-lane Gen2-Compliant Ports
- Dual Controller Area Network (DCAN) Modules
  - CAN 2.0B Protocol
- Up to 247 General-Purpose I/O (GPIO) Pins
- Power, Reset, and Clock Management
- On-Chip Debug With JTAG Technology
- 28-nm CMOS Technology
- 23 mm x 23 mm, 0.8-mm Pitch, 760-Pin BGA (ABC)

- For Silicon Revision 1.1 Information, see SPR915
- ARM® Dual Cortex®-A15 Microprocessor Subsystem
- Up to 2 C66x™ Floating-Point VLIW DSP
  - Fully Object-Code Compatible With C67x™ and C64x+™
  - Up to Thirty-two 16 x 16-Bit Fixed-Point Multiplies per Cycle
- Up to 2.5MB of On-Chip L3 RAM
- Two DDR3/DDR3L Memory Interface (EMIF) Modules
  - Supports up to DDR3-1066
  - Up to 2GB Supported per EMIF
- Dual ARM® Cortex®-M4 co-processors
- IVA-HD Subsystem
- Display Subsystem
  - Full-HD Video (1920 x 1080p, 60 fps)
  - Multiple Video Input and Video Output
  - 2D and 3D Graphics
  - Display Controller With DMA Engine and up to Three Pipelines
  - HDMI™ Encoder: HDMI 1.4a and DVI 1.0 Compliant
- 2x Dual-Core Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-JCSS)
- 2D-Graphics Accelerator (GB2D) Subsystem
  - Vivante™ GC320 Core
- Video Processing Engine (VPE)
- Dual-Core PowerVR SGX544™ 3D GPU
- Crypto Hardware Accelerators
  - AES, SHA, RNG, DES and 3DES
BELLE2 TALKS AT TIPP’17

• The Belle II / SuperKEKB Commissioning Detector - Results from the First Commissioning Phase (Gabriel MIROSLAV)
• Belle-II Silicon Vertex Detector (Bahinipati SEEMA)
• Integration of readout of the vertex detector in the Belle II DAQ system (Tomoyuki KONNO)
• Thermal mockup studies of Bellell vertex detector (Hua YE)
• CLAWS - A Plastic Scintillator / SiPM based Detector measuring Backgrounds during the Commissioning of SuperKEKB (Windel HENDRIK)
• Radiation Monitoring with Diamond Sensors for the Belle-II Vertex Detector (Chiara LA LICATA)
• Study of the Calorimeter Trigger Simulation for the Belle II experiment (In-soo LEE)
• Commissioning and Initial Performance of the Belle II iTOP PID Subdetector (Gary VARNER)
• Belle II iTOP optics: design, construction, and performance (Boqun WANG)
• Integration of data acquisition systems of Belle II outer-detectors for cosmic ray test (Satoru YAMADA)
• The Aerogel Ring Image Cherenkov counter for particle identification in the Belle II experiment (Tomoyuki KONNO)
• Behavior of 144ch HAPDs for the Belle II Aerogel RICH in the magnetic field (Ogawa KAZUYA)
• Development of the slow control system for the Belle II ARICH counter (Masanobu YONENAGA)
• Assembly of a Silica Aerogel Radiator Module for the Belle II ARICH System (Makoto TABATA)
• Improvement of the MCP-PMT performance under a high count rate (Kodai MATSUOKA)
• An general high performance xTCA compliant and FPGA based Data Processing Unit for trigger and data acquisition and trigger applications (Mr. Jingzhou ZHAO JINGZHOU)
...moving to CSS monitoring panels
Beagleboard X15

BeagleBoard-X15

Sign up below for notifications of availability and approved distributors to place orders. Check the wiki for the latest production update. If you need a board right away and don’t care about FCC/CE compliance, you can get an early version of X15 as the processor module of the AM5728 EVM.

What is BeagleBoard-X15?

BeagleBoard-X15 is the top performing, mainline Linux enabled, power-users’ dream board with a core tailored for every computing task and a highspeed interface for every connectivity need. Give your algorithms room to stretch!

Processor: TI AM5728 2×1.5-GHz ARM® Cortex-A15
- 2GB DDR3 RAM
- 4GB 8-bit ElMV on-board flash storage
- 2D/3D graphics and video accelerators (GDRs)
- 2×700-MHz C66 digital signal processors (DSPs)
- 2×ARM Cortex-A4 microcontrollers (MCUs)
- 4×32-bit programmable real-time units (PRUs)

Software Compatibility
- Debian
- Android
- Ubuntu
- Clouds: DE on Node.js
- plus much more

Connectivity
- 2×Gigabit Ethernet
- 3×SuperSpeed USB 3.0 host
- HighSpeed USB 2.0 host
- eSATA (500mA)
- Full-size HDMI video output
- microSD card slot
- Stereo audio in and out
- 4×68-pin headers with PCIe, LCD, mSATA
- and much more...

Register your interest

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