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Phase-I Trigger Readout Electronics Upgrade for the ATLAS Liquid-Argon Calorimeters

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On behalf of the ATLAS Liquid Argon Calorimeter group

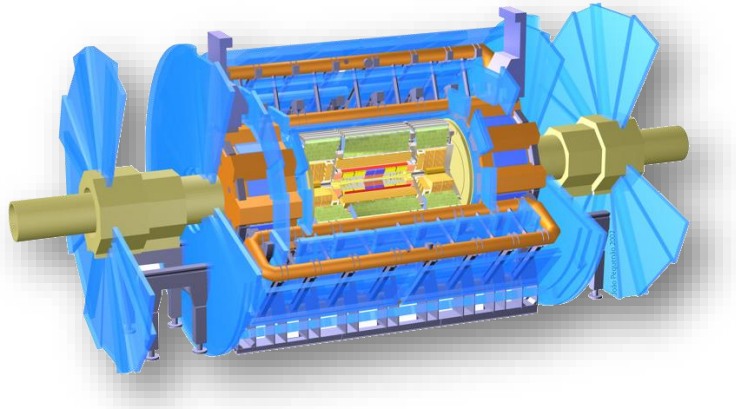
Outline

- Introduction
  - LHC, ATLAS, LAr
  - Phase I Upgrade
- LAr Front End Electronics
  - Baseplane, LSB
  - LTDB with custom ASICs
- LAr Back End Electronics
  - Carrier and Latome
- Demonstrator
- Summary

Introduction

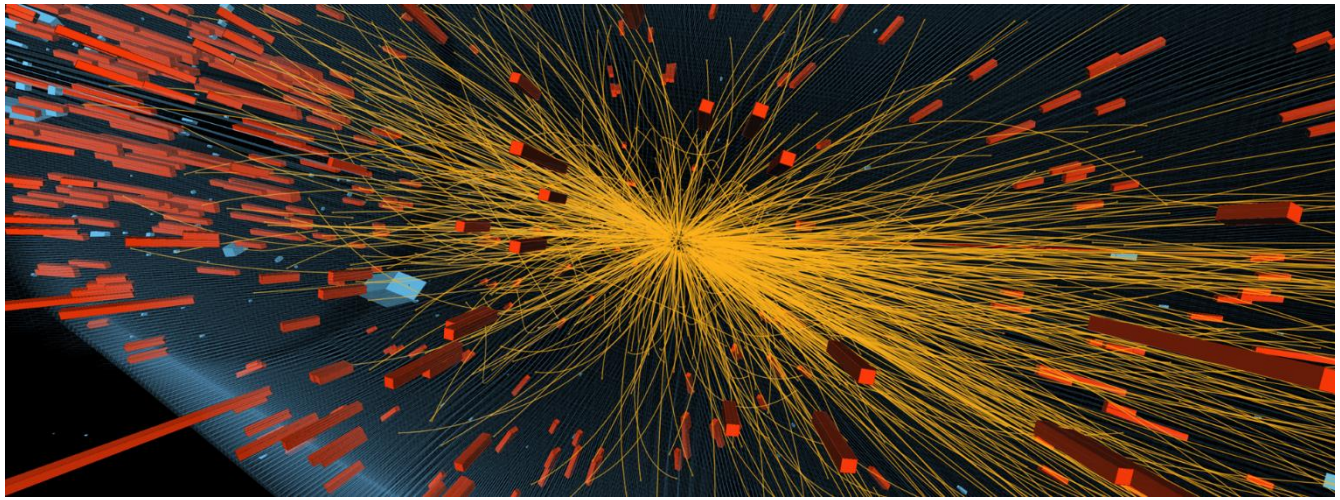
Context – LHC and ATLAS

- **Large Hadron Collider** (LHC) at CERN, Geneva, Switzerland
  - 27km circumference
  - depth between 50 to 175m
  - four collision points
- **A Toroidal LHC ApparatuS:** ATLAS
  - 46m long, 25m diameter and 7000 tons
- **Purpose**:
  - Answer fundamental physics questions about elementary particles and their interactions



Two phase upgrade planned for LHC, ATLAS upgrade:

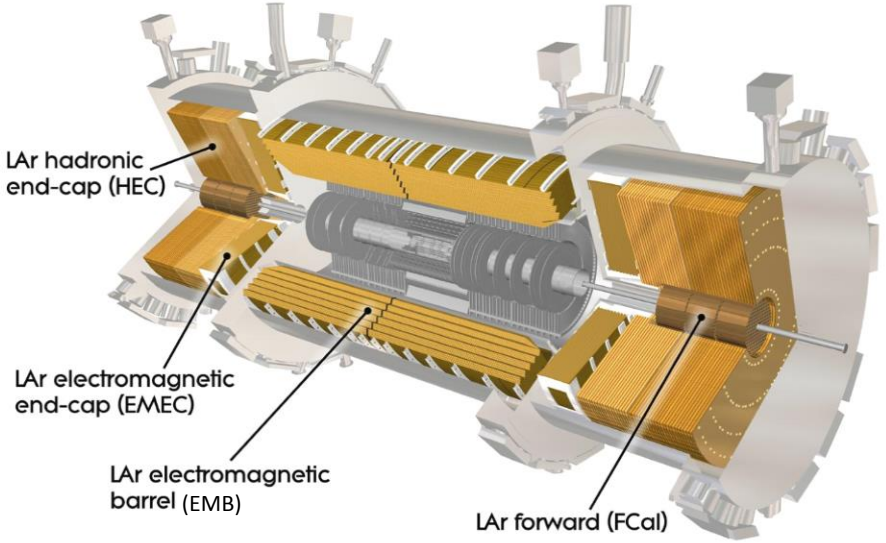
- **Phase-I** (2021-2023)
  - upgrade of trigger path, installation in 2019-2020
  - $L \cong 3 \times 10^{34} cm^{-2} s^{-1}$
- **Phase-II** (after 2025)
  - upgrade of data path, installation in 2024-2025
  - $L \cong 7.5 \times 10^{34} cm^{-2} s^{-1}$

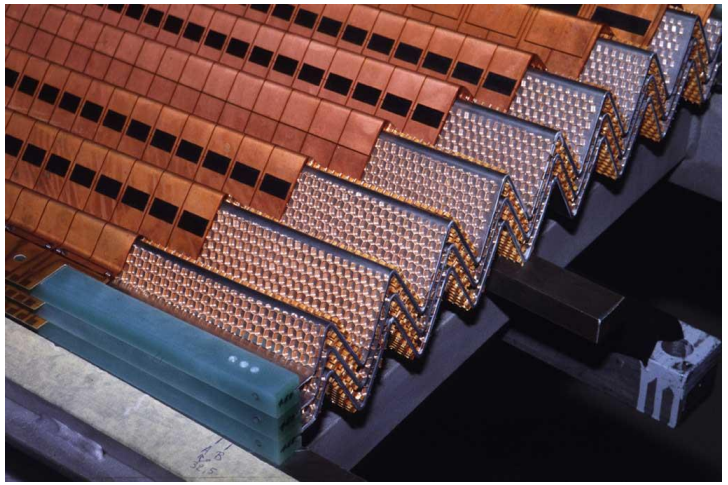


The Liquid Argon (LAr) Calorimeter

The **LAr calorimeter** is a sampling calorimeter with accordion-shaped lead absorbers, Liquid Argon as active material and copper-kapton electrodes.

- 180k channels for the full readout of the electromagnetic (EMB+EMEC), hadronic (HEC) and Forward (FCal) calorimeters
- 3k channels for analog Trigger readout
- Front End crates: 1524 Front End Boards (FEB)
- Back End crates: 192 Readout Out Driver boards (ROD)





LAr Calorimeter played a critical role for Higgs Boson discovery with two photons as a final state.

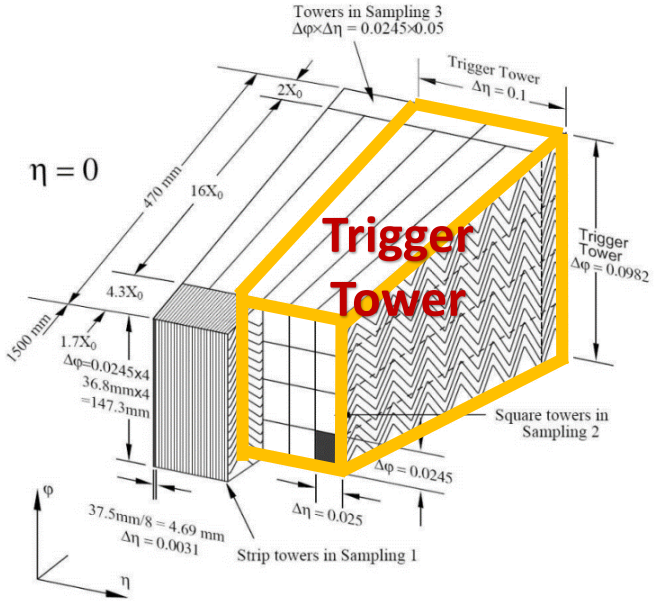
The current electronics

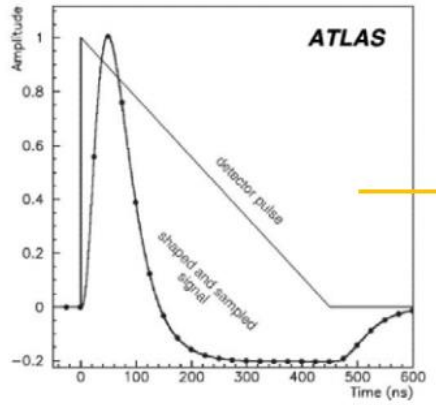
Regular (full granularity) readout:

- Cells signals are amplified, shaped, sampled, digitized at 40MHz
- Data are transmitted at 100 kHz upon level-1 trigger

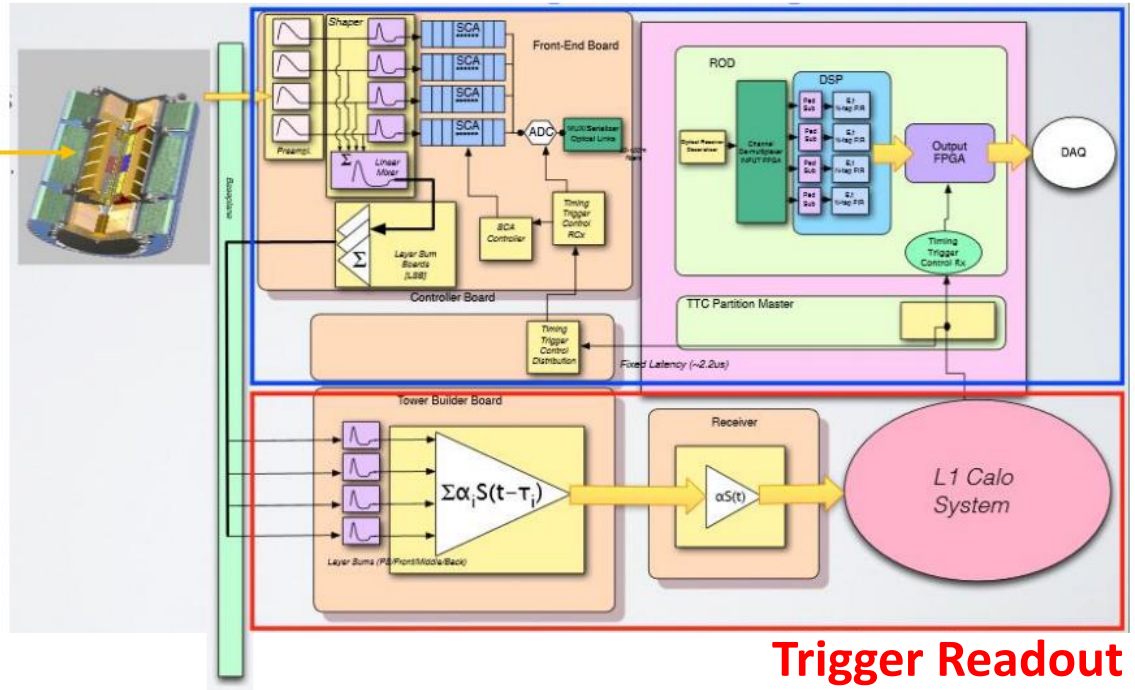
Trigger readout:

- Summing signals on Layer Sum Board (LSB)
- Tower Builder Board (TBB) to form 0.1×0.1 ($\Delta\eta \times \Delta\phi$) trigger towers: analog signals sent to L1 Calo system





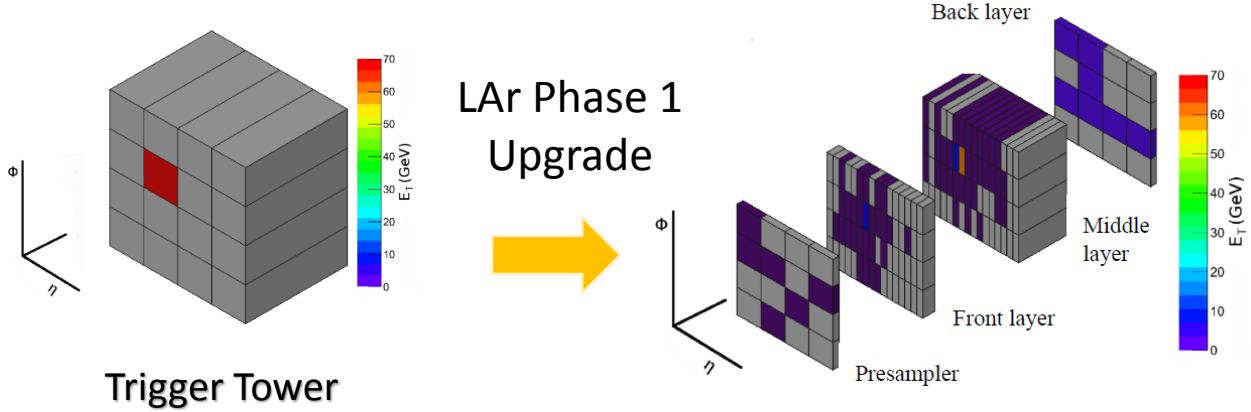
Regular Readout



Trigger Readout

Calorimeter Upgrade

LAr Phase-I upgrade: **new calorimeter trigger electronics** with increased granularity and functionality for LAr calorimeter level 1 trigger

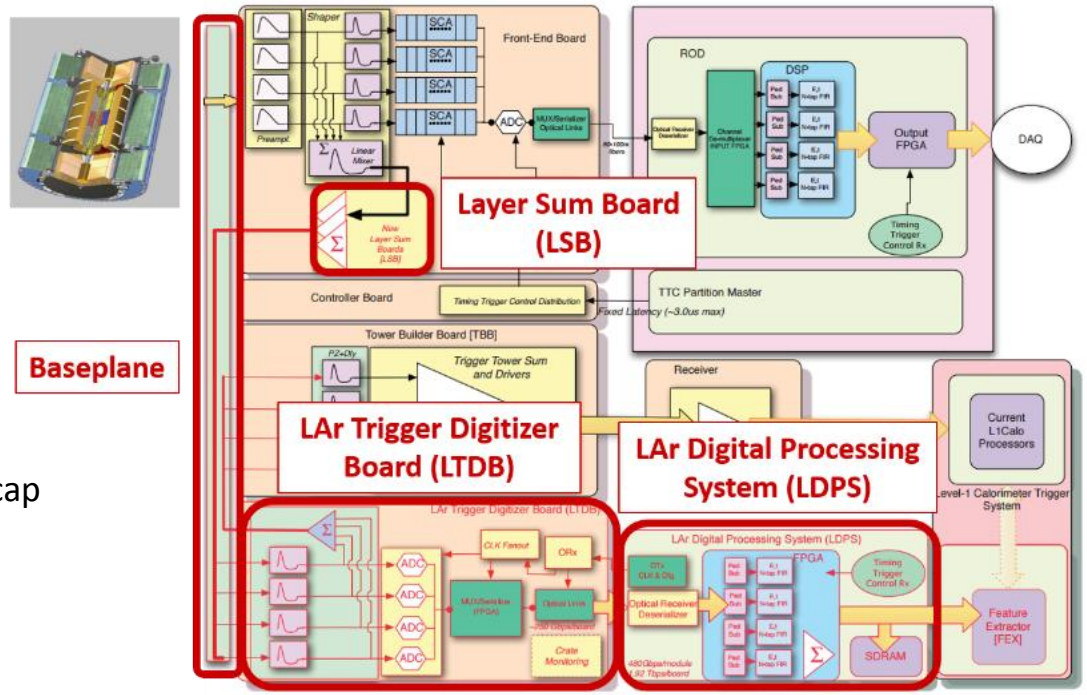


Trigger Tower to Super Cells:

- 10 times granularity increase per each trigger tower
- Information provided for each calorimeter layer for the full η range
- Finer segmentation in the front and middle layers of the EM barrel and endcap
- Higher resolution and shower information

New FE and BE electronics:

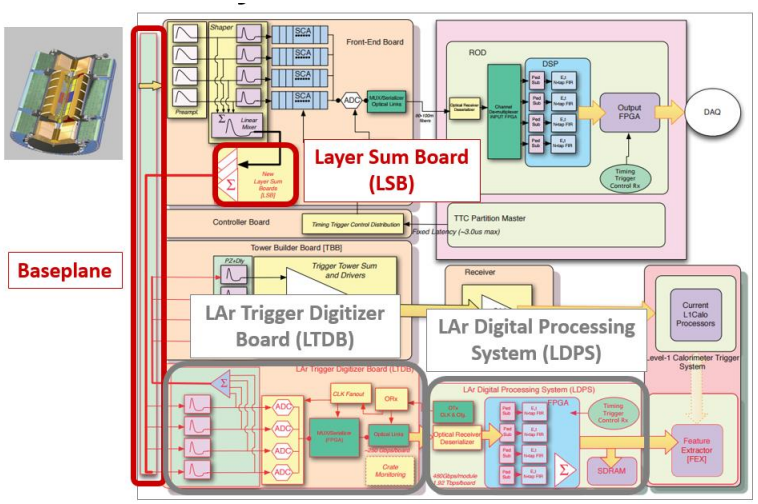
- 40 MHz digitization with 12 bit precion
- Dense and high speed data transfer
- Real time data processing with a fixed latency on FPGA



➢ Deal with the **luminosity increase,** maintaining a **low-pT lepton threshold** and keeping the **same trigger bandwidth** with respect to Run2

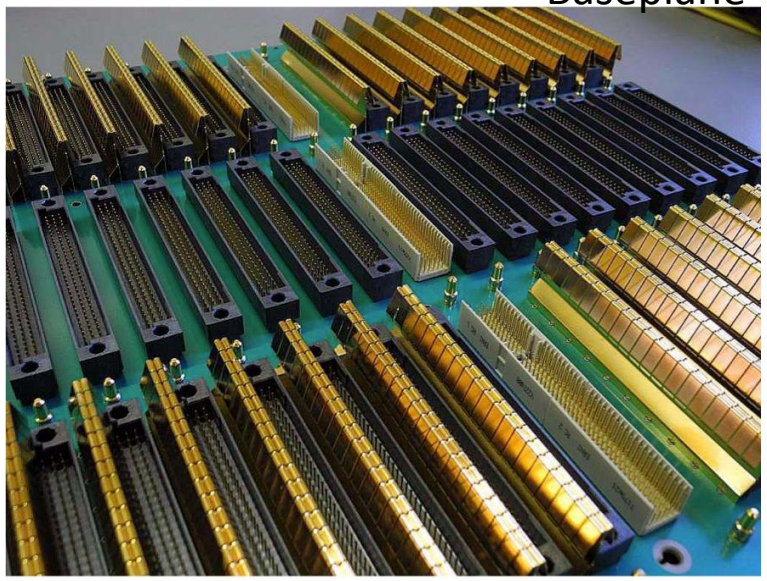
Front-End (FE) Upgrade

FE electronics components

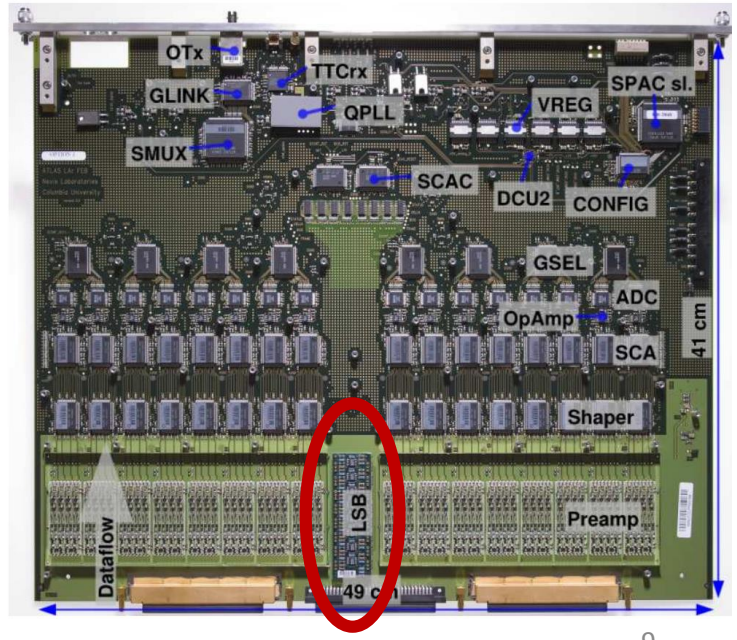


- **New Layer Sum Boards (LSB)** to perform analog sums for super cells
- **New Baseplane** to keep compatibility with existing setup and route new SC signals
- **LAr Trigger Digitizer Boards (LTDB)** with radiation-tolerant custom ASICs
  - ADC
  - Serializer (LOCx2)
  - Transmitter driver (LOCld)

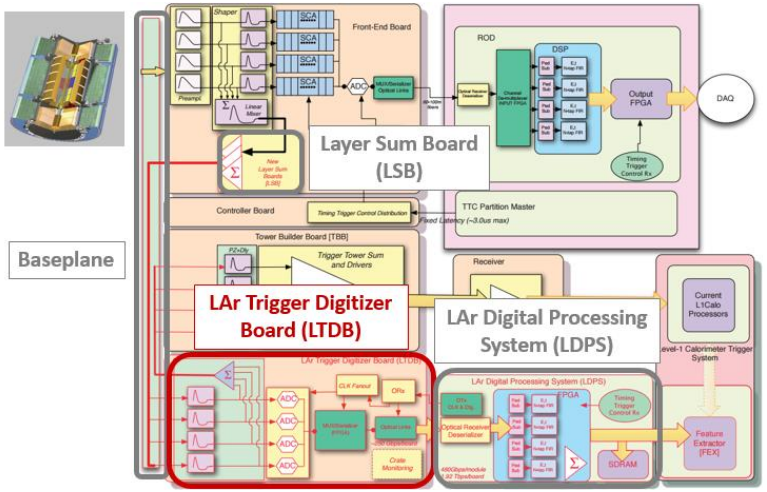
Baseplane



FEB currently installed on the detector



LAr Trigger Digitizer Board (LTDB)

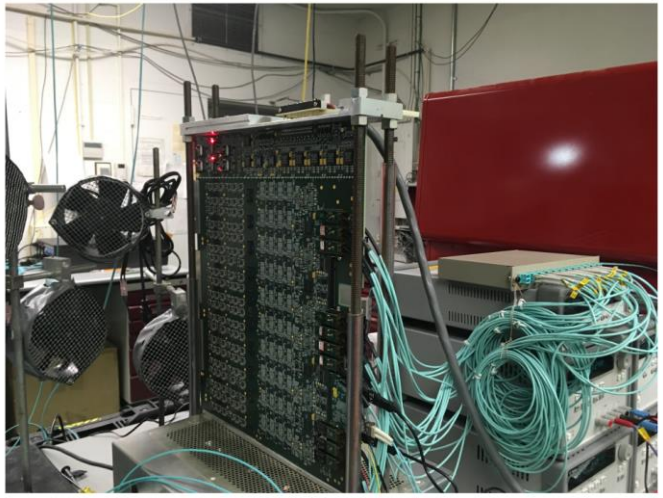


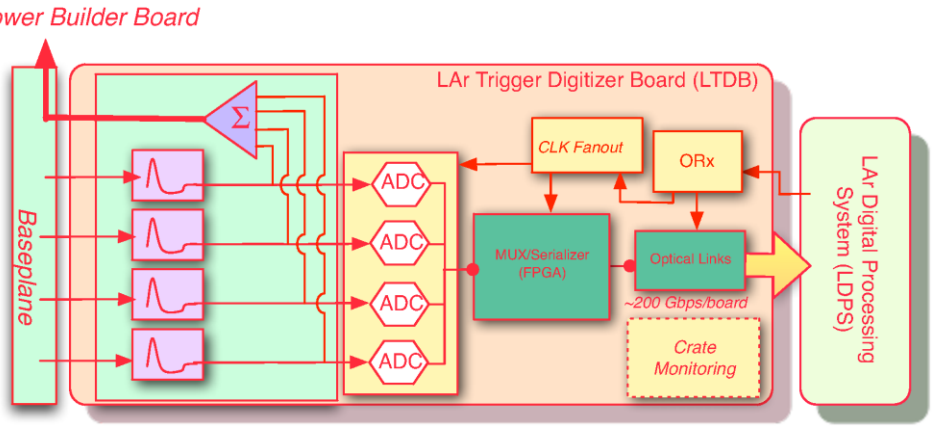
- 124 LTDBs to readout the 34k Super Cells of the LAr calorimeter
- 1 LTDB handles analog input up to 320 Super Cells
- Digitizes all analog signals at 12 bits @ 40MHz using 80 custom ADCs
- Generate analog sums to keep compatibility with old system
- Transmits digital signals using 40 optical links @ 5.12Gbps via custom ASICs

- Receive LHC clock and Trigger signals through 5 GBTx links
- Analog and Digital part are merged at the gerber file level
- Power section is realized on a mezzanine (PDB)

- Phase-II compatible

LTDB prototype



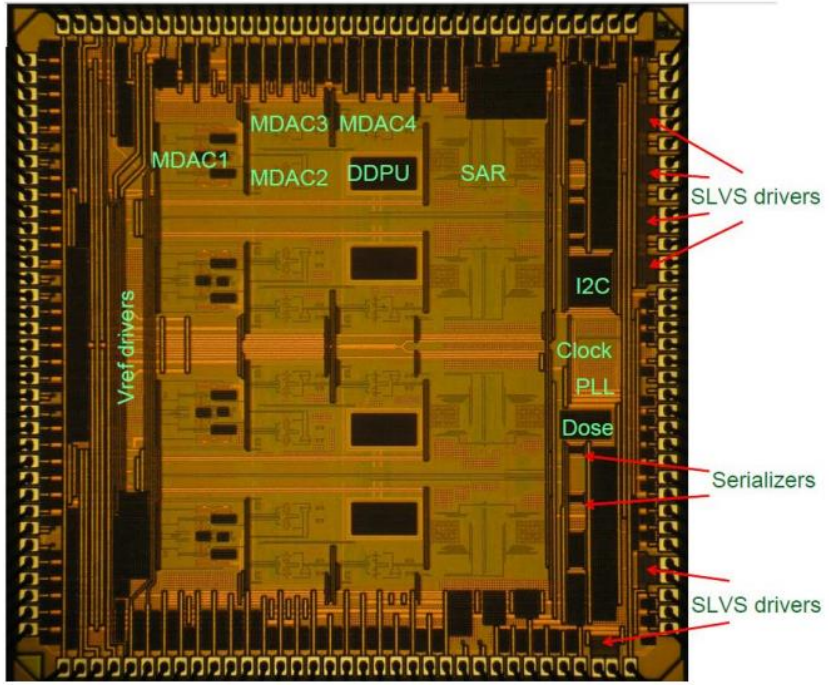


PDB

LTDB: custom ASICs (1)

ADC

- Quad 12 bits hybrid pipeline SAR ADC (IBM8RF 130nm CMOS)
- 40 MSPS
- ENOB 11 bits
- Dynamic range
  - Typically 11.8 bits
- Power dissipation < 50 mW/channel
- 112.5 ns latency
- Die:
  - 3.6 x 3.6 mm
  - 72 pins QFN



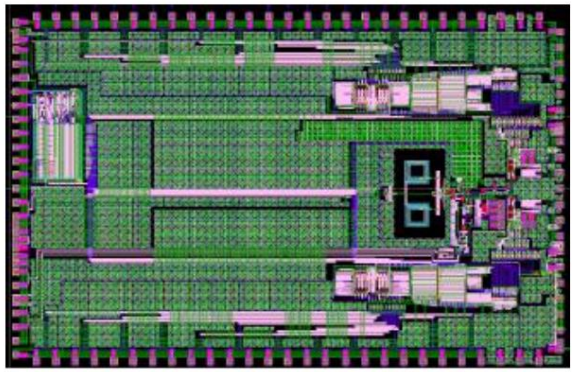
Status

- New test board is being developed to screen and categorize the production chips quickly
- 180 recently produced Nevis15 chips to develop and validate the QA/QC procedures
- Radiation tolerance for Nevis ADC designs was established up to ~10 MRad (requirement of 100 kRad)

LTDB: custom ASICs (2)

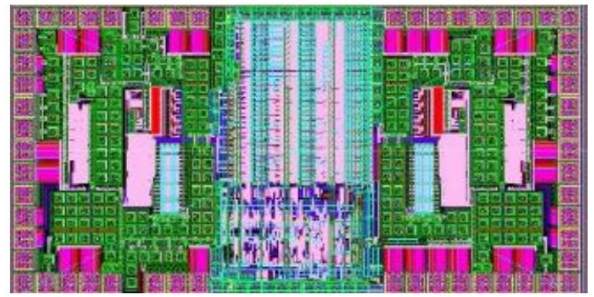
LOCx2:

- Silanna Foundry 250 nm, Silicon-on-Sapphire
- DUAL 8 x 14 bits serializer
- 5.12 Gbps outputs
- Nevis ADC compatible
- Power consumption 1 W
- Fixed Latency < 75 ns
- Die:
  - 6.036 x 3.68 mm
  - 100 pins QFN



LOCld:

- Dual channel VCSEL driver
- Die:
  - 2.114x1.090mm
  - 40 pins QFN

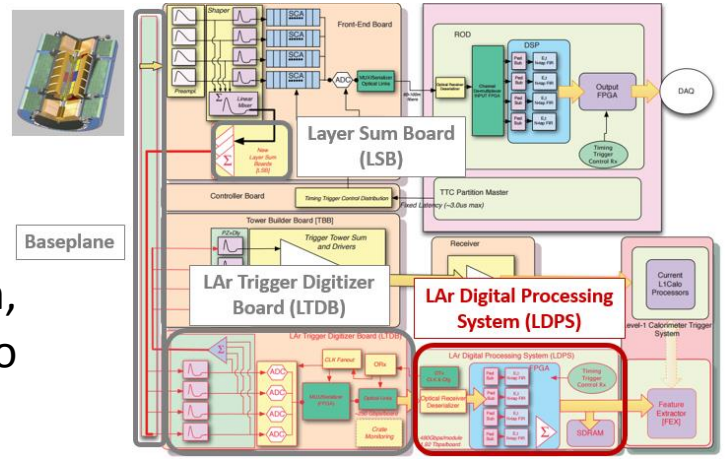


Status:

- The wafers of the baseline ASICs, LOCx2 and LOCld, have been produced and soon will be tested
- Both ASICS radiation tolerant
  - Irradiated up to 200 krad
  - No change in the output eye diagram has been observed

Back-End (BE) Upgrade

LAr Digital Processing Blade(LDPB)

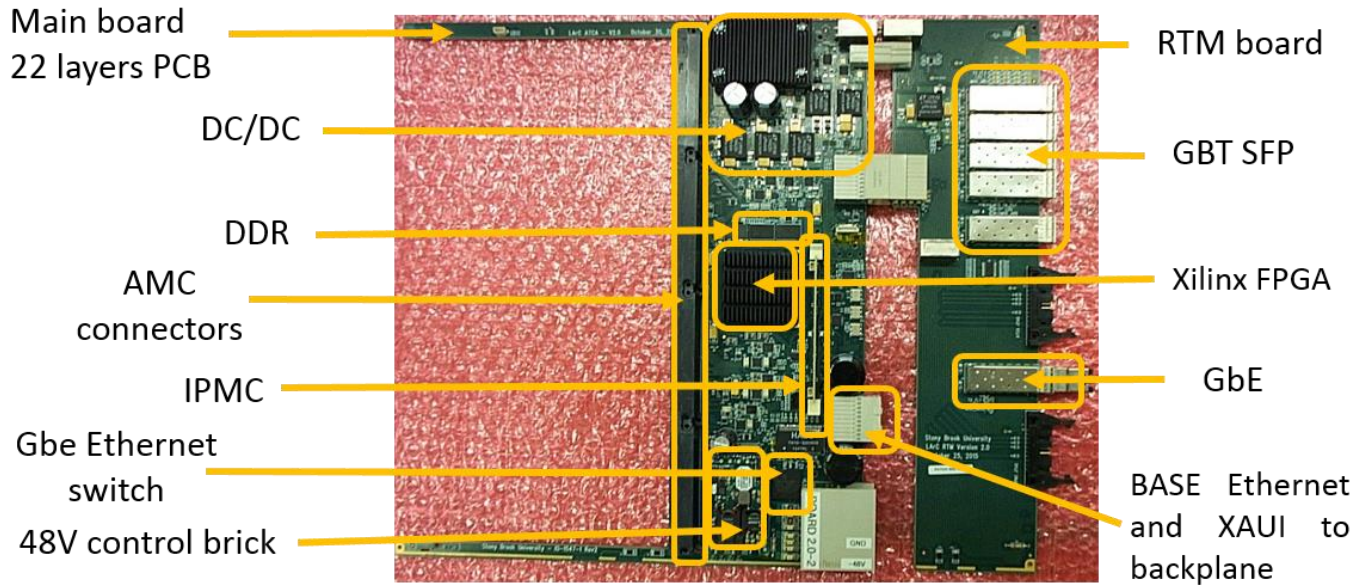


LDPB: **receives** digital SC data from the LTDBs of the upgraded FE system, **reconstructs** E_TSC (the transverse energy of each SC), and **transmits** the results to the Level-1 Calorimeter Trigger System every 25 ns.

Total number of boards:
32 ATCA Carrier board and 128 AMC mezzanine (LATOME) boards

- ATCA Carrier board + RTM
  - Monitoring data through RTM and ATCA
- 4 LATOME per each Carrier
  - main data flow only through LATOME (in: 20 Tbps, out: 41 Tbps in total)
- ARRIA10 (Altera) and Virtex7 (Xilinx) FPGAs
- 192 input fibres @ 5.12 Gbps
- 192 output fibres @ 11.2 Gbps

LDPB Carrier board

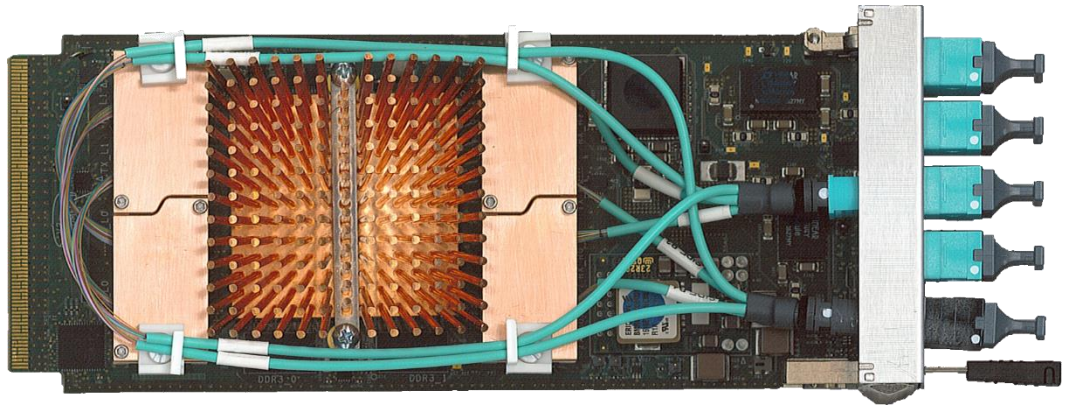


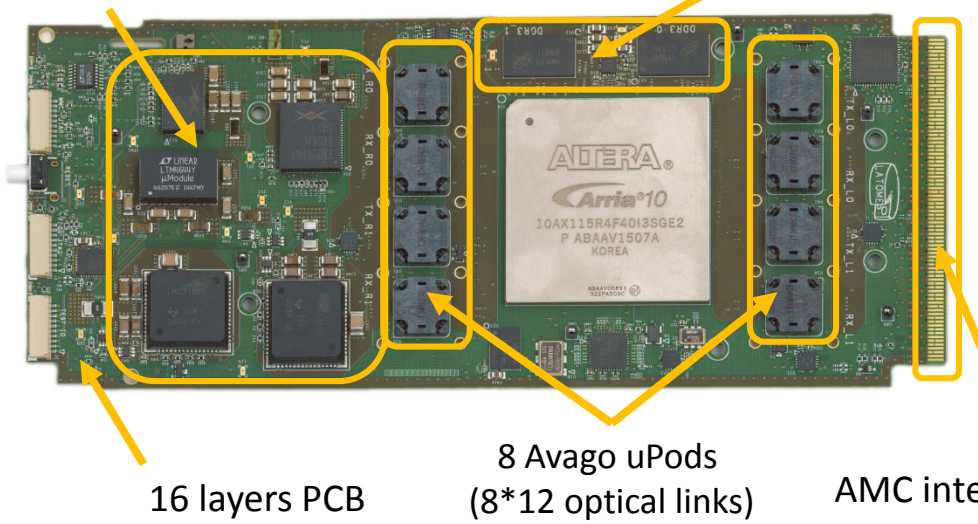
LAr Trigger prOcessing MEzzanine: LATOME

- **Main data path**
  - Receives Super Cells data from LTDB @5.12 Gbps on up to 48 optical links
  - Computes Super Cells transverse energy (ET) using optimal filter at each 25 ns bunch crossing
  - Builds trigger tower transverse energy and assigns it to the correct bunch crossing
  - Sends trigger tower data @11.2 Gbps on up to 48 optical links
  - System has fixed latency less than 375 ns

- **Receives** Timing, Trigger Control (TTC) commands and clock and data from the Carrier board

- **Monitors** data and **sends** report to Central data acquisition system upon request





Back End System Test

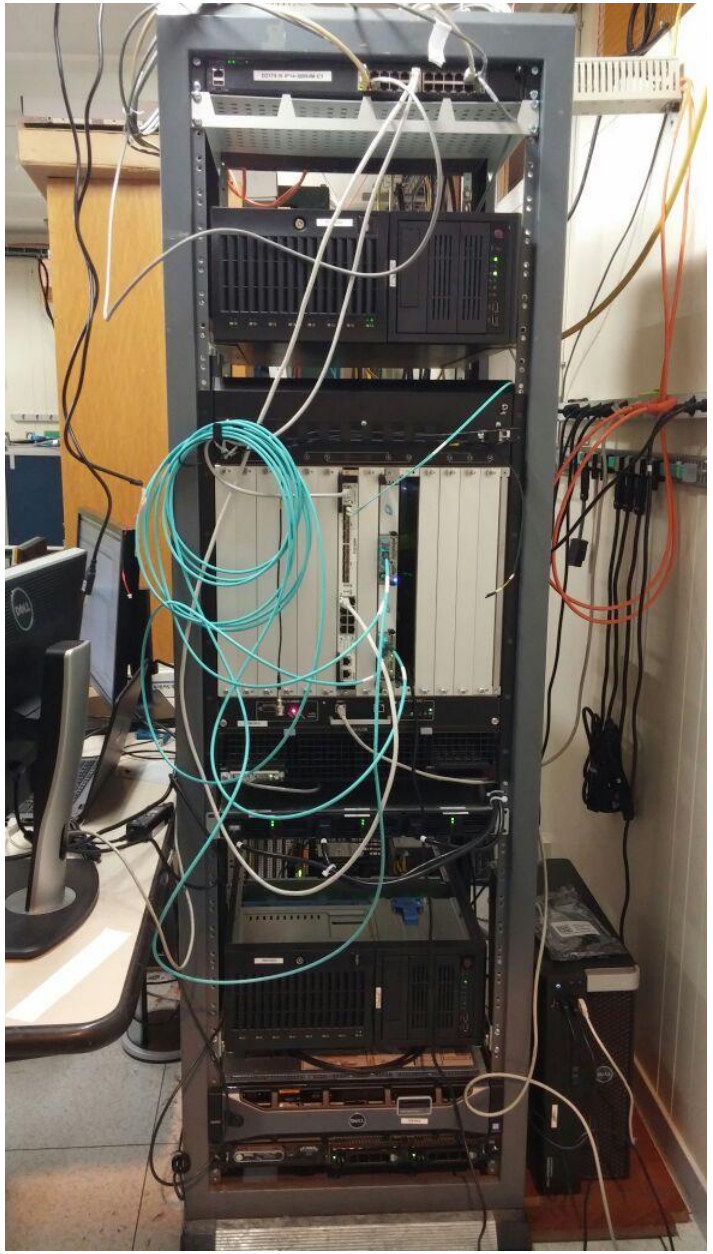
Build a system with the final prototype

Connect to the real environment @CERN
- Timing, Trigger Control commands and clock
- Atlas Development Network
- Development PCs

First system test done in march 2017
- Checks simple configuration

More system tests in Q2 2017
- Until fully functional

Purpose
- Confirm all functionalities before mass production



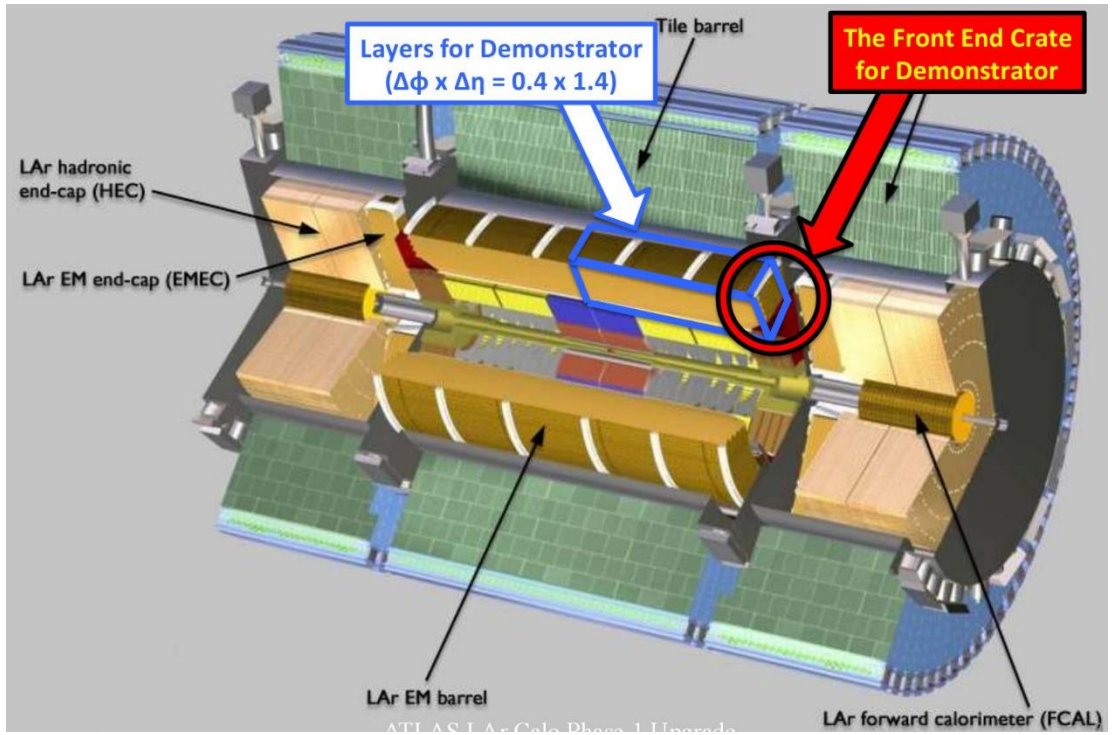
Demonstrator

Demonstrator motivations

A **demonstrator** was installed in ATLAS in the EM barrel (coverage 1/32 of barrel region) in summer 2014 to show the feasibility of the Phase I Upgrade:

- Demonstrator FE: 2 LTDBs
- Demonstrator BE: 3 (originally 2) ATCA test Board for Baseline Acquisition (ABBA)

- **Reads** data from Super Cells
- **Validates** energy reconstruction and bunch crossing identification and **collects** real collision data for the filtering algorithm development
- **Gain experience** in installation and operation of such equipment in the ATLAS environment

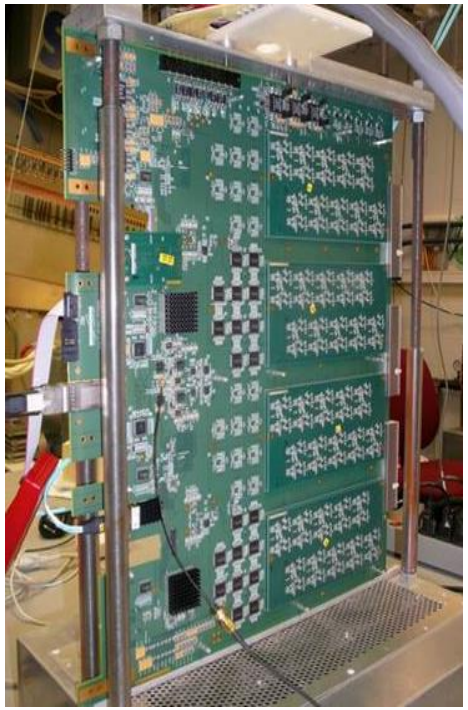


FE Demonstrator: LTDB

- Handles up to 320 Super Cells signals
  - 284 Super Cells in EM Barrel
- Super Cells signals are digitized with 12bits ADC@ 40MHz
  - Commercial ADC COTS : TI ADS5272 (not radiation tolerant)
- Multiplexing 8 Super Cells on one 4.8 Gbps optical link
  - 8B10B encoding, K-code sent every Bunch Crossing revolution
  - Xilinx FPGAs
  - 48 optical links
- Throughput ≈ 200 Gbps/LTDB

- **Status:**
  - 2 LTDB versions developed and installed in August 2014
  - Taking collision data in LHC Run 2

Digital Motherboard + analog mezzanines

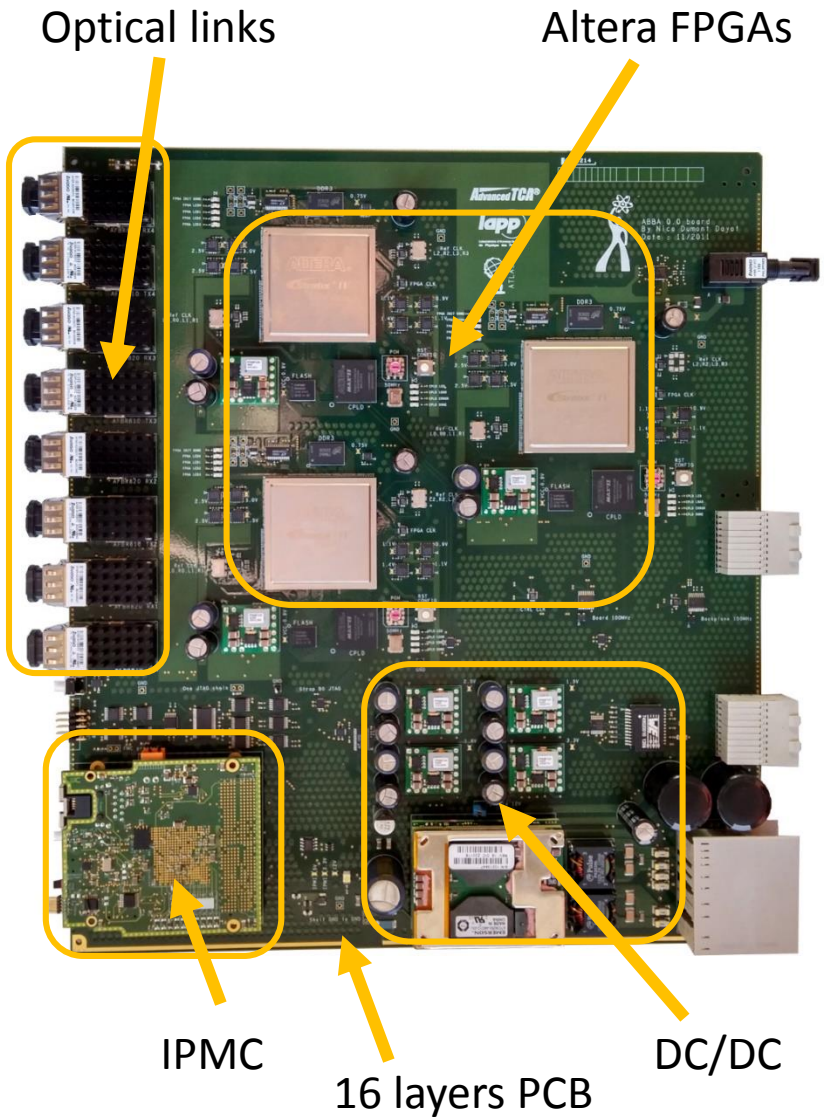


Analog Motherboard + digital mezzanines

BE Demonstrator: ABBA

- ATCA board: 3 Altera FPGAs (Stratix IV)
- Receives up to 320 Super Cells signals (SC) from one LTDB
  - Up to 48 optical links @ 4.8Gbps
- Stores Super Cells data into circular buffer
  - Latency up to 2.5us
- Waits for Level-1 trigger to readout Super Cells data
- Readout using IPbus protocol over UDP on 10 GbE network
  - Readout with ATCA fabric interface

- **Status:**
  - 3 ABBA boards installed in USA15
  - Online software operational
  - Concurrent readout in parallel with ATLAS default readout since October 2015
  - Since November 2016 integrated in the automated ATLAS data taking
  - Successful data taking in LHC Run 2



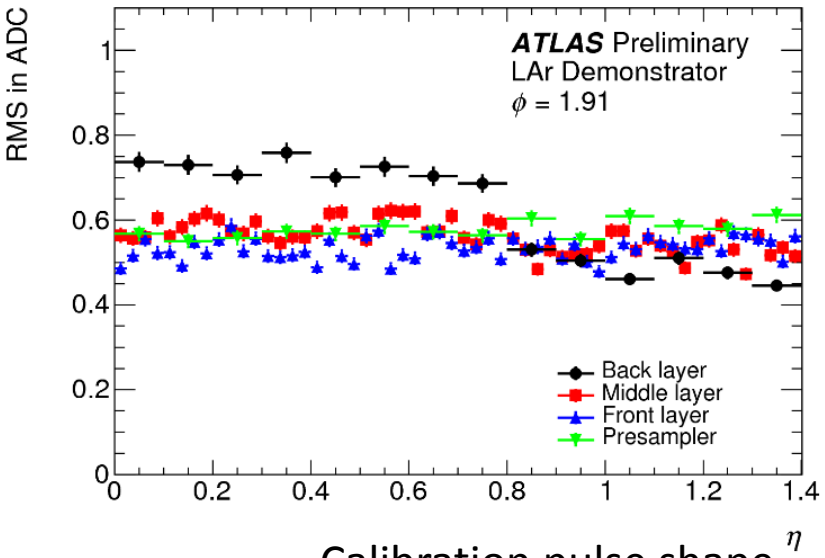
Demonstrator data taking

Calibration:
- electronic pulses sent by calibration board

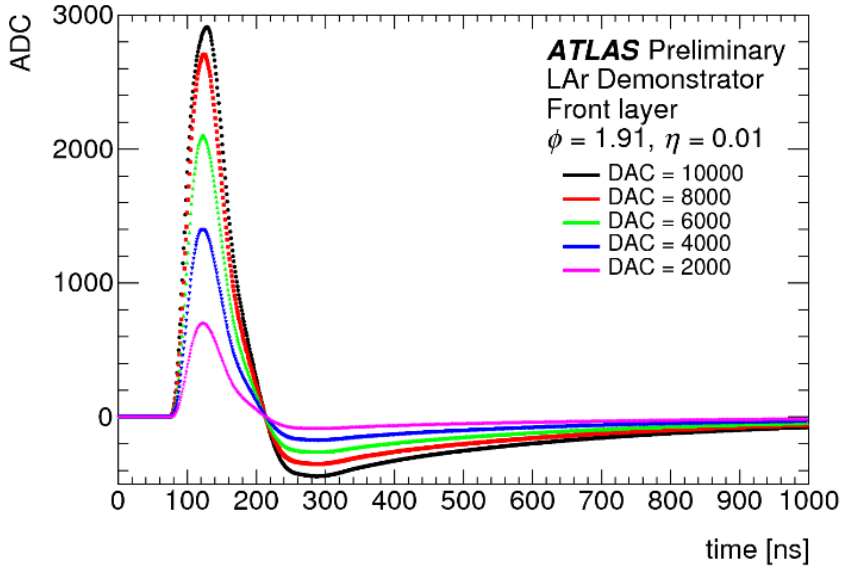
Collisions (proton-proton and heavy ion):
- successful data taking in 2015 and 2016:
  - collected data triggered in Demonstrator region
- in-system debugging of firmware quite successfully
  - ready for 2017 pp data taking
- special Level-1 topological trigger item is used
  - thanks to the L1 community
- compared Demonstrator readout and ATLAS main readout

- Total noise on main readout of calorimeters cells of demonstrator similar to neighboring crates
- Plan for early 2018 to have final prototype installed and running in end of Run 2

Noise levels of SCs



Calibration pulse shape



Summary

Summary

- The **ATLAS Lar calorimeter electronics will be upgraded for Phase-1** after Long Shutdown 2 (2019-2020)
- The **trigger path** will be digitized at Front-End level with an improved granularity
- **LTDB and LDPS systems** are being developed and produced
  - Radiation tolerant ADC and Optical links specifically designed
  - System input data rate is 20Tbps and output data rate is 41 Tbps in total
  - LTDB prototype being assembled
  - LDPB ATCA carrier board and LATOME AMC boards being tested
- A part of the new Trigger scheme (**Demonstrator**) has been installed
  - Both Front End and Back end electronics have been validated
  - One Front End Crate (1/32) is equipped with the demonstrator
  - Readout through TDAQ software
- **Production will start in 2018**

Backup slides

LHC Schedule

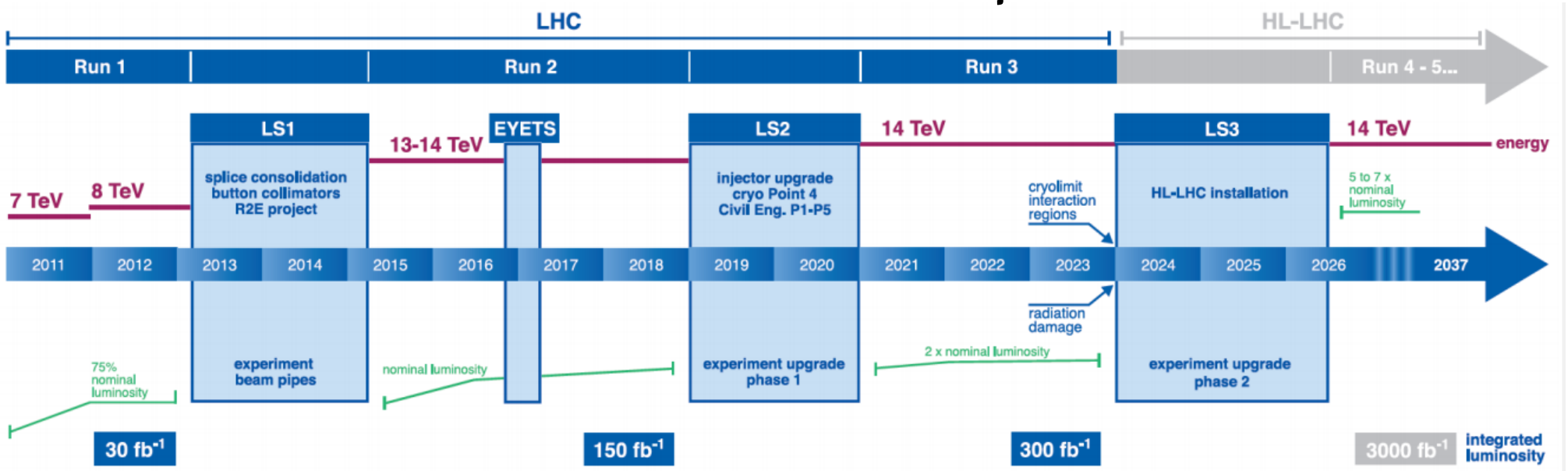
Two phase upgrade planned for LHC, ATLAS upgrade:

- **Phase-I** (2021-2023): upgrade of trigger path, installation in 2019-2020
  - $L \cong 3 \times 10^{34} cm^{-2} s^{-1}$
  - $\langle \mu \rangle = 80$ (Average number of vertices per bunch crossing)
  - Keep trigger max 100 KHz, latency $\leq 3\ \mu s$

  } Upgrade of LAr trigger readout

- **Phase-II** (after 2025): upgrade of data path, installation in 2024-2025
  - $L \cong 7.5 \times 10^{34} cm^{-2} s^{-1}$
  - $\langle \mu \rangle = 200$ (Average number of vertices per bunch crossing)
  - Keep trigger max 1 MHz, latency $\leq 10\ \mu s$

  } Upgrade of LAr main readout



ADC: radiation tolerance

Table 1: Measurements of ADC performance before and immediately after irradiation in a 227 MeV proton beam at $f_{in} = 10$ MHz. The change in the ENOB is within the measurement errors of the testing setup.

Chip no.	Dose [MRad]	SNDR [dBc] Pre/Post-Irradiation	SFDR [dBc] Pre/Post-Irradiation	ENOB Pre/Post-Irradiation
1	2	62.43/61.05	67.27/70.06	10.08/9.85
2	1	63.54/62.36	70.92/72.98	10.26/10.10

Total Ionizing Dose

- **1 Mrad is 10 times the dose expected in 4000 fb-1**

Table 2: Measurements of ADC SEE performance in a 227 MeV proton beam.

Single Event Effect

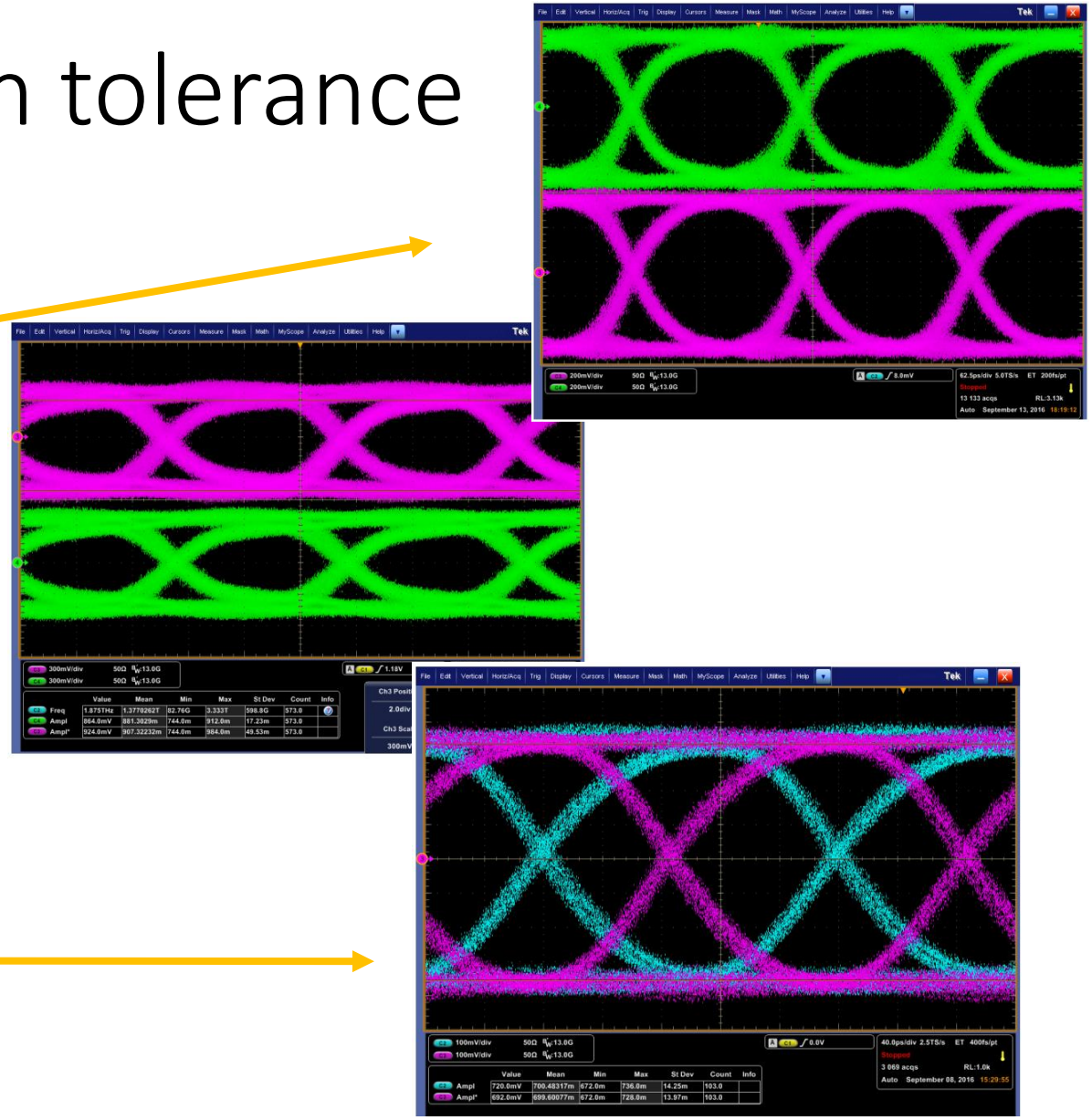
Chip no.	Rate [10^8proton/cm^2/s]	Dose [kRad]	SEFI	SEU (Analog)	SEU (Digital)	SEE	Cross section (w/analog errors) [10^{-12} cm^2]
3	19.0	101	0	8	1	9	0.6 (5.7 ± 1.9)
3	76.0	283	0	41	2	43	0.6 (9.8 ± 1.5)
4	18.6	203	1	10	0	11	0.3 (3.5 ± 1.1)

LOCx2 & LOCld: radiation tolerance

LOCx2

- Eye Diagram 5.12 Gbps
- 2 Channels chip soldered on PCB
- Total jitter ~ 50 ps (loop filter = 800 kHz)

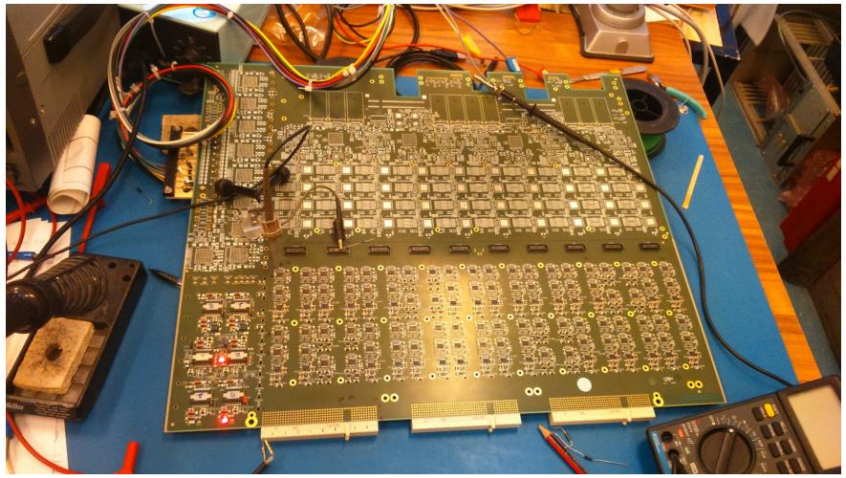
- Eye Diagram after 182 krad TID
- Low or high dose rate (3krad/hr or 30 krad/h)



LOCld

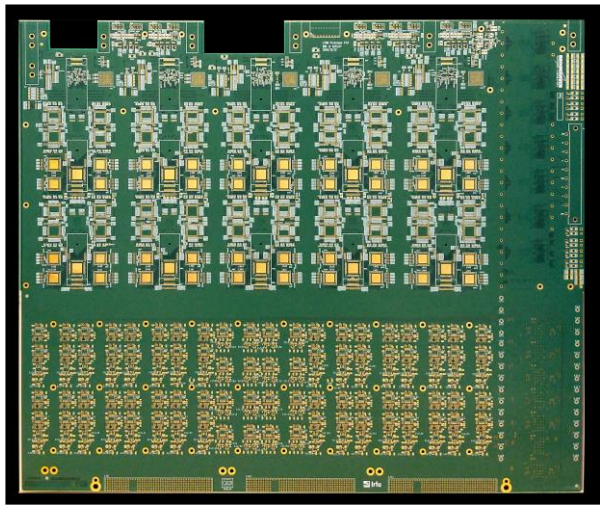
- No eye diagram change after 200 krad
- 2 channels shifted for display clarity
- Current change after irradiation < 10%

LTDB Development



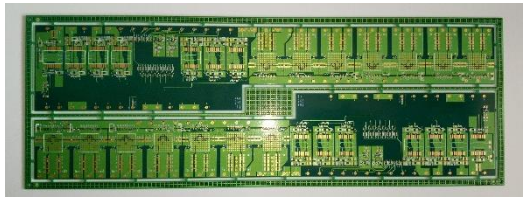
LTDB pre-prototype 320ch

- Pre-prototype PCB
  - FPGA used to replace LOCx2



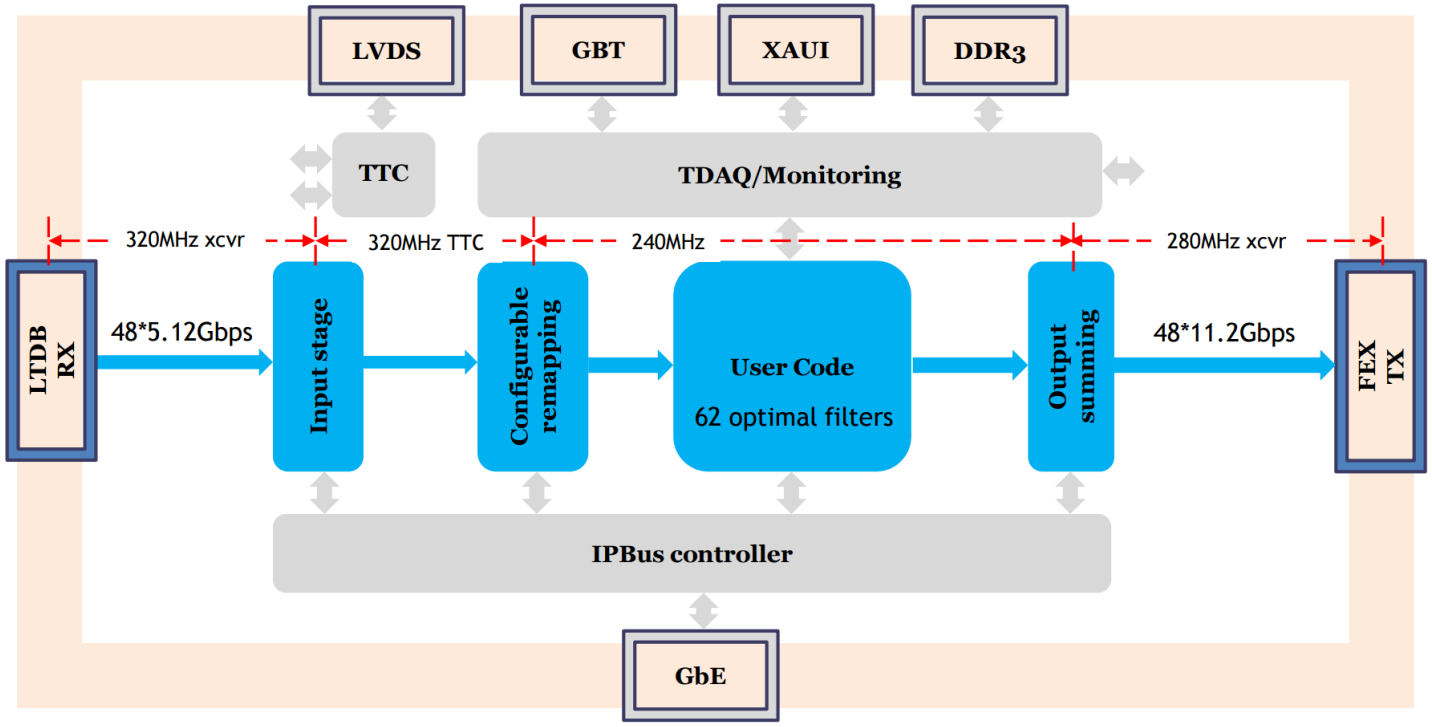
LTDB prototype

- Analog section and digital section are designed by different institutes, and Gerber merged for fabrication
- Power section is realized on a mezzanine
- 2 LTDB prototypes could be used to replace LTDB demonstrators in January 2018



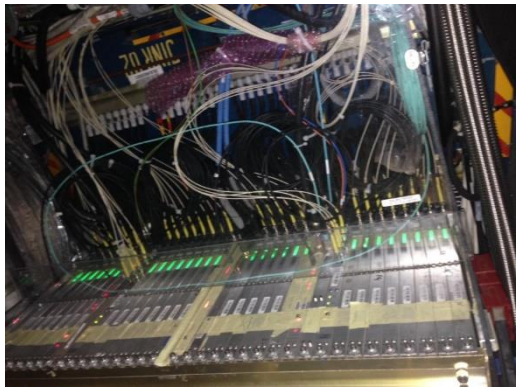
LATOME Firmware

- **Input stage** aligns all inputs to the same BCID
- **Configurable remapping**: reorders input data according to detector's topology
- **User Code**: computes Et and time using Finite Impulse Response filter (FIR)
- **Output summing**: builds trigger tower energies



Demonstrator readout in ATLAS

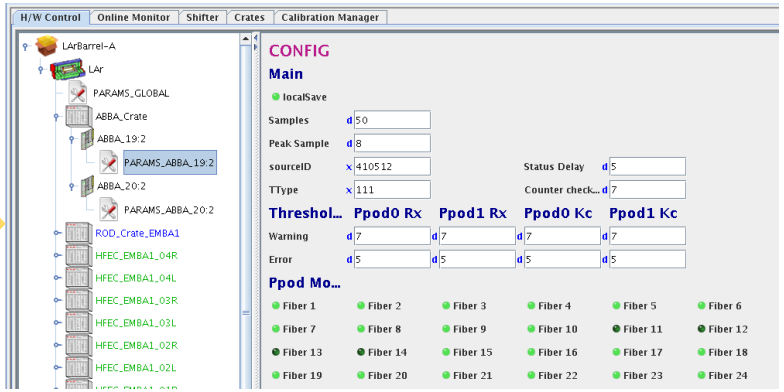
LTDBs in FE crate



ABBAs in ATCA crate
with 10GbE ethernet switch

#1 #2 #3

Readout computer
(10GbE)



ATLAS LAr TDAQ software

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