Update of full silicon tracking

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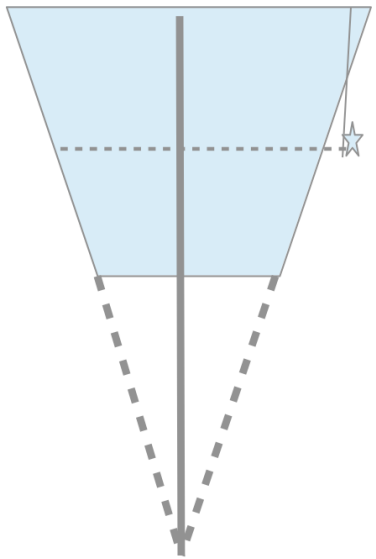
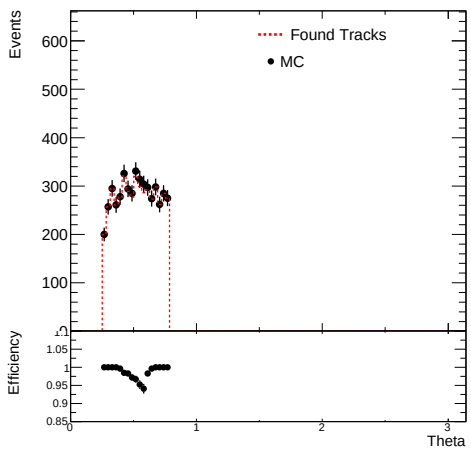
Introduction

- Chengdong and I have checked the FTD construction code seems OK (segment vs petal)
- After digi, the strip z or v position is reset to the center of strip, which causes them out of boundary.
- At the moment, the fiducial check is based on geometry of module, but it depends on actual hit position.

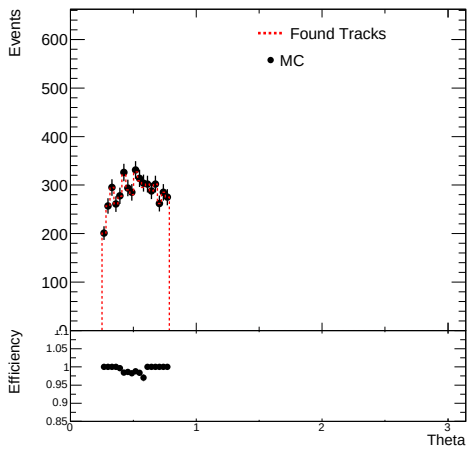


Tracking Efficiencies vs eta

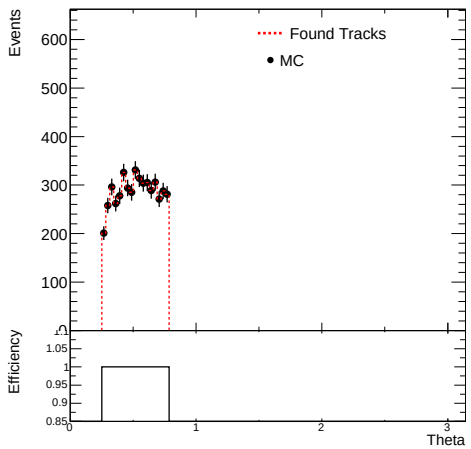
- Requiring $P_T > 1.0$ GeV and in barrel and endcap overlap region.
- Tracking eff improves after fixing the boundary and δ-ray



(b) before



(c) after



(d) Without delta-ray

Figure: Efficiencies vs theta

To-do List

- The full silicon tracking seems in a good shape.
- The digi and δ-ray is next to fix.
- Dan is starting to generate some zh events and the results will follow.
- Instructions can be found at

  http://cepc.ihep.ac.cn/ cepc/cepc_twiki/index.php/Pure_Silicon_Detector.
- Given more layers of silicon, the tracking seems get slower, about twice CPU time than CEPC V1.
- Will start to document the studies.