A Scalable DAQ System with High-Rate Channels and FPGA- and GPU-Trigger for the Dark Matter Experiment EDELWEISS-III

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***Abstract*–The EDELWEISS experiment, located in the underground laboratory LSM (France), is one of the leading experiments using cryogenic germanium (Ge) detectors for a direct search for dark matter. For the EDELWEISS-III phase, a new scalable data acquisition (DAQ) system was designed and built, based on the 'IPE4 DAQ system', which has already been used for several experiments in astroparticle physics.**

I. Dark Matter Search with EDELWEISS

DARK MATTER search is currently one of the major efforts in particle physics. There is strong evidence that only about 15.8 % of the mass of our universe consists of baryonic (visible) matter; the nature of the remaining part - named *dark matter* - is unknown (values from [1], rounded). Several experiments search for signals of dark matter, assuming it consists of *weakly interacting massive particles* (WIMPs). The EDELWEISS [2] experiment, located in the underground laboratory LSM (France), is one of the leading experiments using cryogenic Ge detectors for a direct search of WIMPs. A WIMP hitting a Ge nucleus within a Ge monocrystal will result in an increase of the crystal temperature in coincidence with a charge signal arising from the ionized recoiling nucleus. The Ge crystals operate as bolometers; they are cooled down to 18 mK and detect sudden increases of the temperature. EDELWEISS started first measurements in 2000 with a detector mass of three 320 gr Ge detectors (total mass: 0.96 kg). Since then the experiment has been continuously extended. EDELWEISS-II started 2009 with ten 400 gr Ge detectors (total mass: 4 kg) and a significantly improved background suppression. The actual phase, EDELWEISS-III, can use up to 40 detectors with 800 gr (total mass: 32 kg). Currently (Nov 2015) 24 detectors (total mass: ~19 kg) are instrumented and in operation (see Fig. 1).

Each bolometer is equipped with two heat and four ionization sensors. The *bolometer boxes* (BB) are the digitizers and are placed close to the bolometer, but at room temperature. They contain 6 ADCs, one FPGA (field programmable gate array) and other electronics for biasing the detector. Each ADC is sampling at 100 kHz and 16 bit resolution. Thus, one BB is producing a 1.2 MB/sec data stream, which is sent to the DAQ system through optical fibers.

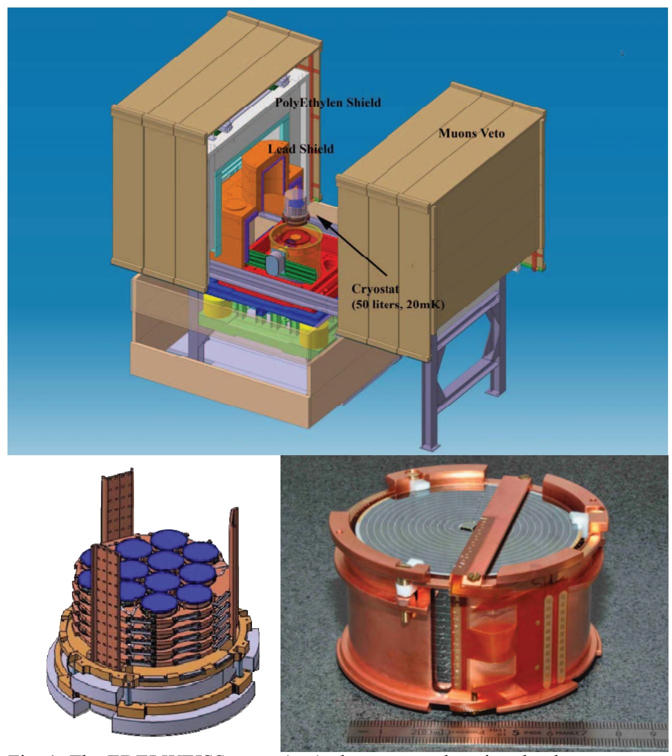

Fig. 1: The EDELWEISS setup (top): the cryostat, housing the detector tower and surrounded by lead and polyethylene shielding and the muon veto detector; scheme of the detector tower (left); a Ge bolometer detector (right): mass 800 g, diameter 7 cm, height 4 cm

Until EDELWEISS-II, the data sink were FPGA boards (rack mounted or standalone boxes), dispatching the ADC data stream to the final trigger computers (Mac Pro) through Ethernet, which required one Mac Pro to read out and trigger 2-4 bolometers (see Fig. 2 for details).

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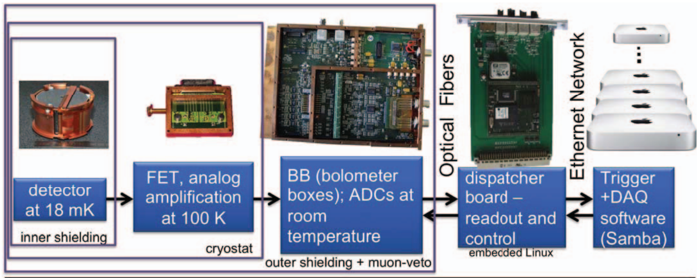

EDELWEISS-II setup:				
1 detector	1x FET box	3x BBs	2x/3x boards	1 PC
EDELWEISS-III up-scale to 40 detectors with EDELWEISS-II dispatcher boards (hypothetical):				
40 detectors	40x FET box	120x BBs	120x boards (?)	40 PCs (?)

Fig. 2: The EDELWEISS-III scale-up with the dispatcher boards used for EDELWEISS-II; this configuration would require a large number of boards and trigger PCs

During EDELWEISS-II operation, configurations changed several times, for some periods the trigger system had been further optimized, so the number '*2-4 bolometers per trigger computer*' is an average value and points to the fact that scalability of the existing system had reached its limit with respect to increasing detector mass. Furthermore for technical reasons 2 or 3 BBs are used to read out one detector, although a BB has enough ADCs to read out one detector, which resulted in unused channels within the data stream.

II. Details of the Upgraded DAQ System

For the EDELWEISS-III extension a scalable new DAQ system was designed. The base of the system is the 'IPE4 DAQ system' [3], a highly modular DAQ system, developed and manufactured in-house at KIT and used for several astro-particle physics experiments (e.g. Auger Observatory [4], KATRIN neutrino experiment [5]).

The system consists of a 6U+2U high 19-inch crate with a custom backplane providing 21 plugin-slots (Fig. 3), up to 20 first level trigger (FLT) boards and one second level controller and data transfer (SLT) board. Each FLT and SLT board is equipped with an FPGA (Cyclone II, Altera). The SLT provides a single lane PCIe External Cable connection [4] to a 'crate computer', a standard PC (currently a SuperMicro server, Xeon quad-core, 3.1 GHz, 8 GB RAM, openSUSE Linux).

Each FLT board has 6 optical fiber input-output pairs and thus may receive data of up to 6 BBs resp. detectors. Through point-to-point serial links from the FLTs to the SLT (capacity up to 20×30 MB/sec = 600 MB/sec) and the PCIe External Cable connection from the SLT to the crate computer, the data stream of all detectors is bundled on the crate computer. For the EDELWEISS-III extension with 40 detectors, this results in a data stream of 48 MB/sec which can easily be handled by the crate. The measurements in [6] indicate that the system is capable of streaming data up to 90 MB/sec, which means, it is ready to operate almost twice the projected EDELWEISS-III number of detectors.

One additional IPE4 DAQ system is currently used at KIT as a development and test system. Two more 'mini-crates', each providing 5 plugin slots, are available, too, and are used as a development and test system at other EDELWEISS collaborators. These additional systems could easily be installed in the EDELWEISS experiment laboratory for future extensions of the experiment.

III. The Data Flow in the DAQ System

The traditional EDELWEISS trigger decision is implemented in software at the DAQ computer. The software used for that is the control and trigger software SAMBA. The IPE4 DAQ hardware enables several additional trigger levels. All trigger levels will be used in parallel during EDELWEISS-III operation. They represent a flexible system, each has its advantages and they complement one another.

A. Full up-stream mode

This is the traditional EDELWEISS full up-stream mode. The crate computer is sending out the collected detector data continuously in UDP packets to the trigger computers (Fig. 3, Samba is the triggering software on the trigger computers). The new DAQ system supports the traditional command and

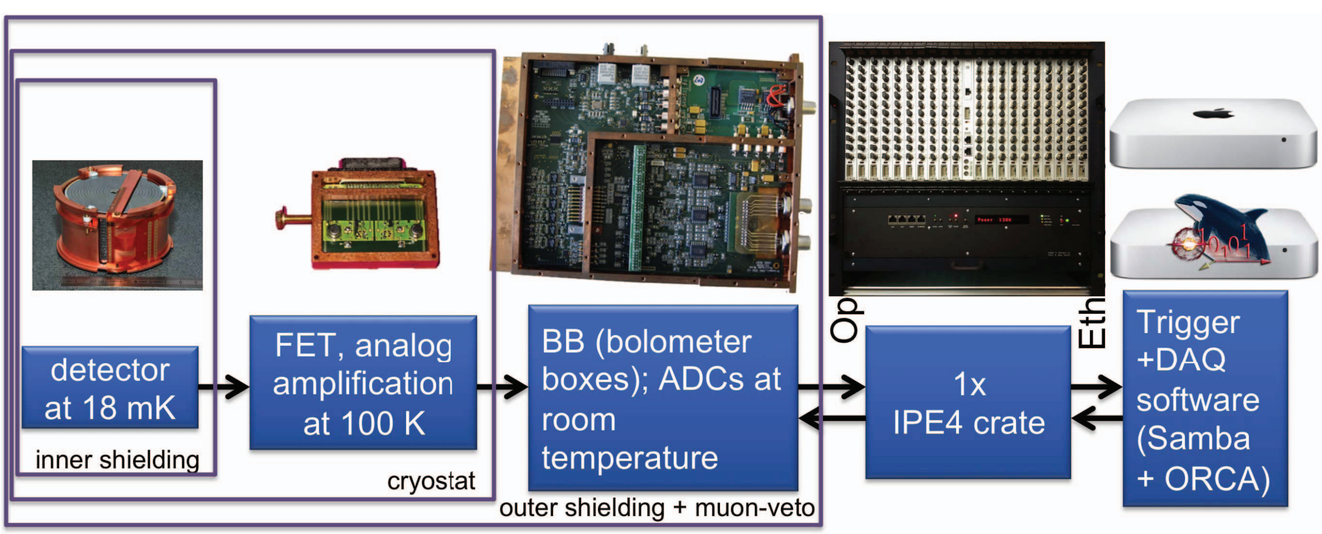

Fig. 3. The EDELWEISS-III update: dispatcher boards replaced by one IPE4 crate. It provides 6 optical fiber I/O pairs per FLT boards (up to 120 in total).

data protocol, thus it integrates seamlessly into the EDELWEISS environment.

The three trigger levels described in the next three sections run on FPGAs or a graphics processing unit (GPU), parts of the IPE4 DAQ system.

B. In-crate FPGA trigger

On the FLT board FPGA triggers on the heat and ionization channels are implemented. These triggers are less complex than the algorithms on the trigger computer, however they operate massively parallel on the input data and have the potential to make fast data rejection decisions and to further reduce the data rate. The FPGA triggered events are read out from an SLT buffer by a dedicated DAQ computer using the DAQ software ORCA [7,8] (see Fig. 4).

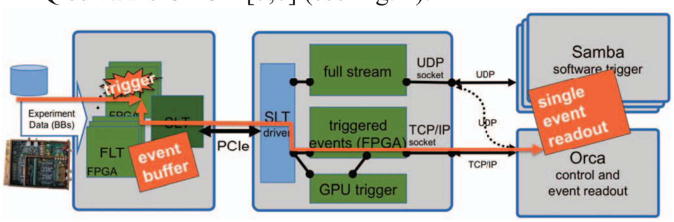

Fig. 4: The FPGA trigger scheme: trigger decision takes place in the FPGAs (left box), event data is transferred through the crate computer (middle box) to the DAQ computer (right).

C. Time resolved ionization channels

Two ionization channels of one dedicated detector are sampled at 40 MHz. These are the so called *fast ionization channels*. The 40 MHz sample readout is triggered by the FPGA trigger, as the software trigger is not fast enough. The fast channel signals are buffered continuously in internal memory on the BBs and the event readout needs to be triggered, before the buffers overflow.

A detailed analysis of first data acquired with the new fast ionization channel is on-going, showing the potential of discriminating near-surface events via the rise time of the ionization pulse [9].

D. GPU trigger

We use a GPU in the crate computer to run additional trigger algorithms. Modern GPUs provide thousands of simple computing processors, which run in parallel and are predestined to run an additional trigger level in software.

Since the full data stream is read out anyway for streaming to Samba, the data can be streamed to GPU memory asynchronously in the background, which requires minor system resources. After a trigger decision on the GPU, only a few event characteristics like channel number and trigger timestamp need to be transferred back to the CPU, so no large data transfer is required into this direction. The GPU trigger was implemented in a test setup; several algorithms were realized and tested. The implementation of a GPU trigger on the experiment site in LSM is still in progress.

E. Unused channel removal

An additional benefit of the IPE4 DAQ system was simply removing unused channels from the data stream. This is possible, because the data stream is collected in the IPE4 crate and the integrated FPGAs provide enough computing power to rearrange the data sets.

F. Reliability

The IPE4 DAQ system is now taking data since almost two years and proved its stability. All data of the EDELWEISS-III phase were taken with the IPE4 DAQ system and no breaks in exposure time on system crashes occurred since then. This is an important improvement and characteristics of the new DAQ system.

IV. Conclusion

The EDELWEISS DAQ system has been updated by the IPE4 DAQ system. The architecture of this system provides several advantages and improvements: 1) The new DAQ system integrates seamlessly into the existing EDELWEISS environment. 2) It improves scalability for a larger number of detectors with respect to the number of trigger computers. 3) Unused channels can be removed from the data stream in an early state and thus reduce the data rate. 4) Additional triggers have been implemented in the input board FPGAs. 5) Parallel to the standard 100 kHz ADC sampling, two channels of one dedicated detector are sampled at 40 MHz. The 40 MHz sample readout is triggered by the FPGA trigger. 6) The crate computer can be equipped with GPUs to use additional trigger levels in software.

The new DAQ system was commissioned successfully in 2014, is now in use in the new EDELWEISS-III setup and is well-prepared for future extensions of the experiment.

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