Progress on ATLAS & CEPC Silicon Detector Projects

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18 November 2016

ATLAS Phase-II Upgrade: Inner Tracker (ITk)

- New full silicon tracker to maintain or improve the tracking performance under the harsher HL-LHC environment → state-of-the-art silicon detector/electronics technologies

ITk-STRIP: Outer tracker

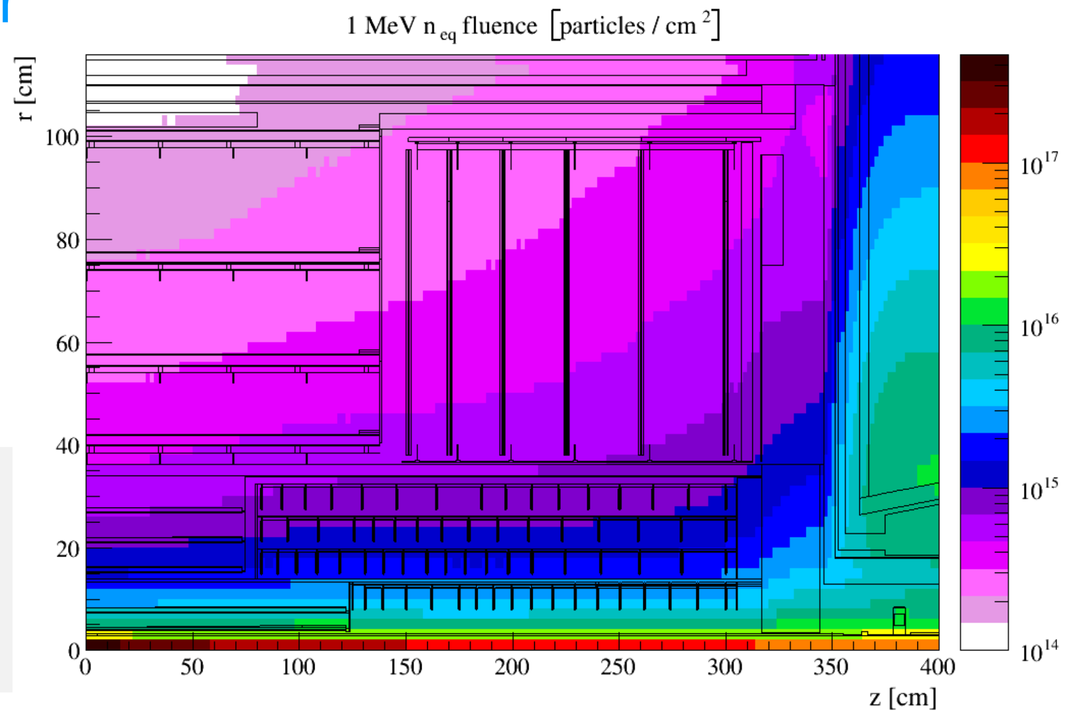
Barrel layers (3-4): long strip (LS) sensor (4.8 cm)

Barrel layers (1-2): short strip (SS) sensor (2.4 cm)

Radiation Tolerance: NIEL

Barrel SS : $1.1\times10^{15}/cm^2$

Barrel LS : $0.6\times10^{15}/cm^2$



ITk-Strip Project Timeline

2016 2017 2018 2019 2020 2021 2022 2023 2024 2025 2026 2027 2028

Remaining R&D towards TDR
6m iMoU
ITK Strip Final Design (TDR)
TDR approved by LHCC
6m Order material for preproduction
1 year Module pre-production (5%)
1,5 years Getting ready (MoU etc.)
1 year Production Readiness Reviews
1 year Order material for parts production
1 year Production global structures (barrel and end-cap
3,5 years Detector parts production
3 years Off-detector and services
2,5 years Barrel integration at CERN
2,5 years EC integration at DESY/NIKHEF
1 year Commissioning (in labs)
Transport to CERN
Merge barrel and end-cap
1 year 1 year test on surface
1,5 years Installation/Com
6m Starting up o
Start of HL-

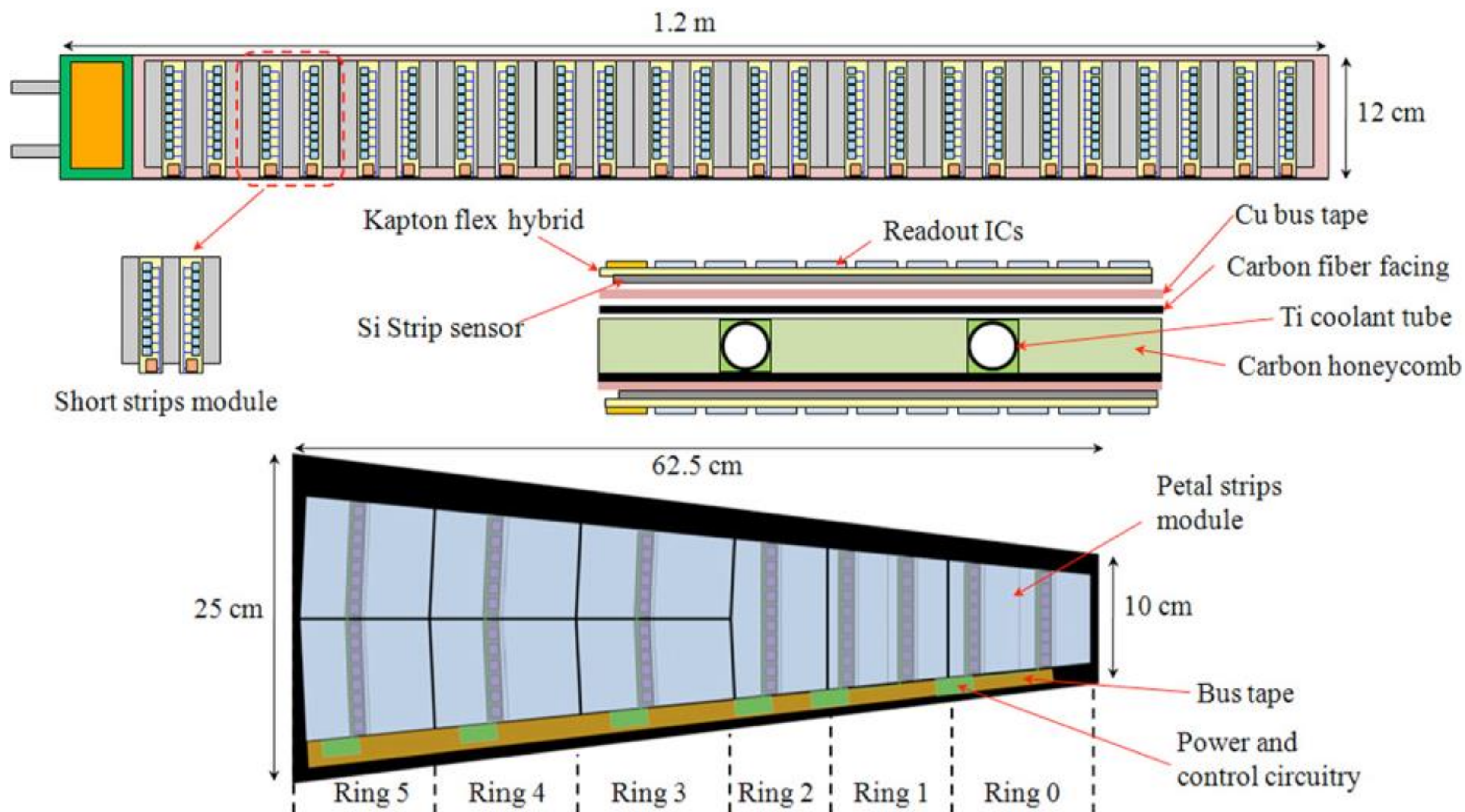
2016: Completion of Technical Design Report (TDR)

2018-2019: Pre-Production

2020-2023: Production

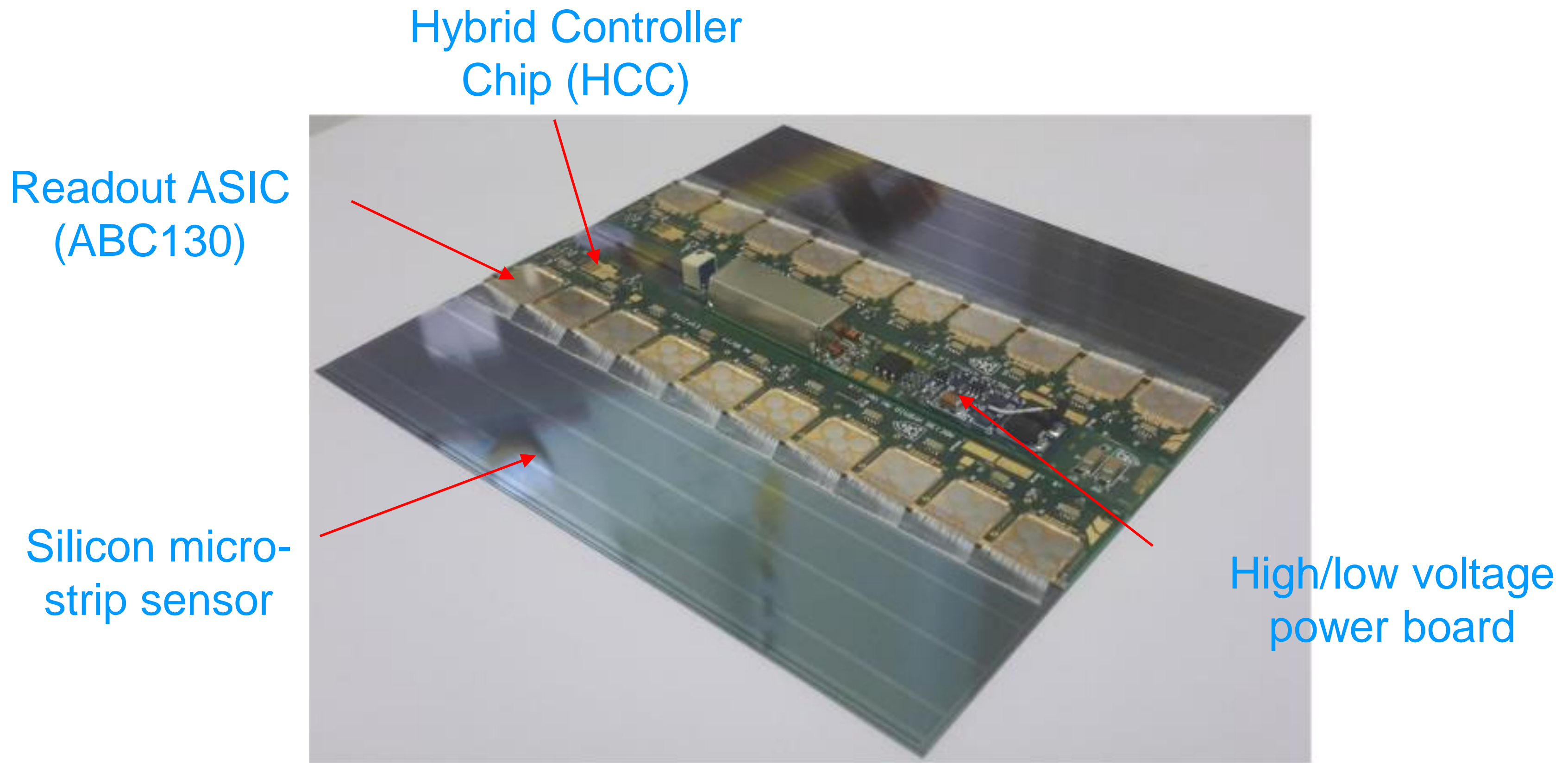
Stave/Petal Concept

- Basic mechanical element of the Stave/Petal concept: **module**



Strip Detector Module

- Components on the detector module: silicon micro-strip sensor, readout ASIC's (ABC130), hybrid and power boards, etc.



Research Topics

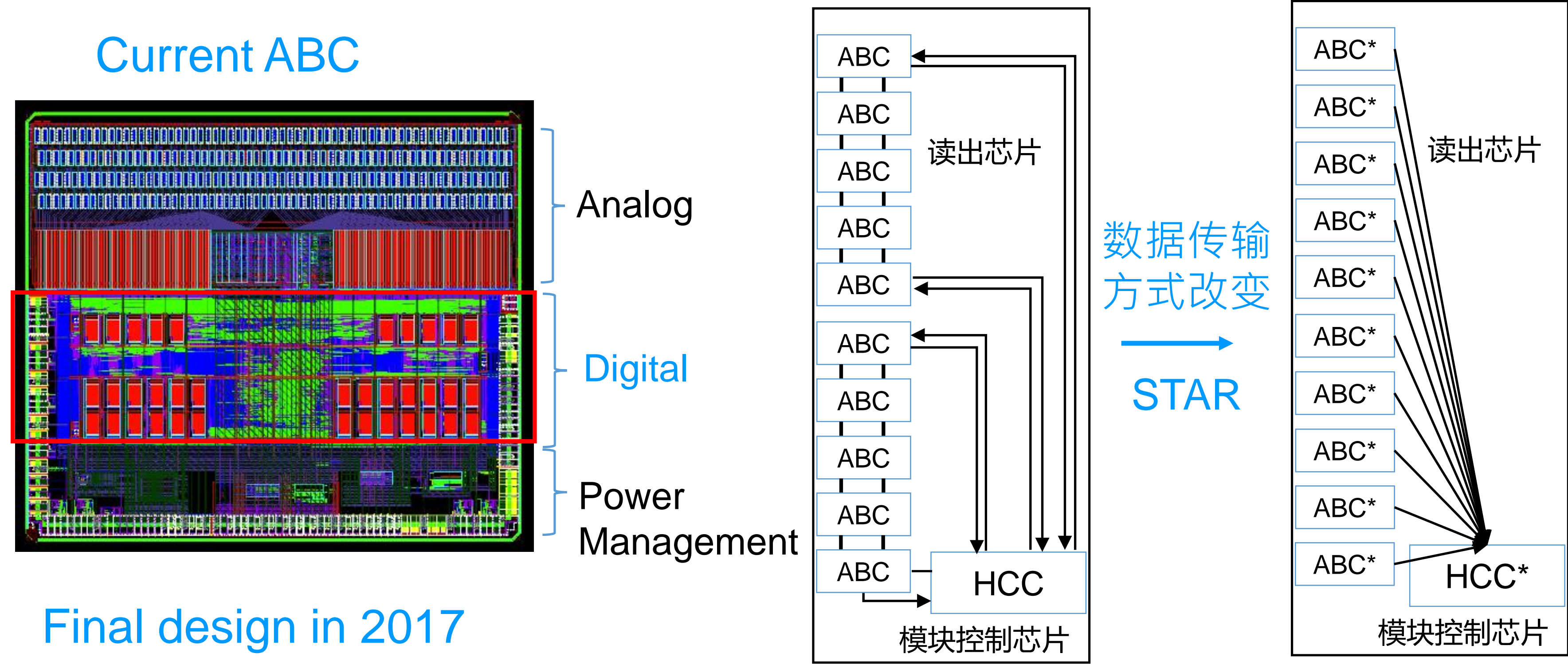
- Design of the front-end readout ASIC $\rightarrow$ digital function blocks, baseline design
- Detector module design and assembly $\rightarrow$ mass production, CORE contribution ~ 1000 detector modules
- CMOS strip sensor R&D $\rightarrow$ novel technology, candidate technology for the CEPC silicon tracker

Funding Supports:

- The MOST National Key Program for S&T Research and Development (13,45 MRMB): prototyping, pre-production and early production
- *To request for ~10 MRMB from NSFC to complete the production*

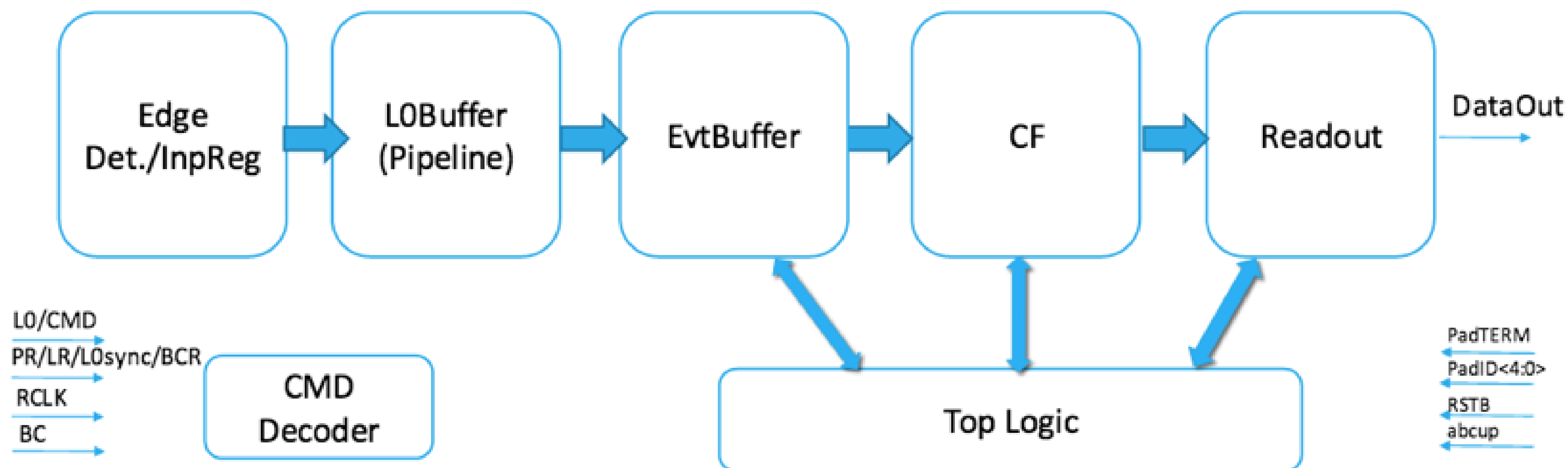
Front-End Readout ASIC

- New data transmission architecture to cope with the increase L0 trigger rate → re-design the digital part of the FE readout ASIC, in collaboration with CERN/UPenn



Design and Verification

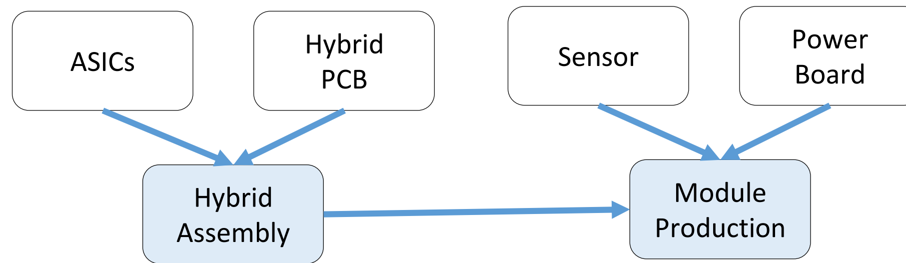
- Re-design the digital function blocks and verify them with the verification system based on the modern UVM method

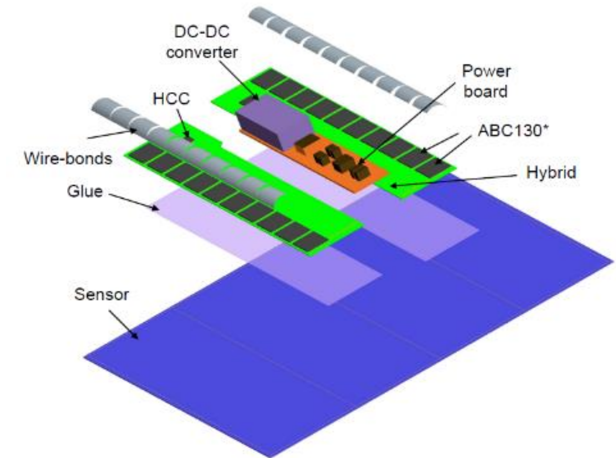


- To complete the design (+ verification and post-simulation) early next year

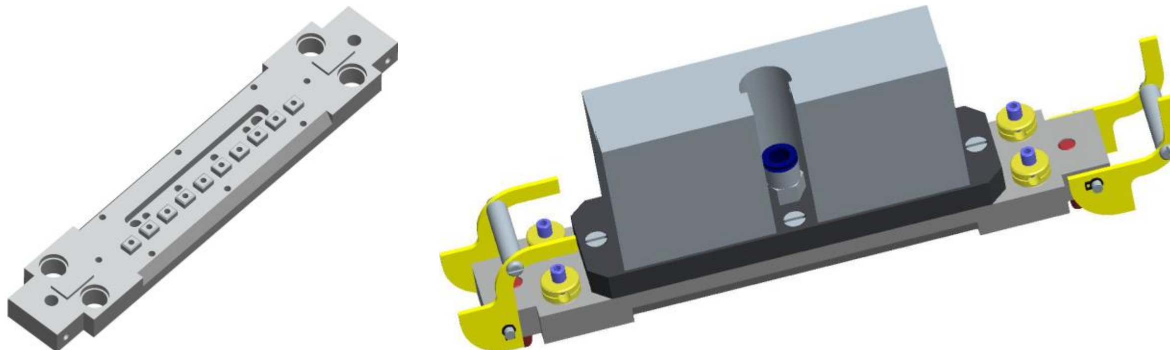
Detector Module Design and Assembly

- Intended to produce in total 1000 detector modules
- Module assembly procedure:





- Making jig tools with drawings from Liverpool



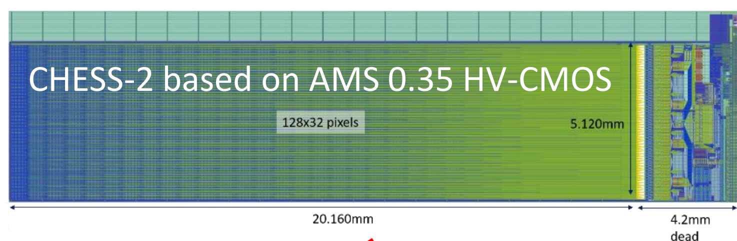
Collaboration with RAL

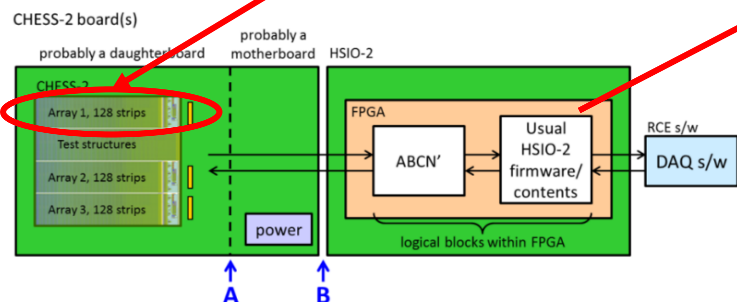
- Decided to collaborate with RAL on detector module production
  - To gain experience

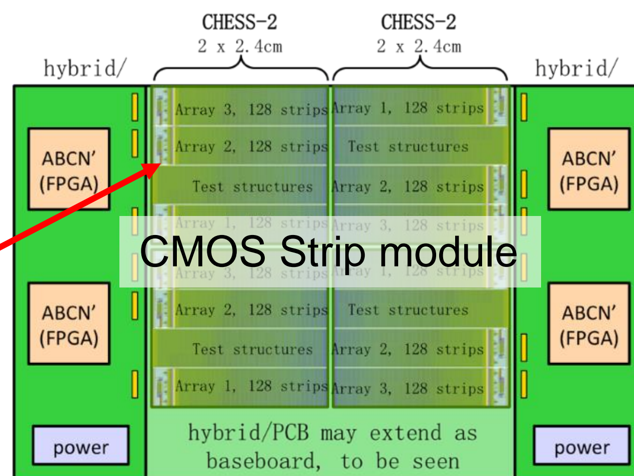
- To rotate

CMOS Strip Sensor R&D

- Alternative to the conventional silicon strip sensor → industry standard CMOS, cost effective, resolution …





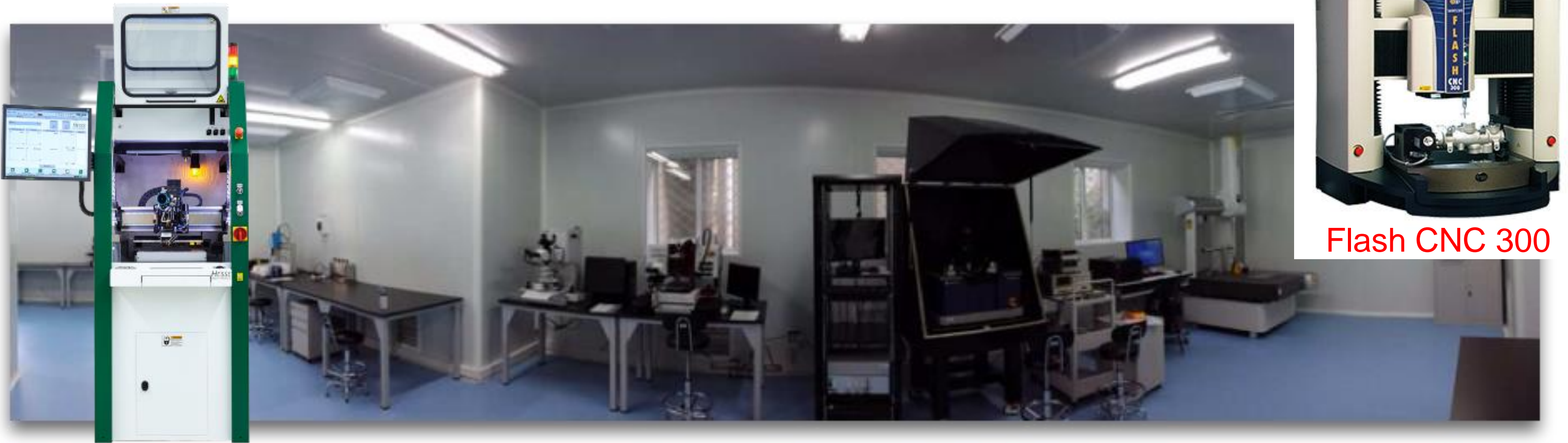


Very promising technology for the CEPC silicon tracker

IHEP/Tsinghua University are actively involved in the CMOS Strip sensor characterization and readout electronics development

Local Infrastructure

- Improving the local infrastructure for silicon detector development
- Class 1k clean room (150 m2) equipped with basic instruments, e.g. probe station, wire-boning machine, etc.



- Purchasing metrology system (OGP CNC 300), budget requests for high speed wire bonder (HESSE BJ820) and several other important equipment

CEPC CMOS Pixel Sensor R&D

Performance Requirements

- Vertex detector essential for heavy flavor (b/c) tagging (track impact parameter resolution) $\rightarrow H \rightarrow b\bar{b}/c\bar{c}$ branching ratios

$$\sigma_{r\varphi} = 5 \oplus 10/(p \cdot \sin^{\frac{3}{2}}\theta)\ \mu\text{m}$$

- Imposing stringent requirements on the vertex detector
  - Single point resolution 3 μm → small pixel size
  - Material budget ≤0.15% X_0 per layer → monolithic pixel sensor + air cooling
  - Low detector occupancy < 0.5% → high granularity and fast readout
  - Radiation tolerance (preliminary, per year): 1 MRad (TID) and 10^{12} n_{eq}/cm^2 (NIEL)

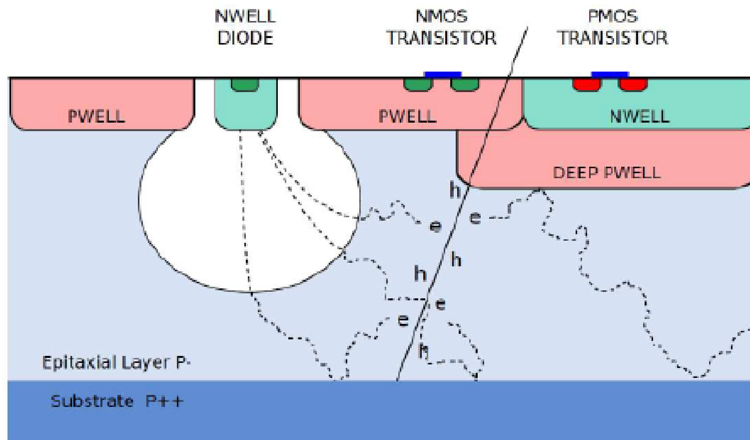
顶点探测器预研

- 基于CMOS图像传感器工艺（高阻外延层+多阱），研制高分辨率、高读出速率、低物质量且低功耗的CEPC硅像素探测器。

	三年指标	最终指标
空间分比率（μm）	10	3
探测效率	99%	≥99%
读出时间（μs）	100	20
探测器功耗（mW/cm²）	150	50
抗辐照水平	不要求	1 MRad/年及10^{12} n_{eq}/cm²/年

- 中远期预研计划
  ① 2015年：二极管参数优化设计，提交首次流片。重点完成电荷收集效率等测试，清晰像素内基本电路性能（如噪声水平等）。
  ② 2016年：完成首次流片所有芯片性能测试。设计复杂像素内电子学及外围电路，提交第二次流片。继续电荷收集效率研究，考虑辐照测试。
  ③ 2017年：完整读出架构设计，基本实现首期技术指标。
  ④ 2018年 - ：调整读出架构，优化像素内电子学及外围电路性能，强化抗辐照性能。

TowerJazz Process



- Integrated pixel sensor and readout electronics on the same silicon bulk with the industry "standard" CMOS process → low material budget, low power consumption, low cost …

- **TowerJazz CIS 0.18µm process features:**
  - Quadruple well process: deep PWELL shields NWELL of PMOS transistors, allowing for full CMOS circuitry within the active area
  - Feature size of 0.18µm and 6 metal layers: high-density and low power
  - Thin gate oxide (3 nm): radiation tolerance
  - Thick (>20µm) and high resistivity (1 kΩ · cm) epitaxial layer: possible improvement of charge collection

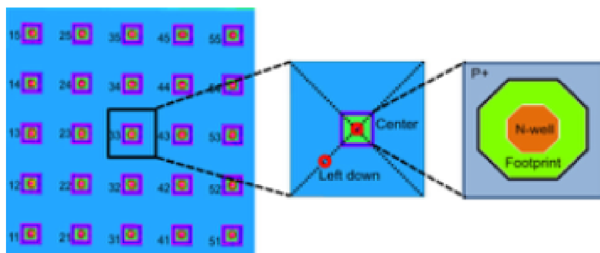
Charge collection and non-ionizing radiation tolerance of CMOS pixel sensors using a 0.18 µm CMOS process, NIMA, doi:10.1016/j.nima.2016.03.031

Sensor Design & TCAD Simulation

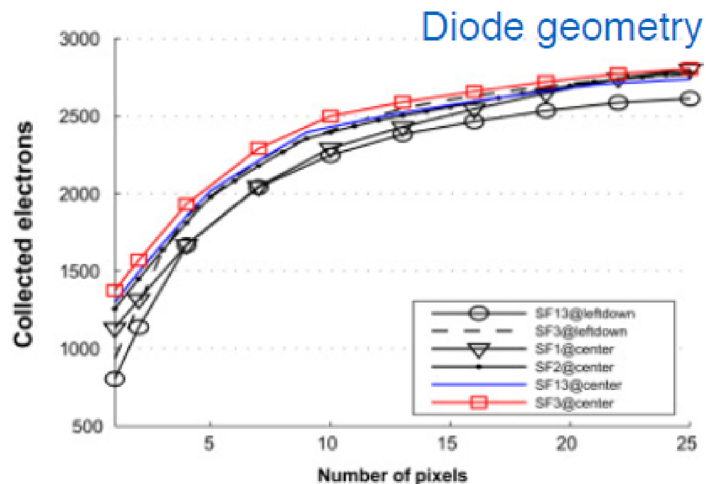
张颖、赵梅

- Charge collection performance with different sensor diode geometries, epitaxial-layer properties and radiation damages evaluated with TCAD simulation

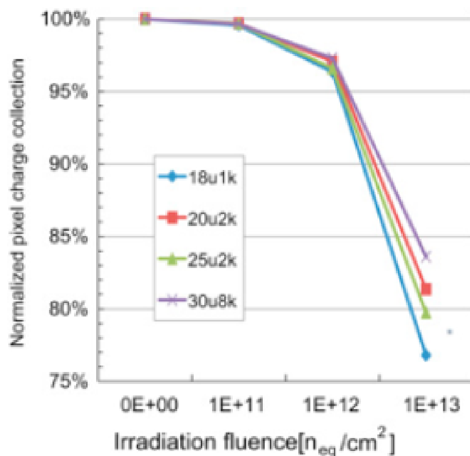
Pixel geometry parameters

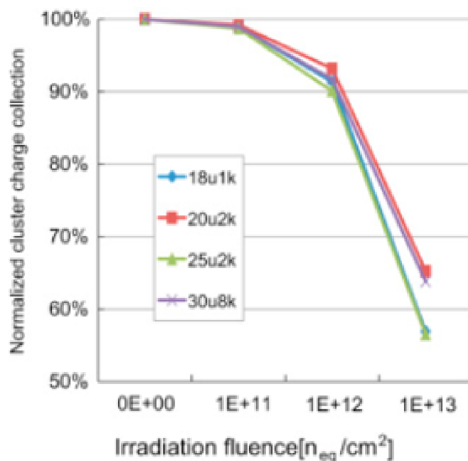


Diode geometry

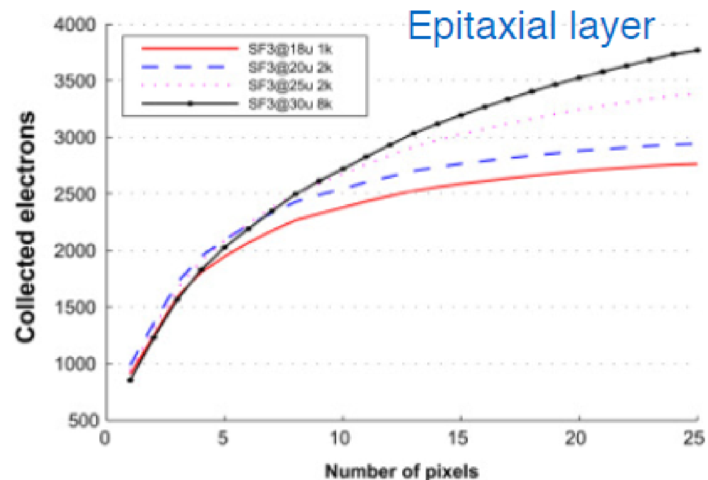


Radiation damage





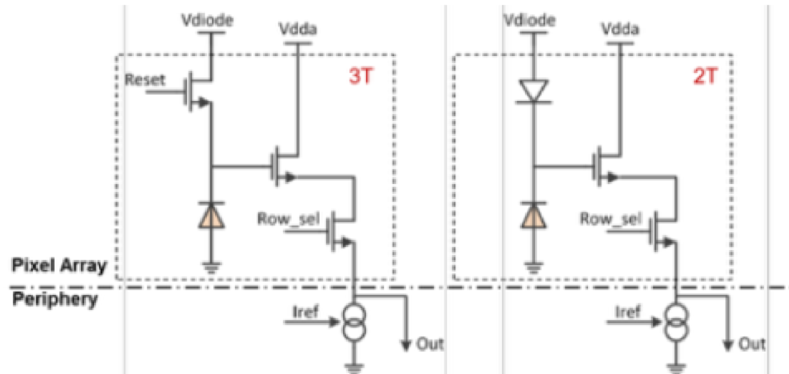
Epitaxial layer

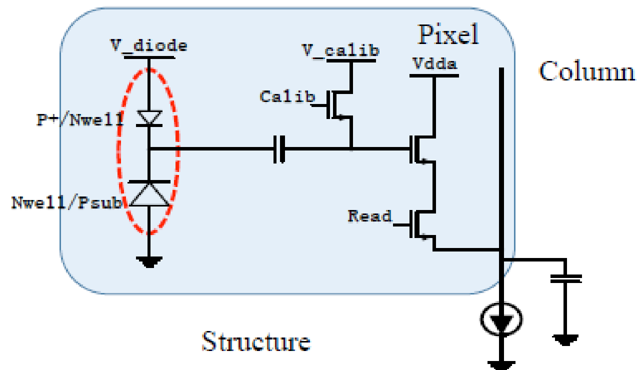


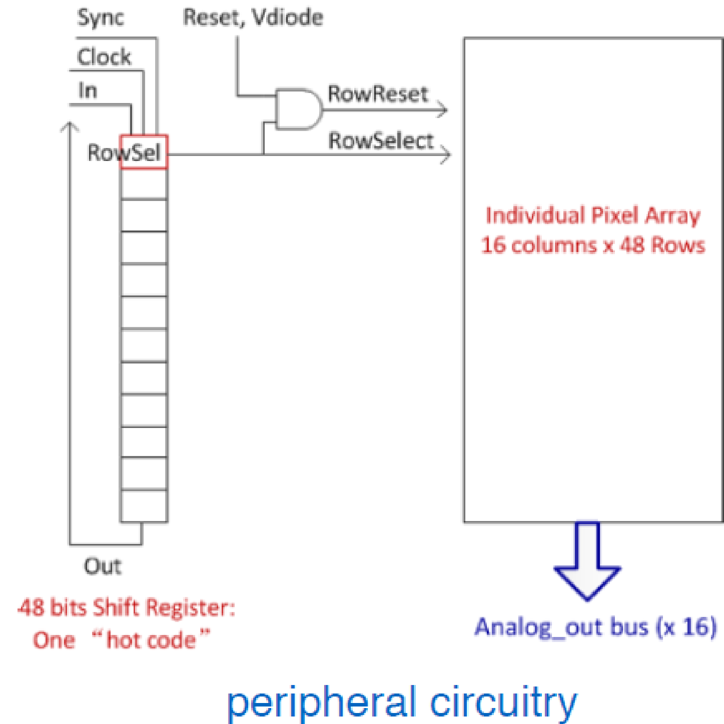
Readout Electronics

张颖、周杨、卢云鹏

in-pixel electronics





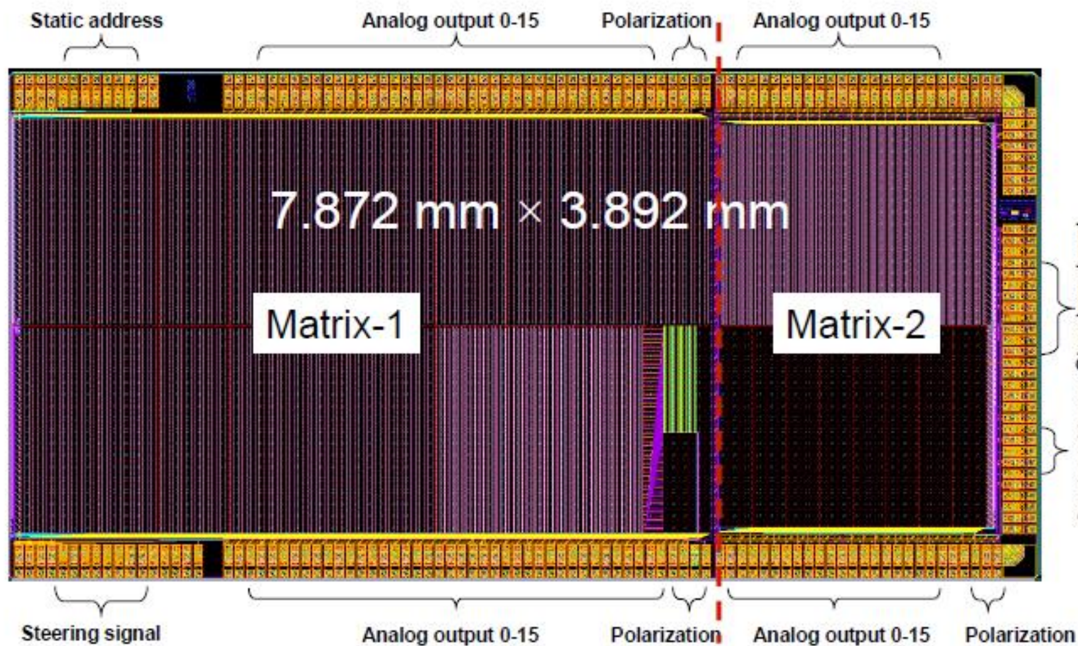


peripheral circuitry

- Conventional (simple and robust) 2T/3T in-pixel readout electronics, AC coupling structure with biased voltage up to 10 V (enlarged depleted region/electric field → potential improvement in charge collection).
- Analog signal read out with the robust rolling shutter scheme

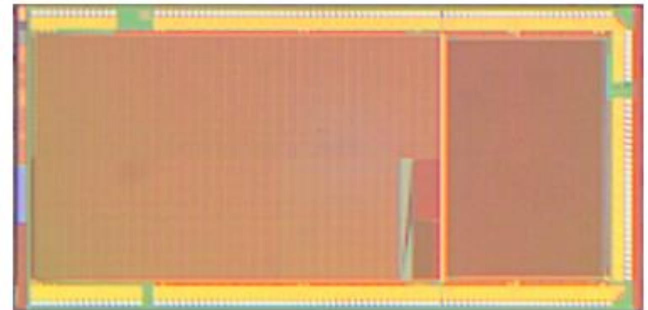
1st Submission

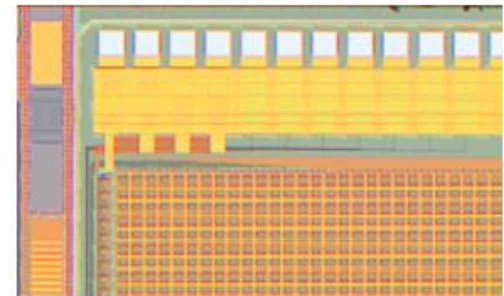
- Joint MPW submission with IPHC in November 2015; diced samples (2+2) already (finally) returned from the foundry
- Aimed to understand charge collection performance with different diode geometries and epitaxial-layer properties and potential radiation tolerance



33×33 μm² (Matrix-1) and 16×16 μm² (Matrix-2)

Diced pixel sensor

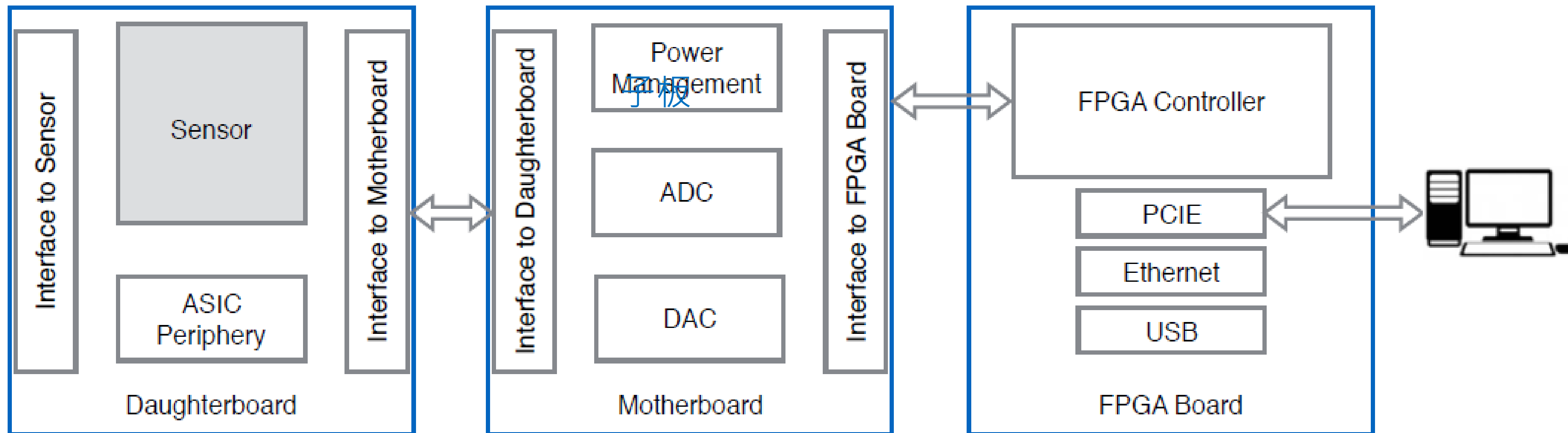


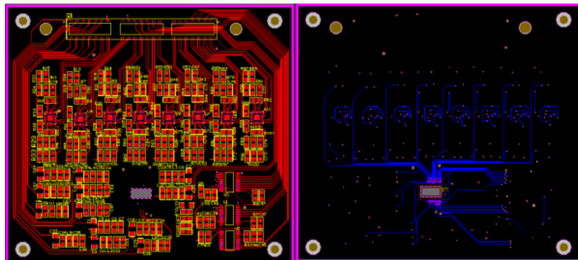


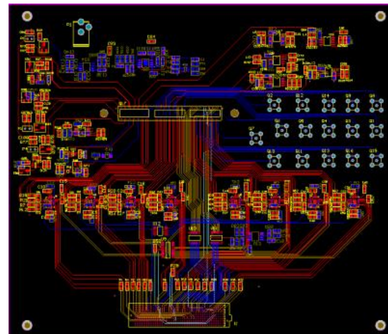
Test System

王科、王娜、史欣

- Test system being developed to characterize the pixel sensors from the 1st submission





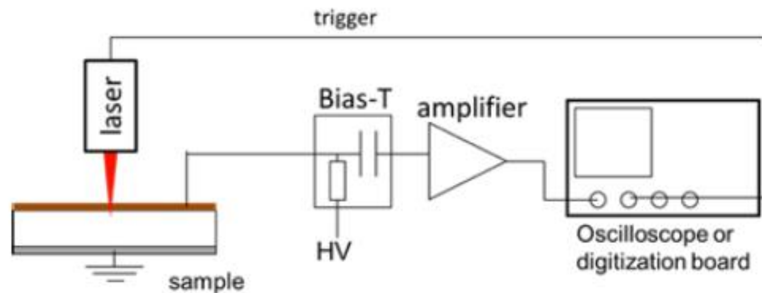


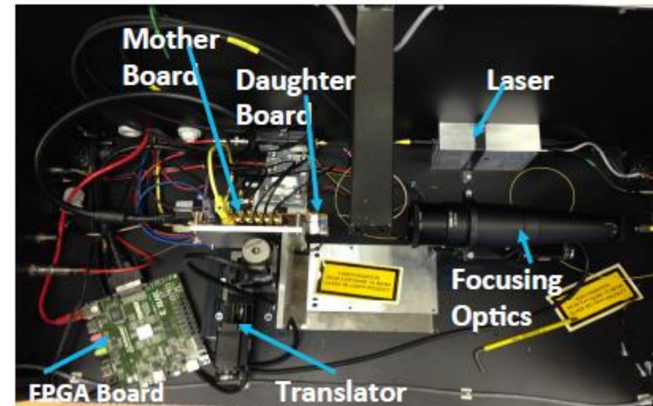
Daughter/mother-boards designed and sent out for fabrication

DAQ interface being developed

陈列建、修青磊、朱宏博

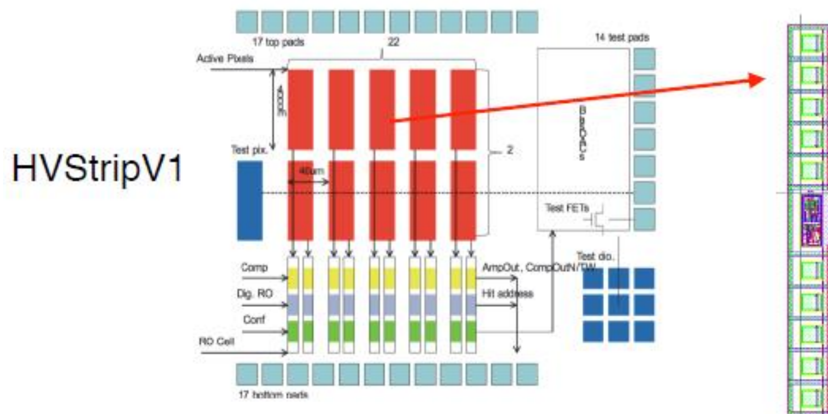
TCT System

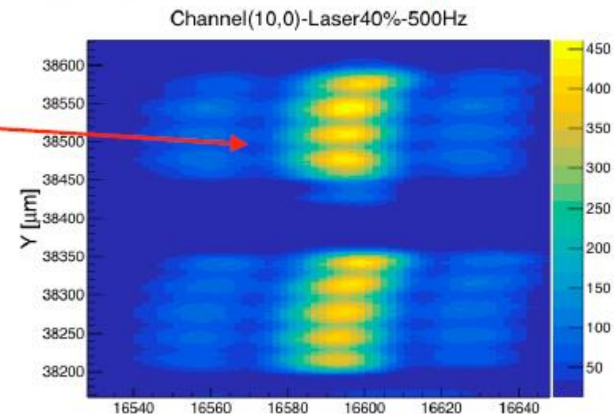




- Transient Current Technique: popular technique to investigate trapping, electric field profiles and carrier transport in semiconductors
- TCT system purchased with the funding support from the State Key Lab
- System fine-tuned to achieve resolution better than ~5 µm; tested with micro-strip sensor, HVStripV1 and CHESS-1 TJ; system ready to probe the CEPC pixel structure

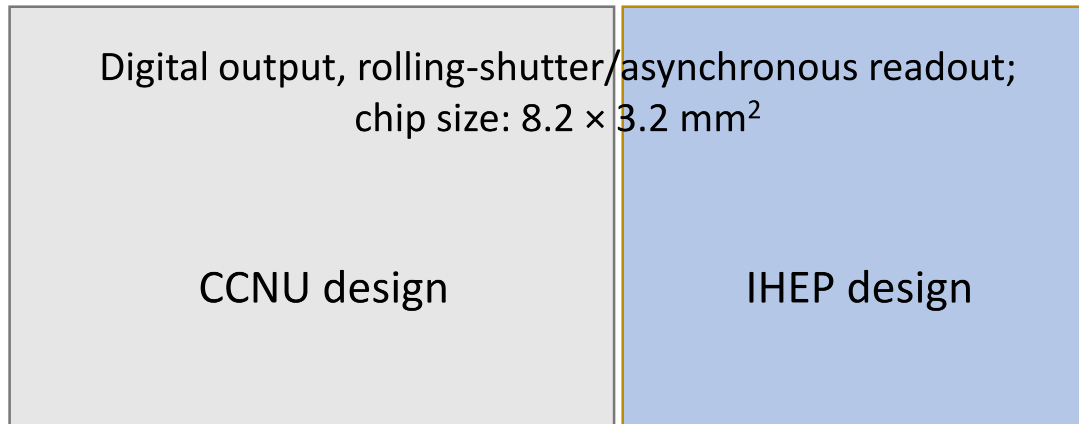
HVStripV1





Next Submission

- To design in-pixel electronics and readout architecture



- Next submission expected in Feb 2017
- R&D now supported by the MOST project

Summary

- ATLAS Phase-II ITk-Strip project
  - Readout ASIC design, module assembly and CMOS sensor R&D
  - Close collaboration with RAL
  - Project supported by the MOST National Key Program for S&T Research and Development

- CEPC CMOS pixel sensor R&D
  - Sensors from the 1st submission back from foundry, to be characterized with the test system (almost ready)
  - Charge collection efficiency, TCT-scan, irradiation tests, beam tests
  - 2nd submission expected in Feb. 2017, on in-pixel electronics and readout architecture