Status and plan of Si pixel detector

*New funding from MOST (2016-2021)

- R&D targeting on
  - σ_{sp} *3-5μm*
  - *Power consumption <100mW/cm^2*
  - *Integration time 10-100μs*

- CMOS pixel sensor (CPS)
  - *Small pixel size*
  - *In-pixel functional circuitry*
  - *Novel readout scheme → faster & less power*
  - *Full functional chip*
  - *~2 MPW and 1 engineering run*
  - *TowerJazz CiS 0.18μm process*

Charge collection simulation

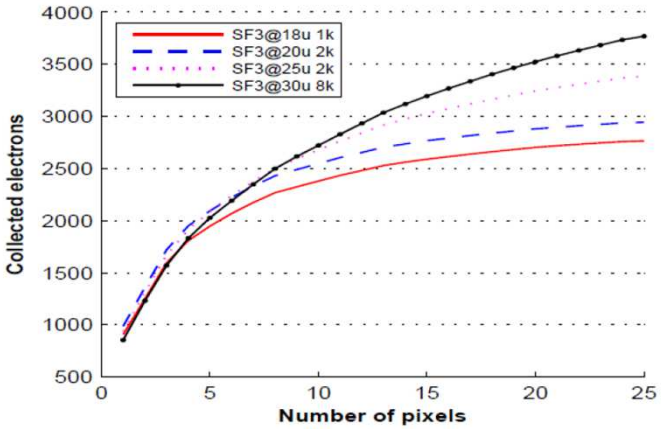
Y.Zhang, et al, NIMA 831(2016)99-104

Motivation:

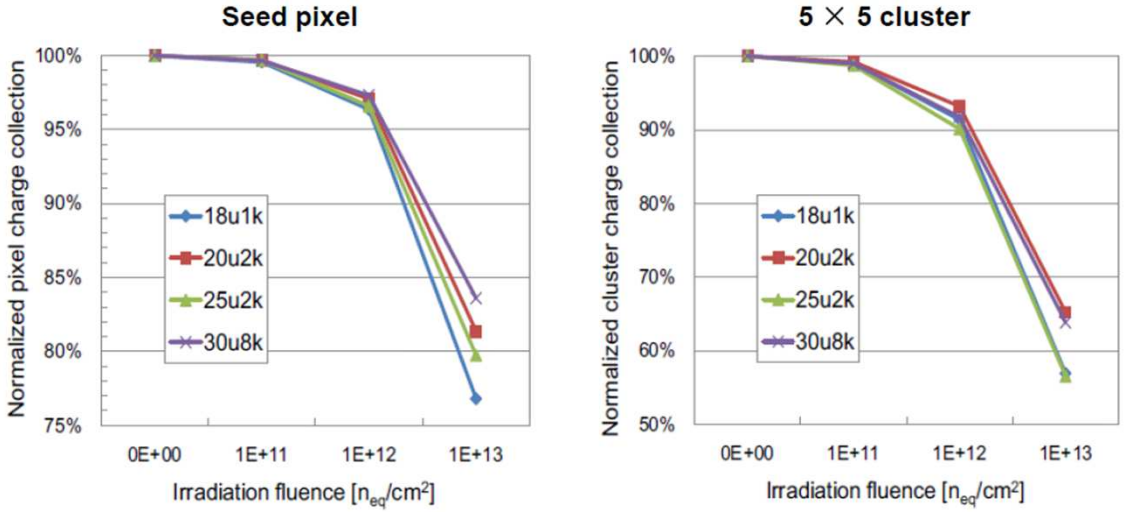
- Guide the diode geometry optimization and study radiation damage with different types of epitaxial layer

Simulation with different parameters

- Hit position
- Diode geometry
- Thickness and resistivity of the epitaxial layer
- Radiation damage



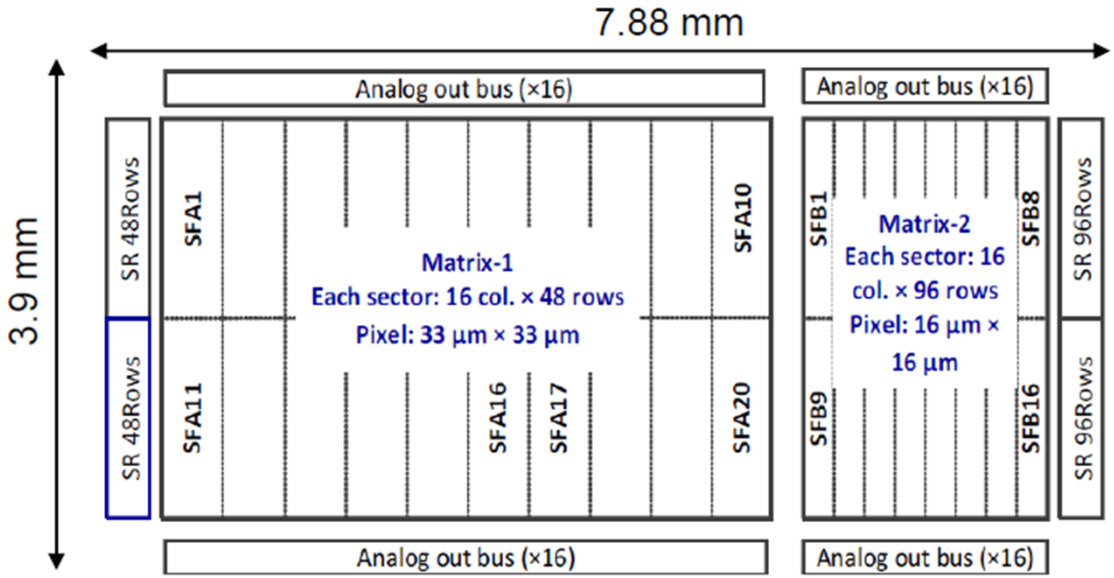
Pixel cluster with four different epitaxial layers



Charge collection with non-ionizing damage

1st CPS prototype design

- Goals: sensor optimization and in-pixel pre-amplifier study
- Floorplan overview:
  - Two independent matrices: Matrix-1 with 33 × 33 μm² pixels (except one sector SFA20 with 16 × 16 μm² pixels), Matrix-2 with 16 × 16 μm² pixels.
  - Matrix-1 includes 3 blocks with in-pixel pre-amplifier
  - SFA20 in Matrix-1 contains pixel with AC-coupled pixels



- Tower Jazz CIS 0.18 μm, November 2015 submission
- Two types of wafer:
  - 18μm HRES epi-layer wafer
  - 700Ω Czochralski wafer
- Sensor arrival at IHEP
- Test board and system in preparation, including the NIEL measurement.

2nd CPS prototype design

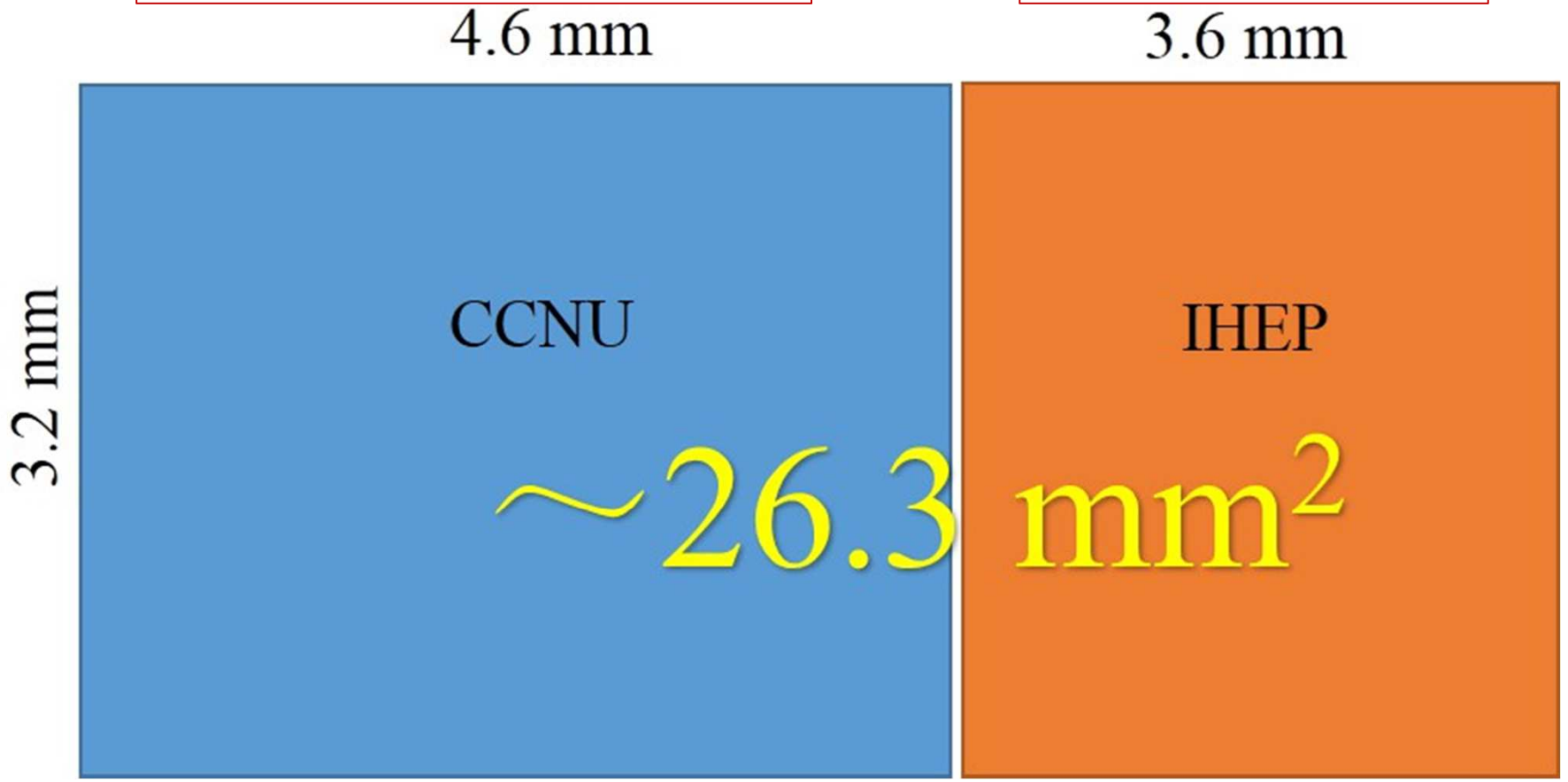
IHEP: Y. Zhang, Y. Zhou
CCNU: P. Yang

- Purpose: small-size digital pixel design verification, fast readout
- Pixel design:
  - Pixel size: smaller than 22 ×22 μm^2
  - Each pixel contains a sensing diode, a pre-amplifier and a discriminator
  - AC coupling: rolling-shutter readout with higher biased voltage
  - DC coupling: asynchronous readout with high gain and low noise
- Readout design:
  - Matrix readout using XYZ solution
  - Pixel size: 26×26μm^2
  - Signal duration time:< 3μs
  - Readout speed: 25 ns/hit
  - Power consumption: < 80 mW/cm^2

Proposed area

DC coupling pixel design + XYZ readout scheme

AC coupling pixel design



MPW submission：Feb., 2017

Items to be addressed in the future

- Sensor characterization needs more time.
- Overall sensor architecture should be considered now.
- Optimization study of vertex system will be critical.
- CDR requirements needs to be raised.
- Possible changes of sensor design
  - *Beam related background level*
  - *Impact of partial-double ring scheme, with time-stamp of microsecond*
  - *Impact of Z-pole running*