Waveform Sampling ASICs and Front-End Electronics for HEP/NP

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HONOLULU, HI, USA

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Mission statement:
- Design house for DOE electronics needs with commercial grade support

Personnel:
- 5 engineers and experimental physicists
- 30+ years combined experience

Tools:
- Commercial grade ASIC and electronic design tools

Funding:
- DOE SBIRs and contracts

Collaborations:
- U. of Hawaii Department of Physics- Professor Gary Varner

Incubated at the Manoa Innovation Center Near University of Hawaii

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Expertise, Tools and Experience

ASIC Design

- Mixed signal SoC
- Power optimization
- Full suite commercial grade Cadence license and server + design kits

Hardware Design

- FPGA, VHDL development
- Implementation
- Bring up and debugging
- Complex multi-layer boards

Expertise in:

- Radiation detection , fast timing, time of flight measurements
- Readout electronics for HEP/NP: large scale or benchtop

Belle II detector, KEK Japan- Two subdetector electronics developed and commissioned by Hawaii (KLM: 20k channels, iTOP: 8k channels)

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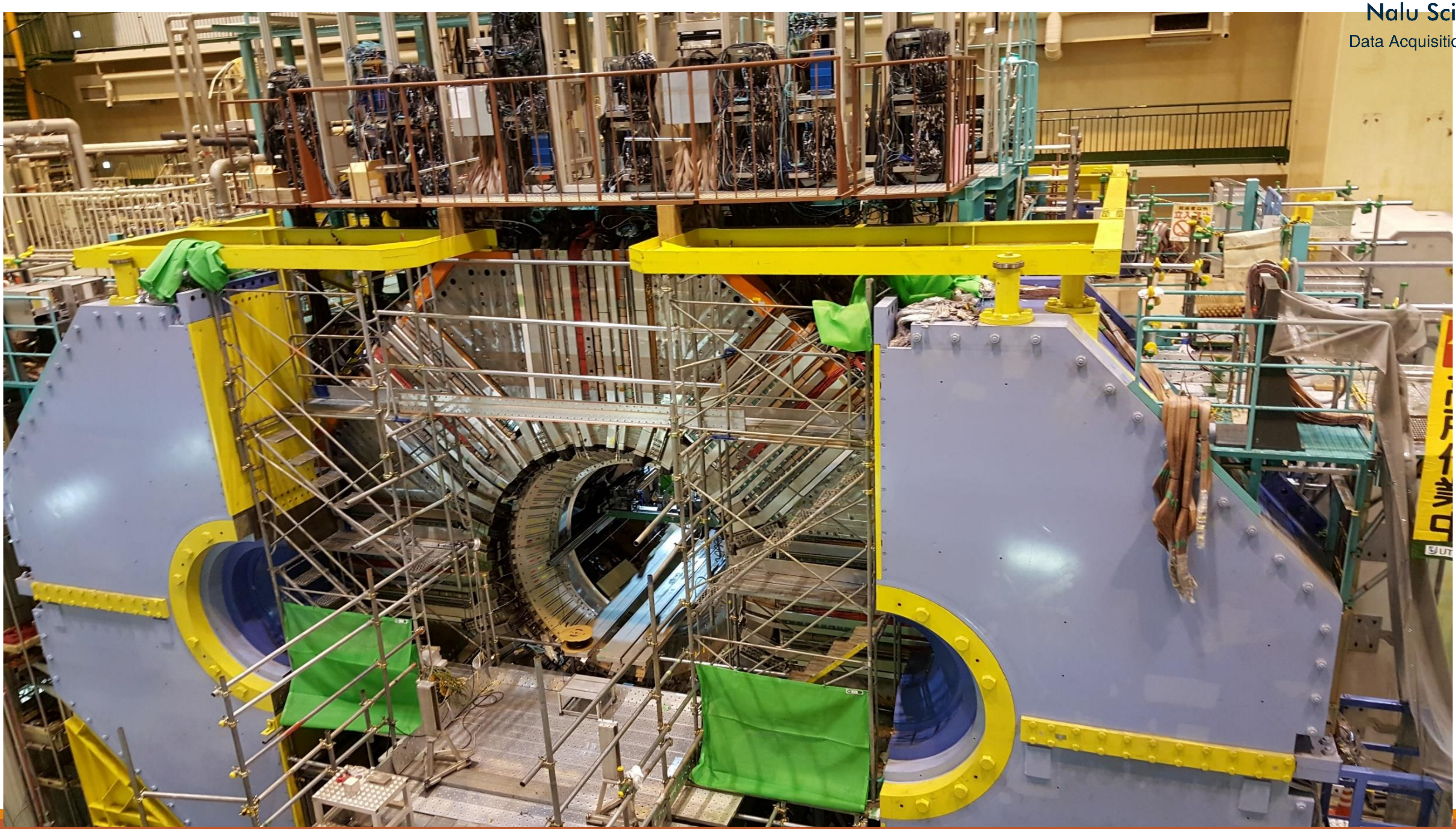
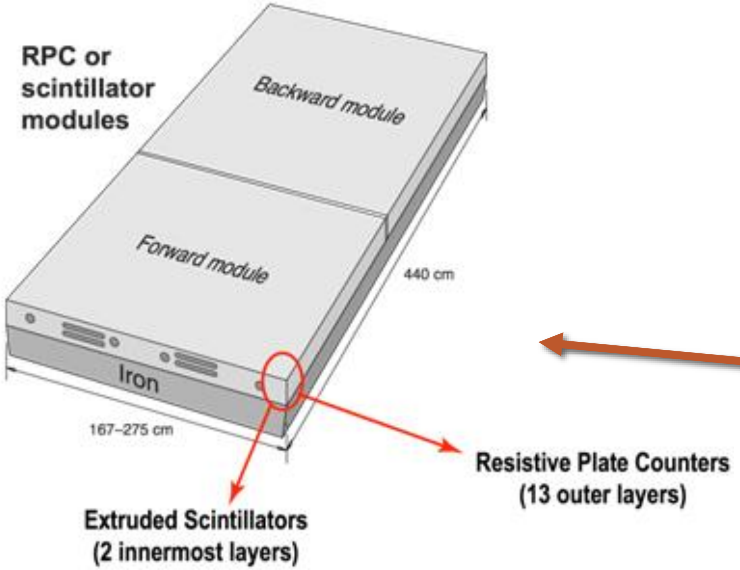


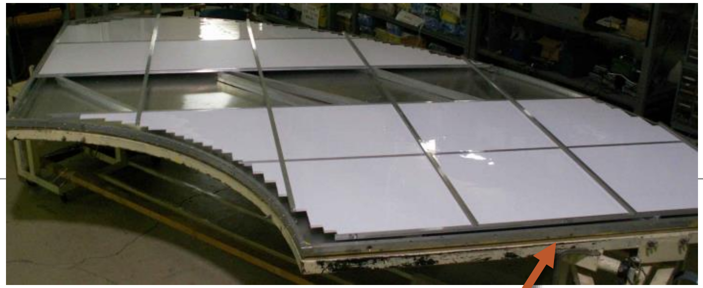
Belle II: KLM Scintillator Upgrade
20k+ channels at 1 GSa/s ea.

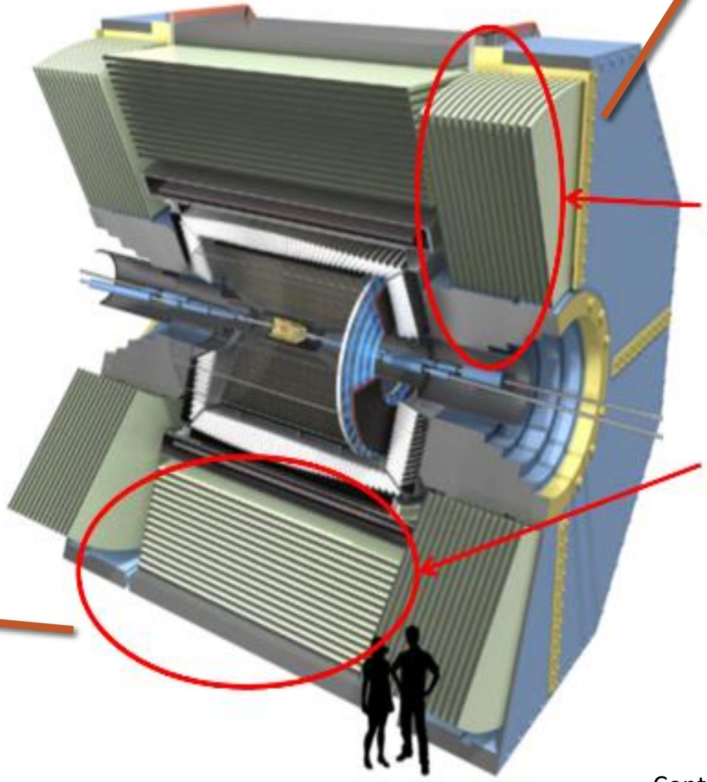
KLM detectors:

- Endcap: scintillators
- Barrel: scintillators +RPCs

Located outside the magnet



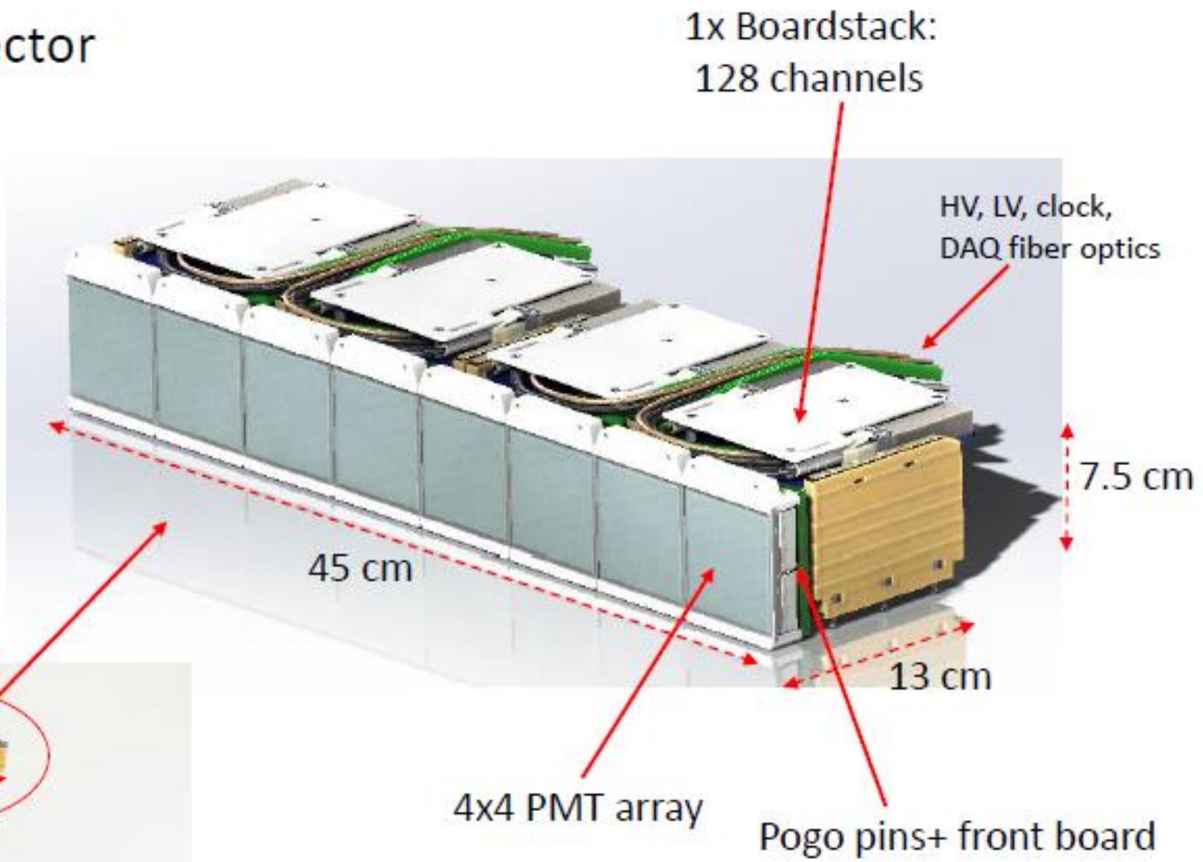


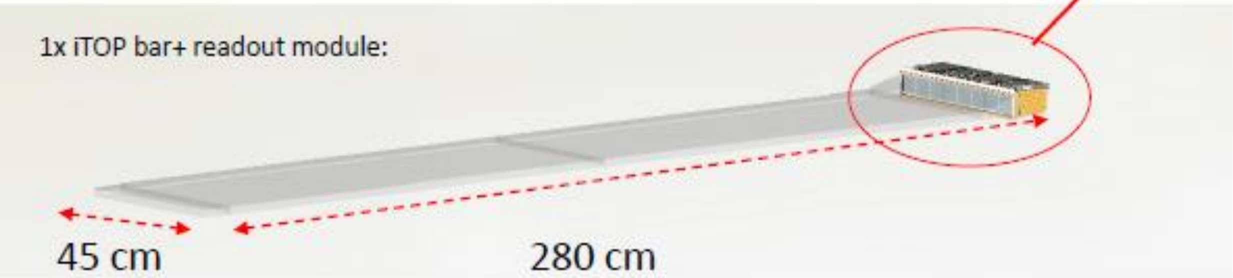


Content from Belle II collaboration

TOP and KLM Subdetectors fully commissioned

- 8192 channels of readout for iTOP subdetector
- 16 quartz bars, 1x module/bar
  - 1x readout module:
    - Photons in, DAQ data out
    - PMTs, interconnectes, amps, ASICs, FPGAs, heatsinks
    - 45 cm x 7.5 cm x 13 cm
    - 512 channels
    - Dense and compact- operates inside magnet
- All modules installed in detector





Content from Belle II collaboration

Lessons Learned - Opportunities

- Given new challenges:
  - Increased number of channels
  - Higher luminosity
  - Hardware cost and complexity
  - Requirements for better timing resolution
- Opportunities exist for innovation:
  - Size, power
  - Built-in signal processing
  - Built-in calibration
  - Cheaper overall design and faster deployment
- Solution: full waveform sampling + System-on-Chip
  - Allows feature extraction
  - Process pileups within FEEs
  - Immediately convert to digital and zero suppress
  - Avoid expensive/complex FPGAs

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Currently Funded ASIC Projects

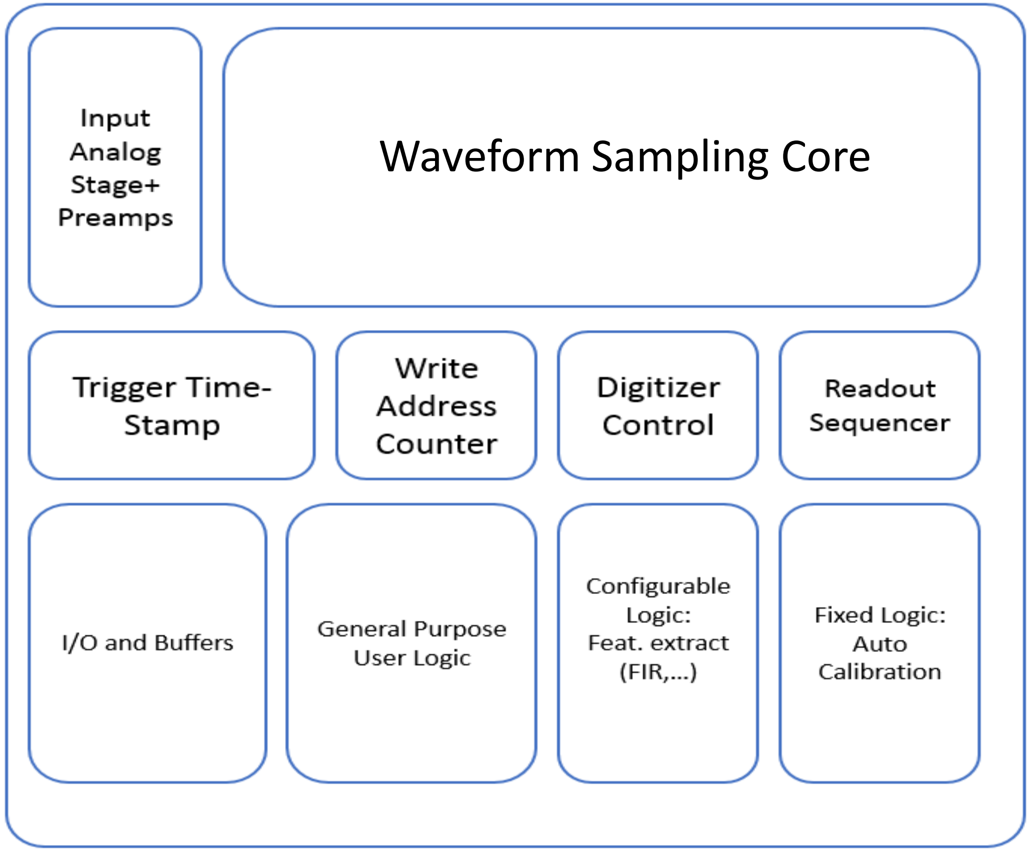
Project	Sampling Frequency (GHz)	Input BW (GHz)	Buffer Length (Samples)	Number of Channels	Timing Resolution (ps)	Integrati on	Built-in	Readout	Available Date
ASoC	3-5	0.8	8k	8	35	SoC	Pre amps	Fast serial	Feb 2018
SiREAD	1-3	0.7	4k	64	35-50	SoC	Amp, bias	Fast serial	Jan 2018
AARDVARC	6-10	2.5	4k	4-8	4-8	SoC	Pre amps	Fast serial	Mar 2018

- **ASoC**: Analog to digital converter System-on-Chip
  - Completed Phase I design, started Phase II
- **SiREAD**: SiPM specialized readout chip with bias and control
  - Phase I in progress
- **AARDVARC**: Variable rate readout chip for fast timing and low deadtime
  - Phase I about to start

All chips, are designed with commercial grade tools and licenses and can be sold once commercialized.

Feasibility study: **ASoC**- System on Chip

Compact, high performance waveform sampling- Finished Phase I SBIR

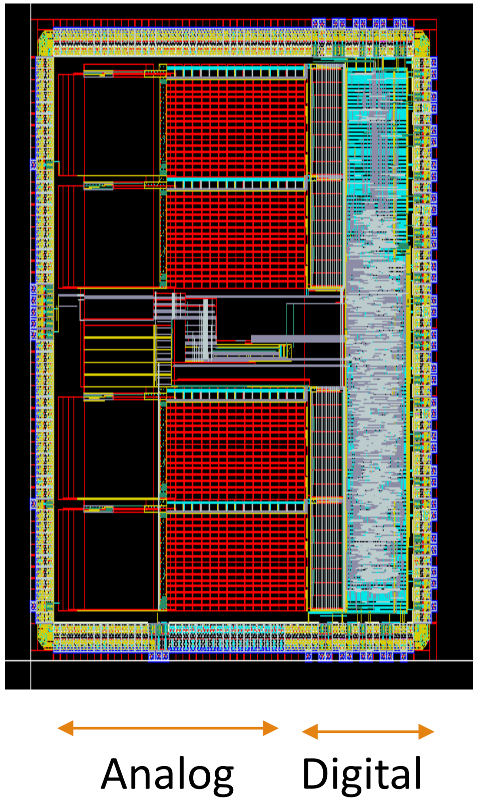


Spec	
Sampling rate	3-5 Gsa/s
ABW	0.8-1.1GHz
Depth	8k Sa
N channels:	8-32
Fab	250nm CMOS

Key Contribution:

- High performance digitizer: 3+ Gsa/s
- Highly integrated
- Commercially available
- On chip:
    - Analog storage
    - Reconfigurable DSP
    - Calibration

Funded Phase II Project



Layout ready for fab

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Summary

New generation of waveform sampling chips

- R&D funding and commercialization
- Roll out plan

Working with first adopters

- Identify needs
- Problem areas

Next steps

- Design schematic and layout
- Perform extensive simulations
- Stick with tight tape-out schedule
- Design eval boards according to first adopters’ needs