Readout Electronics Design for MRPC

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Content

- Upgrade of BESIII Endcap TOF
- High precision time measurement design based on HPTDC
- Readout electronics for T0 detector of CSR in HIRFL

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- **Upgrade of BESIII Endcap TOF**
- High precision time measurement design based on HPTDC
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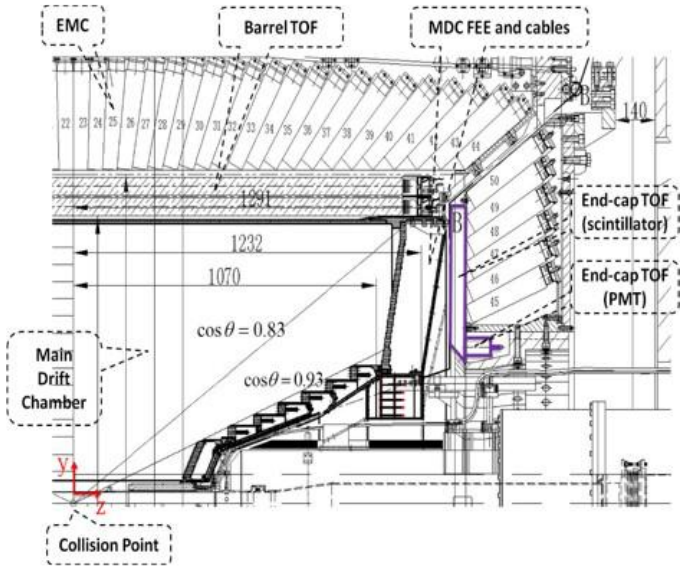
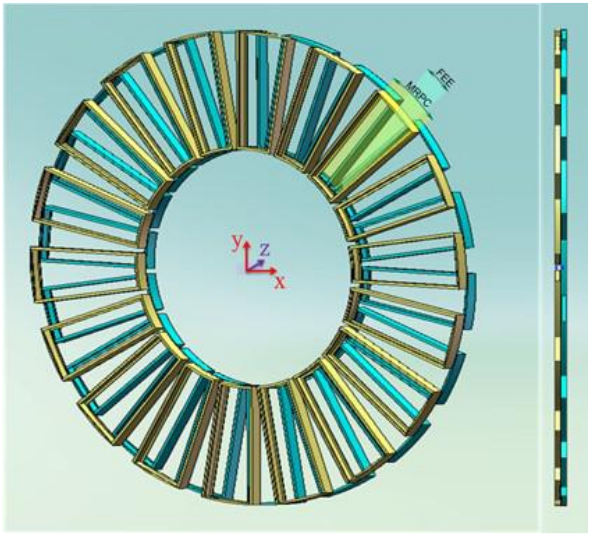
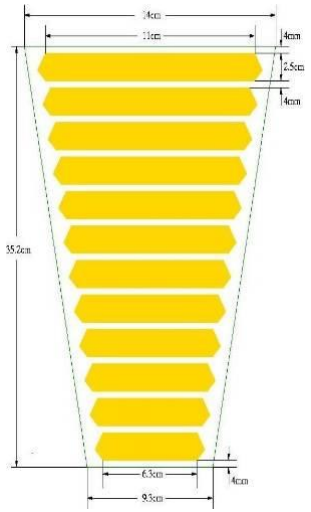
Upgrade of BESIII Endcap TOF

- Participate in upgrade of Endcap TOF (ETOF) in BESIII
- Replace the original PMT with MRPC to enhance system time resolution
- USTC group is in charge of time digitization electronics design & Test

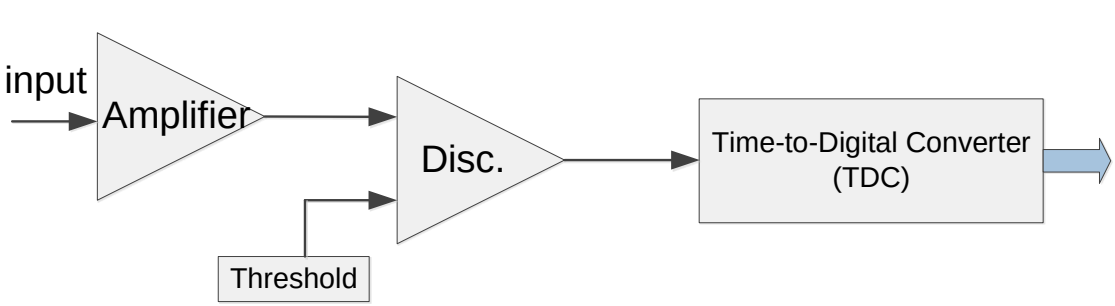


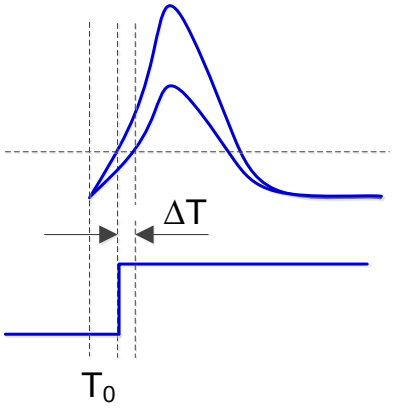




Basic method

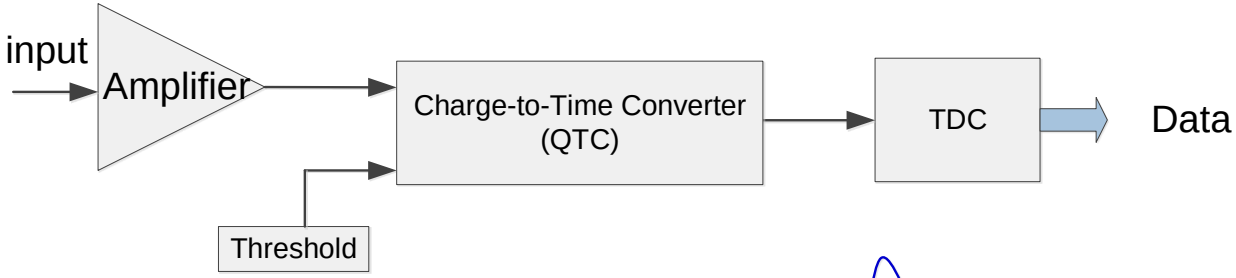
- Typical time measurement method: amplification + discrimination +TDC

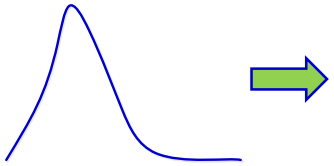


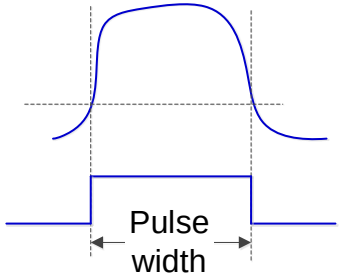


  - In high precision time measurement, leading edge discrimination is often employed -> time walk exits when signal amplitude varies

- One charge measurement method: amplification + QTC +TDC

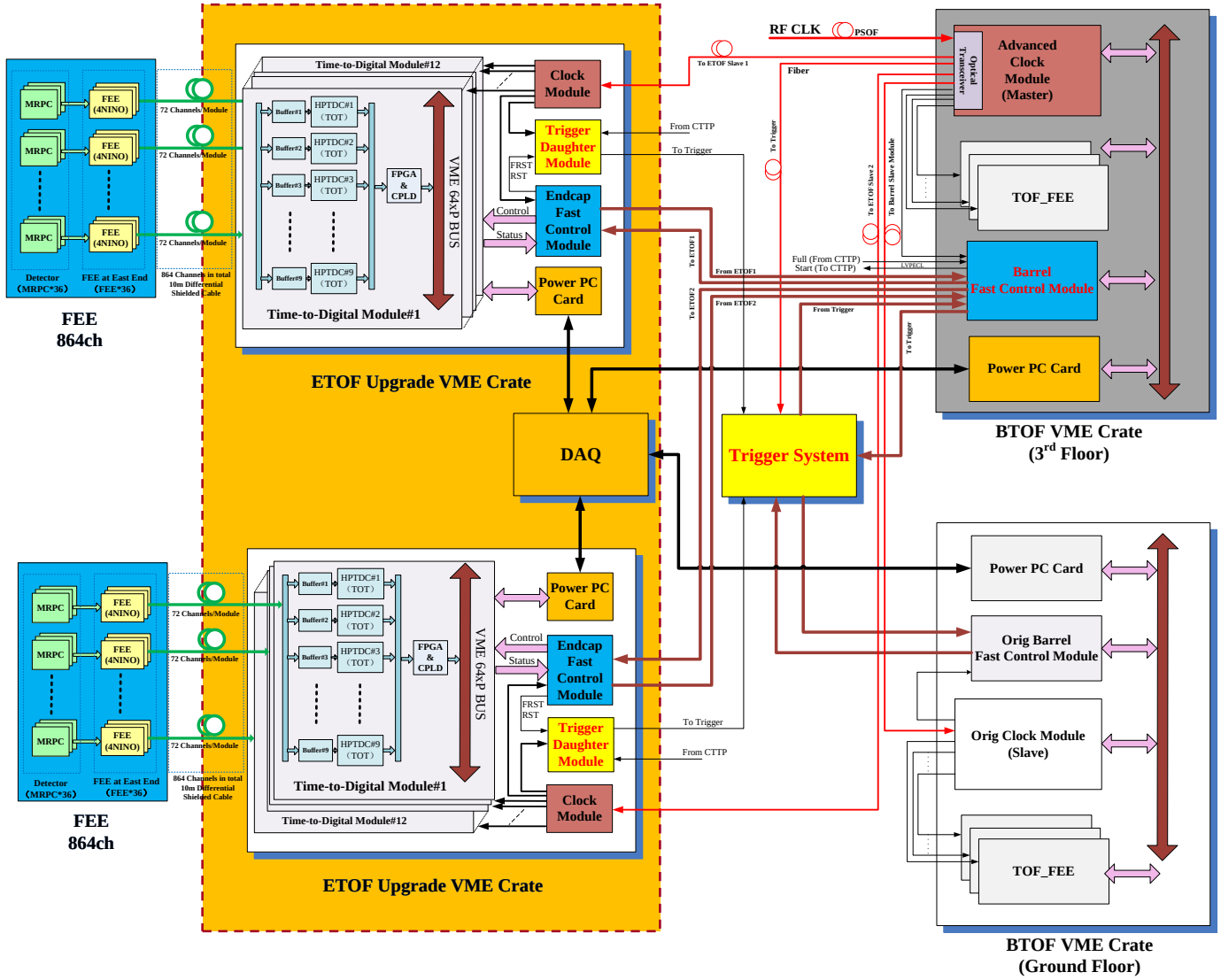




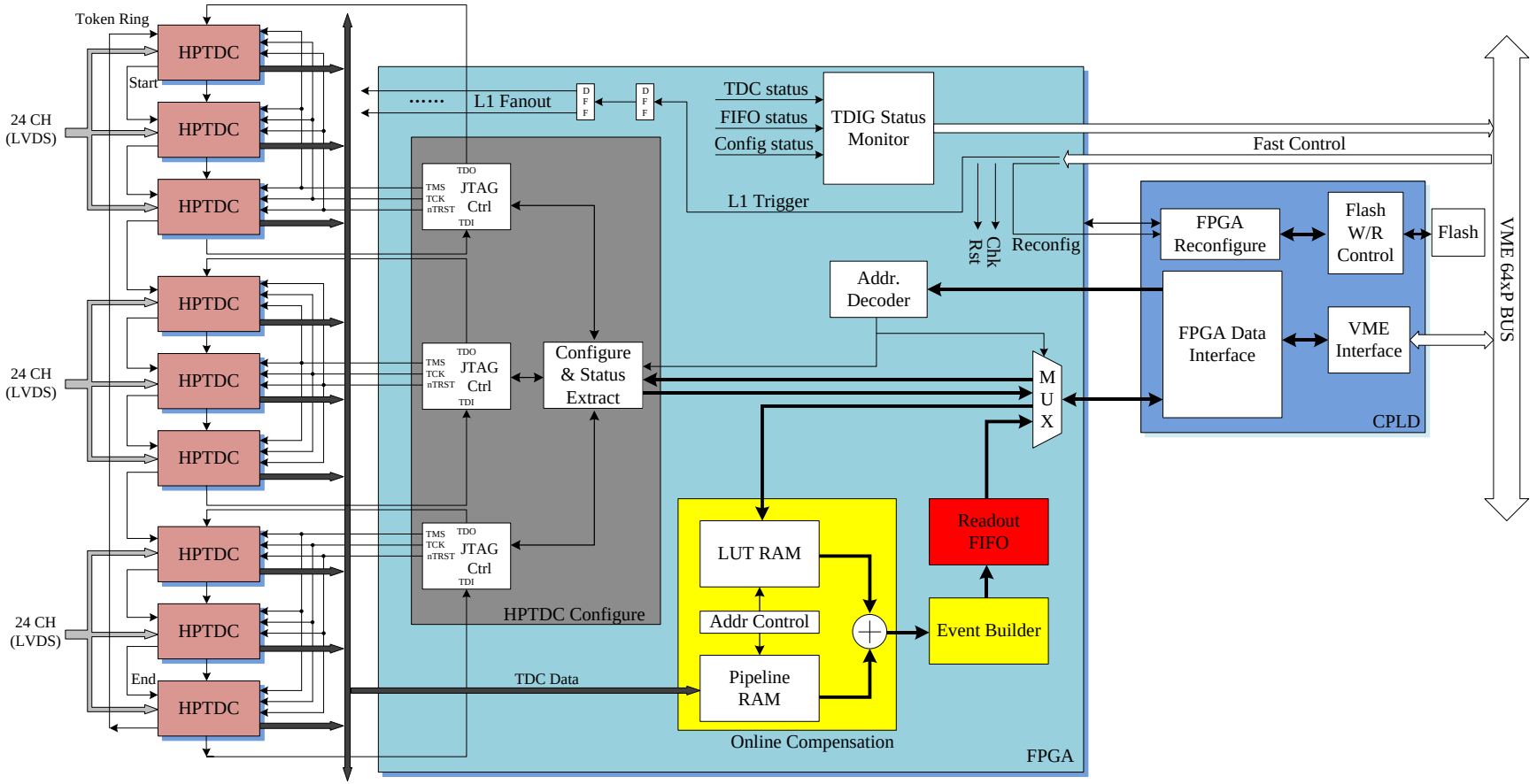


  - Time-Over-Threshold method: convert the amplified signal to a digital pulse:
  - leading edge ↔ time, pulse width ↔ charge

Time digitization module in ETOF



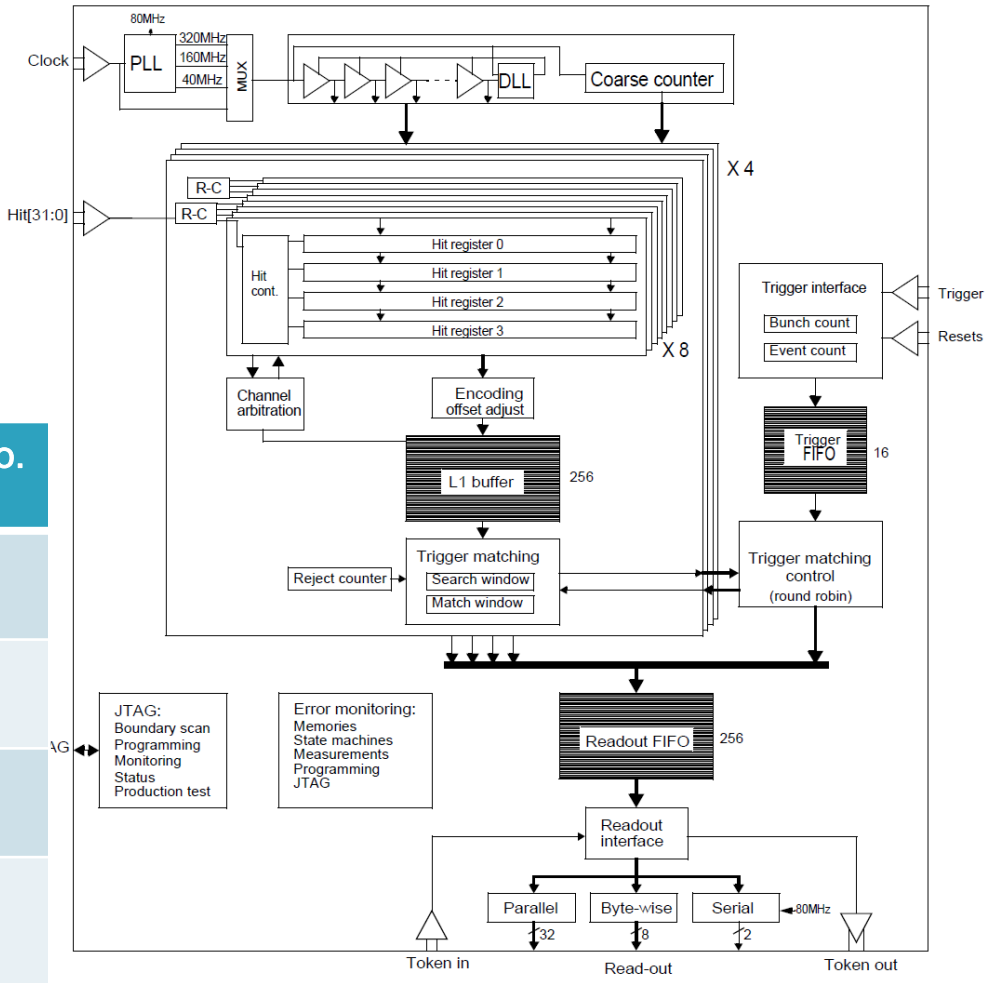
Time digitization module in ETOF



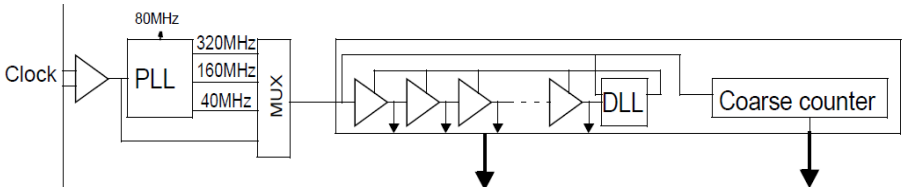
HPTDC

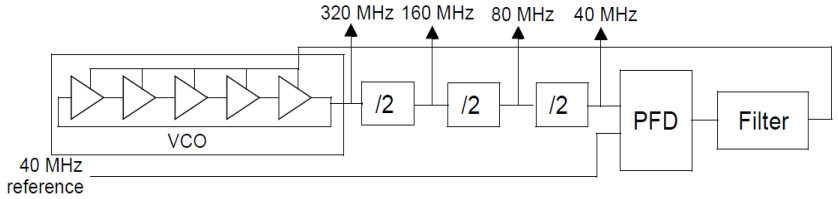
- HPTDC ASIC is employed in the electronics.
- It is a high performance TDC (time-to-digital converter).
- HPTDC features good time resolution:

mode	Bin size (ps)	RMS (ps)	Chan. No.
low resolution	781	265	32
medium resolution	195	86	32
high resolution	98	64	32
very high resolution	24	58 17 (corrected)	8

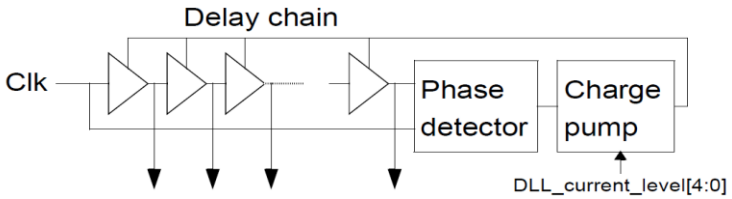


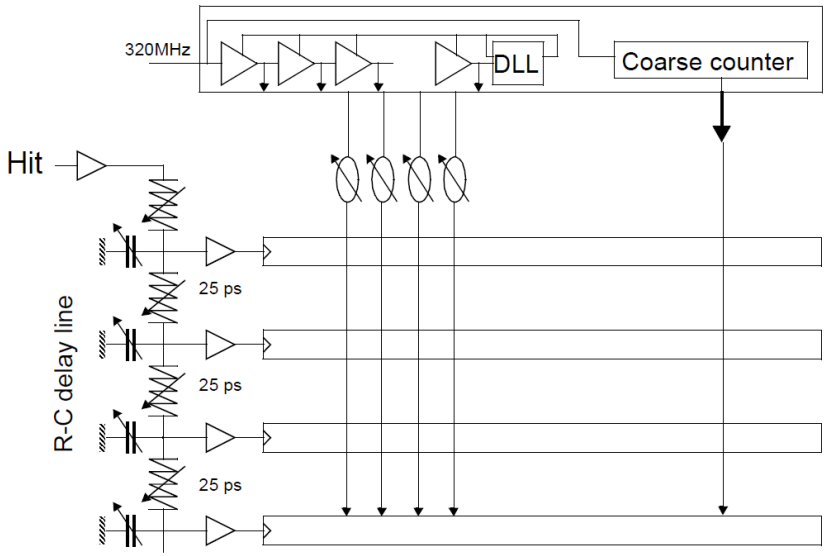
HPTDC





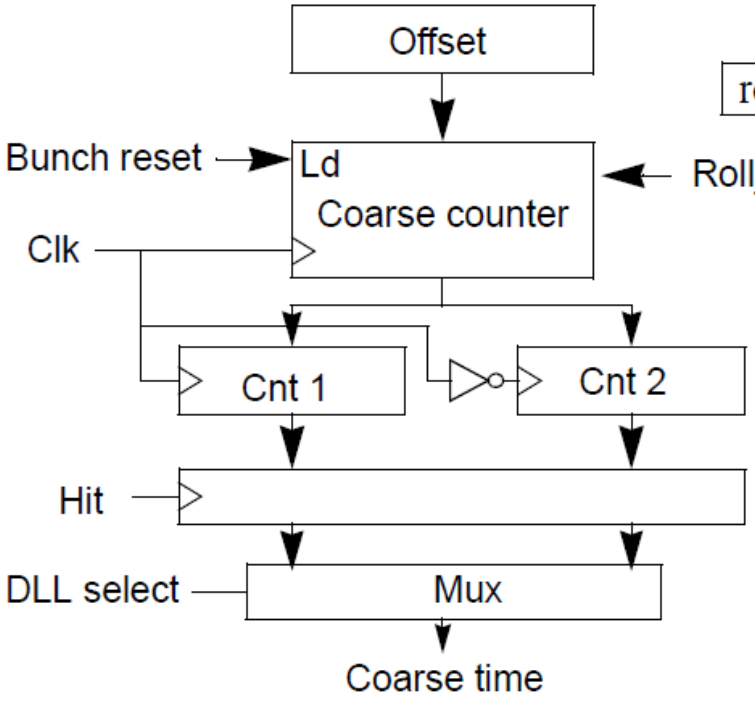
- Three stage time interpolation:
  - PLL with optional outputs ~ 3 ns
  - DLL with 32 outputs ~ 100 ps
  - RC delay cells based on RC structure ~ 25 ps
- Non-Linearity errors exist
- Correction is indispensable to obtain optimum performance

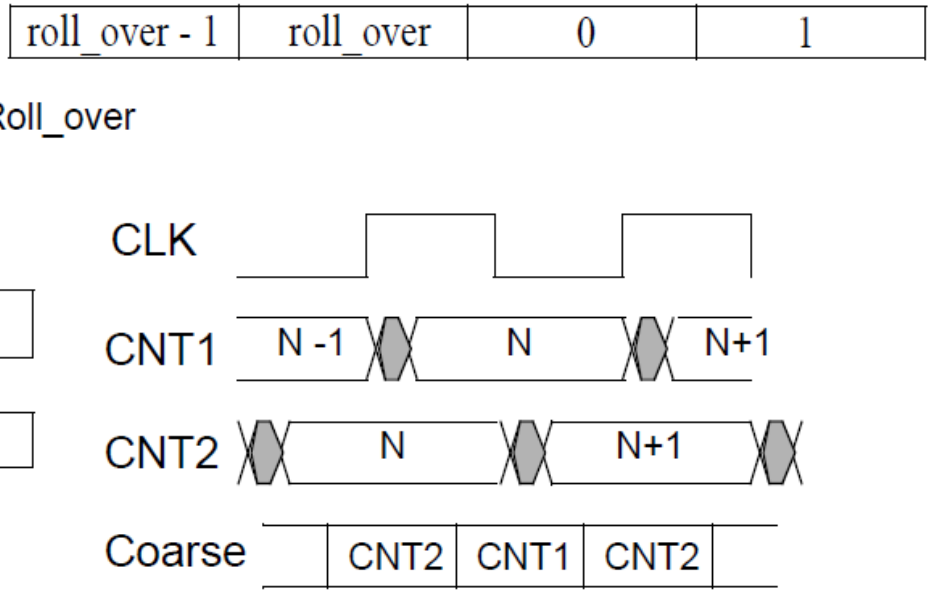




HPTDC

- Since hit is asynchronous with the clock signal, a pair of counters are employed to avoid metastability, with opposite phases of clocks.
- This technique is also employed in our FPGA-based TDC design.

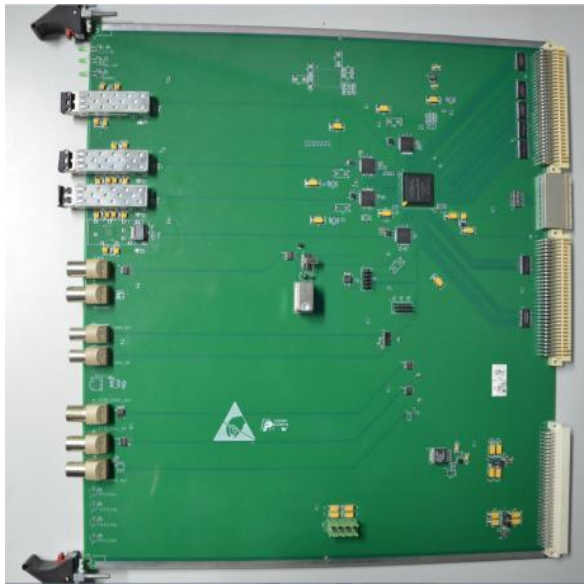




Photograph of elelctronics

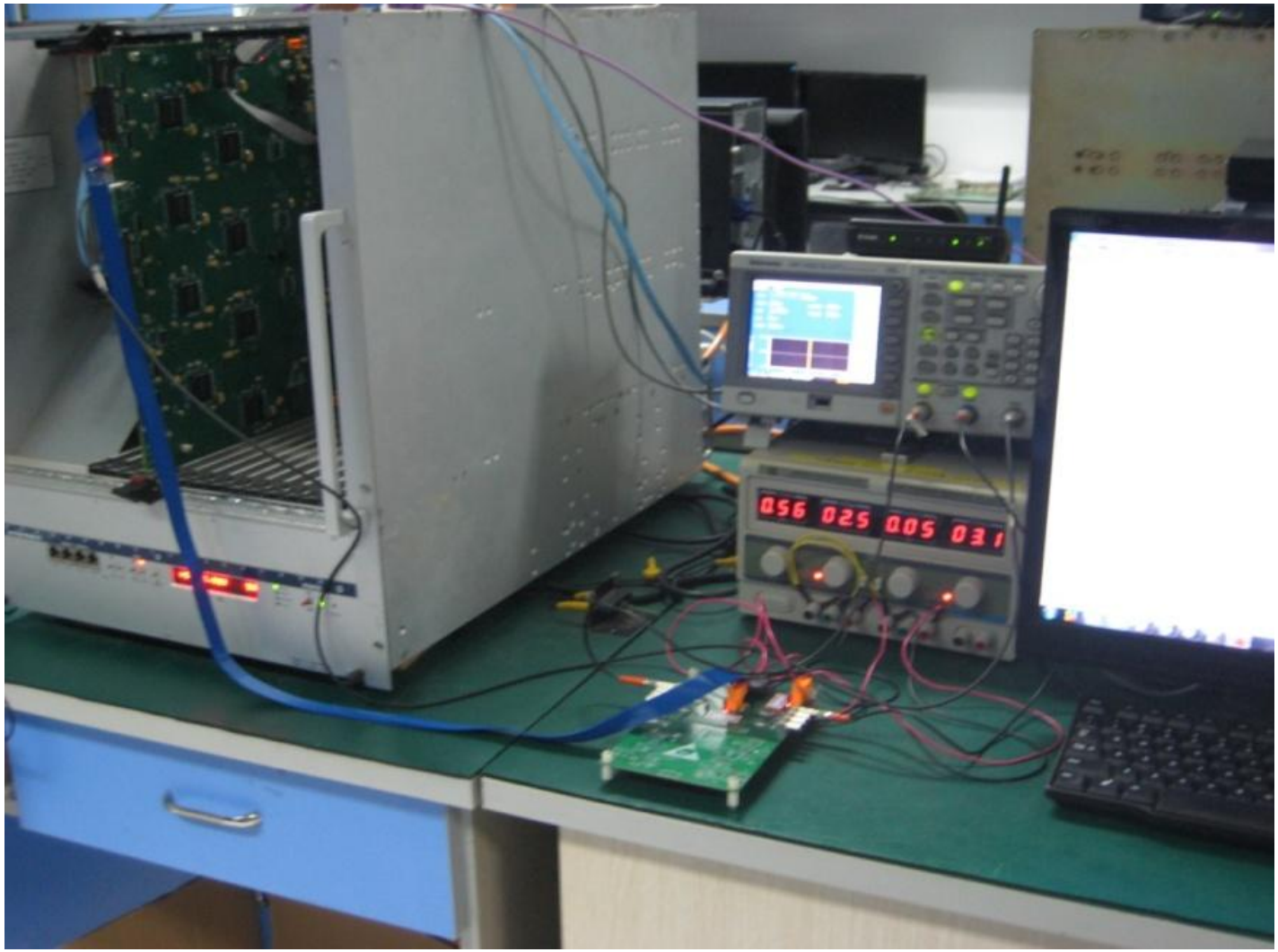
Time digitization module

Clock module



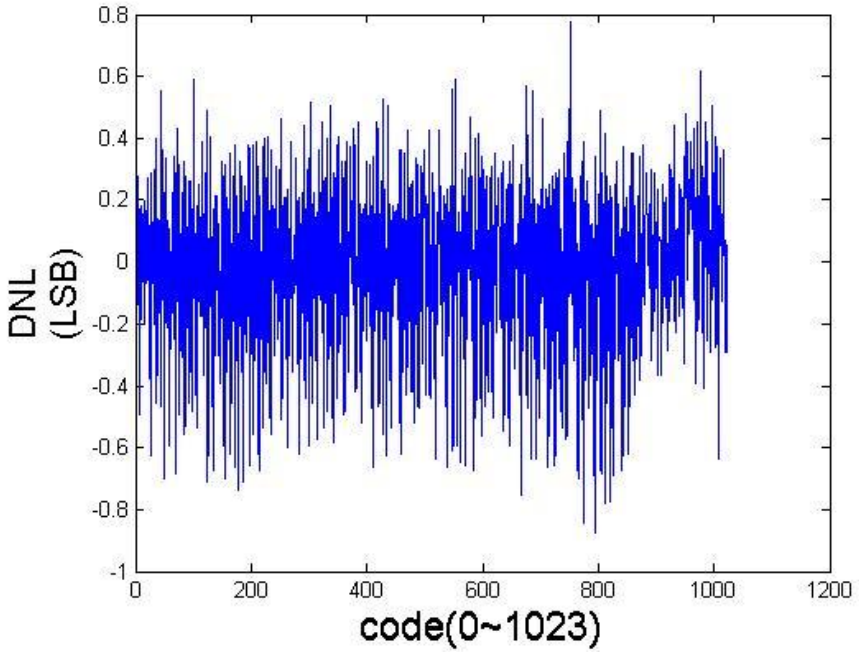
Fast control module

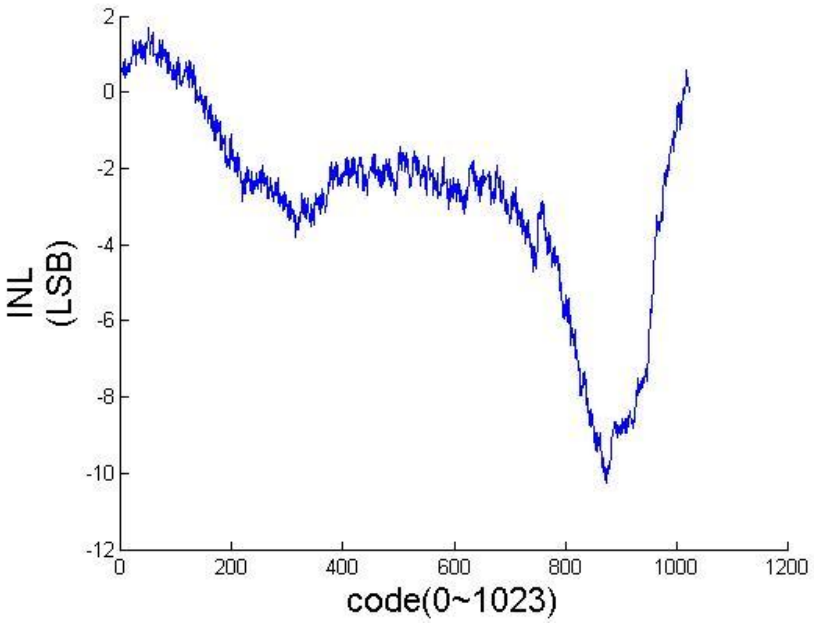
Performance test



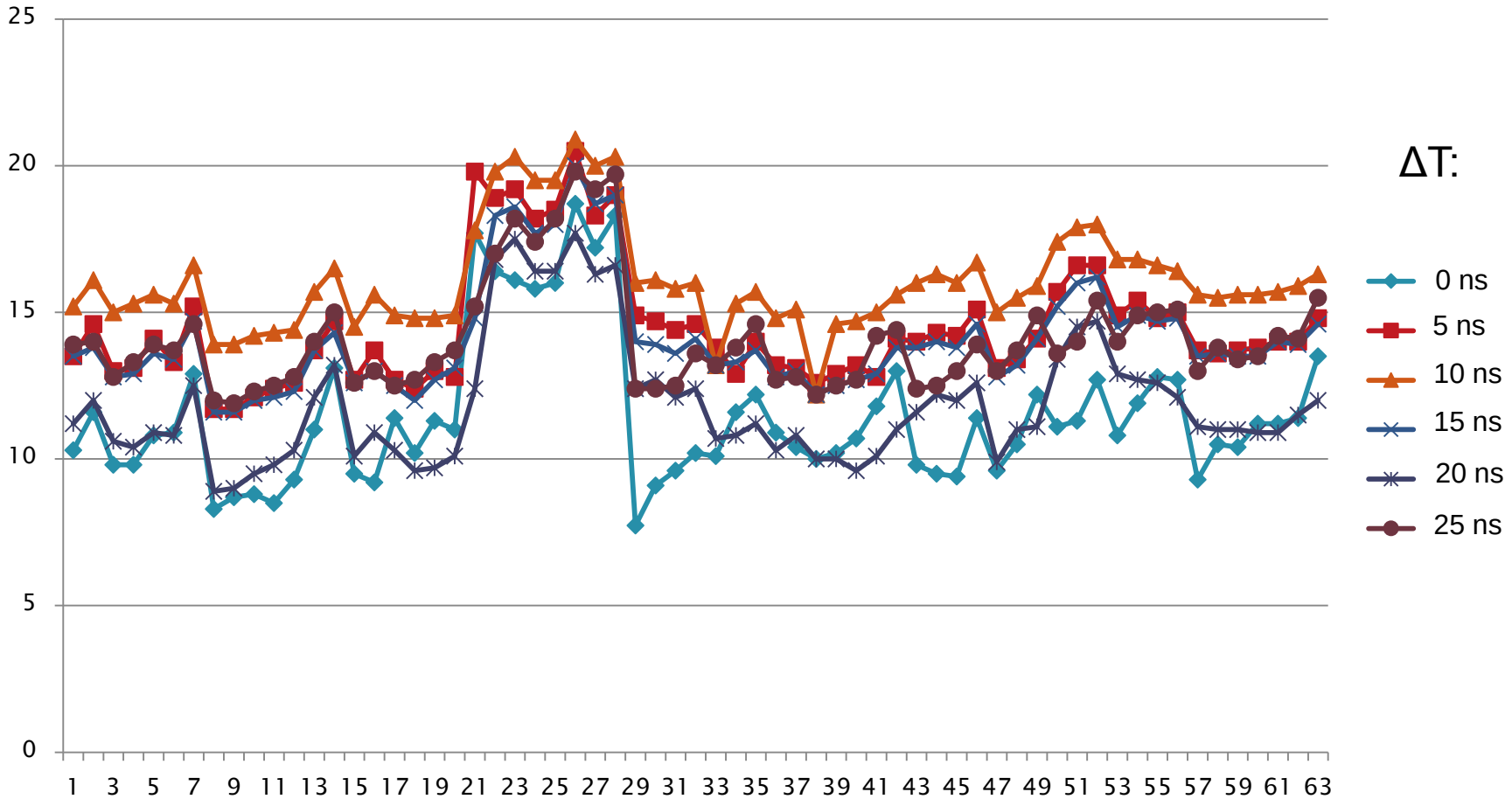
INL

- INL:
  - DNL: Differential Non-Linearity
  - INL: Integral Non-Linearity

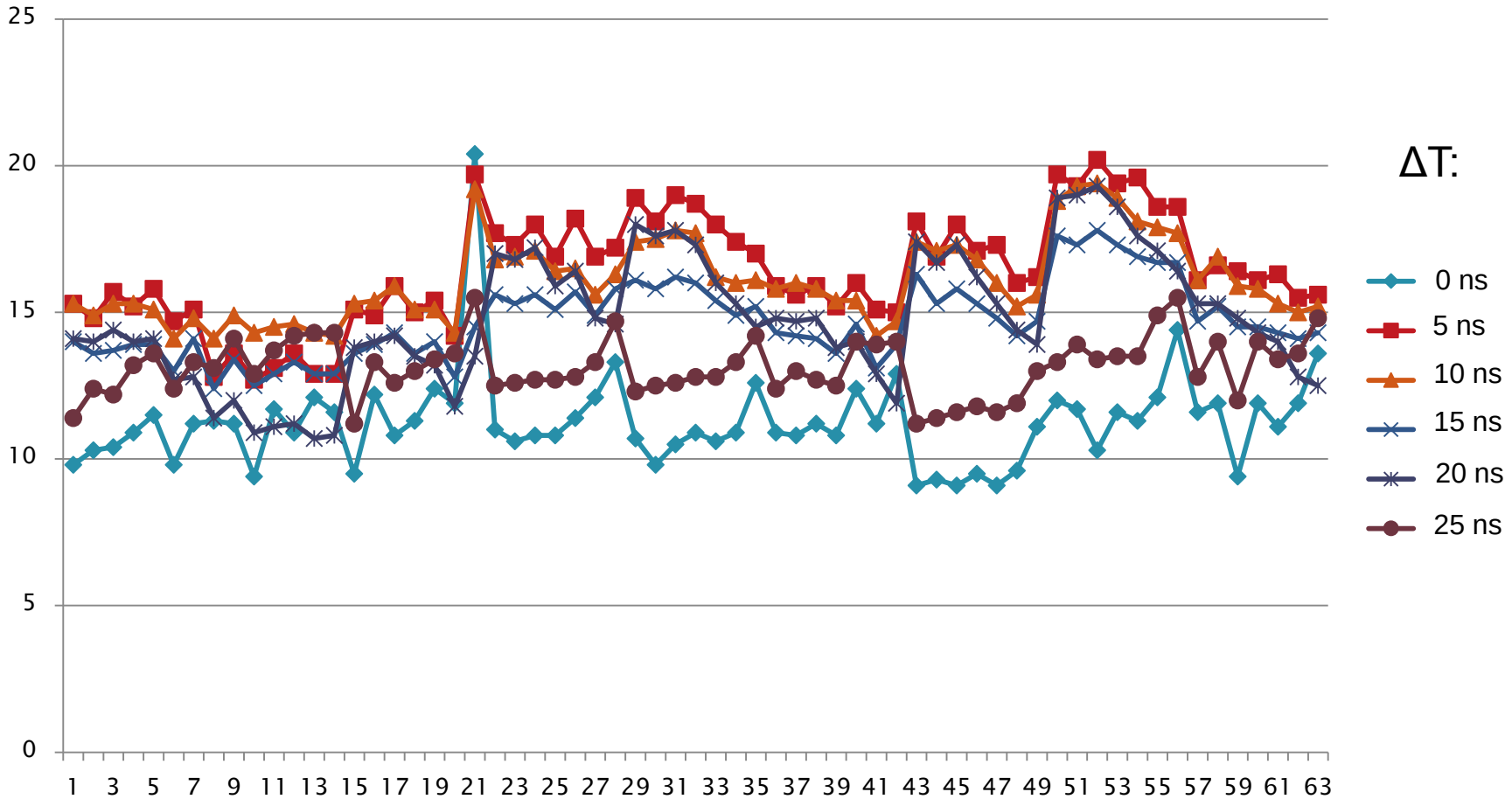




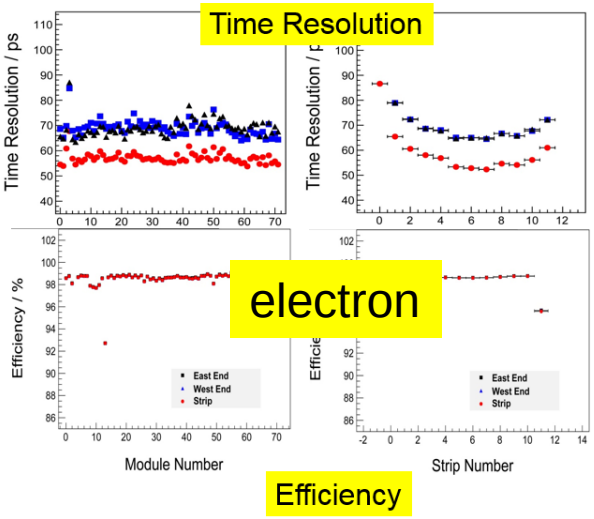
Time resolution – Leading Edge

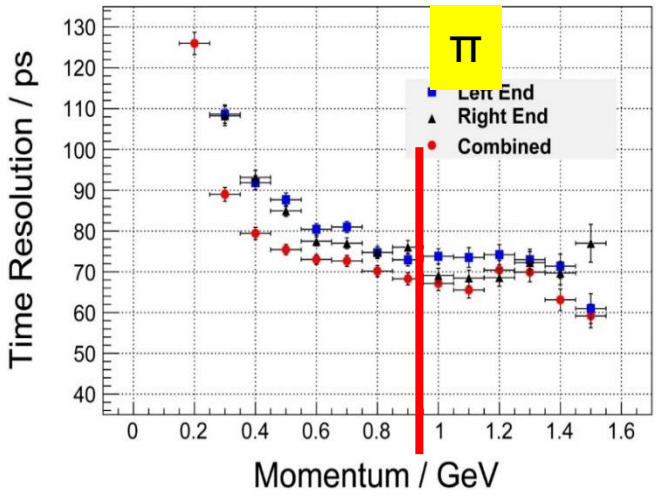


Time resolution – Trailing Edge



Performance after installation





Experiment	Module Size	Pad Size	Pad Number	gap number	gap/um	Readout mode	Resolution(ps)
STAR TOF [1] [2]	6.3×20 cm²	6.3×3.1cm²	6	5	220	Single-end	~80(π)
STAR MTD [3] [4]	93×58 cm² 90×58 cm²	87×3.8 cm² 87×3.8 cm²	10 12	2×5 6	250	Double-end	~90(μ)
ALICE TOF[5][6]	13×120cm²	3.4×2.5 cm²	96	2×5	250	Single-end	86 (π)
BESIII ETOF	L1:13.7 cm L2:20.2 cm H:38.2 cm	L:9.1-14.1 cm W:2.4 cm	12	2×6	220	Double-End	60*（e）- 70*（π）

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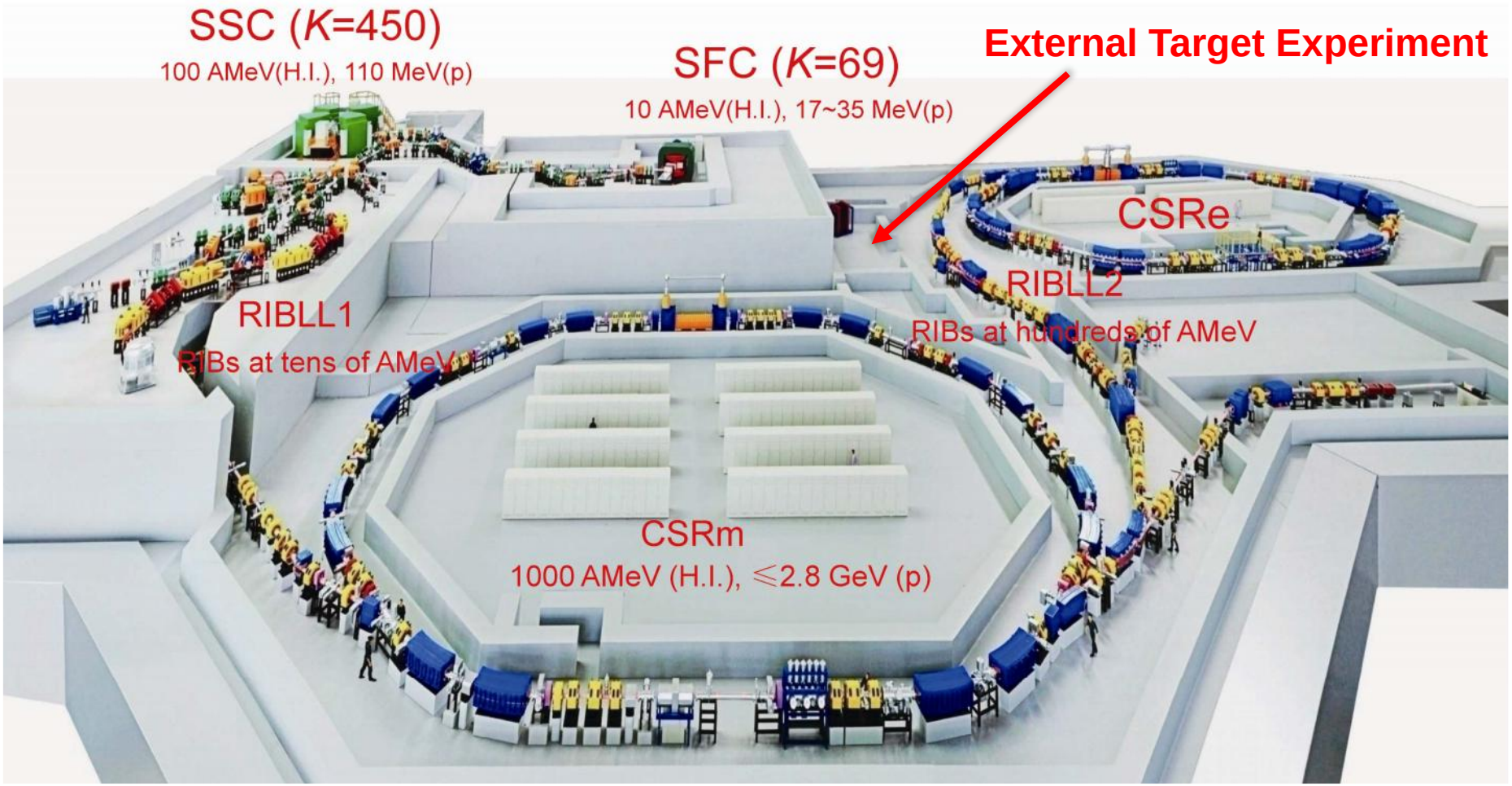
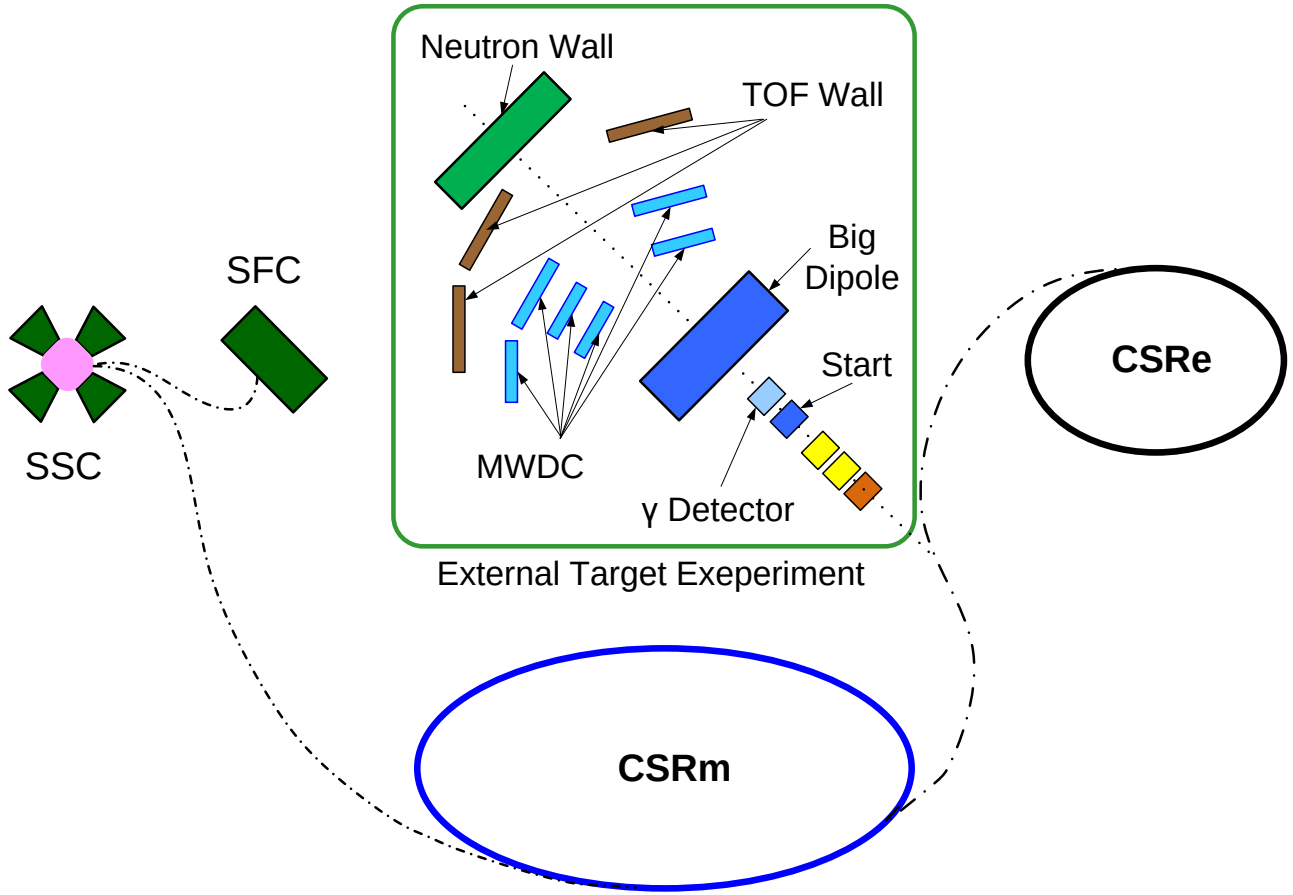
- Readout electronics for T0 detector of CSR in HIRFL

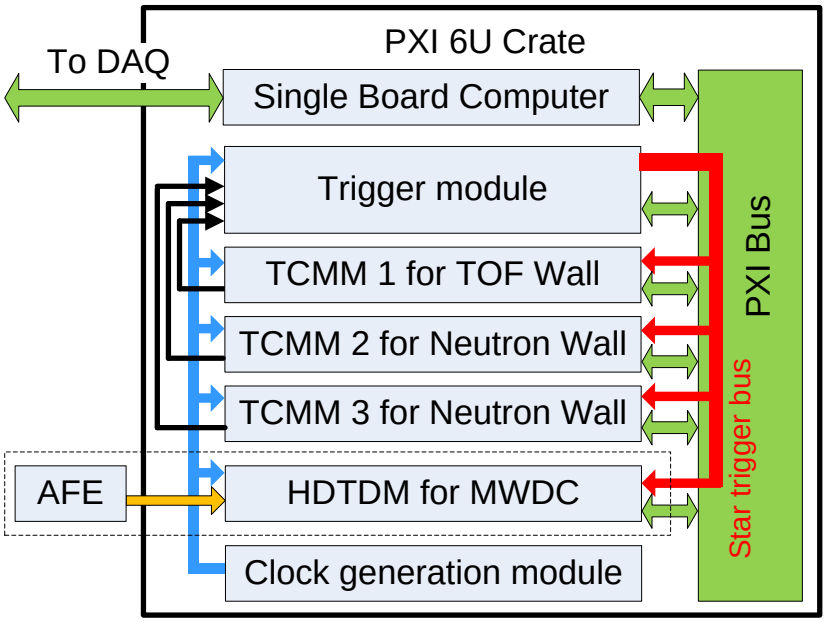
External Target Experiment in CSR of HIRFL



External Target Experiment in CSR of HIRFL



Readout electronics for External Target Experiment



Readout system architecture

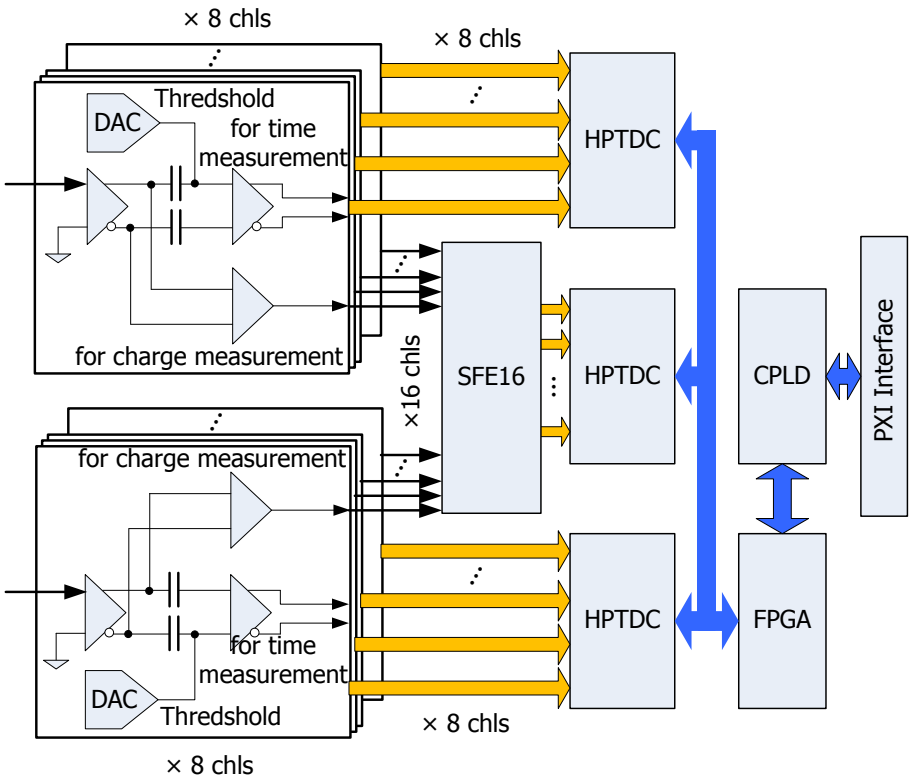
- Based on PXI 6U standard:
  - TCMM: TOF and Neutron wall
  - HDTDM: MWDC(with the Analog Front end)
  - Trigger Module
  - Clock Module

Time and Charge Measurement Module

Photograph of the TCMM

- Input amplitude: 50 mV~1.5 V
- 16 Channels
- Time resolution: 25 ps
- Charge resolution: 5%
- Data transfer: Master mode burst write transaction

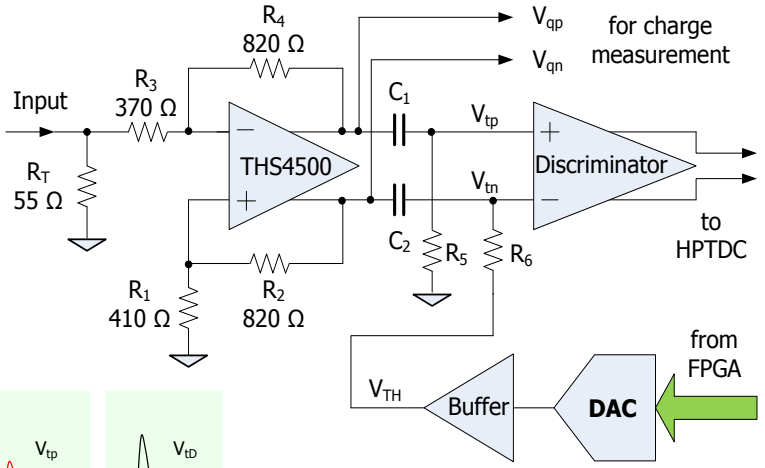
Time and Charge Measurement Module

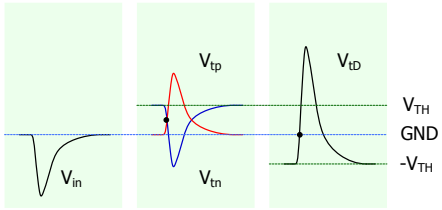


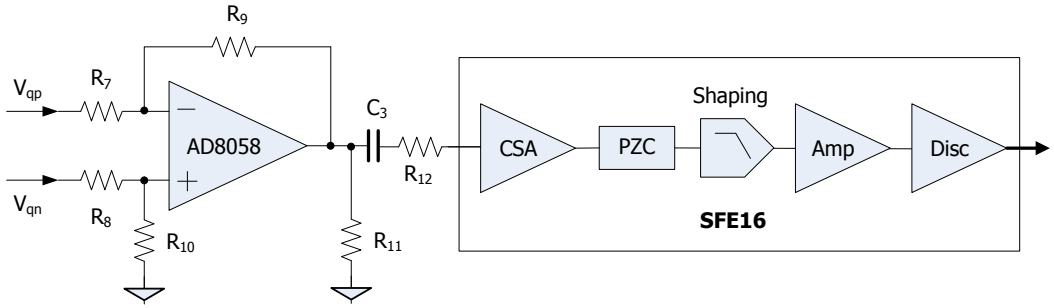
- Amplifier
- Time measurement:
  - Leading edge discrimination
- Charge measurement:
  - TOT(Time Over Threshold)
  - SFE16 chips
- HPTDC chips
- FPGA chips

Time and Charge Measurement Module

- Time measurement:
  - differential amplification + differential discrimination to eliminate common mode noise and influence
- Charge measurement:
  - Time-Over-Threshold (TOT) method
  - Employing SFE16 ASIC
  - Amplification, V/I conversion, CSA, shaping, amplification and discrimination

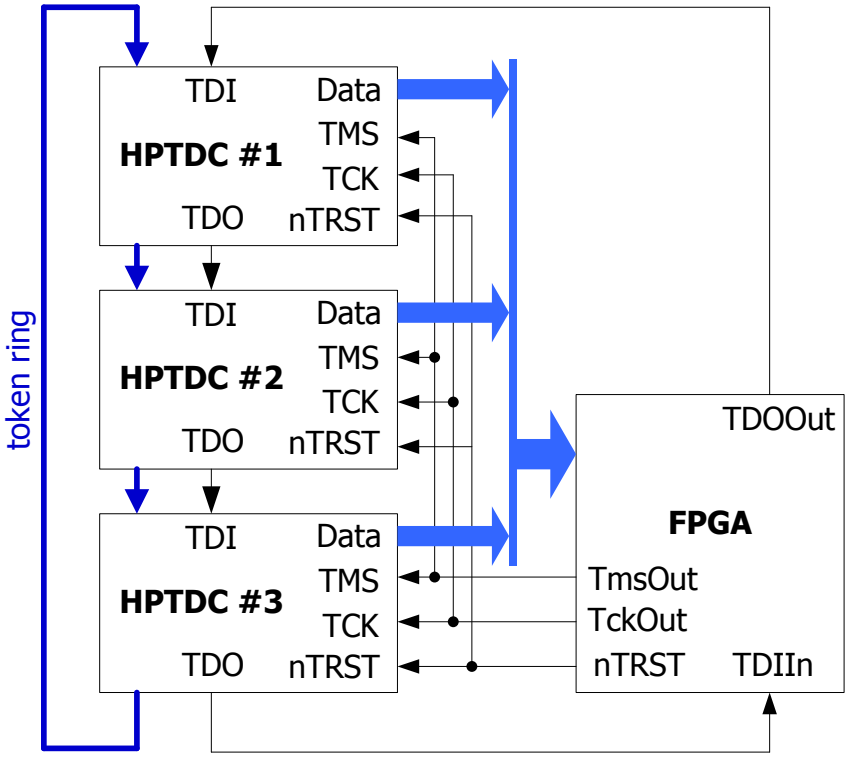






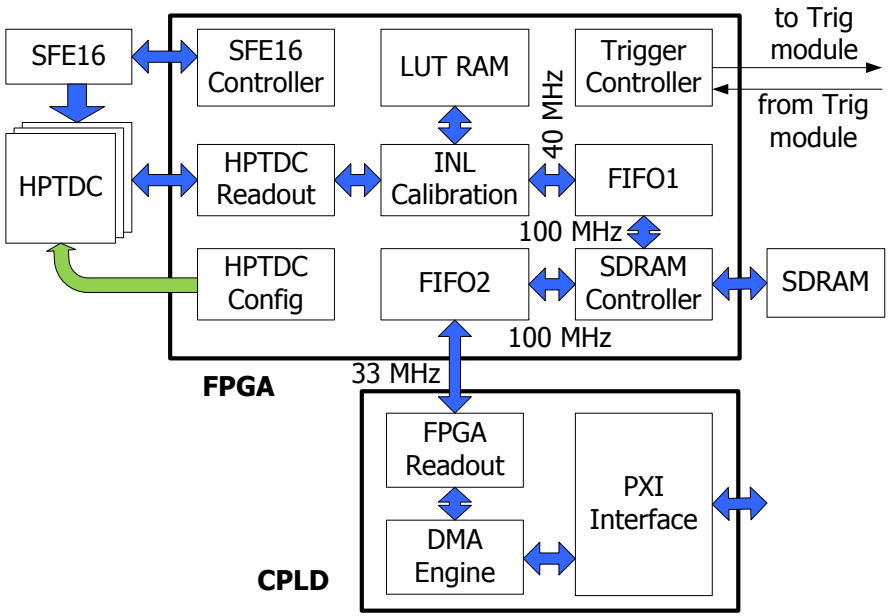
Time and Charge Measurement Module

- Three HPTDCs are employed.
- Two working in the very high resolution mode are responsible for time measurement
- One working in the high resolution mode is responsible for charge measurement.
- These 3 HPTDCs are chained together, and configured and read out based on a token ring method.

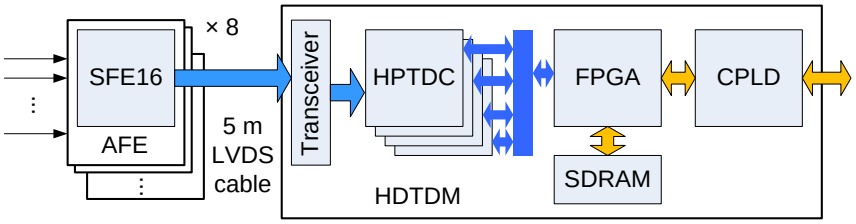


Data readout based on PXI Bus

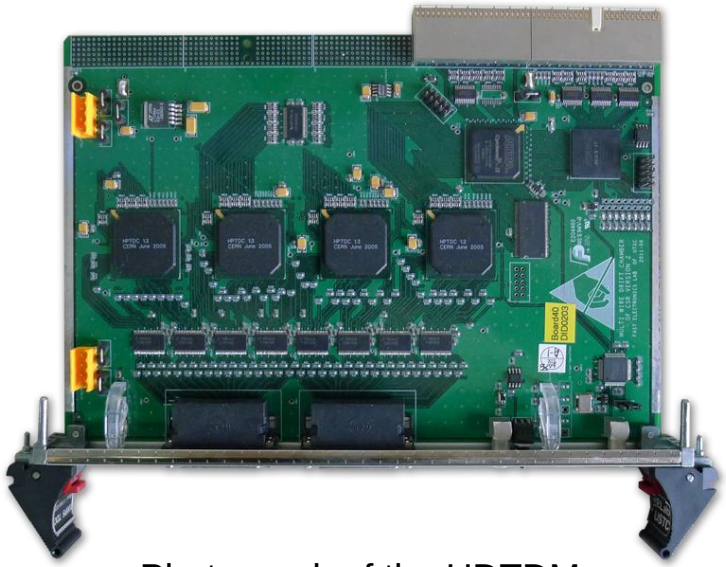
- PXI is extended version of PCI, which features much higher data rate then buses such as VME.
- Star trigger bus is very good structure to fan out the trigger signal to multiple modules in physics experiments.
- External SDRAM provides extra data buffering to avoid data loss in special situation.



High Density Time Measurement Module



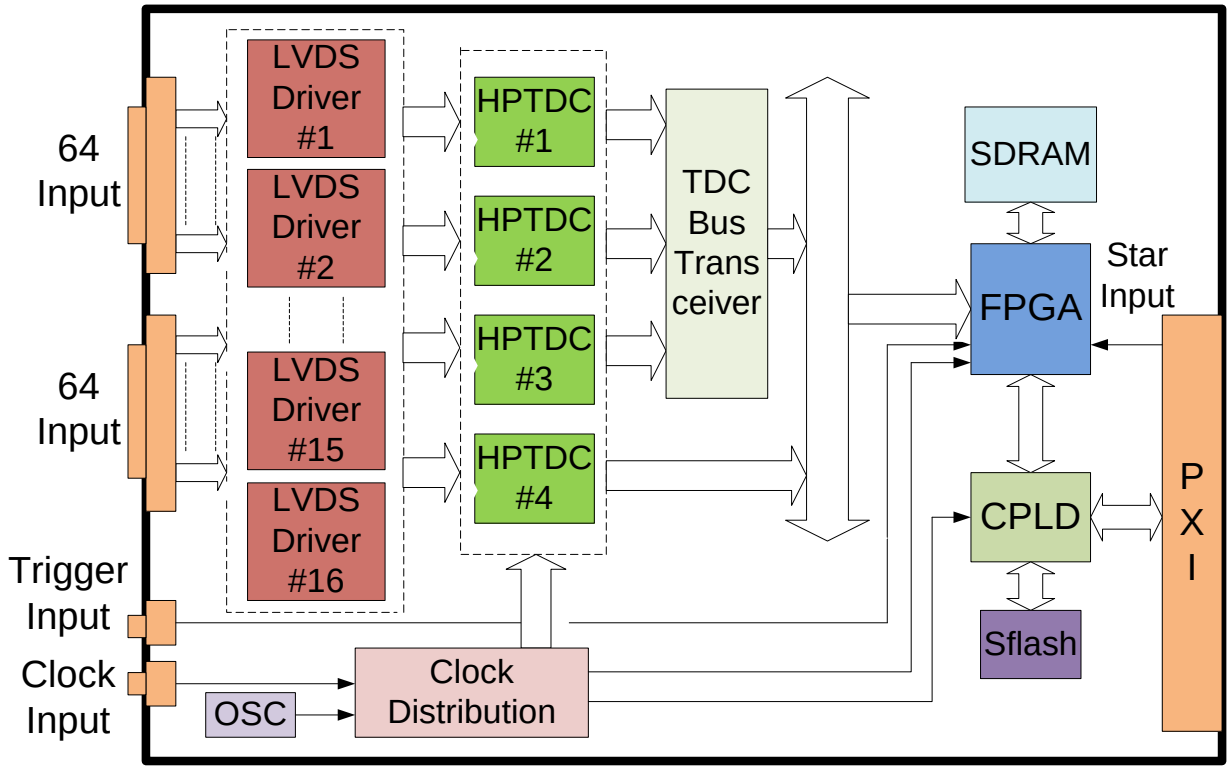
Circuits for high-density time measurement



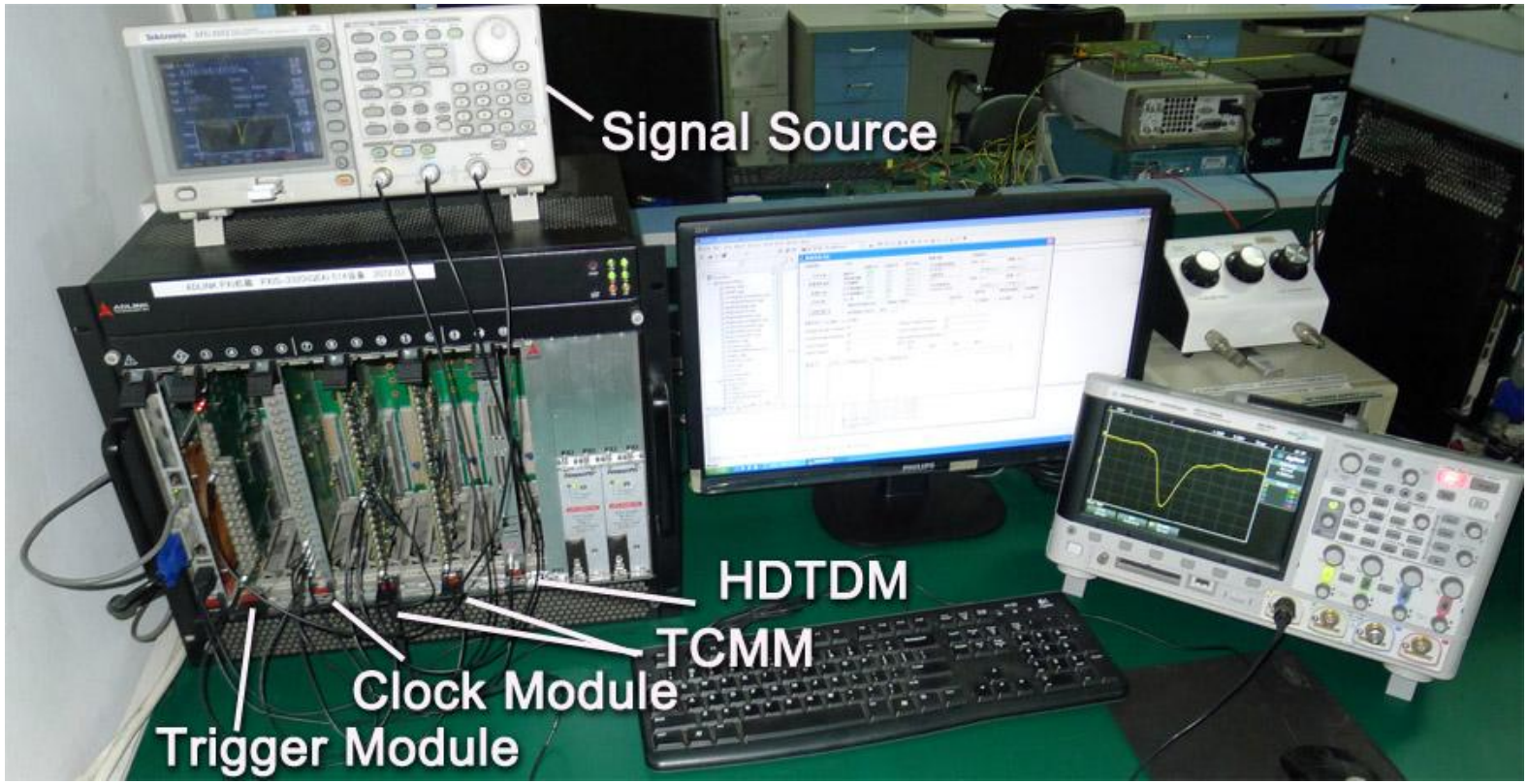
Photograph of the HDTDM

- AFE
  - Charge-to-time conversion
- HDTDM
  - Fully differential
  - 128 channels
  - Time resolution: 100 ps
  - Master mode burst write transaction

High Density Time Measurement Module

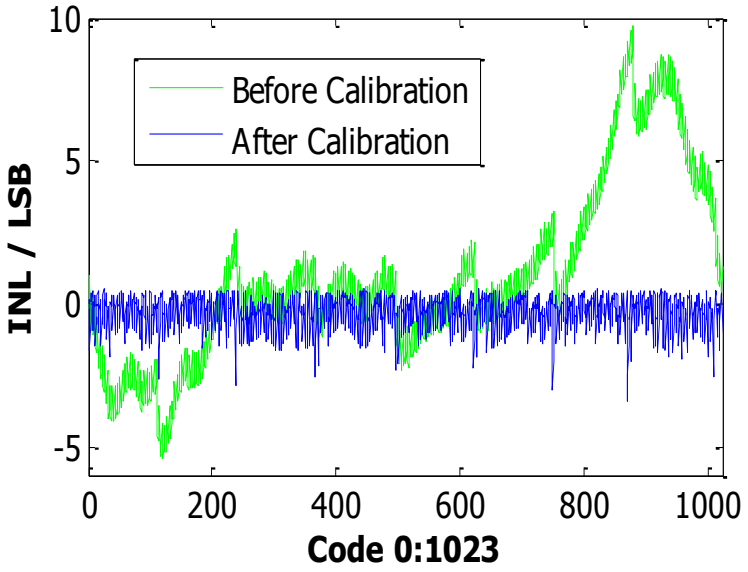


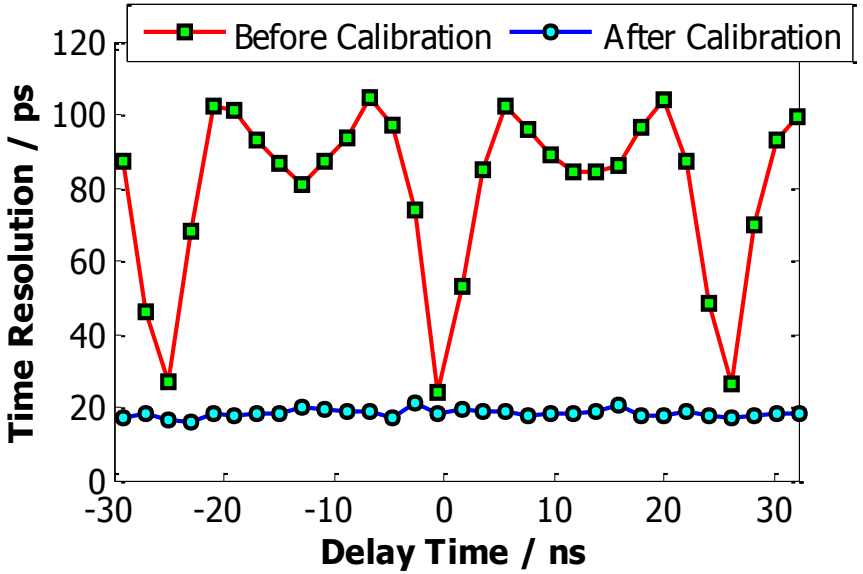
System test



Time and Charge Measurement Module

Time measurement:





Time and Charge Measurement Module

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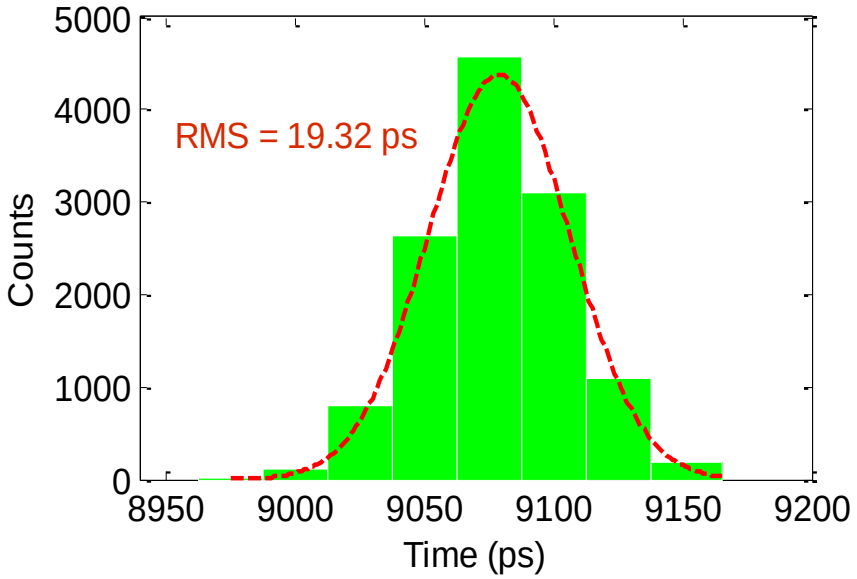
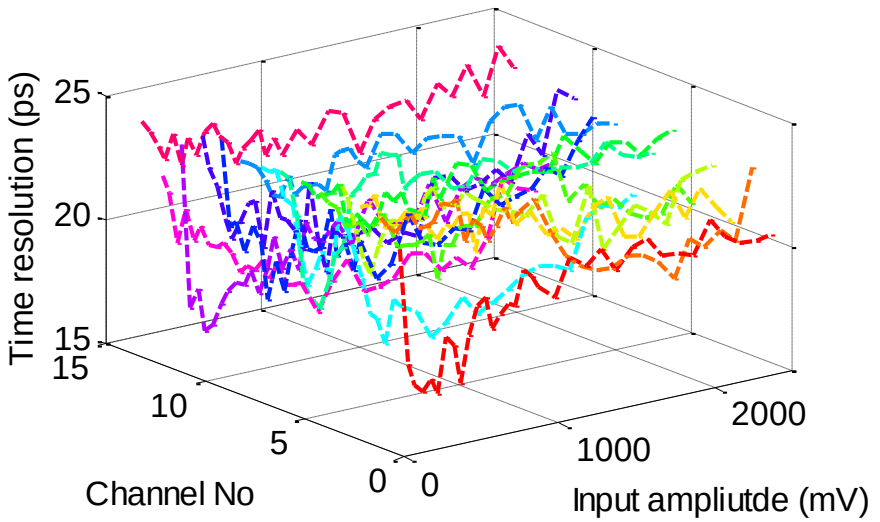
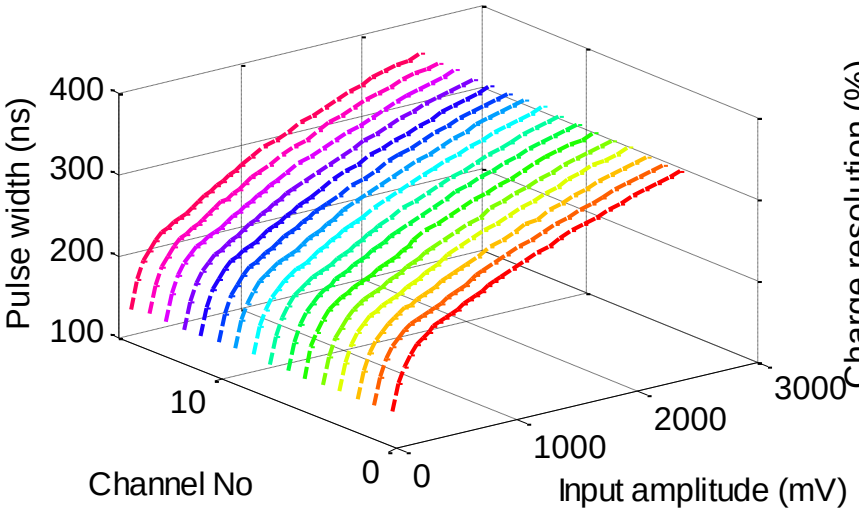
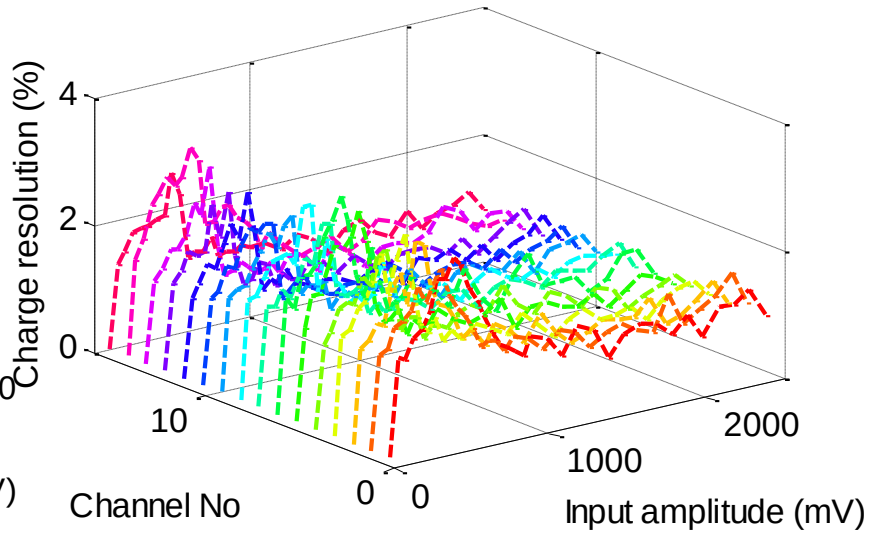




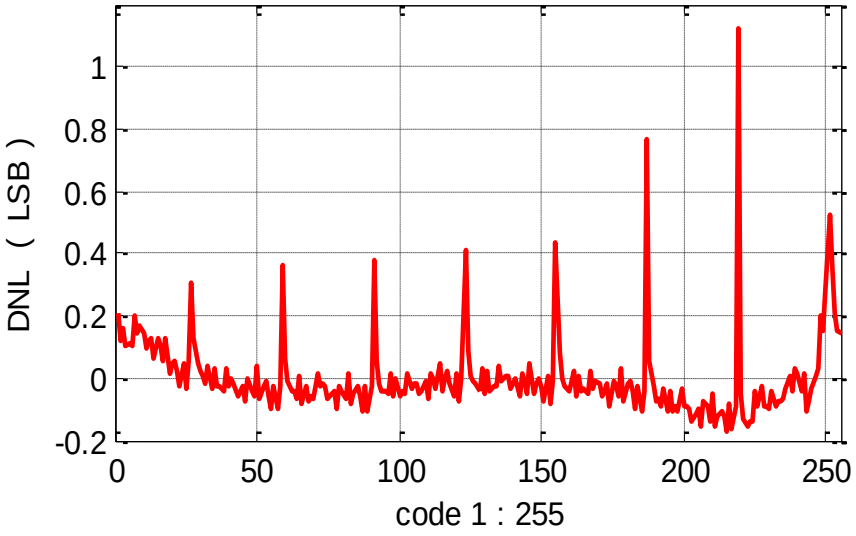
Time and Charge Measurement Module

Charge measurement:

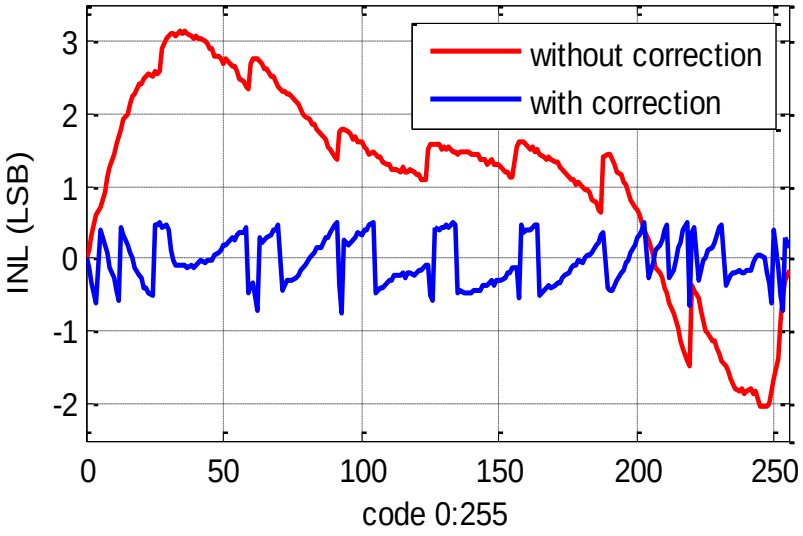




High Density Time Measurement Module

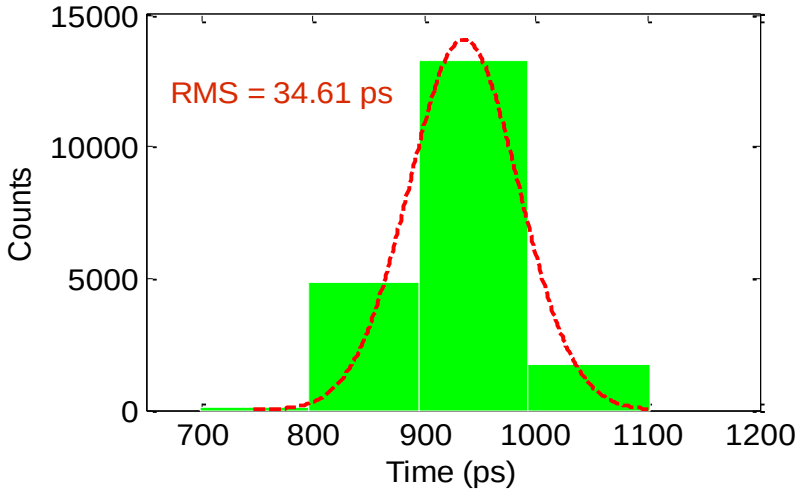


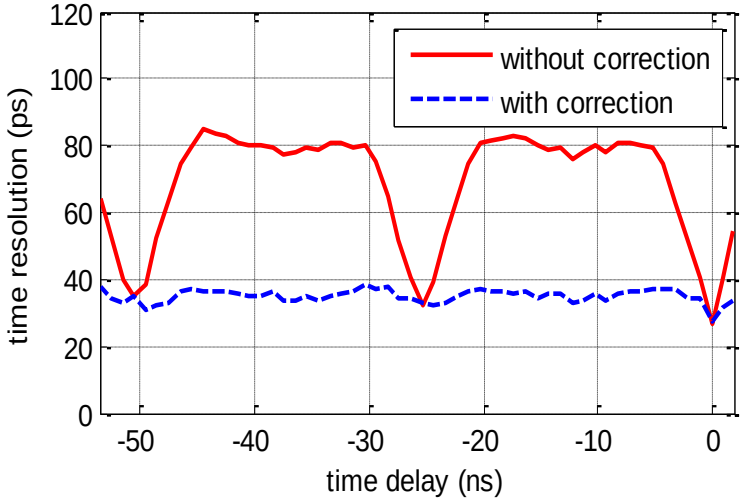
DNL

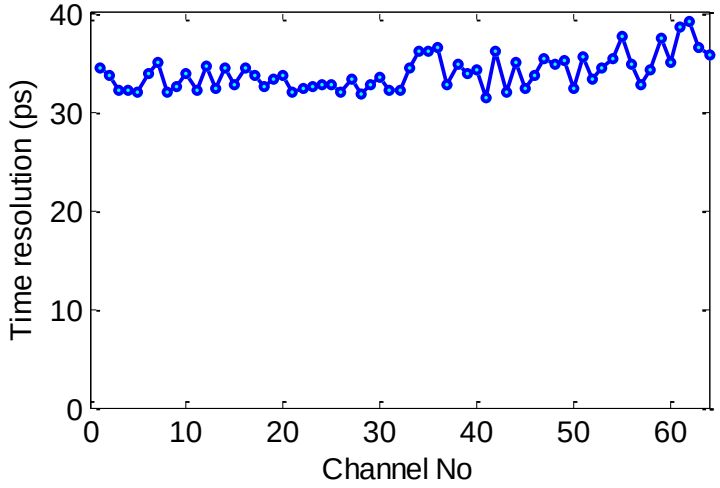


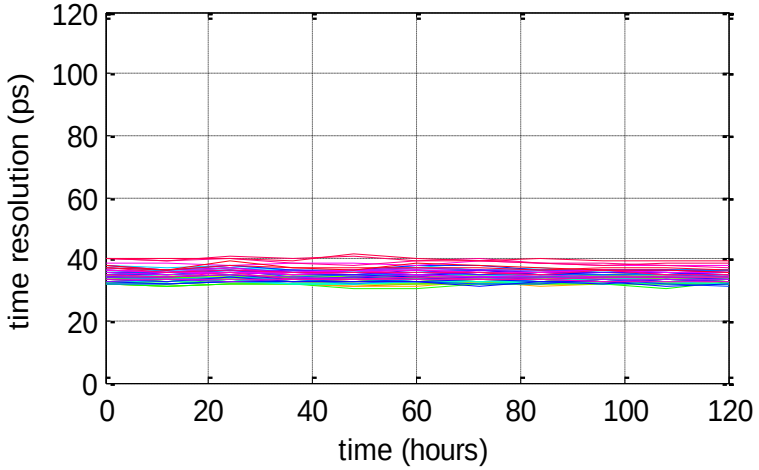
INL

High Density Time Measurement Module









Content

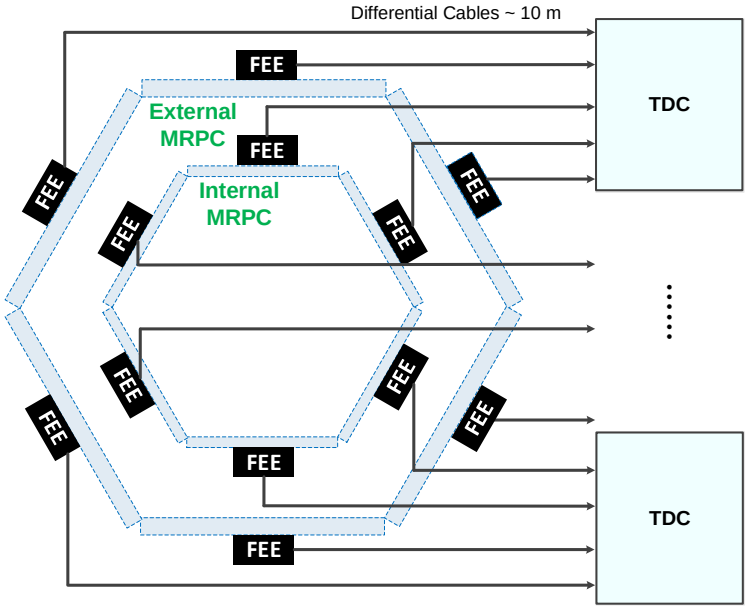
- Upgrade of BESIII Endcap TOF
- High precision time measurement design based on HPTDC
- **Readout electronics for T0 detector of CSR in HIRFL**

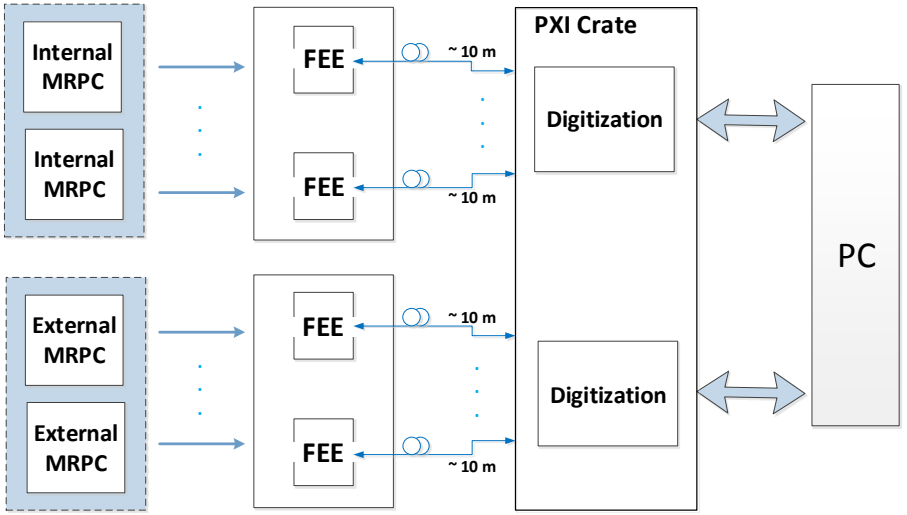
Readout Electronics for T0 Detector

- Readout of MRPC
- Channel Number：
  - Phase I：
    - Internal x 2 = 16 x 2 =32 chl
    - External x 2 = 24 x 2 =48 chl
    - total: 80 chl
  - Phase II：
    - Internal x 6 = 16 x 4 =64 chl
    - External x 6 = 24 x 4 =96 chl
    - total: 160 chl
  - Phase …

- Achieve time and charge measurement simultaneously
- Time resolution：~ 25 ps
- TDC design based on FPGA
- Based on PXI 6U standard

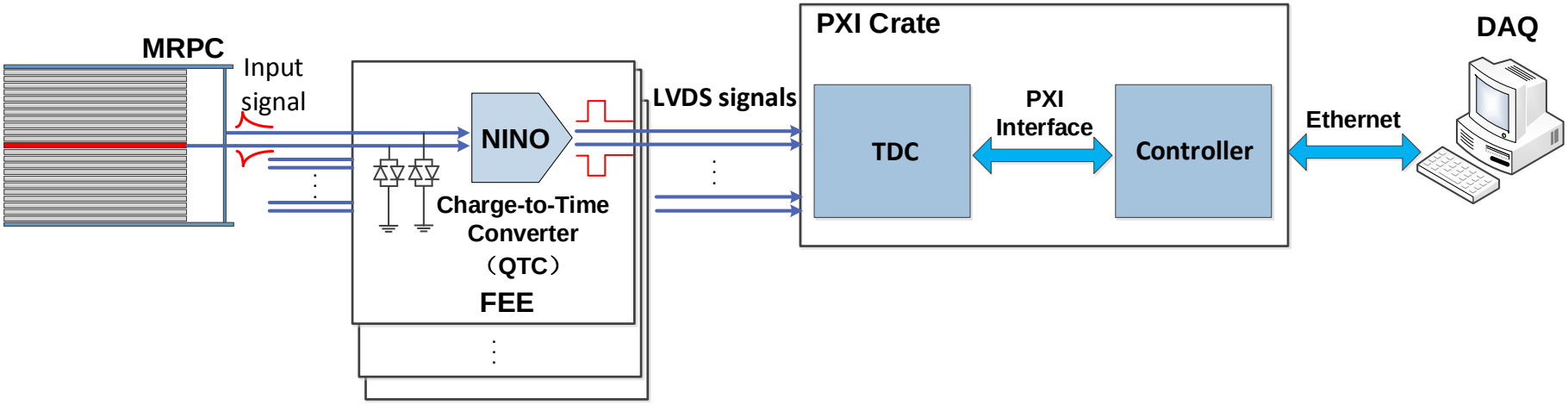
Readout Electronics for T0 Detector





- Time measurement: Leading edge discriminator + TDC (Time-to-Digital Converter)
- Charge measurement: Time-Over-Threshold (TOT) +TDC
- All integrated in PXI crates flexible for system extension

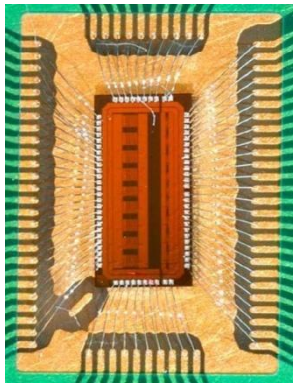
Readout Electronics for T0 Detector



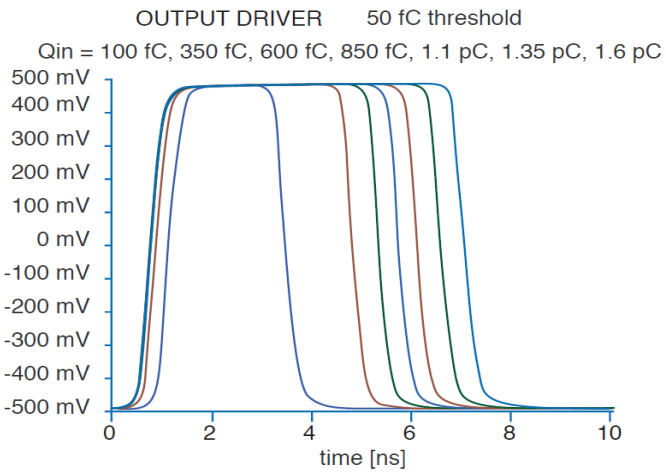
- Full differential signal transmission from MPRC to FEE to time digitization modules
- Using FPGA based TDC for high precision time measurement
- Trigger match and data interface are also integrated in the FPGA device (Xilinx Artix 7 Series)

Front end ASIC：NINO

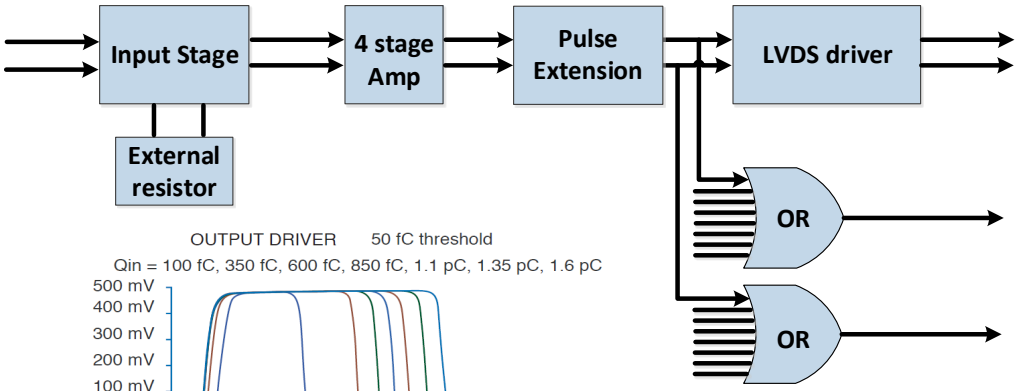
- Implemented in a 0.25 μm CMOS technology
- Integrated Circuit is 2 × 4 mm^2
- 8 channels
  - Differential Inputs (can be operated in single-ended mode)
  - Differential design throughout the channel: differential outputs
- Fast low-power amplifier-discriminator

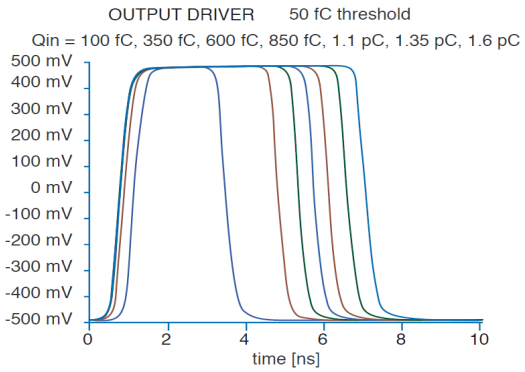


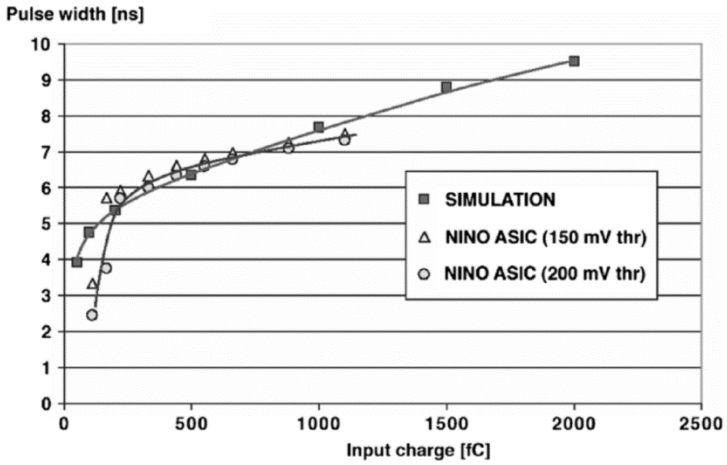
Parameter	Value
Peaking time	1ns
Signal range	100fC-2pC
Noise (with detector)	< 5000 e- rms
Front edge time jitter	< 25ps rms
Power consumption	30 mW/ch
Discriminator threshold	10fC to 100fC
Differential Input impedance	40Ω< Zin < 75Ω
Output interface	LVDS

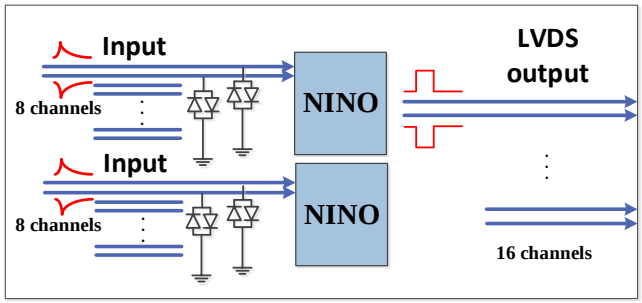


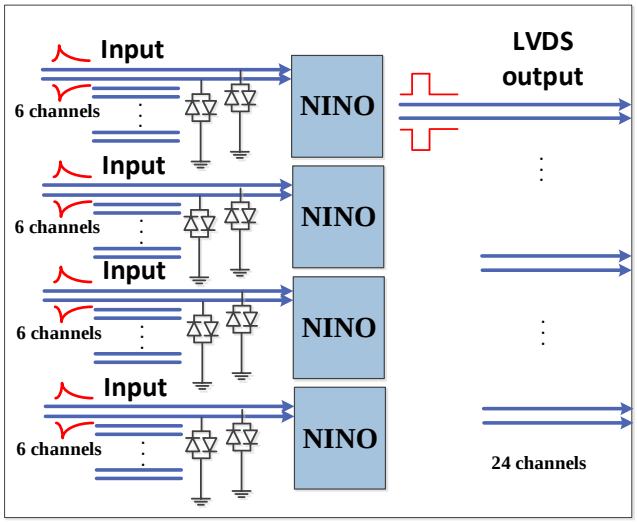
Front End Electronics (FEE)







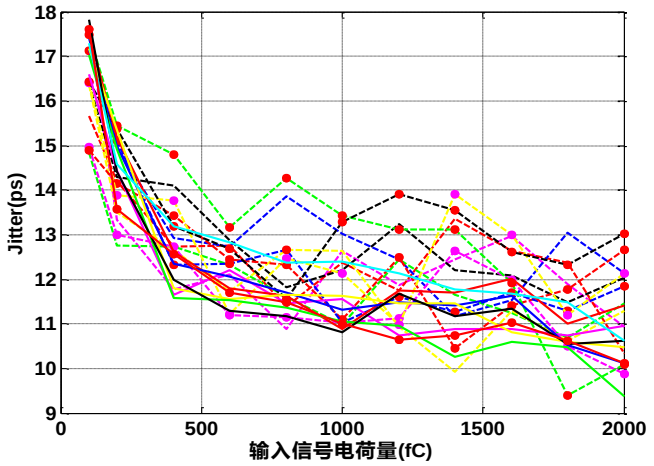




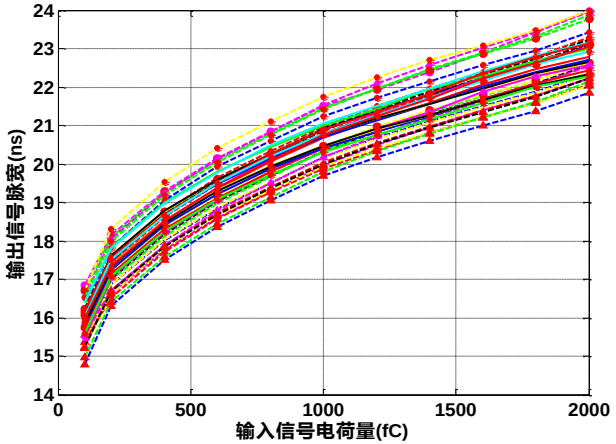
FEE Performance

Internal FEE

External FEE

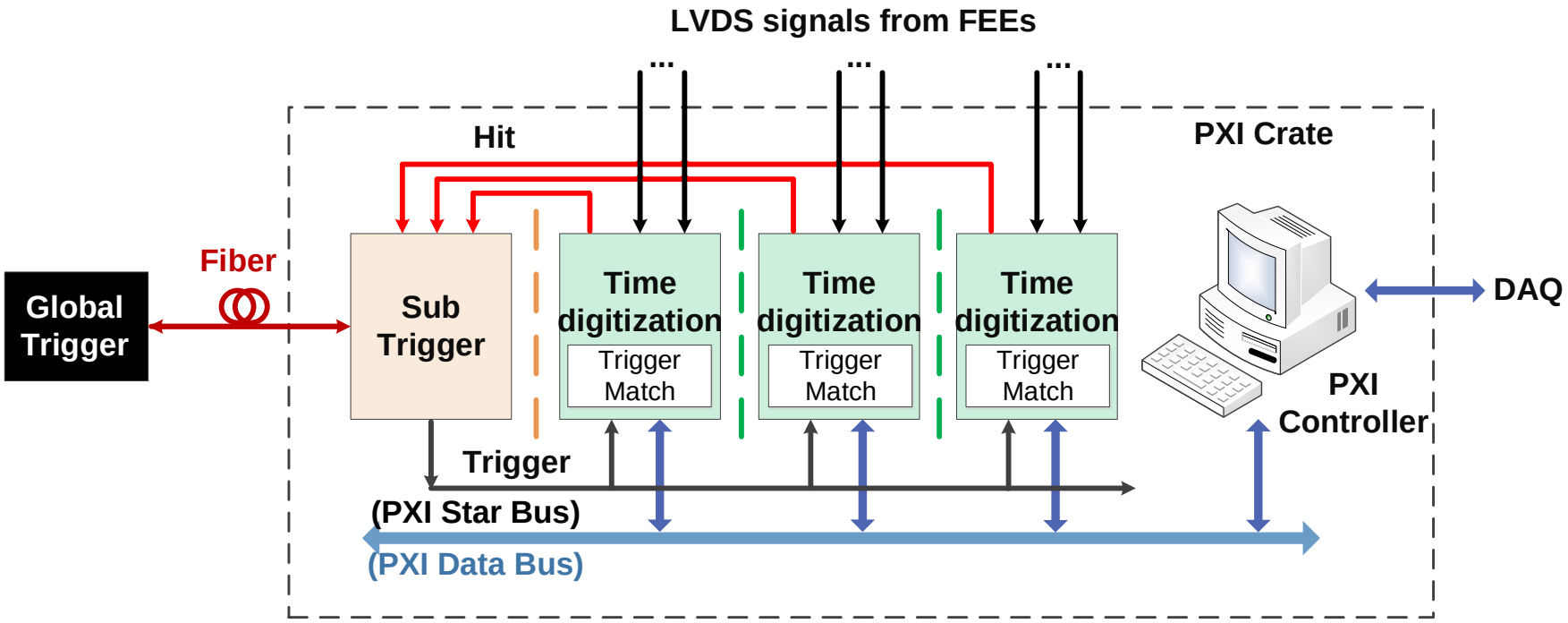


- Time resolution for all FEEs is better than 20 ps RMS
- The output pulse width vs input charge concord with the expected.



Time digitization and data readout

- System structure

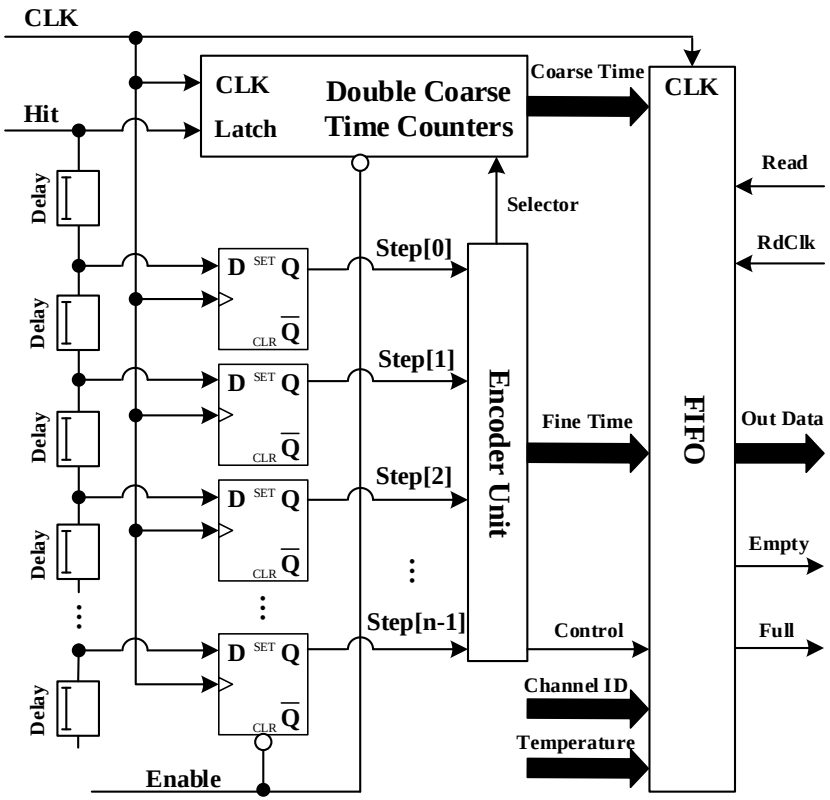


- Using star bus in PXI crates to fan out trigger signals.
- Trigger match function is integrated in FPGA-based TDCs.

FPGA based TDC design

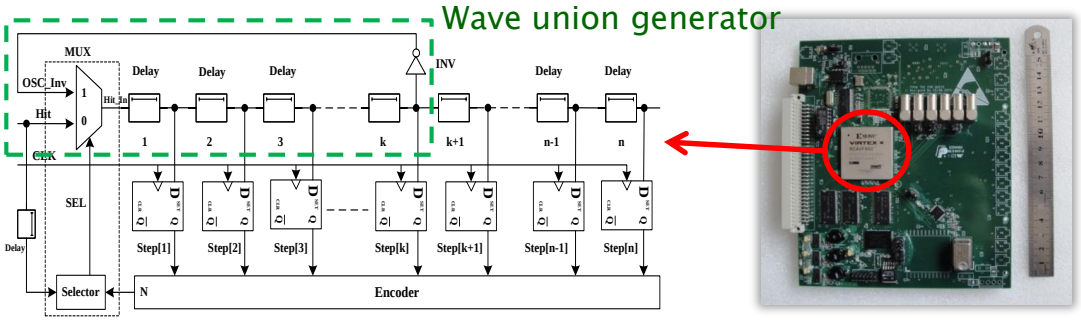
- Propose to design high precision TDC using carry chain in FPGA for first time.

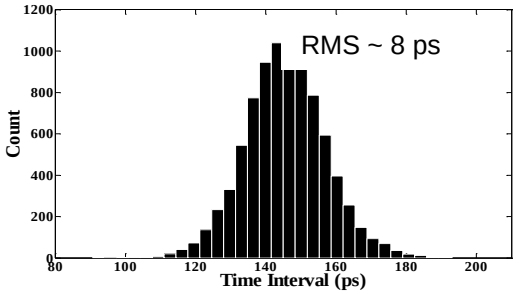
IEEE Transactions on Nuclear Science, vol. 53, no. 1, Feb. 2006, pp. 236-241.

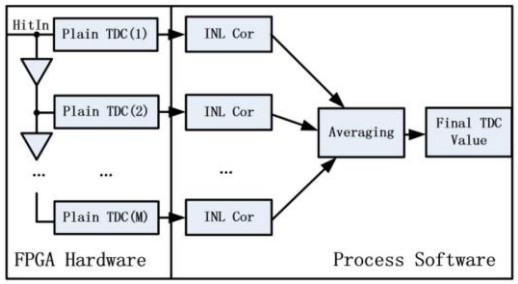


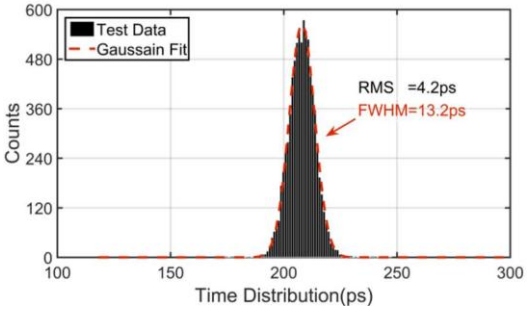
FPGA based TDC design

- In Year 2006，propose to use carry chain for time interpolation, precision ~ 100 ps
- In Year 2009，through calibration and INL correction, precision is enhanced to <25 ps
- In Year 2011，based on combination of wave union method and real-time correction, precision is enhanced to 8 ps, without modification of hardware
- In Year 2015，based on parallel measurement and averaging method, precession is further enhanced to .2 ps (bin size~1.7 ps)



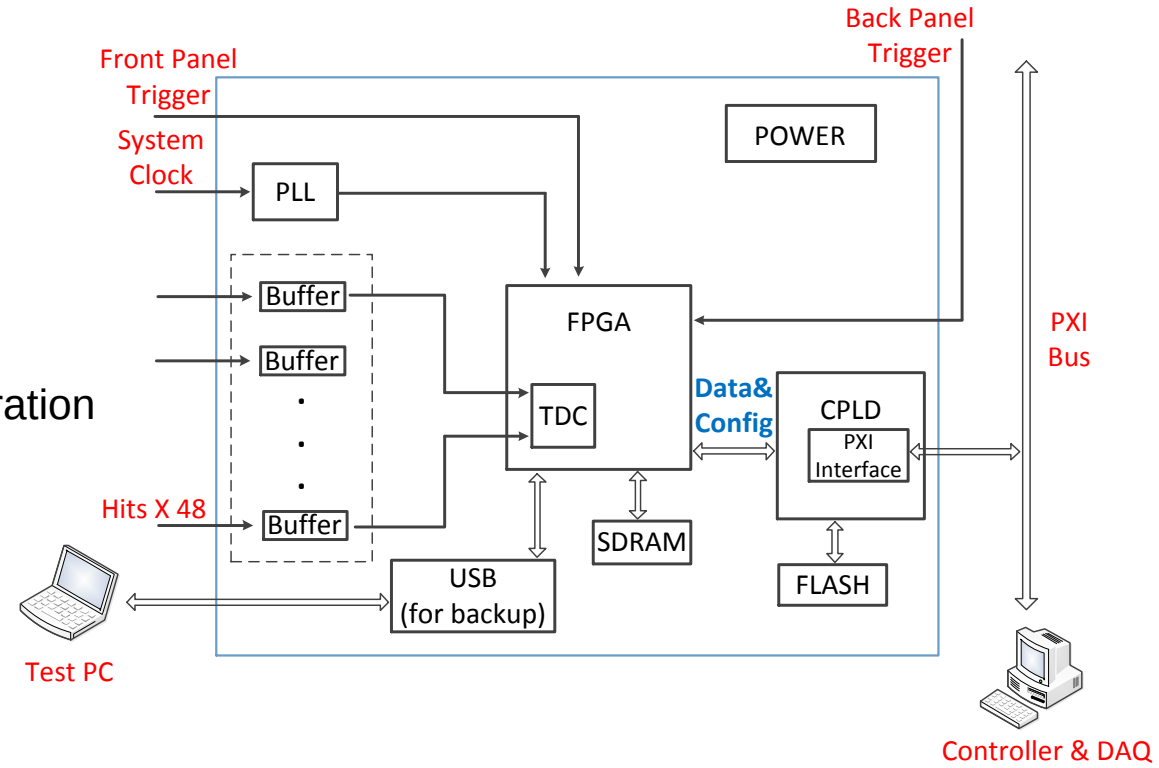






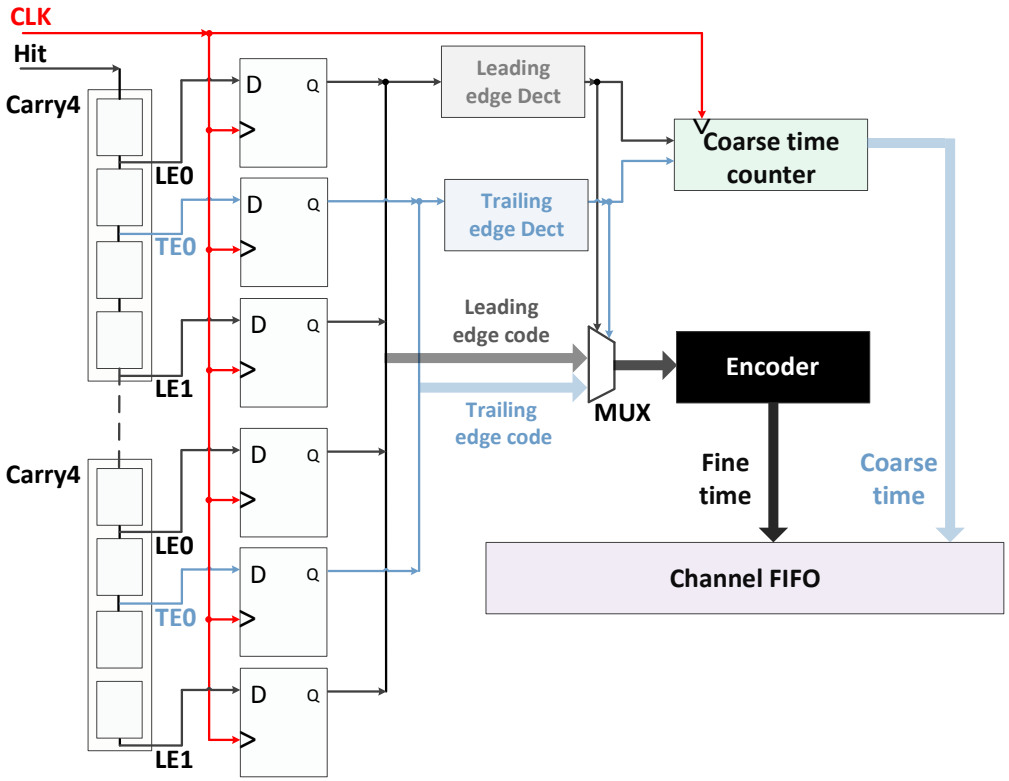
Time digitization module

- Structure:
  - Clock circuits
  - FPGA
    - Time digitization
    - Trigger match
  - CPLD
    - PXI interface
    - FPGA on-line configuration
  - USB Interface

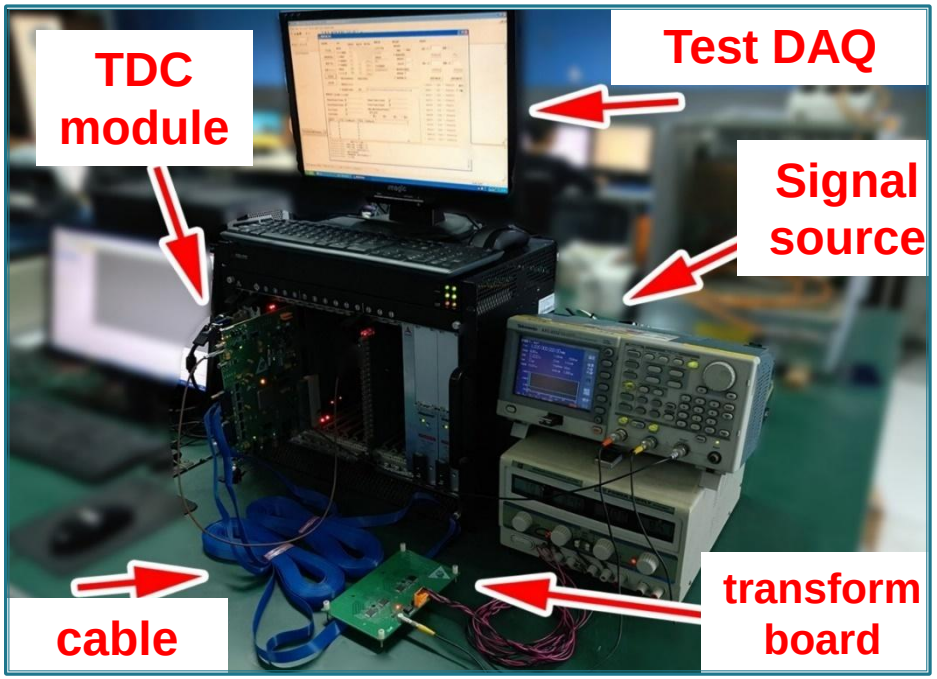


TDC (Time-to-Digital Converter)

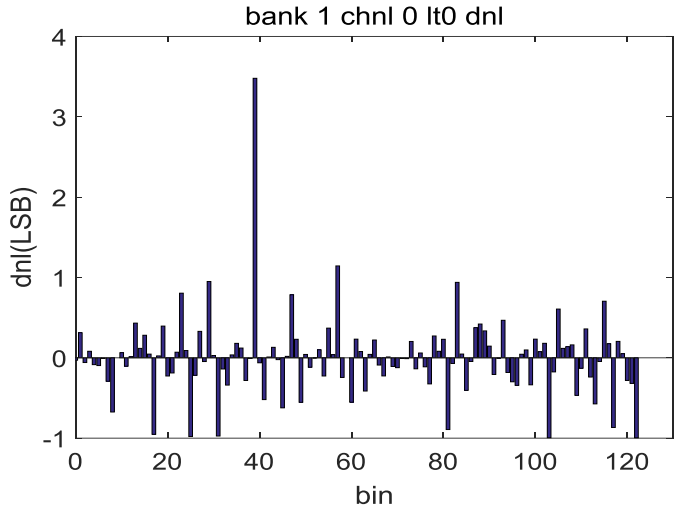
- Based on combination of Coarse time and fine time measurement
  - Coarse time: counter
  - Fine time: time interpolation using carry lines inside FPGA devices

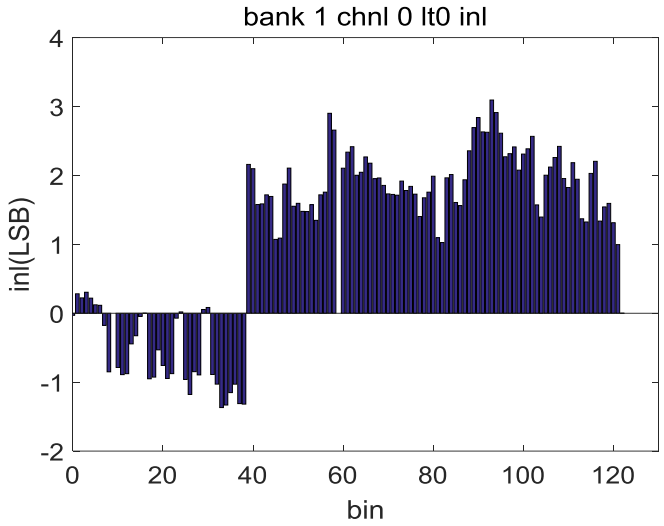


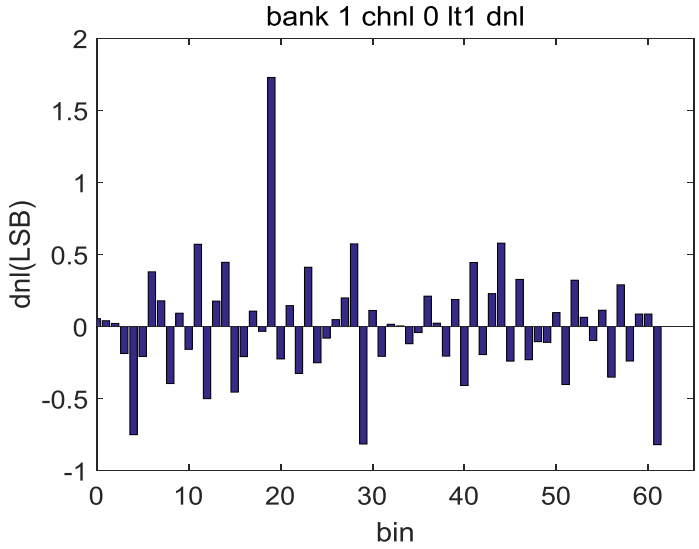
Implementation and test of FPGA TDC Module

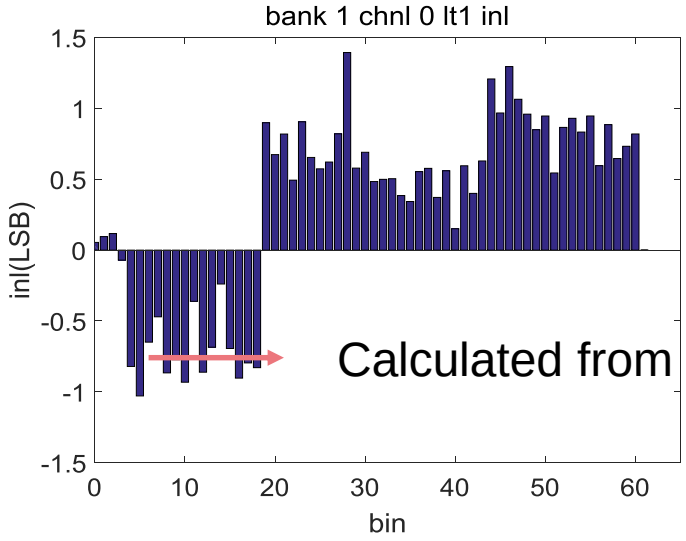


Non-linearity test



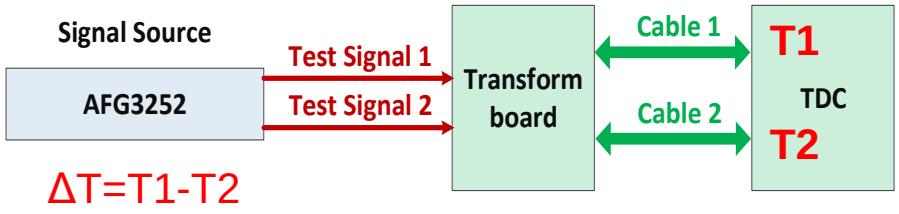


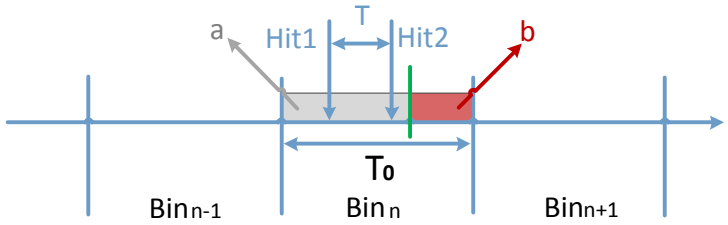




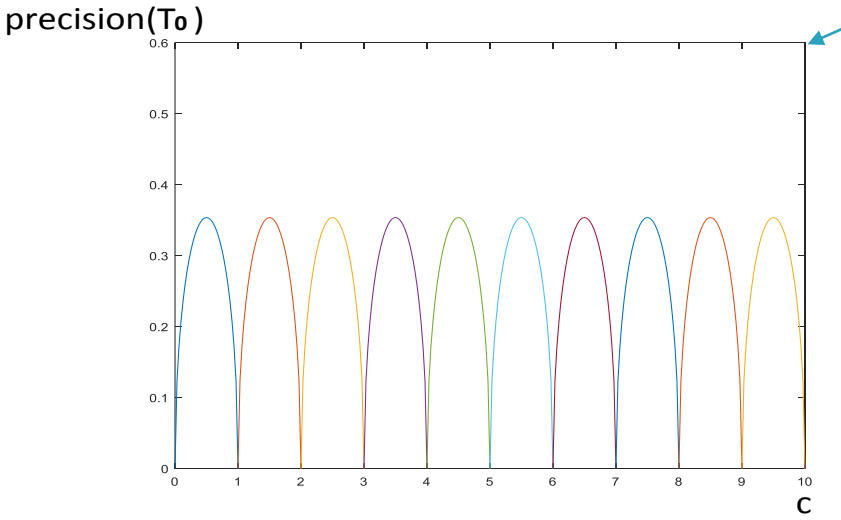
Time resolution test

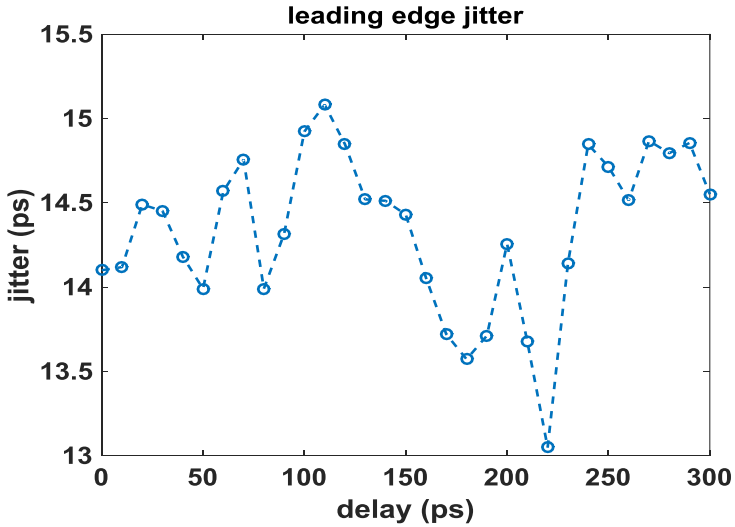
- Cable delay test method, to eliminate the influence of the signal source noise



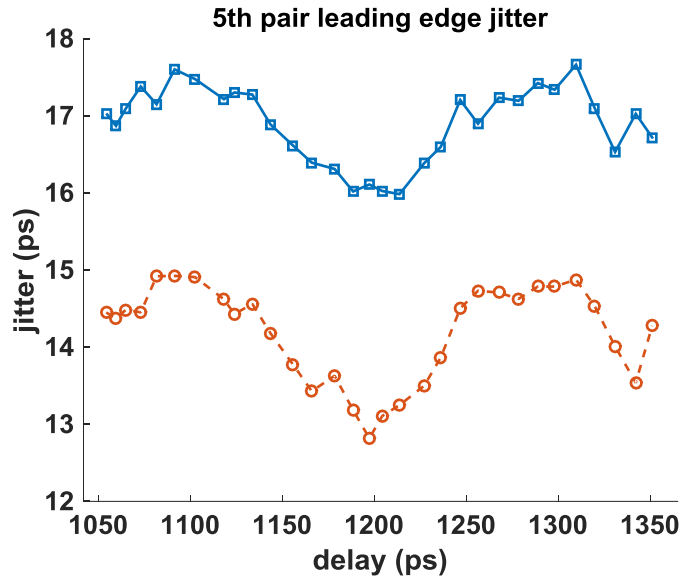


- Time resolution (RMS) varies when ΔT changes
- In ideal situation, the relationship can be well predicted





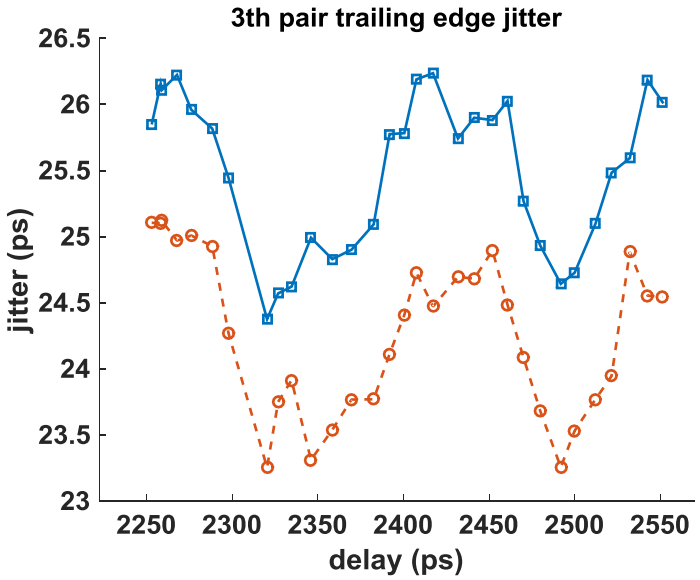
Time resolution test



Test results

Calculated from INL

- Time resolution for leading edge measurement is better than 20 ps

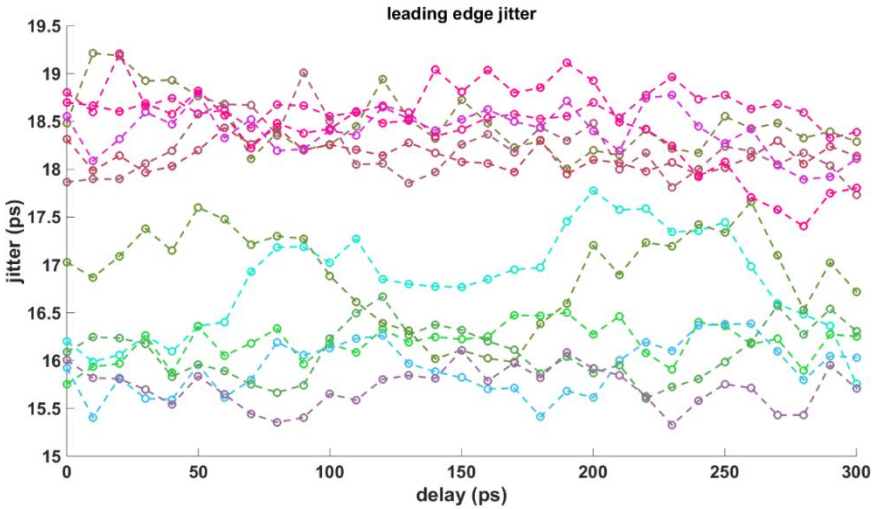


Test results

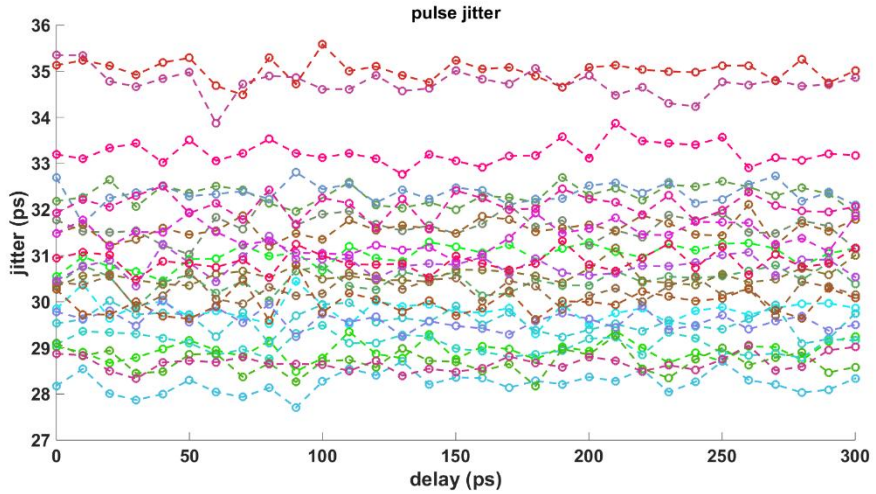
Calculated from INL

- Time resolution for trailing edge measurement is better than 20 ps

Time resolution test

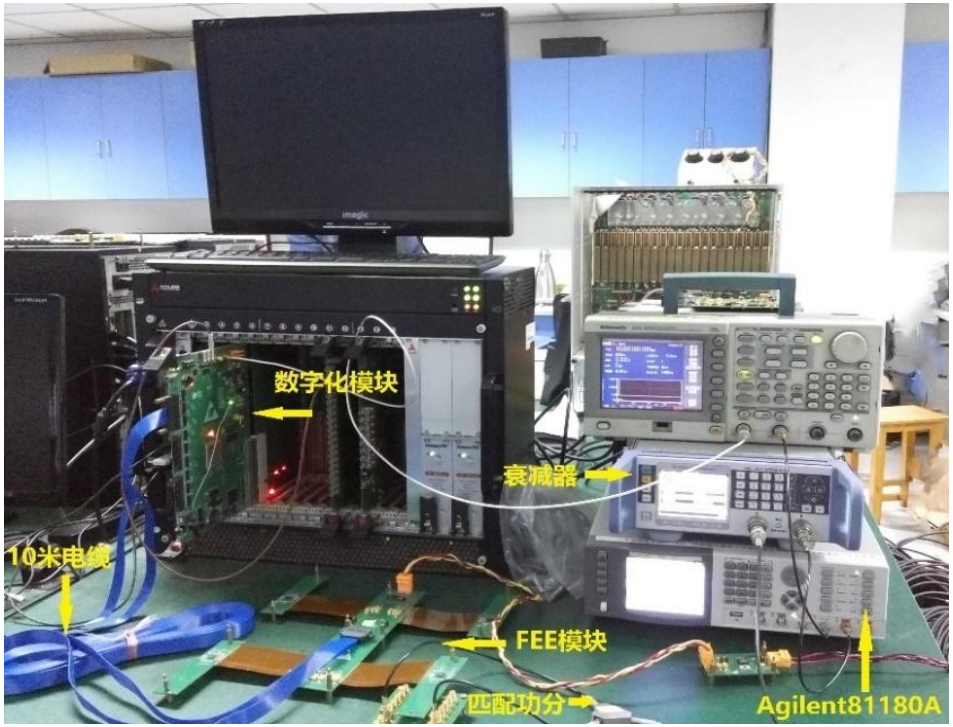


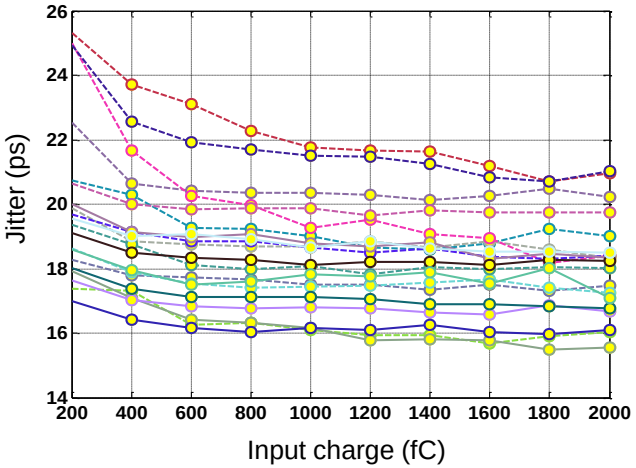
Leading edge time measurement resolution is better than 20 ps RMS for all 24 channels

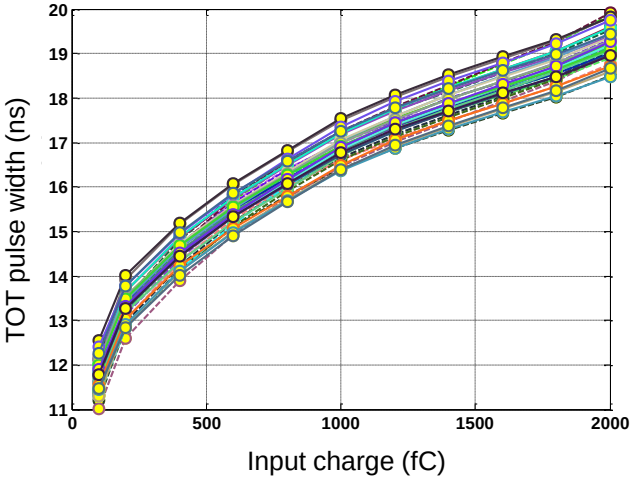


Trailing edge time measurement resolution is better than 36 ps RMS for all 24 channels

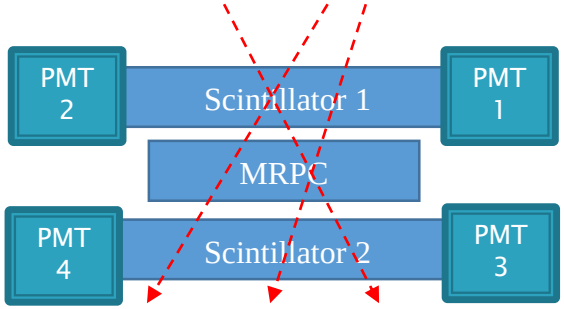
Test of the T0 readout electronics

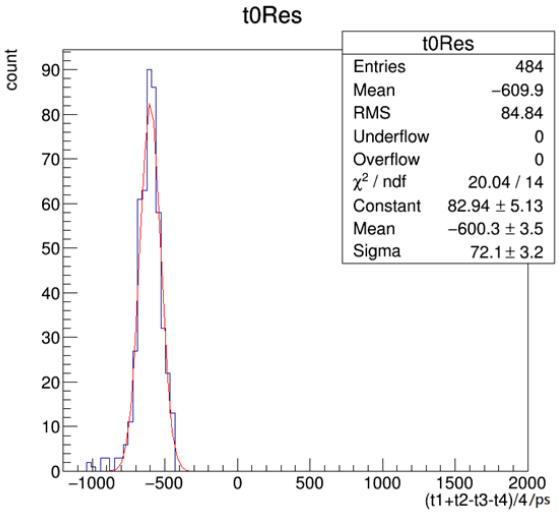


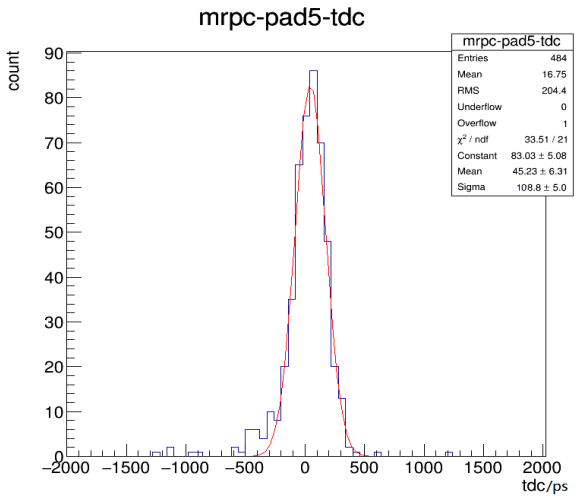




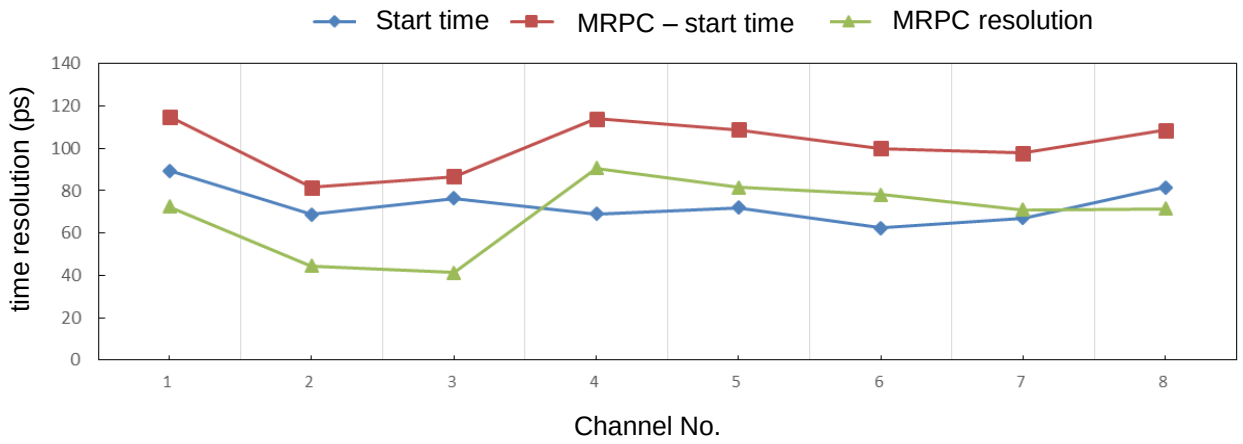
Test with MRPC detector







$$\sigma = \sqrt{{\sigma_t}^2 - {\sigma_{t_0}}^2} = \sqrt{108.8^2 - 72.1^2} = 81.48\text{ps}$$



Thanks