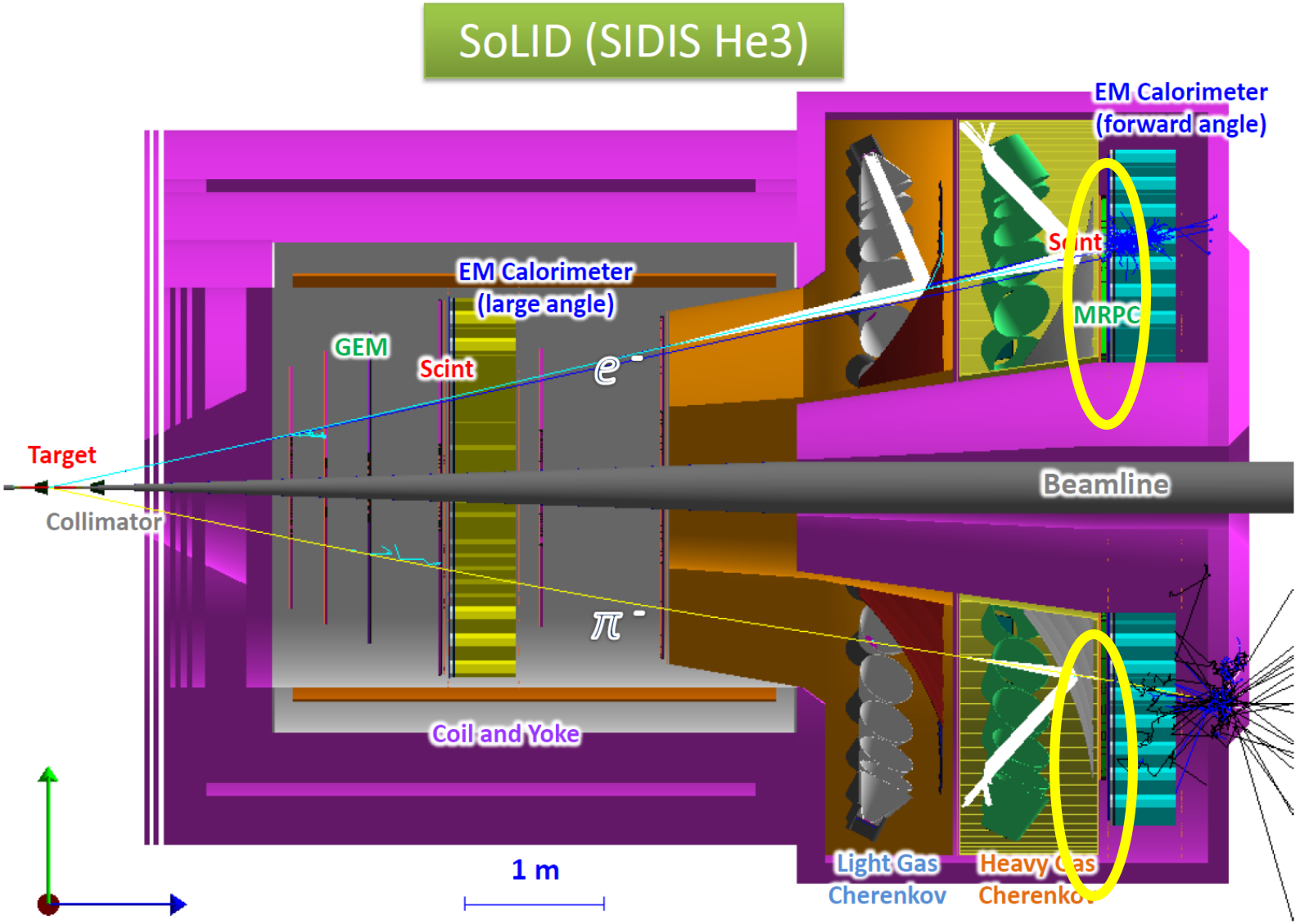
TOF readout for high resolution timing for SoLID

Alexandre Camsonne
Jefferson Laboratory
Hadron China 2017
TOF miniworkshop
July 28 2017

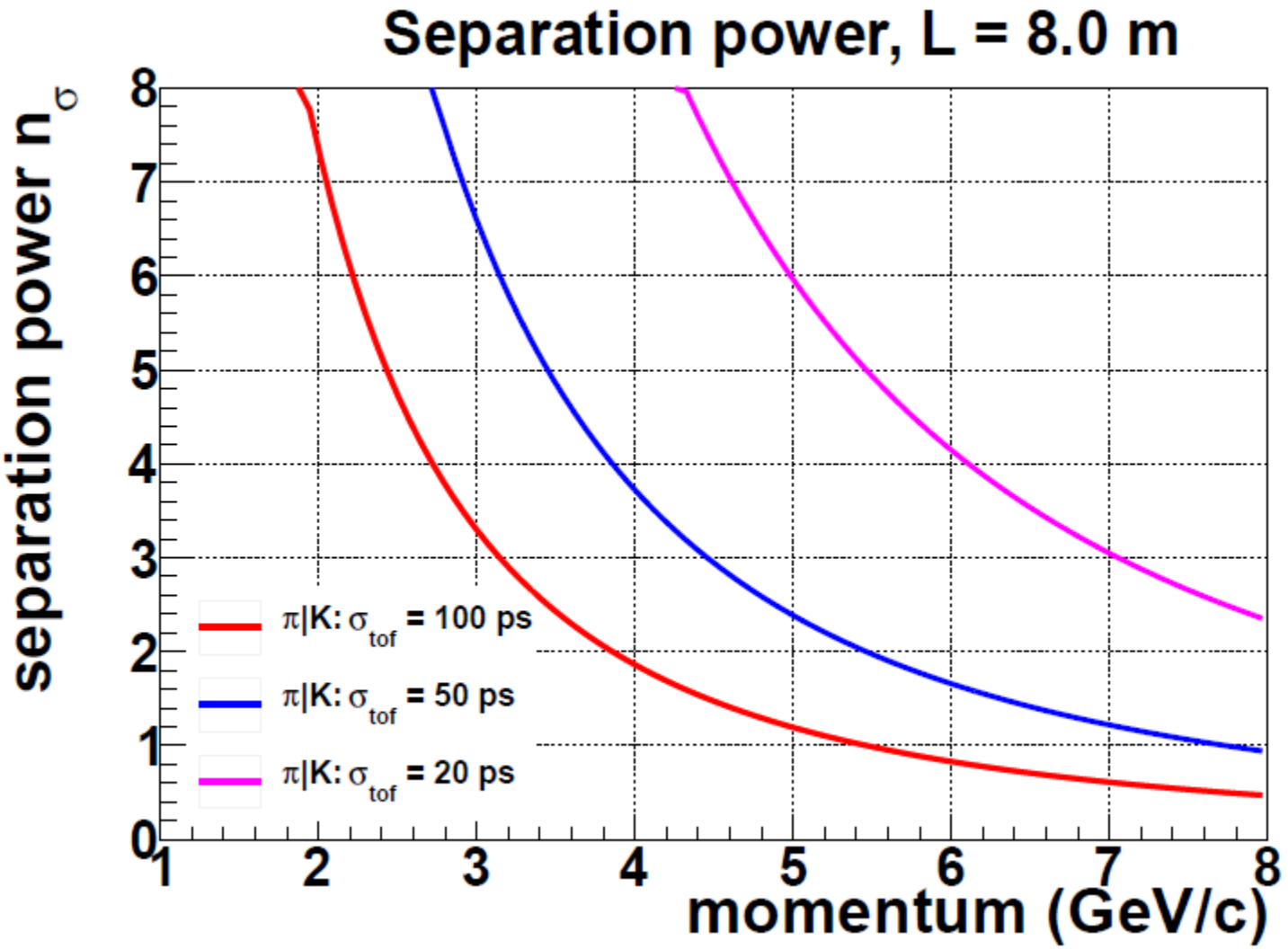
Outline

- SoLID SIDIS
- SoLID requirements for TOF
- Readout options : discriminator TDC vs sampling
- A/D chips
- TDC options
- Sampling chips
- DRS5 option from PSI
- Kansas University Amplifier
- SoLID SIDIS background studies
- SoLID TOF chip specs wish list
- Conclusion

SoLID SIDIS setup



Pion Kaon Separation by TOF



SoLID requirements

- TOF for SIDIS experiment for Kaon ID
- Baseline 80 ps , ideally 20 ps
- Trigger rate 100 KHz min, ideal 200 KHz
- FADC based trigger with up 8 us latency
- GEM readout 4 us latency
- Need 4 us latency for TOF ideally 8 us

Two options

- Depends on detector performance : Usual method : discriminator + TDC
  - Amplifier discriminator
  - TDC : ASIC or new FPGA technique
- Waveform sampling
  - No discriminator
  - Full bandwidth
  - Better timing resolution up to 1 ps
  - Need algorithm to extract time on board
  - Or readout full waveform (very large amount of data)

Readout options

- Amplifier Discriminators front end
  - NINO (CERN) (8 channels – 32 channels version)
  - GSI Padiwa (16 channels) 150 $ for 16 channels
  - MAROC (Omega IN2P3)
  - VMM3 (BNL)

  Need to check timing performance of discrimination and amplification, bandwidth, timewalk corrections

TDCs

- HPTDC 25 ps
  - V1290 (32 channels about 10 K$)
  - CAEN planning to develop better TDC
- FPGA TDCs
  - TRB3 11 ps (192 channels / 2300 euros)
  - VETROC JLAB 20 ps (need development) 128 channels about 6 K$ (5 board ordered for Compton, can test TDC)

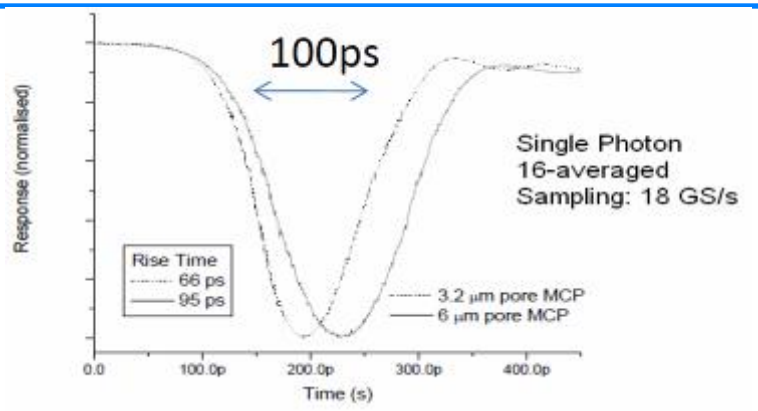
Sampling chip

Chip	Sampling Frequency (GHz)	Bandwidth GHz	Number of samples	Number of channels	Readout frequency (MHz)	Resolution (ps)
PSEC4	4 to 15	1.5	256	6	40 to 60	9
SAMPIC	3 to 8.2	1.6	64	16 – 8 (at 10 GHz)	80	5
DRS4	0.7 to 5 GHZ	0.950	1024	9	33	1
DRS5	10	3	4096	32	300?	5?
PSEC5	5 to 15	1.5 to 2	32768	4	500	5?

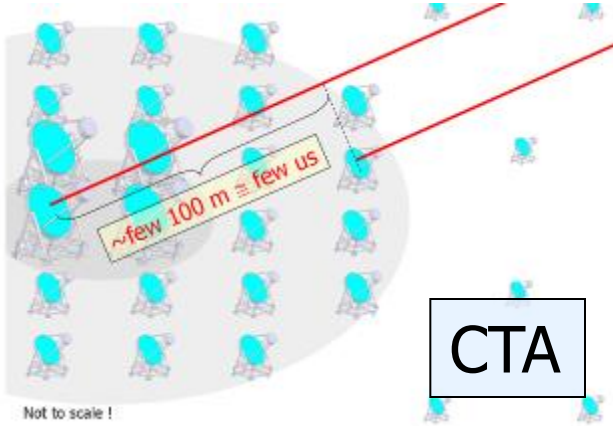
Latest generation with multilevel analog buffer : dead time less up to a few MHz and allow for L2 (DRS5)

Plans for DRS5

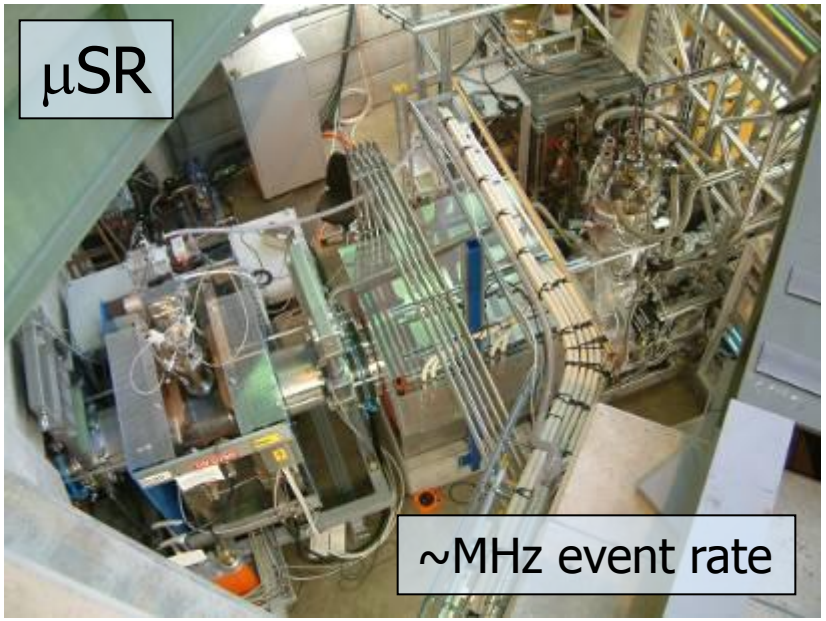
- Increase analog bandwidth ~5 GHz
  - Smaller input capacitance
- Increase sampling speed ~10 GS/s
  - Switch to 110 nm technology
- Deeper sampling depth
  - 8 x 4096 / chip
- Minimize readout time ("dead time free") for muSR & ToF-PET
  - (minor) reduction in analog → 20 ns)
  - ology



J. Milnes, J. Howoth, Photek



CTA



Next Generation SCA

Short sampling depth ⟷ Deep sampling depth

- Low parasitic inp… capacitance
  → High bandwid…
- Large area
  → low resistance bus, low resistance analog switches
  → high bandwidth

How to combine best of both worlds?

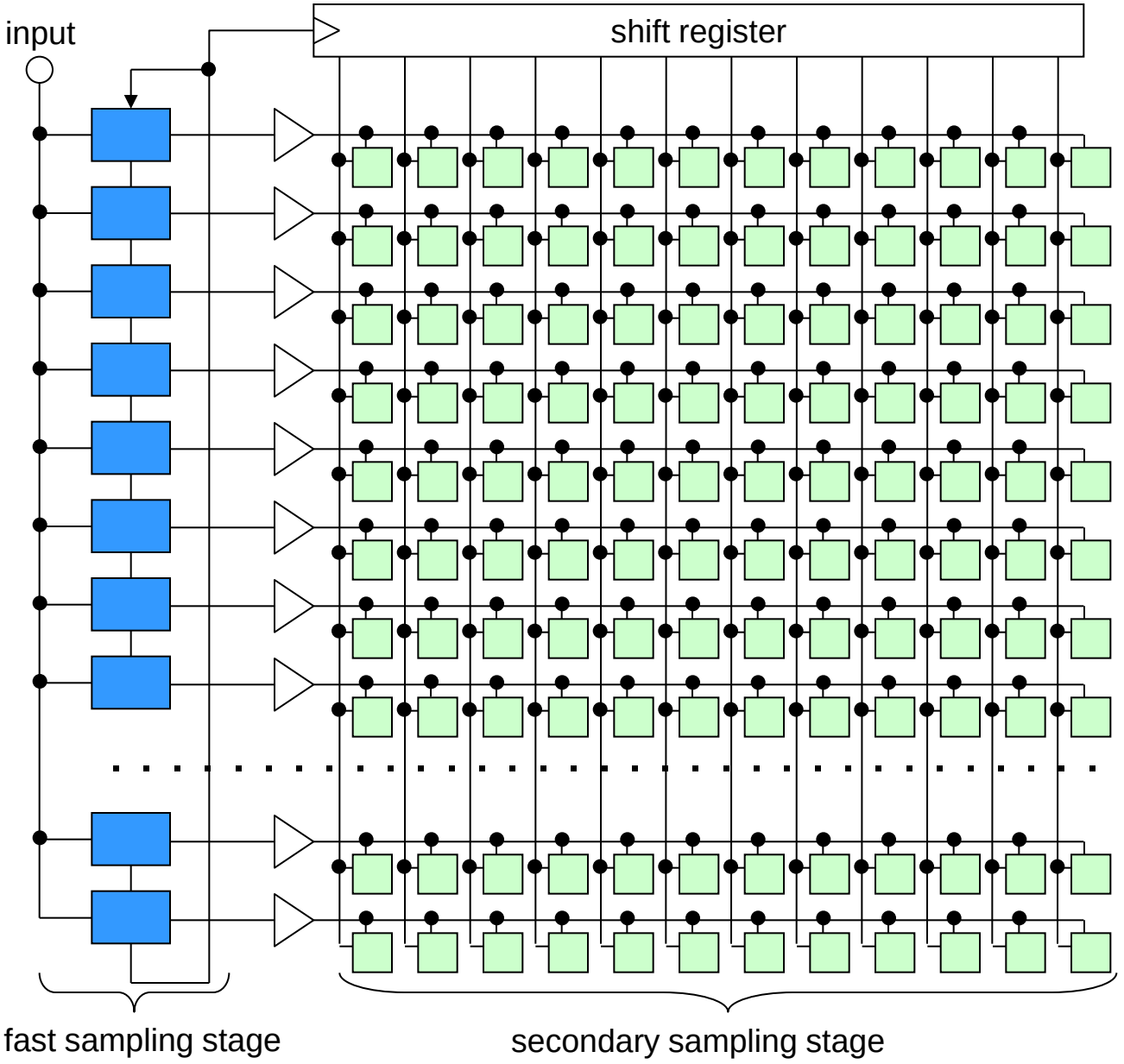
…long waveforms

…nodate long trigger delay

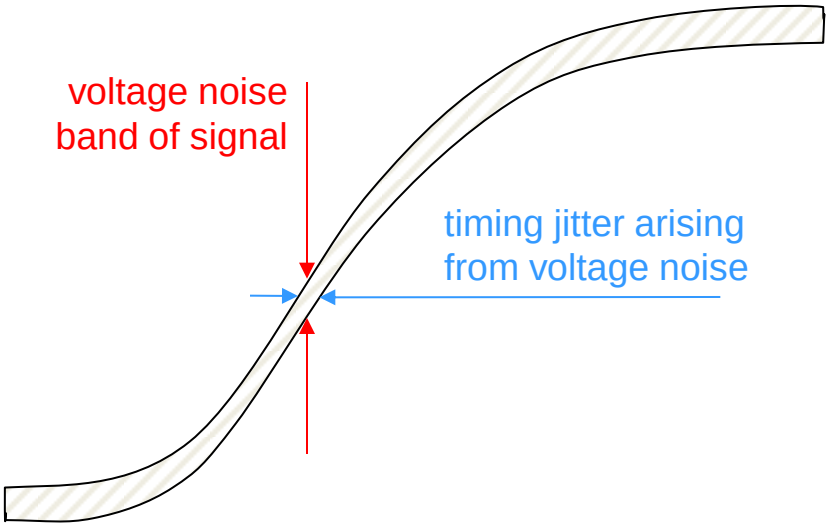
- Faster sampling speed for a given trigger latency

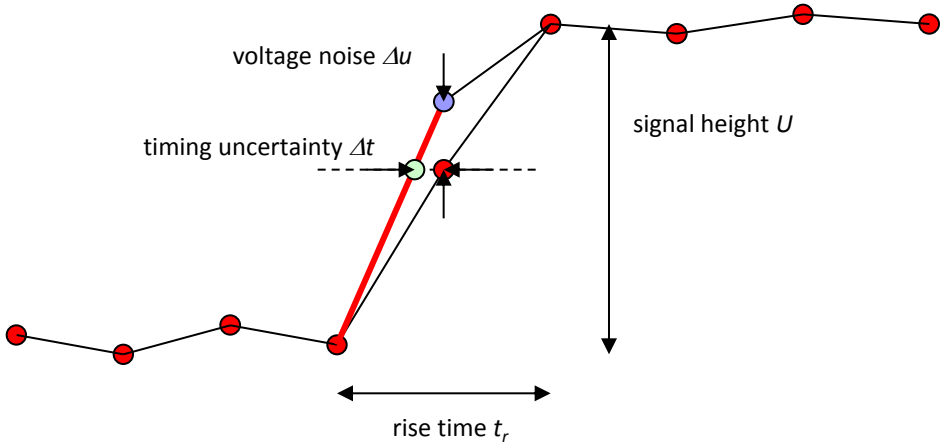
Cascaded Switched Capacitor Arrays

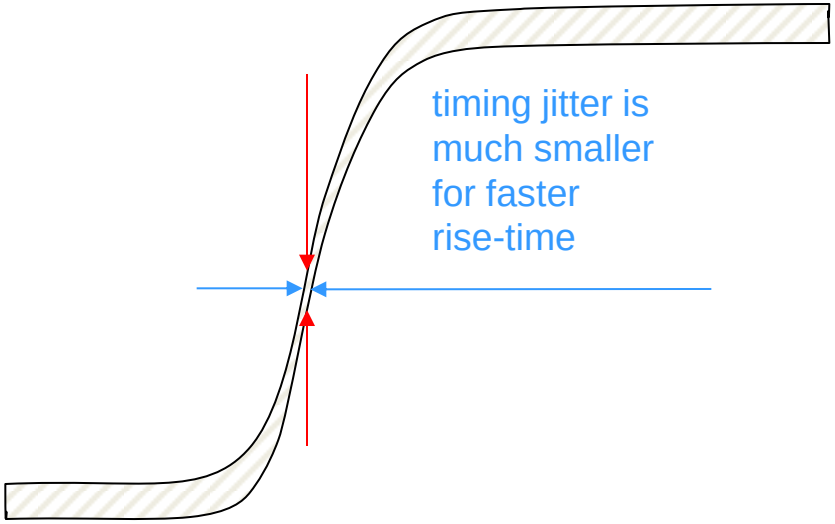
- 32 fast sampling cells (10 GSPS/110nm CMOS)
- 100 ps sample time, 3.1 ns hold time
- Hold time long enough to transfer voltage to secondary sampling stage with moderately fast buffer (300 MHz)
- Shift register gets clocked by inverter chain from fast sampling stage



How noise affects timing





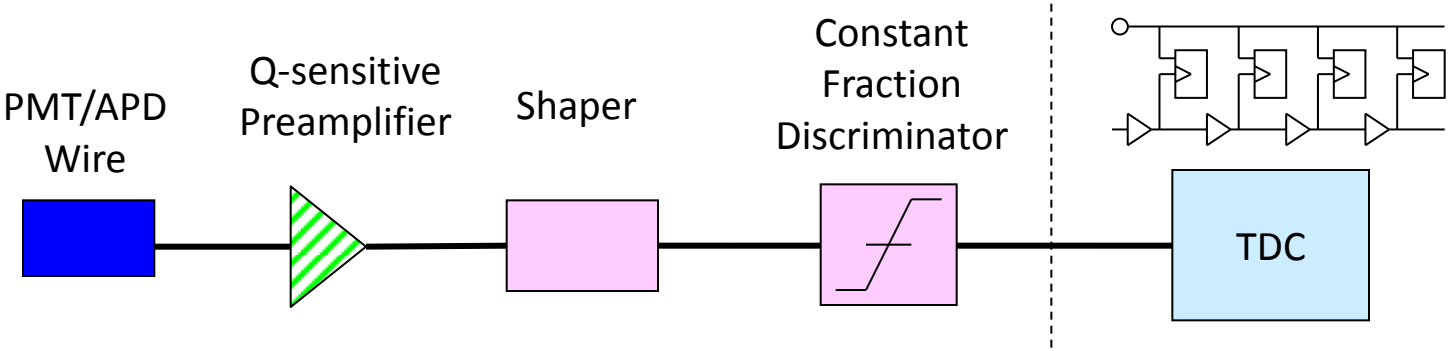


$$\Delta t = \frac{\Delta u}{U}\cdot t_r = \frac{\Delta u}{U\sqrt{n}}\cdot t_r = \frac{\Delta u}{U}\cdot\frac{t_r}{\sqrt{t_r\cdot f_s}} = \frac{\Delta u}{U}\cdot\frac{\sqrt{t_r}}{\sqrt{f_s}}$$

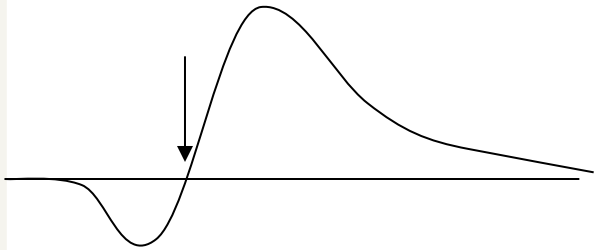
$\frac{1}{SNR}$

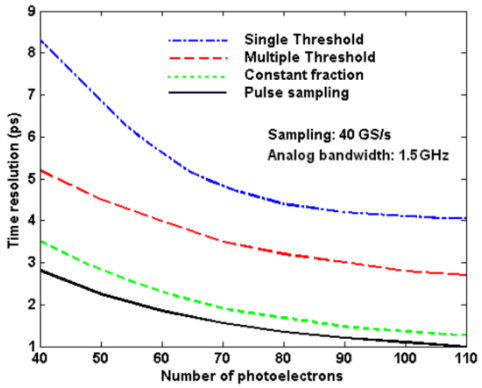
number of samples on slope

TDC vs. Waveform Digitizing

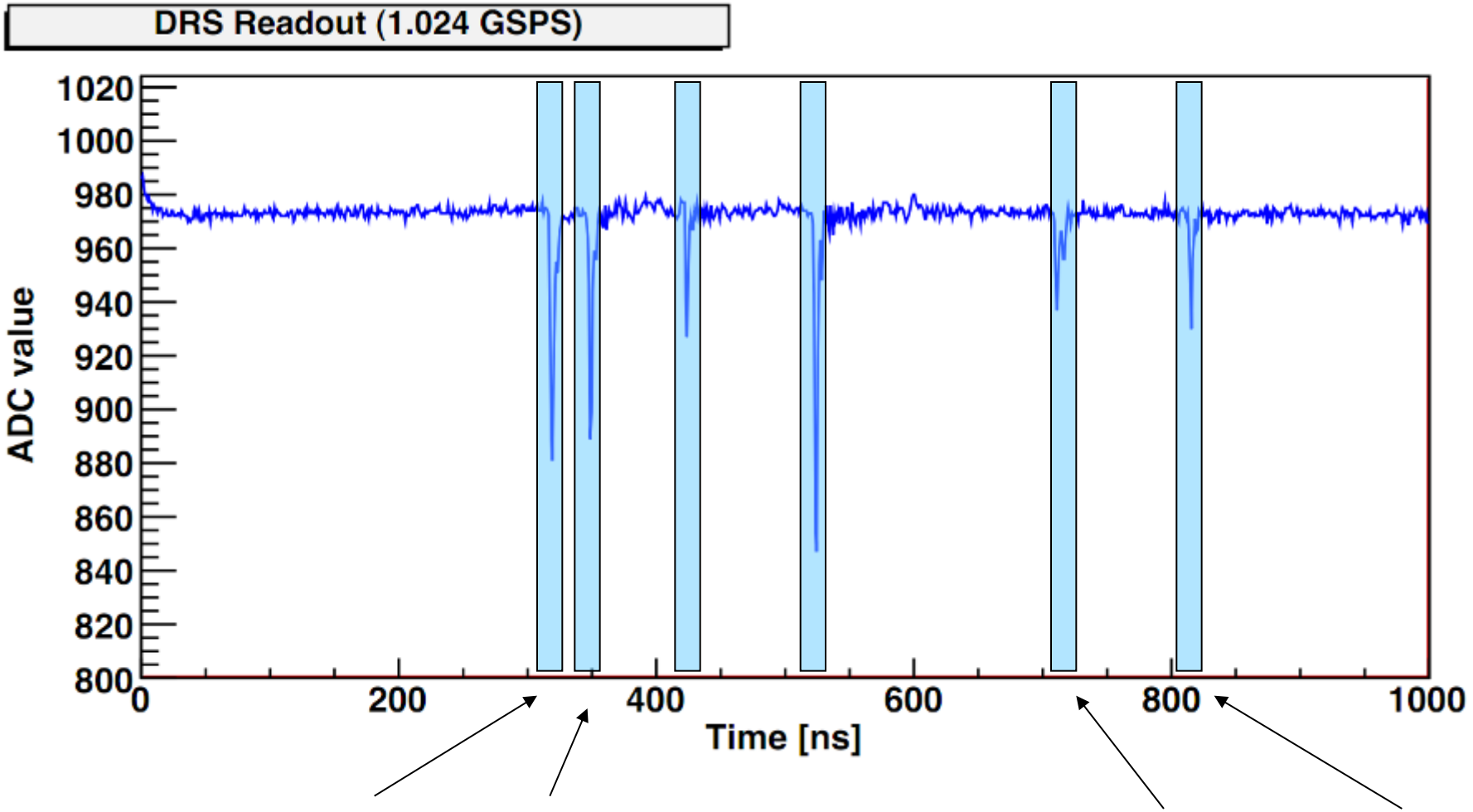


- CFD and TDC on same board → crosstalk
- CFD depends on noise on single point, while waveform digitizing can average over several points
- Inverter chain is same both in TDCs and SCAs
- Can we replace TDCs by SCAs?
  → yes if the readout rate is sufficient





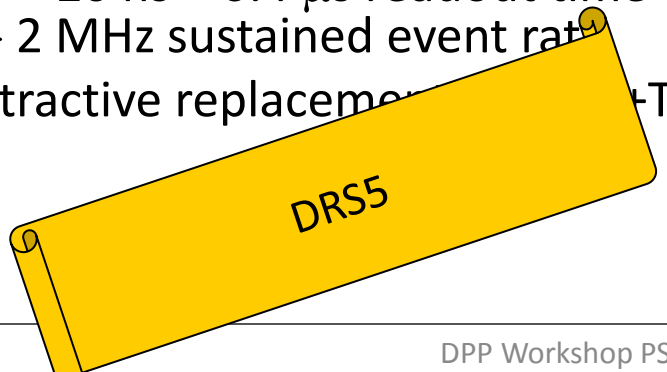
Typical Waveform

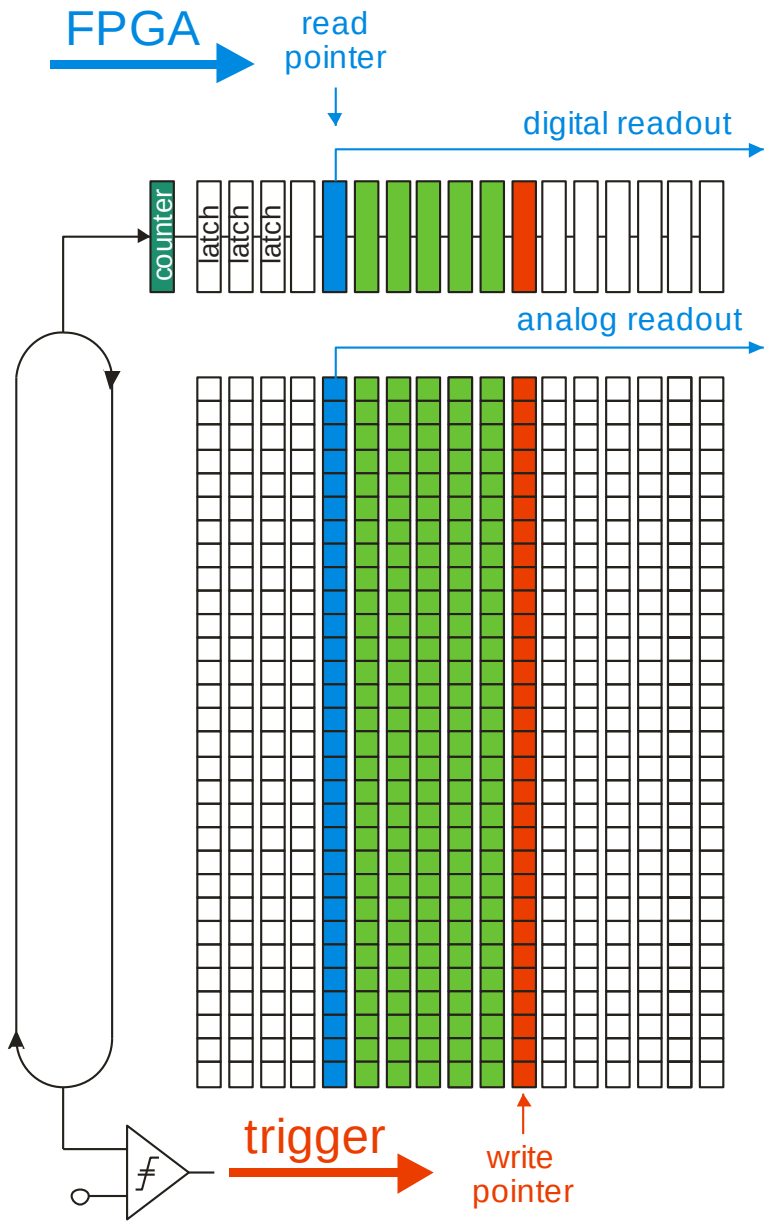


Only short segments of waveform need high speed readout

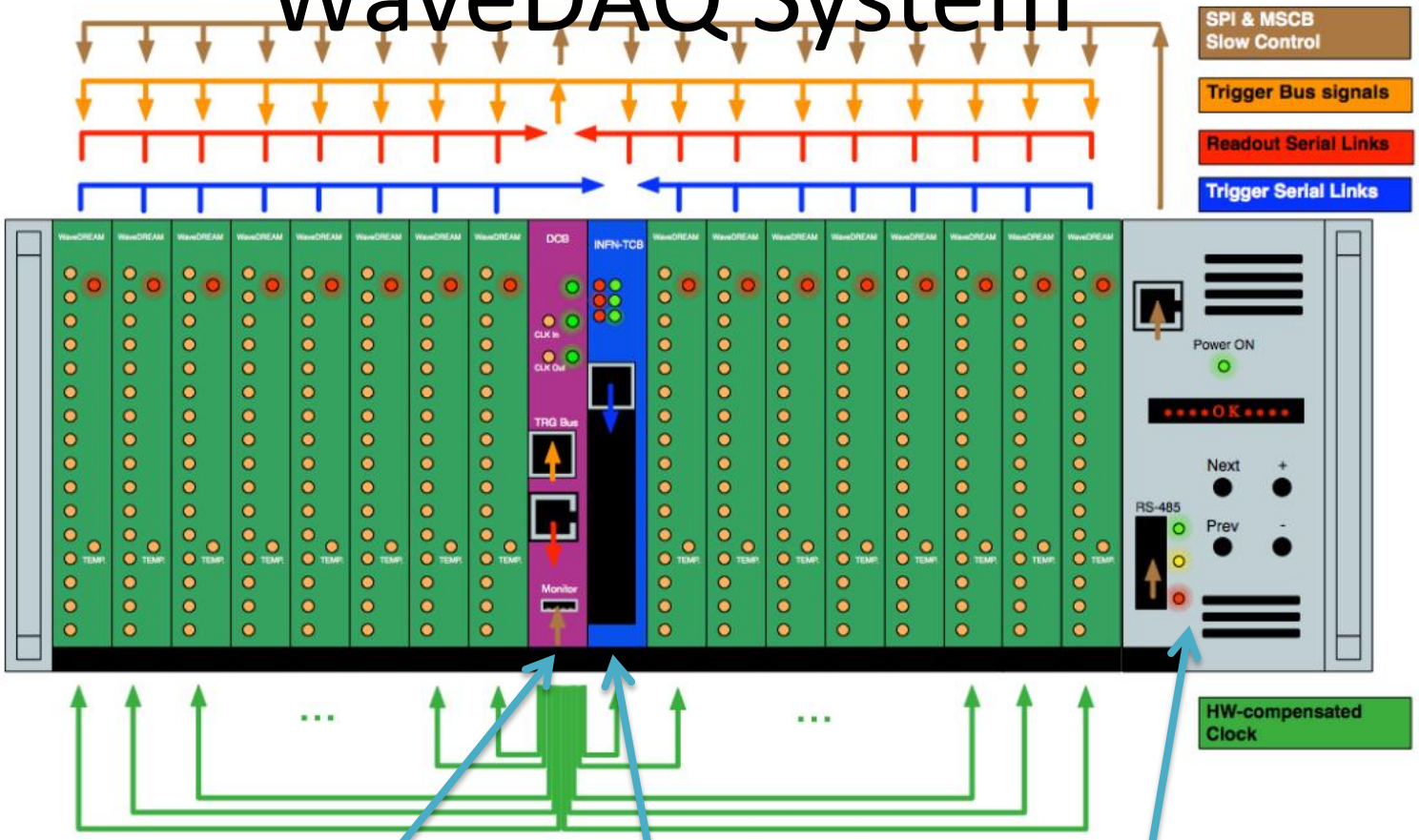
Dead-time free acquisition

- Self-trigger writing of short 32-bin segments
- Simultaneous reading of segments
- Quasi dead time-free
- Data driven readout
  - Ext. ADC runs continuously
  - ASIC tells FPGA when there is new data
- Coarse timing from 300 MHz counter
- Fine timing by waveform digitizing and analysis in FPGA
- 20 * 20 ns = 0.4 µs readout time
  → 2 MHz sustained event rat
- Attractive replacem -TDC





WaveDAQ System



Data Concentrator Board (DCB)

Trigger Concentrator Board (TCB)

Crate **M**anagement **B**oard
- Power supply 24V / 300W
- Fan / Temp. control
- Power cycle each slot
- FPGA Firmware upload
- Local control via buttons
- Ethernet remote control

PSI WaveDAQ

- WaveDAQ system has been designed to fulfill needs of MEG II experiment
- System has huge potential for many others
  (costs: ~150 US$ / channel incl. crate, power, HV)
- Status: Crate fully working, trigger board and WaveDREAM board successfully tested, beam test 2015, DCB under design
- 4 crate system end of 2016,
  full system (35 crates) in 2017
- DRS5 chip (no dead-time) planned for 2018+

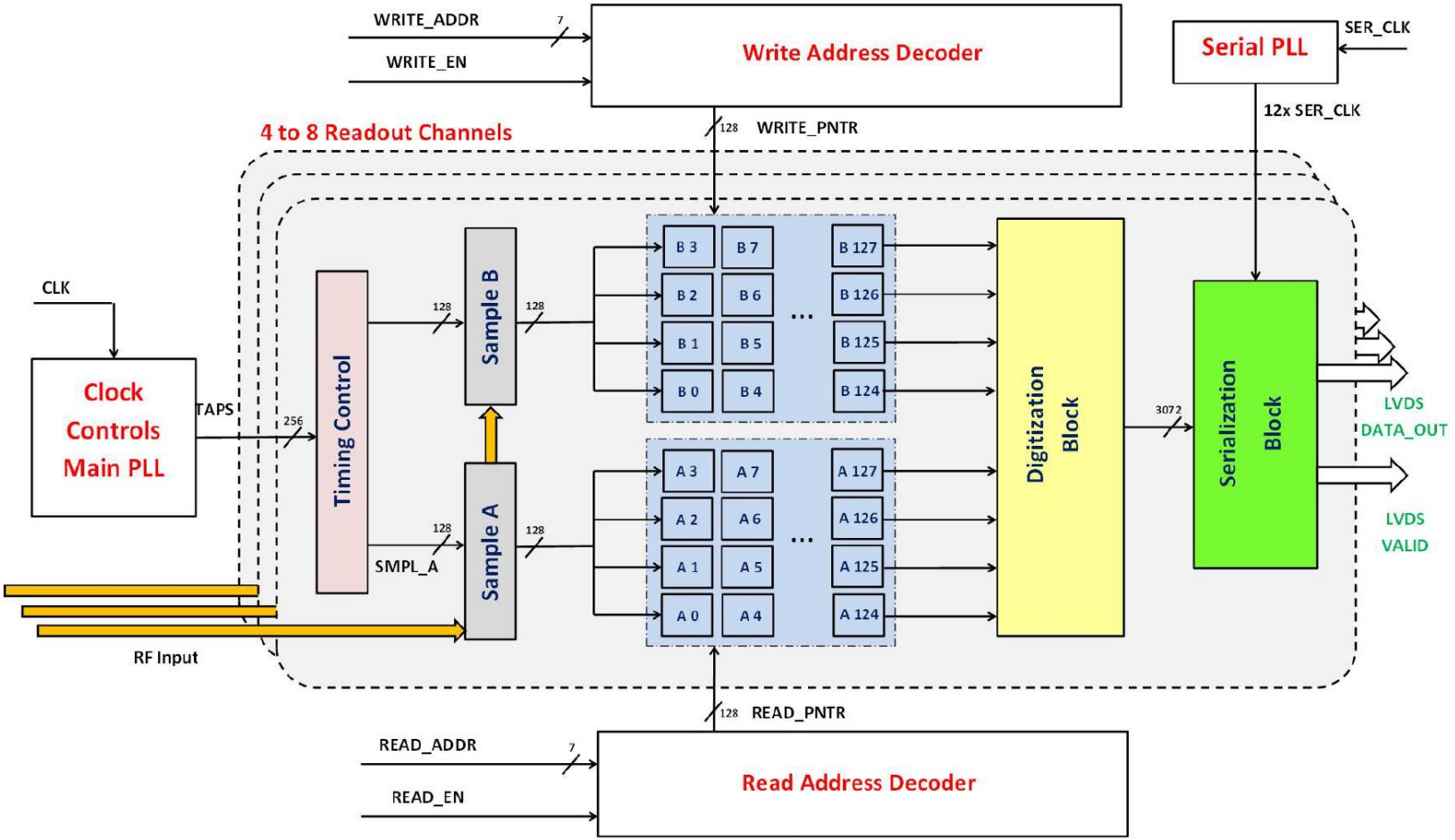
PSEC

PSEC4 compared to **deeper buffer samplers**

Parameter	PSEC4	PSEC5
Channels	6	4
Sampling Rate	4-15 GSa/s	5-15 GSa/s
Primary Samples/channel	256	256
Total Samples/channel	256	32768
Recording Buffer Time at 10 GSa/s	25.6 ns	3.3 μs
Analog Bandwidth	1.5 GHz	1.5 - 2 GHz
RMS Voltage Noise	700 μV	<1 mV
DC RMS Dynamic Range	10.5 bits	10 - 11 bits
Signal Voltage Range	1 V	1 V
ADC on-chip	yes	yes
ADC Clock Speed	1.4 GHz	1.5 - 2 GHz
Readout Protocol	12-bit parallel	serial LVDS: one per channel
Readout Clock Rate	40 MHz	500 MHz
Average Power Consumption	100 mW	300-500 mW
Core Voltage	1.2 V	1.2 V

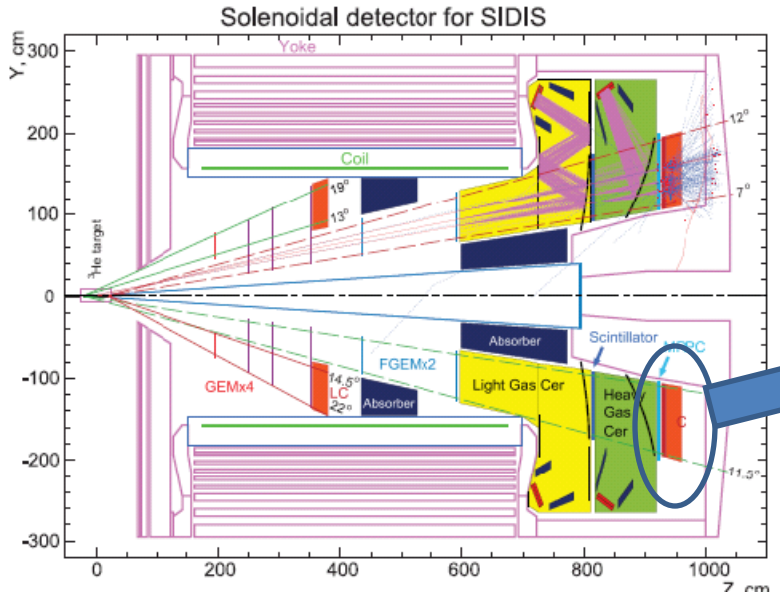
Deeper buffer (PSEC5 and related Hawai'i ASICs)

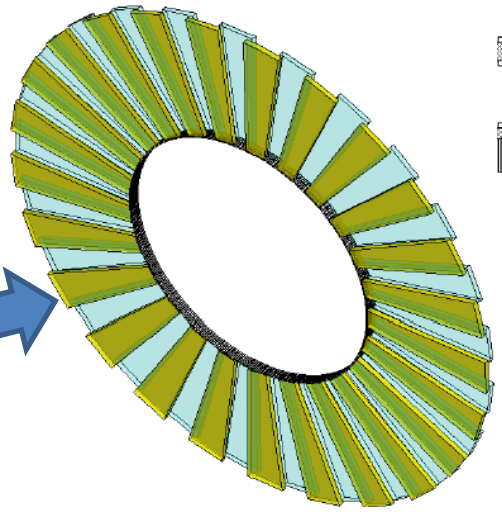
- Potential for 'dead time-less' operation depending on chip sampling rate, readout rate, and experiment trigger rate

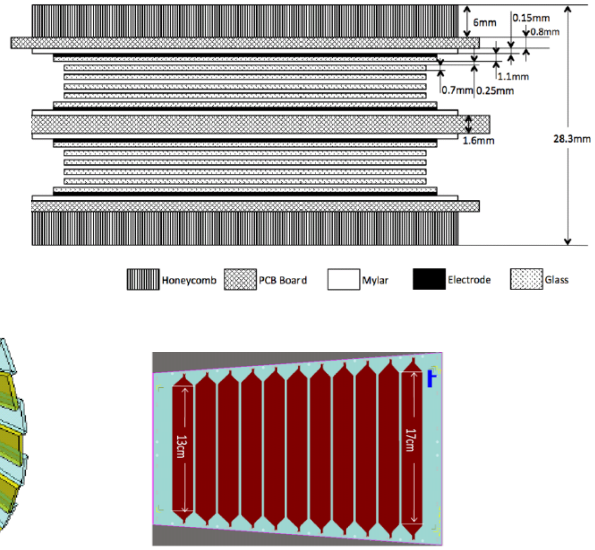


http://annie.uchicago.edu/lib/exe/fetch.php?media=2014_3_1_annie_electronics.pdf Eric Oberla

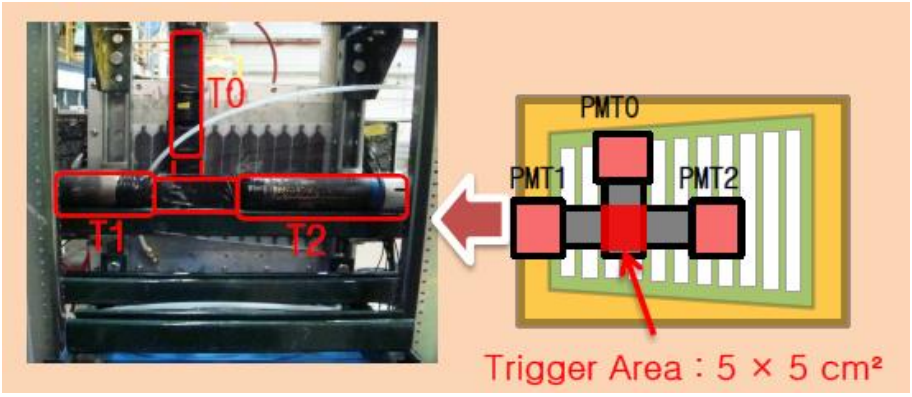
SoLID MRPC High resolution TOF

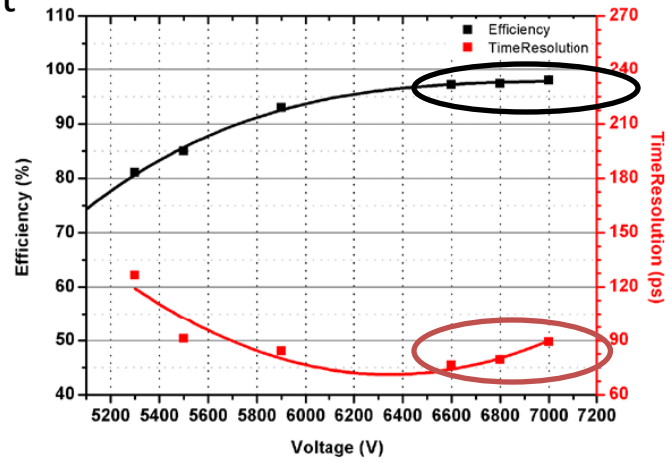






Test in beam at JLAB in 2011 during g_{2p} experiment





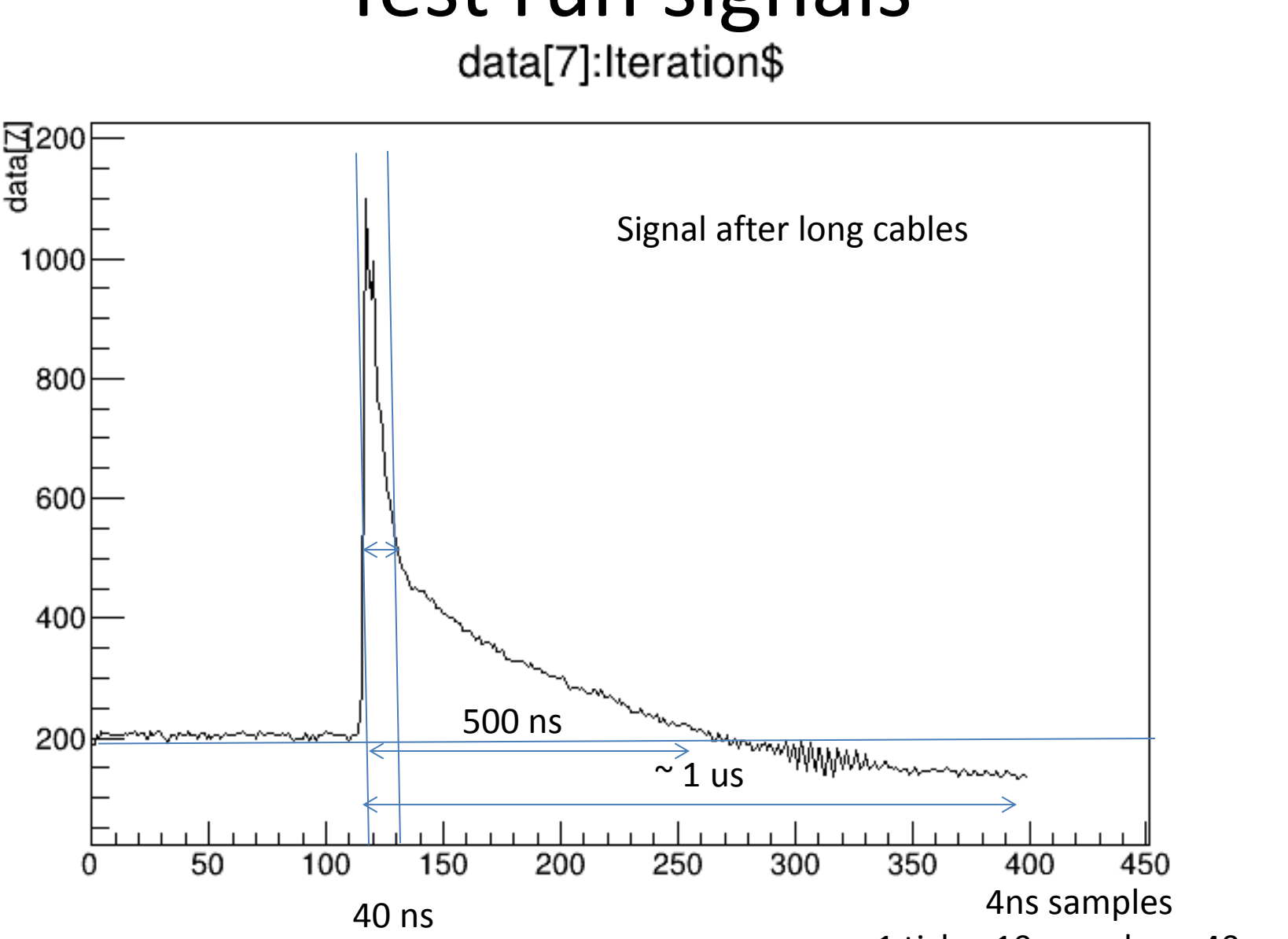
Better than 95 % efficiency

Timing resolution ~ 85 ps

A MRPC prototype for SOLID-TOF in JLab

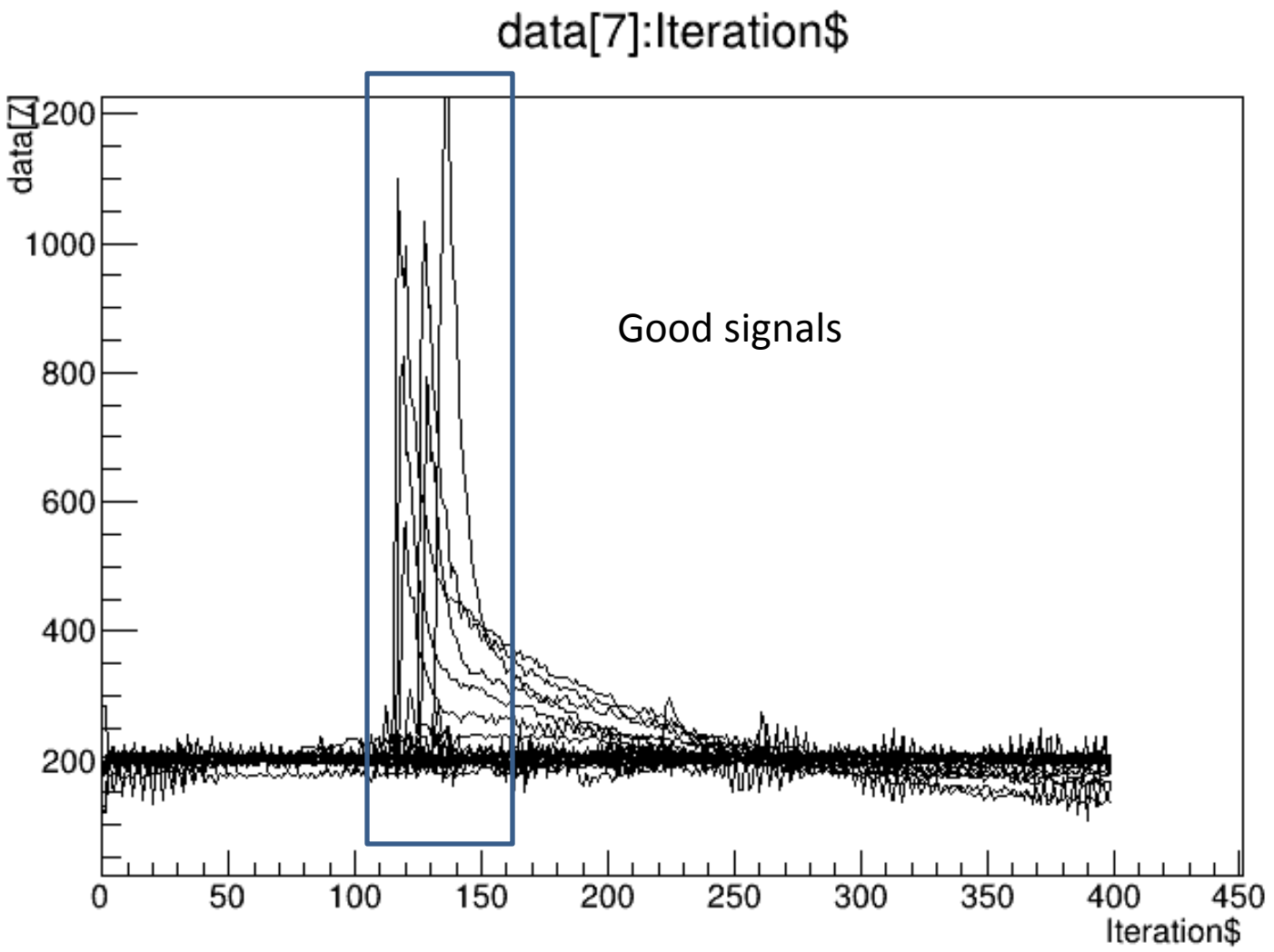
Y. Wang, X. Fan DOI: 10.1088/1748-0221/8/03/P03003 **JINST 8 (2013) P03003**

Test run signals

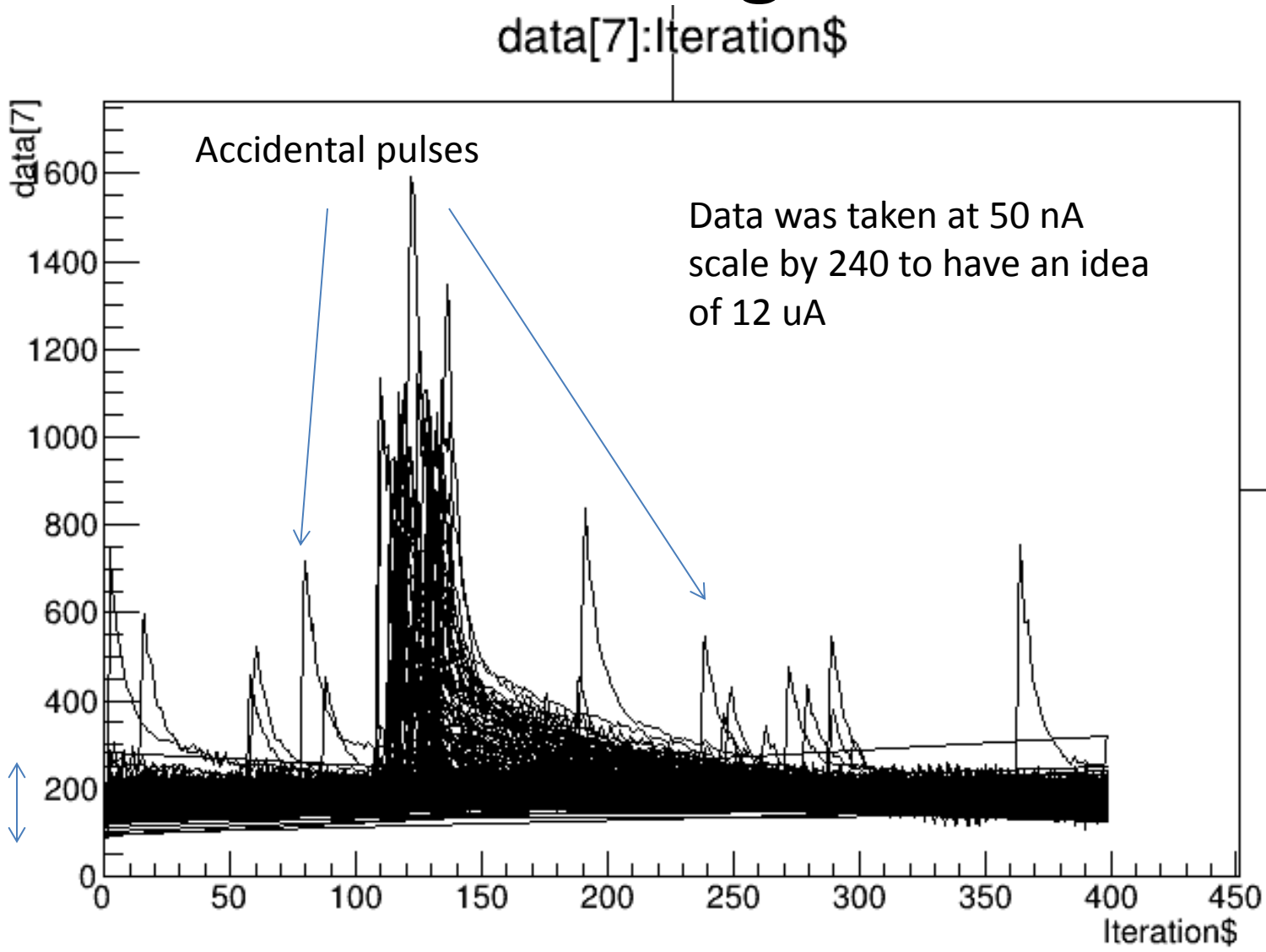


1 tick = 10 samples = 40 ns

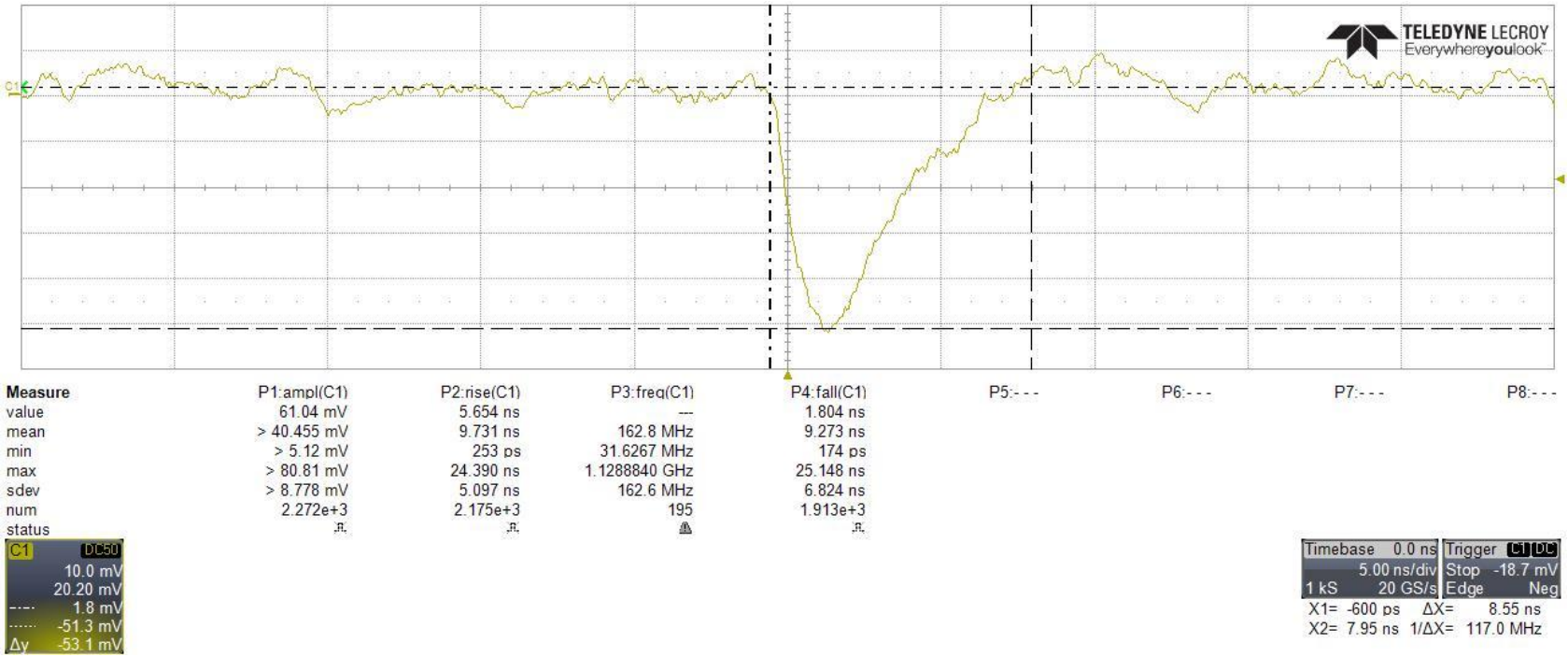
In time signal



Effect of background

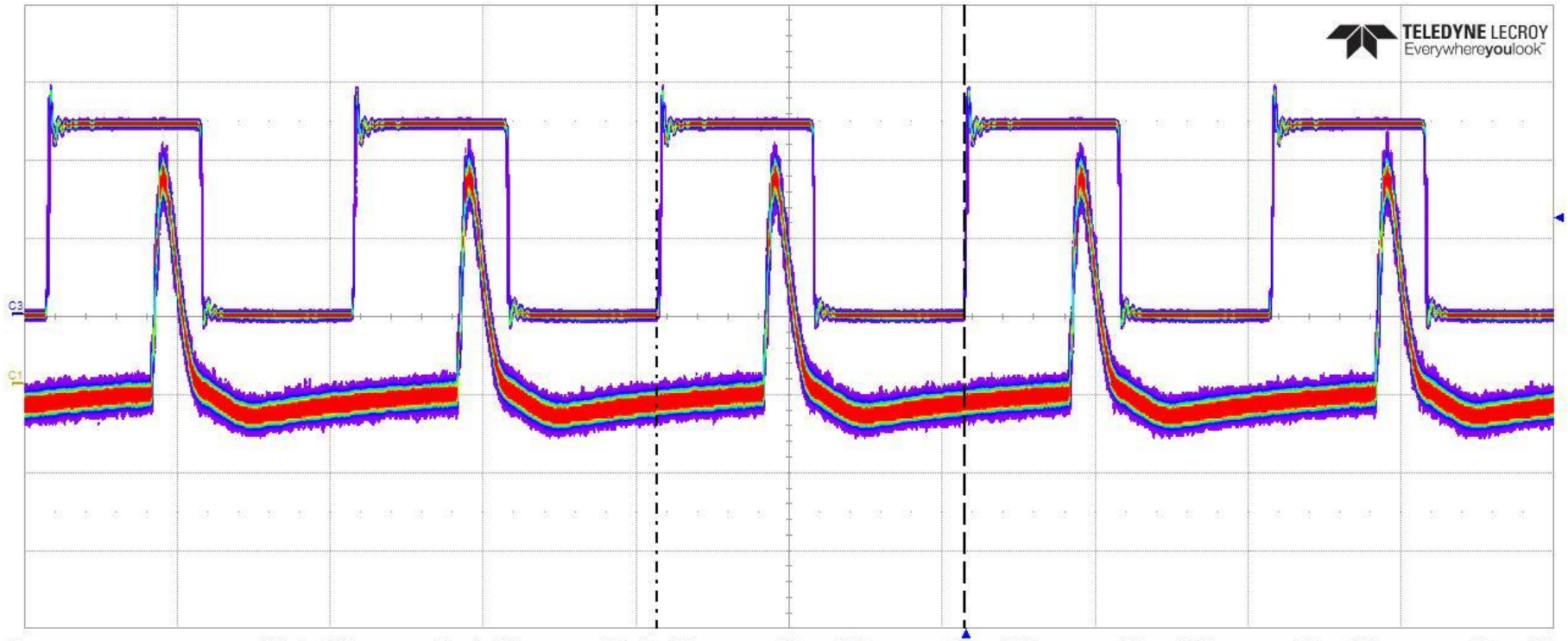


Amplifier Kansas University



- SiGe amplifier developped to TOTEM Ultra Fast silicon detector by Kansas University
- less than 10 ns width with diamond detector

Amplifier laser signal silicon

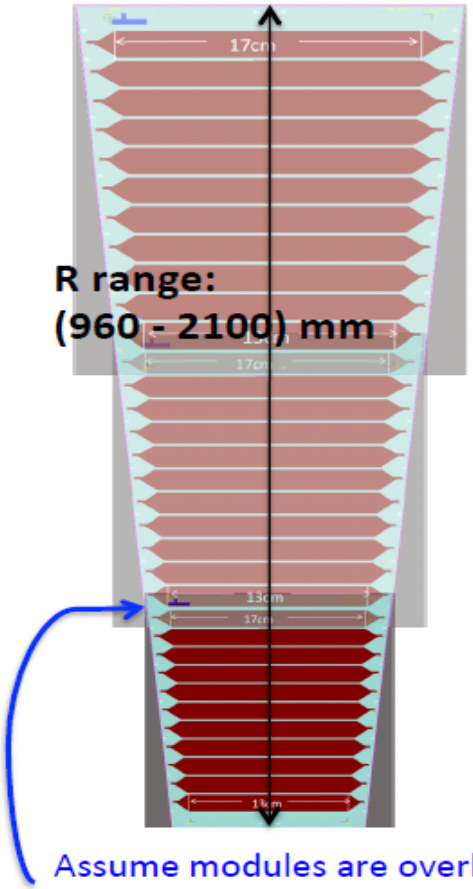


Measure	P1:sdev(C1)	P2:sdev(C2)	P3:sdev(C3)	P4:ampl(C1)	P5:ampl(C2)	P6:ampl(C3)	P7:ampl(C4)	P8:area(C1)
value	33.6 mV	5.4 mV	1.219 V	173.2 mV	42 mV	2.457 V	14 mV	-147.5122 pWb
mean	33.4559 mV	5.30300 mV	1.2190896 V	172.908 mV	42.771 mV	2.456510 V	14.6845 mV	-78.58 pWb
min	31.8 mV	5.1 mV	1.218 V	103.7 mV	37 mV	2.445 V	12 mV	-276.2827 pWb
max	34.7 mV	5.5 mV	1.220 V	194.9 mV	52 mV	2.470 V	17 mV	101.7577 pWb
sdev	389.0 µV	69.43 µV	390.3 µV	7.647 mV	2.556 mV	4.283 mV	847.5 µV	67.94 pWb
num	554	554	554	554	554	554	554	554
status	✔	✔	✔	⚓	⚓	✔	⚓	✔

Silicon pulsed at 10 MHz with KU amplifier

SoLID background

Supermodule design

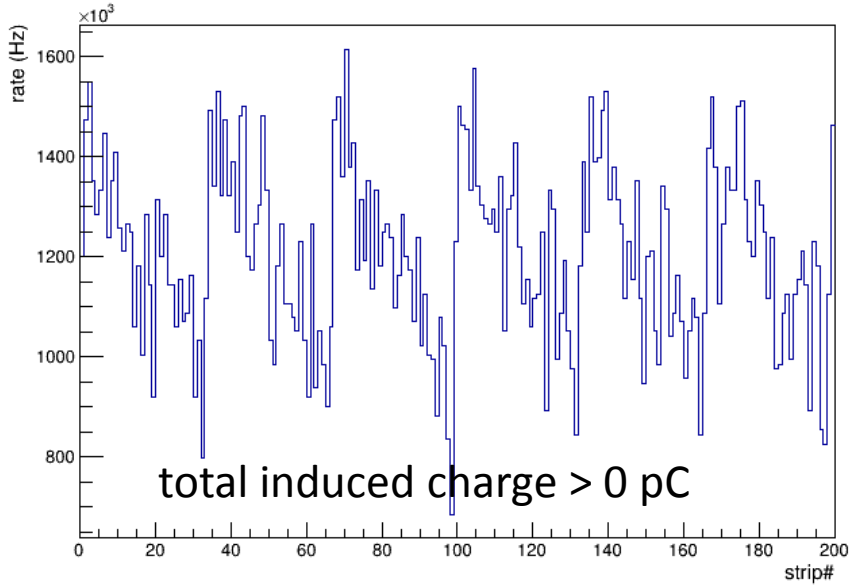


- # supermodules: 50
- # strips: 33
- Strip width: 25mm, gap: 3mm

- Model #3:
  - Start the first strip at R=1050 mm (details in the next slide)

Single rate

- Beam on target
- Average rate/channel:
  - total induced charge > 0.0 pC: 1.2 MHz
  - total induced charge > 0.5 pC: 893.2 kHz

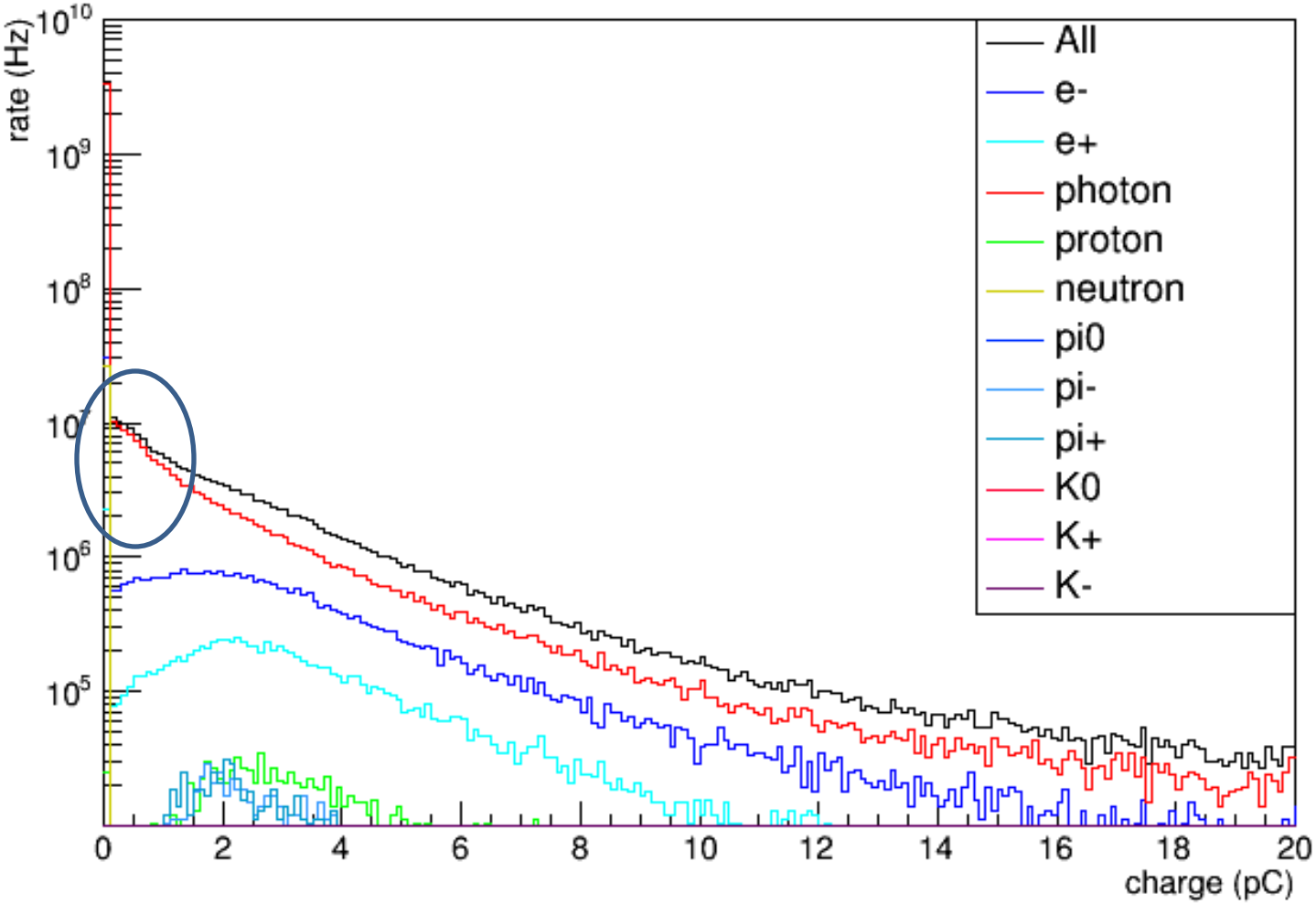


total induced charge cut (pC)	Average rate / channel (MHz)
0.0	1.20
0.1	1.11
0.2	1.06
0.3	1.00
0.5	0.95
0.6	0.84
0.7	0.80
0.8	0.76
0.9	0.72
1.0	0.69
1.1	0.65

Study by Sanghwa Park (Stony Brook)

Total incident particle rate - cut scan

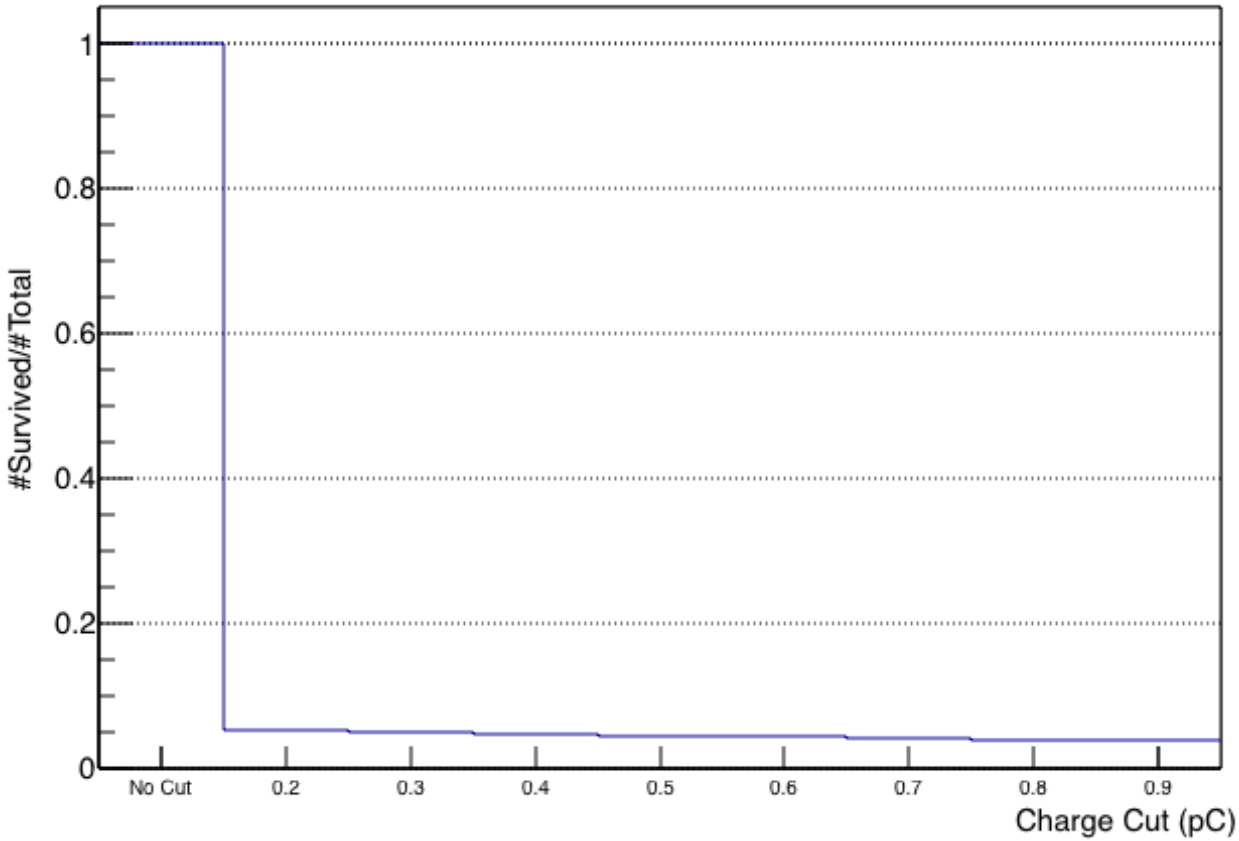
- Charge cut scan: scan range (0.2 - 0.9) pC



Study by Sanghwa Park (Stony Brook)

Total incident particle rate - cut scan

- Charge cut scan: scan range (0.2 - 0.9) pC



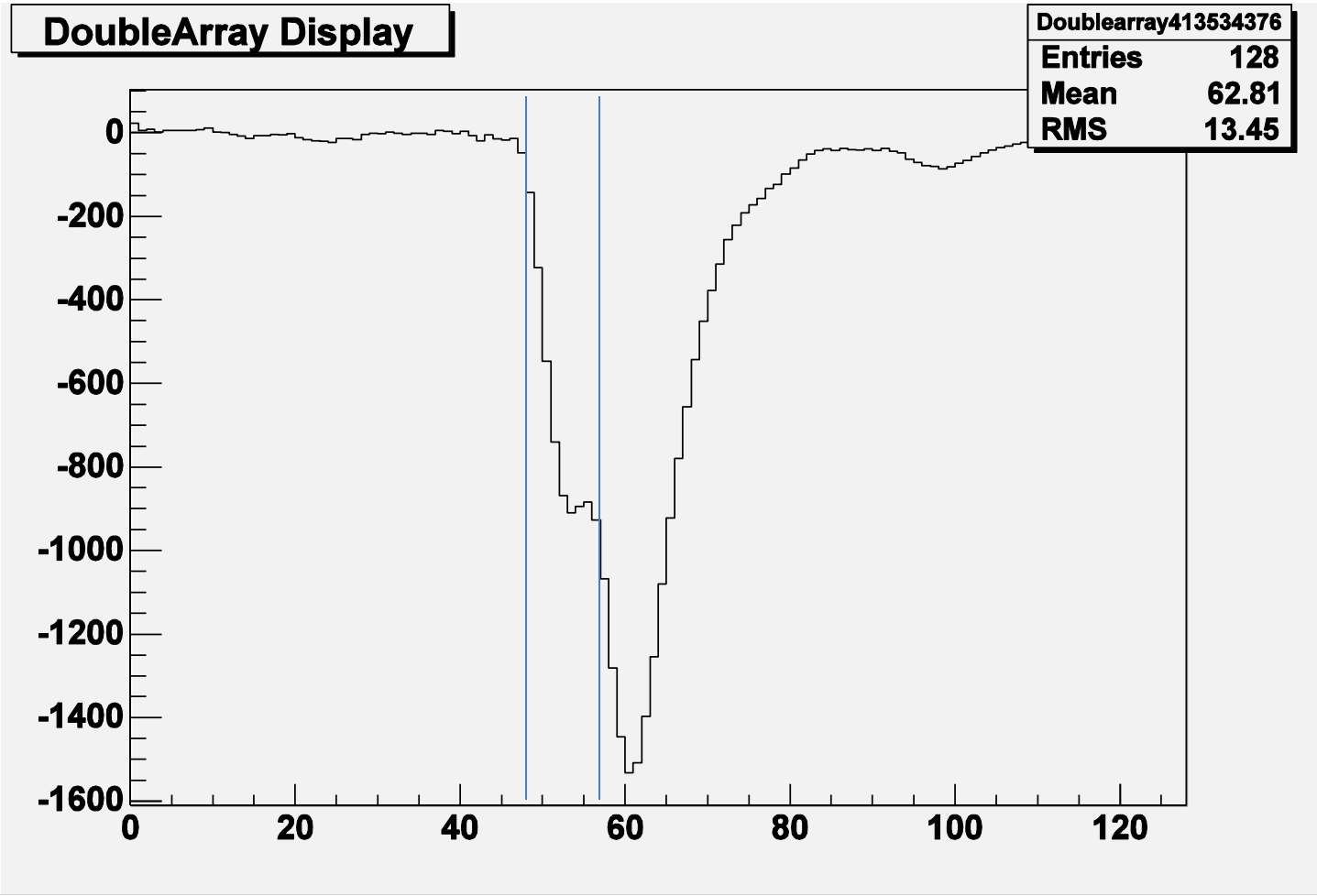
Charge > 0.2 pC
~ 95% reduced
(#total incident particles)

Study by Sanghwa Park (Stony Brook)

SoLID background

- Single channel rate at about 1 MHz level
- Assume 30 ns timing window, about 3% probability to have a hit
- Preliminary rate show pile-up should be ok
- TDC option should work
- Sampling option still desired option for better timing resolution and pile-up events

Pile-up


DoubleArray Display
Doublearray413534376
Entries 128
Mean 62.81
RMS 13.45
0
-200
-400
-600
-800
-1000
-1200
-1400
-1600
0
20
40
60
80
100
120

Pile-up example calorimeter DVCS

http://hallaweb.jlab.org/data_reduc/AnaWork2002/camsonne-ws2002.ps

Linear fit of reference waveform

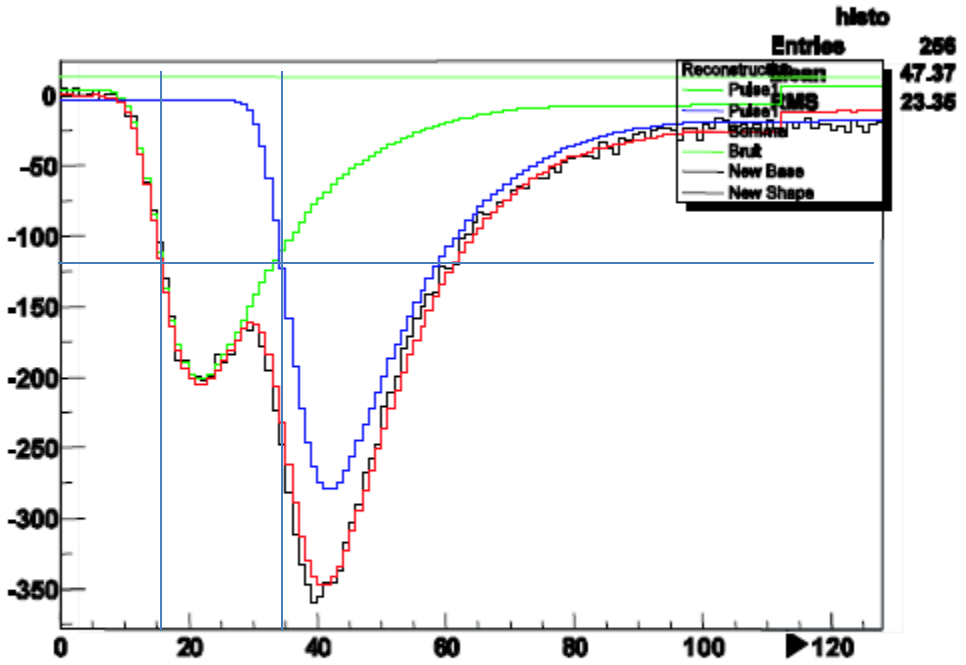
Resolve pile up at

5 ns level

20% of events with pile-up

Timing resolution

0.6 ns



Singles rate in one block up to 1 MHz

Ideal features for SoLID TOF

- 5 to 10 GHz sampling rate
- 20 ps or better timing resolution
- 1 GHz or more analog bandwidth
- Waveform readout
- On chip Zero suppression
- Discriminator for fast trigger
- External trigger (single channel trigger rate is about 1 MHz)
- can handle up to 200 KHz of trigger rates
- Data transfer capability
  - on chip suppression required
  - assume 3300 channels 10 ns at 10 GHz 12 bit
    at 200 KHz and occupancy 1 % : 900 MB/s
    (1.6 MB/s per chip 6 channel per chip : 10 Mbit/s link ok, 100 Mbit/s link desired)
- 8 us buffer latency (4 us minimum)

Conclusion

- SoLID SIDIS experiment requires 80 ps
- 20 ps timing resolution extend K/pi separation at high momentum up to 5.5 GeV
- Preliminary background studies about 1 MHz per channel but need more studies
- TDC and A/D option should work
- New generation chips available in 2018
- Sampling option desired for SoLID DRS5 or AARDVARC good candidates