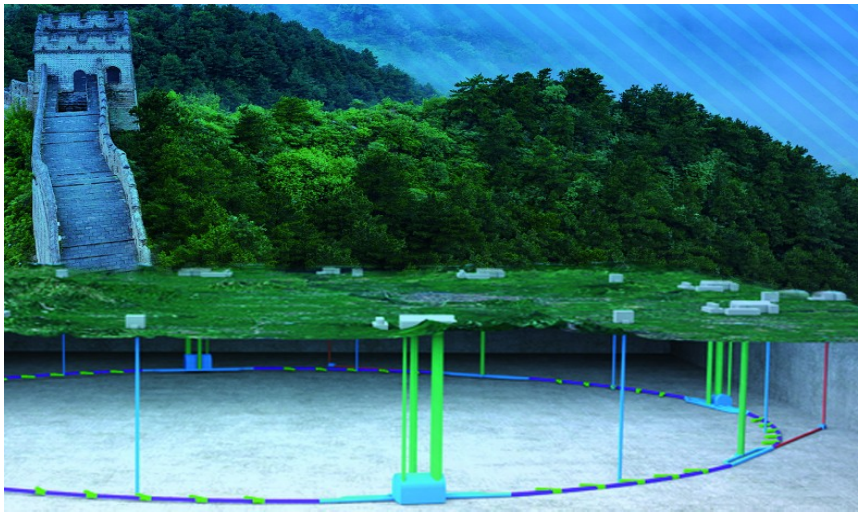
Pixel Sensor Technologies for the CEPC

S. Grinstein (IFAE Barcelona)

CEPC Workshop
6th - 8th November 2017
IHEP, Beijing



ICREA EXCELENCIA SEVERO OCHOA IFAE

Outline

- *Introduction*
- *DEPFET*
- *CMOS*
- *Depleted-CMOS*
  - *Focus on AMS HV-CMOS technology results*
- *SOI*
- *Timing*
- *Conclusions*

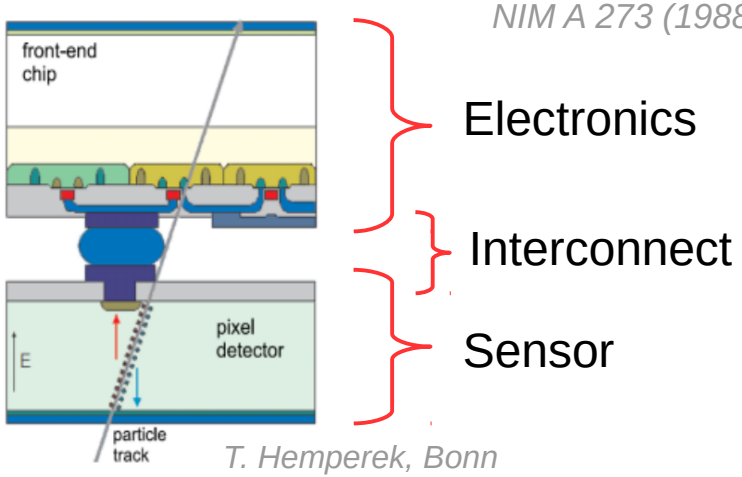
Silicon Detectors in HEP

- Innermost layers of HEP accelerator-based experiments require:
  - **Position resolution**
  - Radiation hardness, rate capability, compactness, low material budget, etc

- Technology of choice: **silicon pixel sensors**

Hybrid detectors

E.H.M. Heijne et al., NIM A 273 (1988) 615

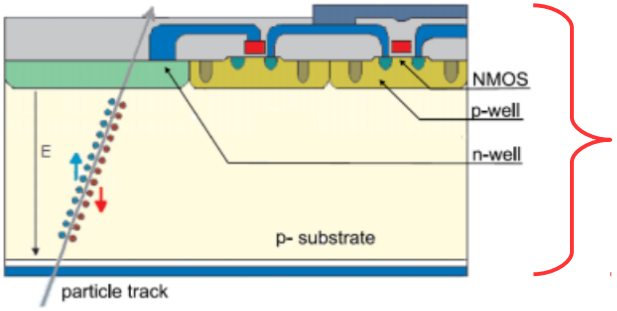


T. Hemperek, Bonn

- Standard in current experiments
- Design allows for optimization of electronics and sensor
  - Radiation hardness, rate, power...

Monolithic detectors

S. Parker, NIM A 275 (1989) 494



- Less material, less complexity
- Smaller pixel possible
  - No pixel size limitation due to interconnection

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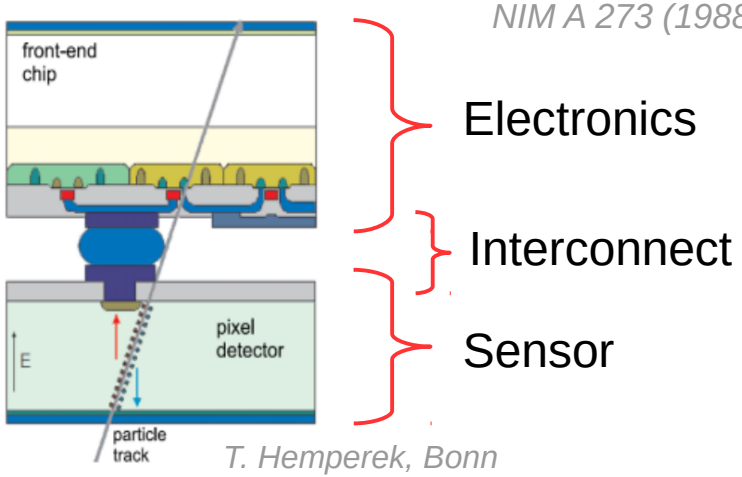

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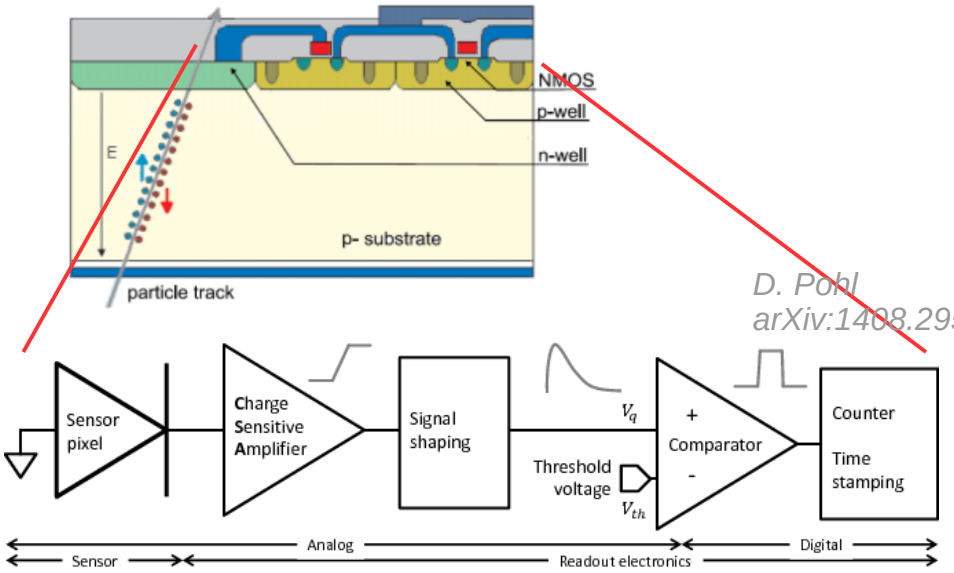


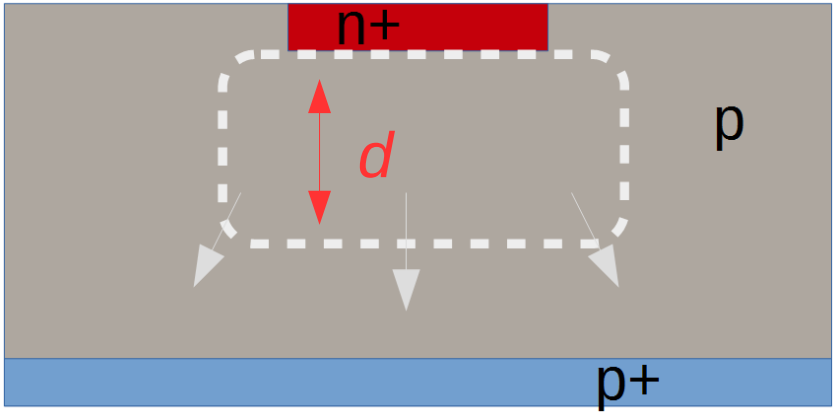
D. Pohl arXiv:1408.2952

Comparator and digital part can be in periphery of chip

Silicon Detectors in HEP

- Silicon bulk:

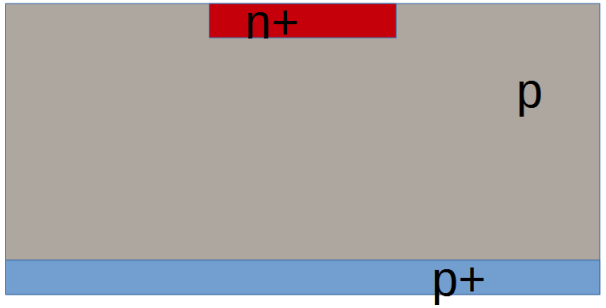
$$d \sim \sqrt{\rho \cdot V}$$



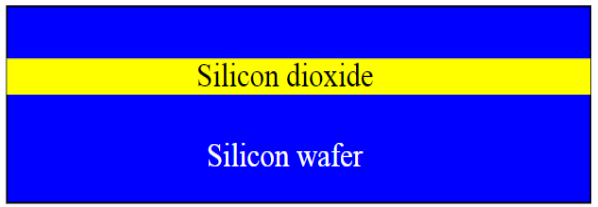
- High resistivity silicon
  - ρ > 1 kΩ.cm
  - Used in most HEP detectors
  - Relatively expensive
  - Charge collection:
    - Can fully deplete (~300 um)
    - By drift
    - Fast (~10 ns)
  - Radiation hard

- Low resistivity silicon
  - ρ < 100 Ω.cm
  - Commercial CMOS processes
  - Relatively cheap
  - Charge collection:
    - Under depleted
    - Usually by diffusion
    - Slow (~100 ns)
  - Not radiation hard

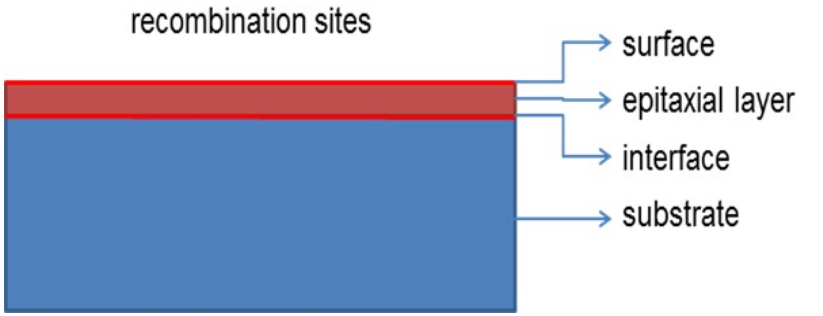
Silicon Detectors in HEP



- Standard HEP detector on **high ρ silicon substrate**
- n-on-p collect electrons, faster



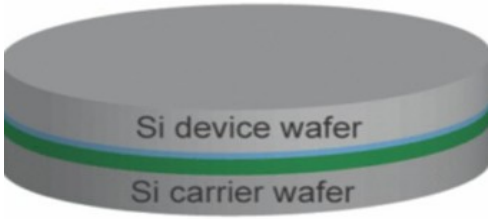
- **Silicon On Insulator** (SOI)
- SiO2 reduces parasitic capacitance
- Top layer varies with application
- Used in specialized processes



few µm

- **Epitaxial layer** on silicon bulk
- Usually deposited through CVD
- Used in CMOS processes

- Wafer to wafer bonding



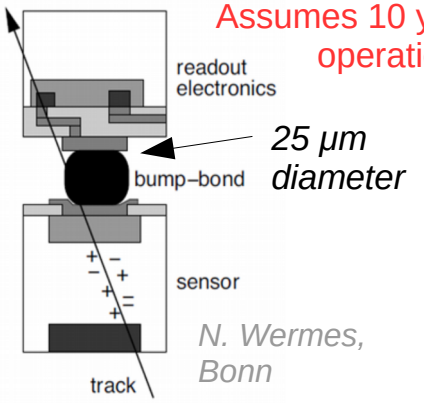
- **Technology selection** driven by experimental **conditions & requirements**, examples:
  - Radiation hard thin SOI 3D sensors (high ρ layer)
  - CMOS sensors on epitaxial wafers

Experimental Conditions

	ATLAS IBL	Belle II	STAR	ALICE ITS Upgrade	ILC	ATLAS ITk HL-LHC	CEPC *
Fluence [neq/cm2]	5E+15	1E+13	1E+12	1E+13	1E+12	1E+16	1E+13
Ionization dose [Mrad]	100	10	0.3	3	1	500	25
Particle rate [kHz/mm2]	1000	400	100	10	200	10000	850
Timing [ns]	25	20000	200000	20000	350	25	30
Pixel size [um x um]	50 x 250	50 x 55	20 x 20	30 x 30	20 x 20	50 x 50	< 20 x 20
Power [mW/cm2]	200	100	170	40	50	100	50
Material [% X0]	1.5	0.2	0.4	0.3	0.2	1	0.15

* J. Gimaraes da Costa, this workshop
Assumes 10 yrs operation

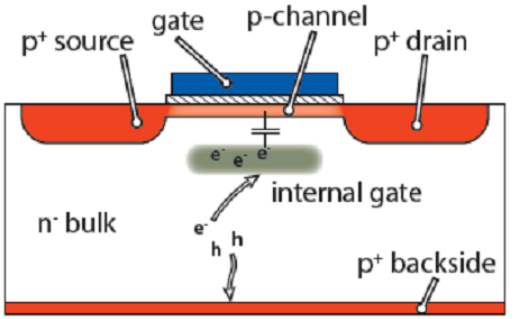
- **Hybrid** devices used in many HEP experiments, however
  - Smaller pixels (limited by bump-bond in hybrids)
  - Lower material budget (*power dissipation!*)
  - Relaxed radiation hardness requirement
- Favor **monolithic** approach
  - Initially development focused on non-standard processing technologies
    - Now target standard CMOS processes



Bump size limits the size of the hybrid pixel to about 50 µm

DEPFETs Devices

- **DE**pleted **P**-channel **F**ield **E**ffect **T**ransistor in a fully depleted bulk
  - *Kemmer and Lutz, NIM A 253 (1987) 365*
- Collected charge that drifts to gate modulates the source-drain current, amplified



Pros

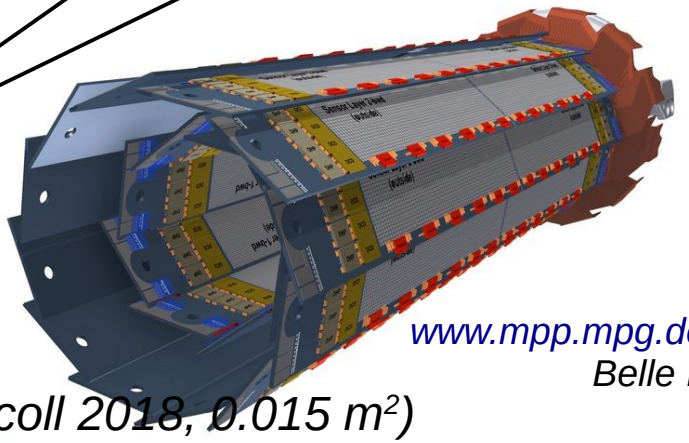
- Fine granularity
- Thin sensors (~80 µm)
- Excellent S/N

pixel: 50 µm x 55-85 µm

H.-G. Moser, NIM A 831, (2016) 85

Cons

- **Not** fully monolithic
  - Only amplifier implemented in pixel cell
  - Needs extra electronics to process signals
- Slow read out
  - Limited by frame readout



www.mpp.mpg.de
Belle II

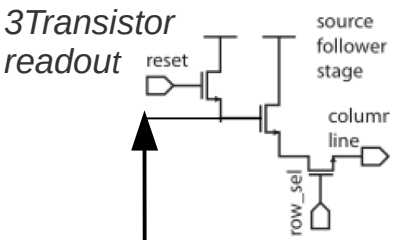
- ✔ ***Belle II*** *(first coll 2018, 0.015 m²)*
- ✔ And being considered for future linear colliders

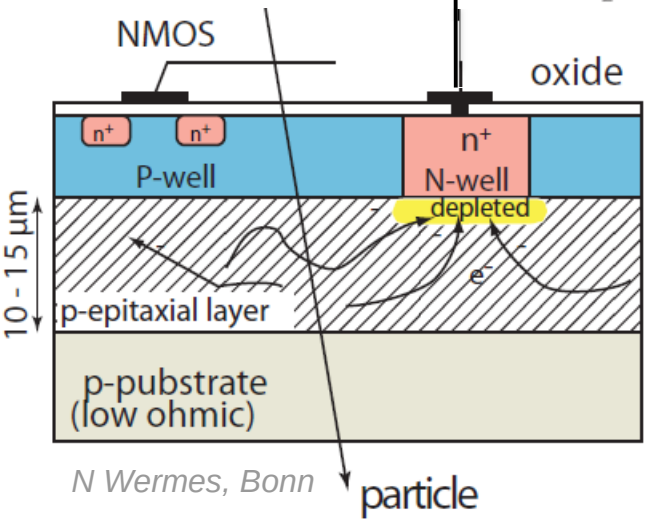
Monolithic Active Pixel Sensors

- **MAPS**: **M**onolithic **A**ctive **P**ixel **S**ensor
  - Initially on ρ-low under-depleted bulk
  - Only NMOS transistors
  - *R. Turchetta et al., NIM A, 458:677–689, 2001*

- A successful line of devices: **MIMOSA**
  - Minimum Ionizing particle MOS Active pixel sensor
  - Developed at **IPHC Strasbourg**
- First generations successfully used in:
  - EUDET particle telescopes
  - STAR Heavy Flavor Tracker

First CMOS vertex detector! (0.16 m²)

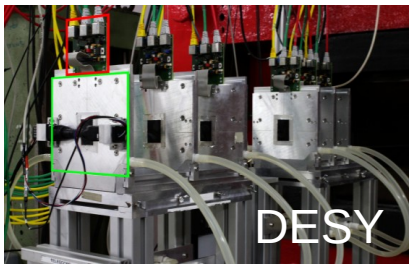




N Wermes, Bonn

MIMOSA 26 Telescope

AMS 350nm CMOS technology



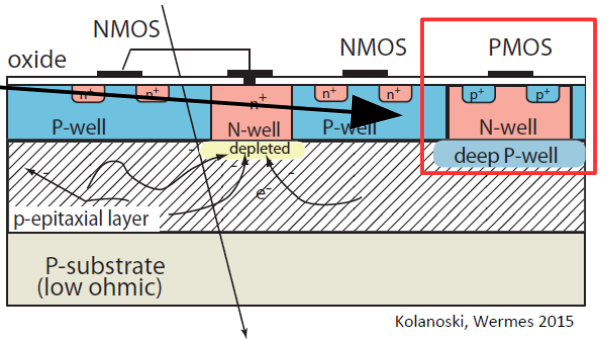
L. Grenier, STAR HFT ladder

Cons

- NMOS limitation, slow (diffusion), radiation soft

Use triple/quadruple well processes to allow PMOS transistors

R. Turchetta et al. Sensors (2008)



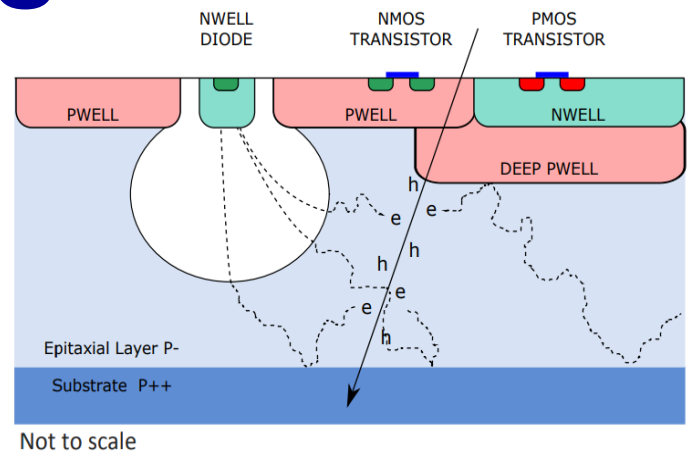
➢ *See talk of **C. Hu** on this workshop*

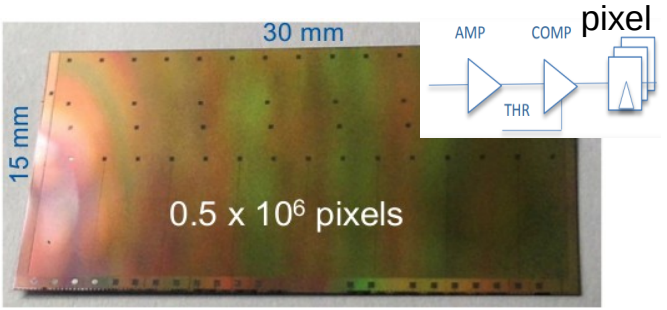
CMOS Devices

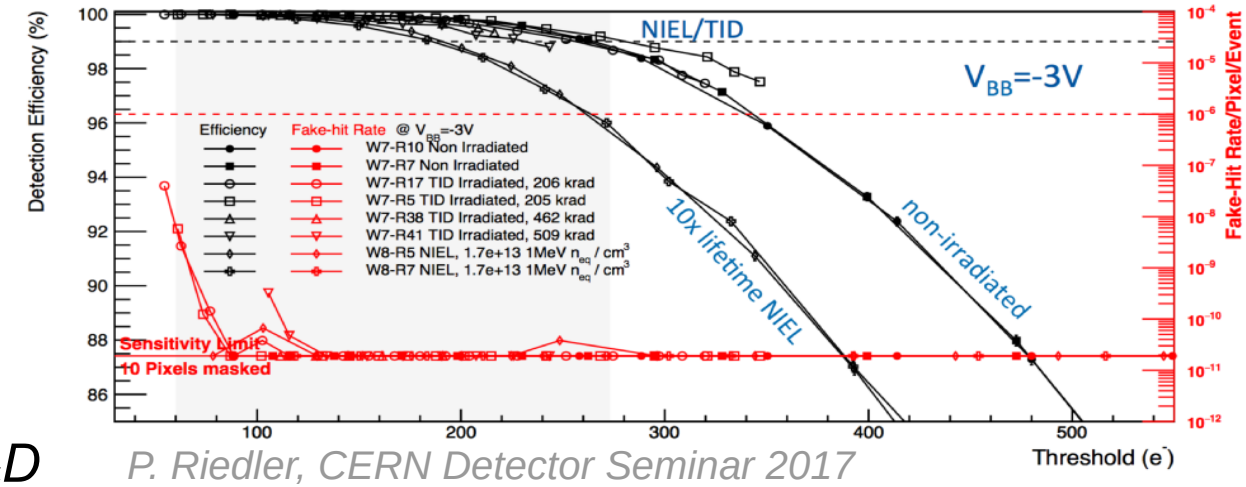
W. Snoeys, CERN

ALICE Inner Tracker System Upgrade

- **ALPIDE** chip: *G. Aglieri et al.,NIM A 845 (2017) 583–587*
  - TowerJazz 0.18µm CMOS imaging process
  - 30 mm x 15 mm with 30 x 30 µm² pixels
- Small n-collection electrode in high-ρ epi-layer
  - Small input capacitance!
    - Low noise, low threshold operation, low power...
  - Moderate bias voltage: increase depletion region
- ALICE ITS Detector
  - ~2019/2020 installation
  - 10 m²
  - 0.3% X_0 /layer (inner)
  - Radiation hardness:
    - 0.6Mrad, 1.7E13 n_{eq}/cm^2







P. Riedler, CERN Detector Seminar 2017

Pros

- Promising technology for CEPC
  - *Selected for initial CEPC R&D*
- …Radiation hard enough?

➢ *See talk of **W. Snoeys** on this workshop*

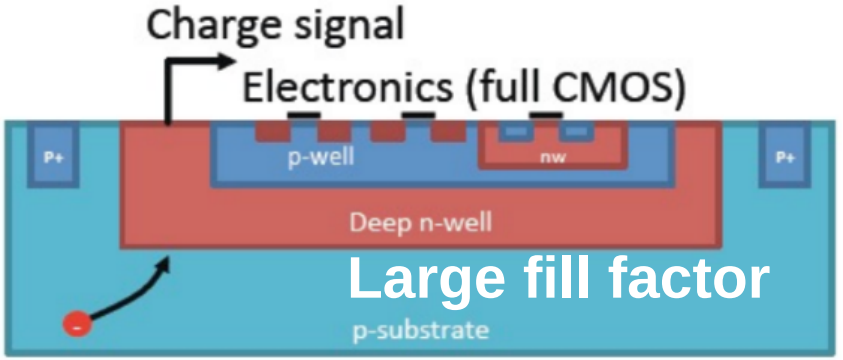
Depleted CMOS for ATLAS HL-LHC

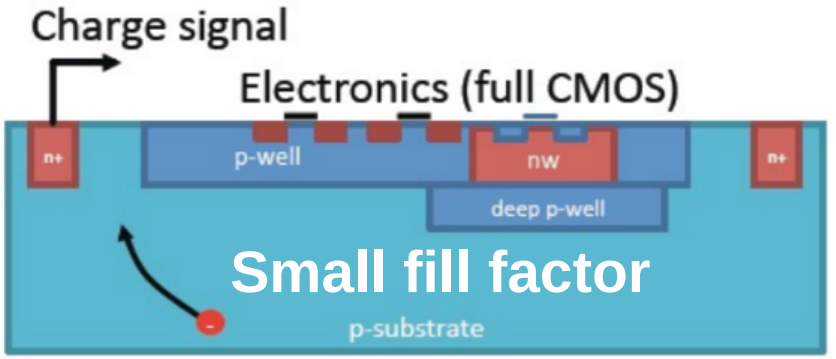
- **HL-LHC** is a **harsh radiation environment** (~1E16 n_{eq}/cm^2, 500 Mrad)
  - **Not** the target for **CEPC**, but lessons to be learned...

- Achieve higher radiation harness with **depleted substrates**:
  - High voltage or high resistivity approach (HV/HR-CMOS)
  - *I. Peric et al., NIM A 582 (2007) 876*

$$d \sim \sqrt{\rho \cdot V}$$

Two approaches to depleted-CMOS





- Electronics **inside** n-well
  - Full CMOS inside
  - Large collection node
  - Shorter drift distances (more rad hard)

Cons

- Higher noise or power (larger capacitance)

- Electronics **outisde** n-well
  - Full CMOS inside
  - Small collection node
  - Small capacitance (less noise & power)

Cons

- Potential lower radiation hardness (larger drift)

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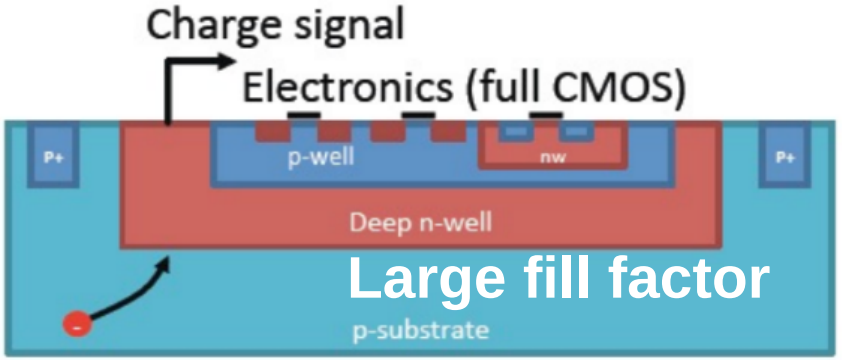
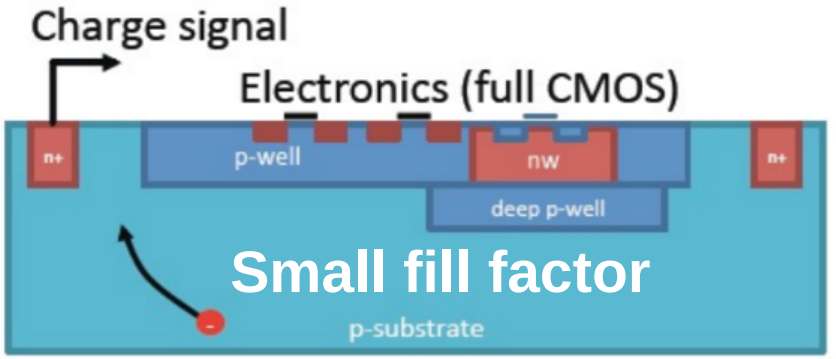




- Electronics **inside** n-well — AMS, LFoundry
  - Full CMOS inside
  - Large collection node
  - Shorter drift distances (more rad hard)

Cons

- Higher noise or power (larger capacitance)

- Electronics **outisde** n-well — TowerJazz, ESPROS
  - Full CMOS inside
  - Small collection node
  - Small capacitance (less noise & power)

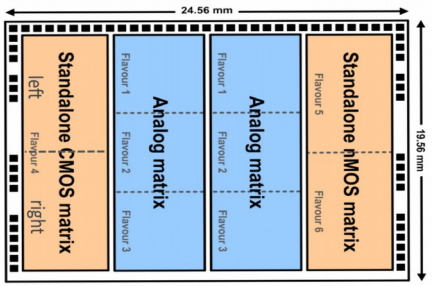
Cons

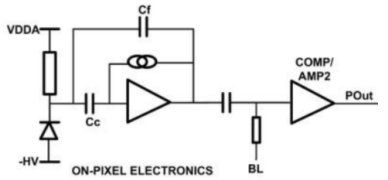
- Potential lower radiation hardness (larger drift)

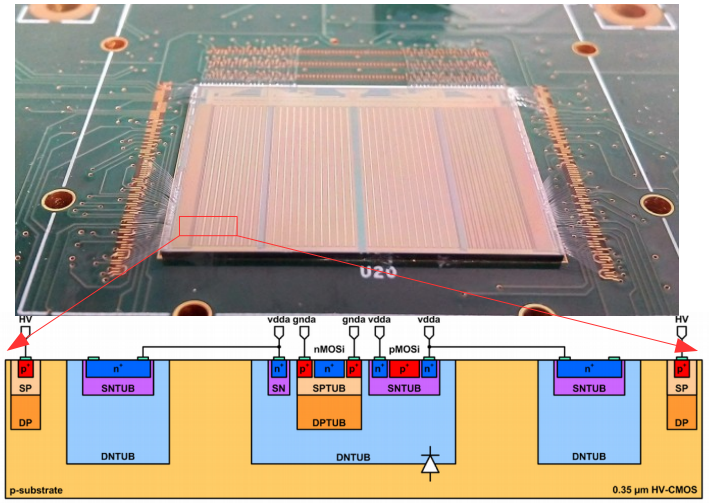
Depleted CMOS for ATLAS HL-LHC

H35demo: first full size investigator with large fill factor

- AMS 350 nm HV-CMOS
- Two monolithic and two analog-only (for AC coupling *) matrices
- Resistivity: 20-80-200-1000 Ωcm
- Pixel: CSA + Discr/2nd Ampl

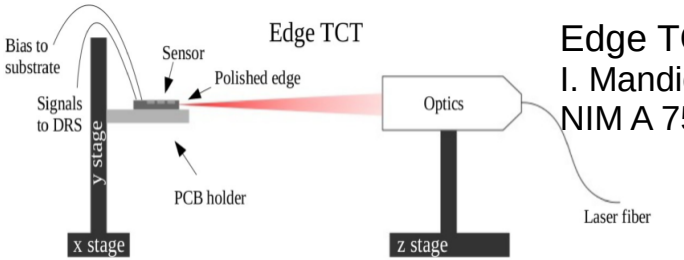




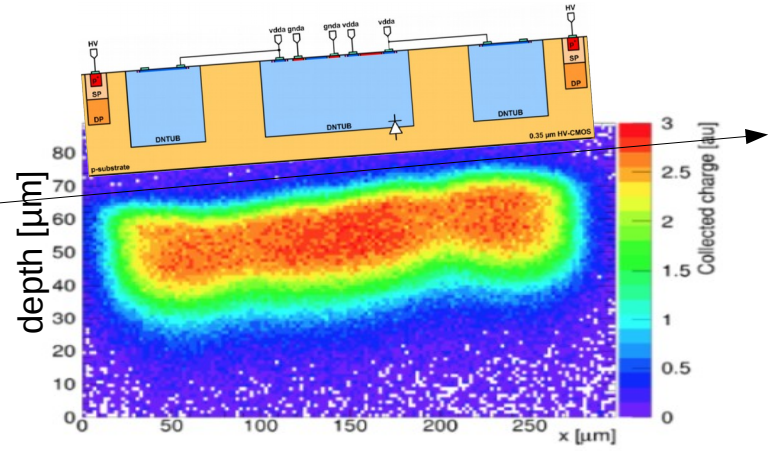


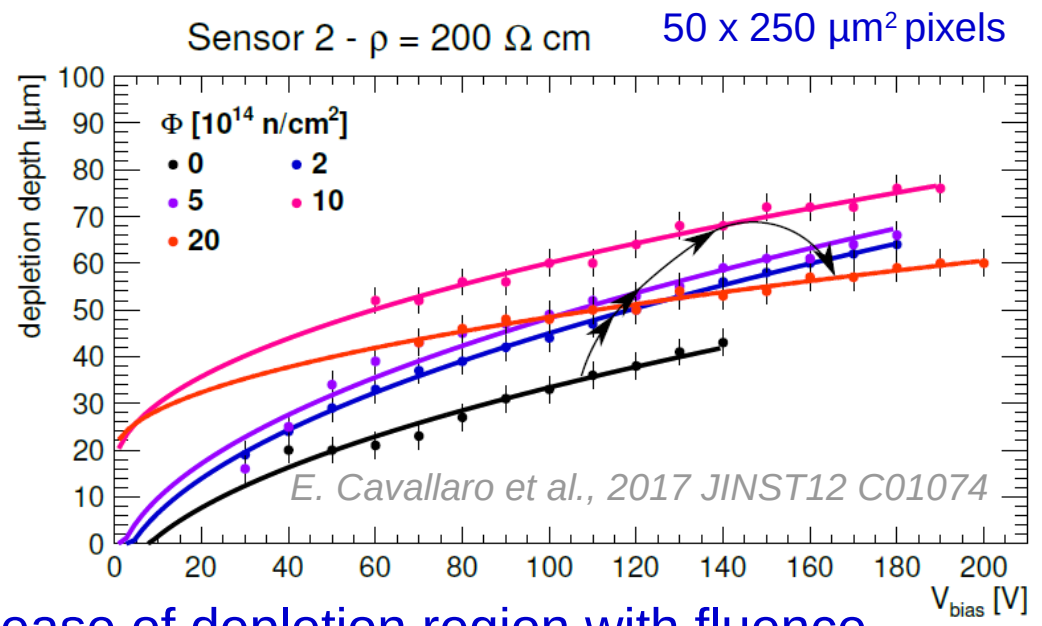
50 x 250 µm² pixels

Charge collection properties



Edge TCT
I. Mandić et al.,
NIM A 751 (2014) 41





➢ Increase of depletion region with fluence up to ~1E15neq/cm2 for this resistivity

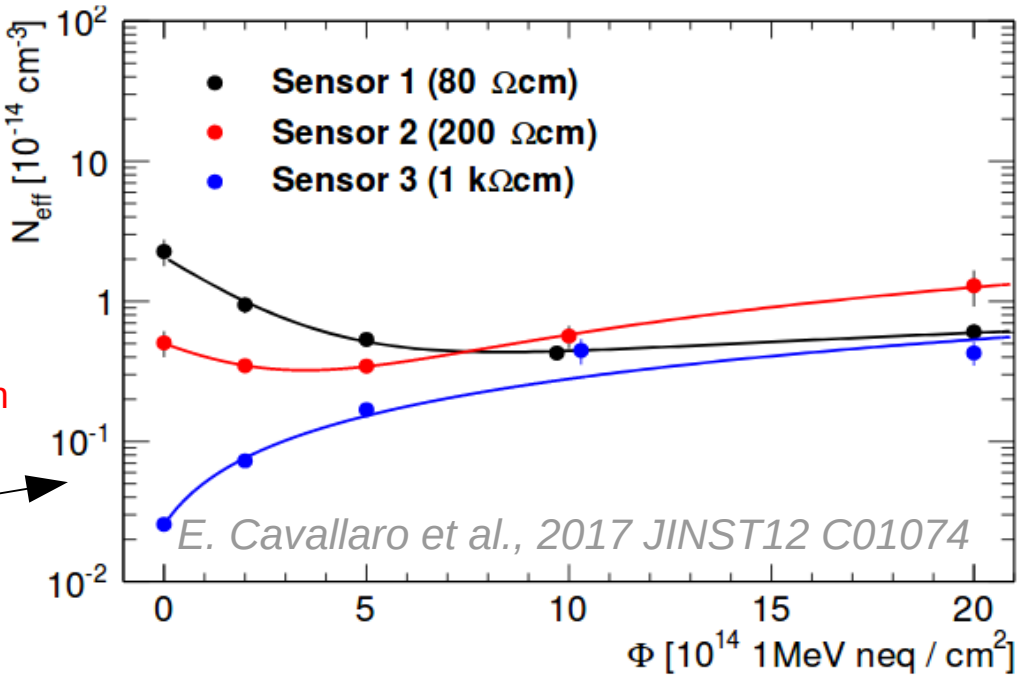
* See backup for AC coupling comments

Depleted CMOS for ATLAS HL-LHC

$$d(V) = d_0 + \alpha\sqrt{\rho V} = d_0 + \sqrt{\frac{2\varepsilon\varepsilon_0}{eN_{eff}}V}$$

$$N_{eff} = N_{eff0} - N_c \cdot (1 - exp(-c \cdot \Phi_{eq})) + g_c \cdot \Phi_{eq}$$

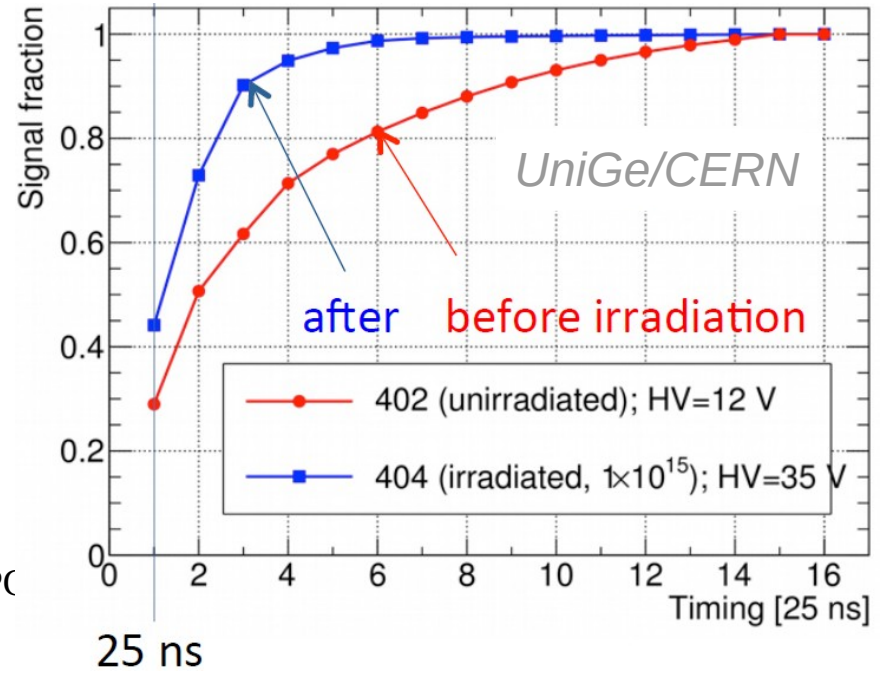
Initial doping — Acceptor removal — Acceptor introduction



- Initial acceptor removal beneficial for **low resistivity** substrates (up to 1E15 n_{eq}/cm^2)

- In-time signal fraction increases with irradiation

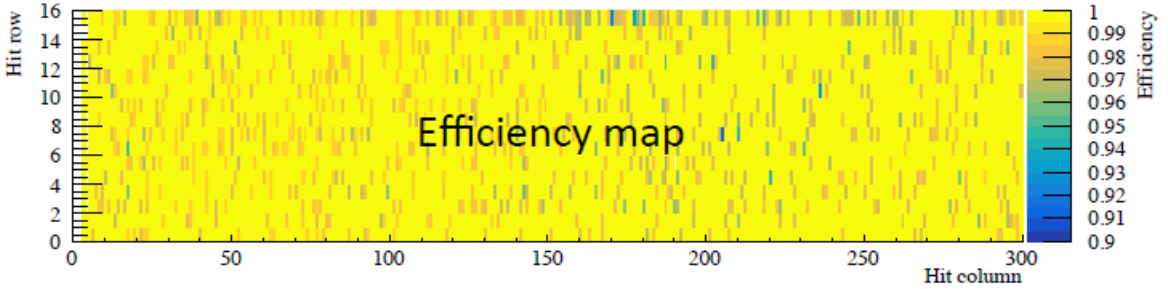
AMS 180 nm CCPDv4



- For moderate fluencies **low resistivity** may be favorable
  - *However, not common to have good control of resistivity!*

Depleted CMOS for ATLAS HL-LHC

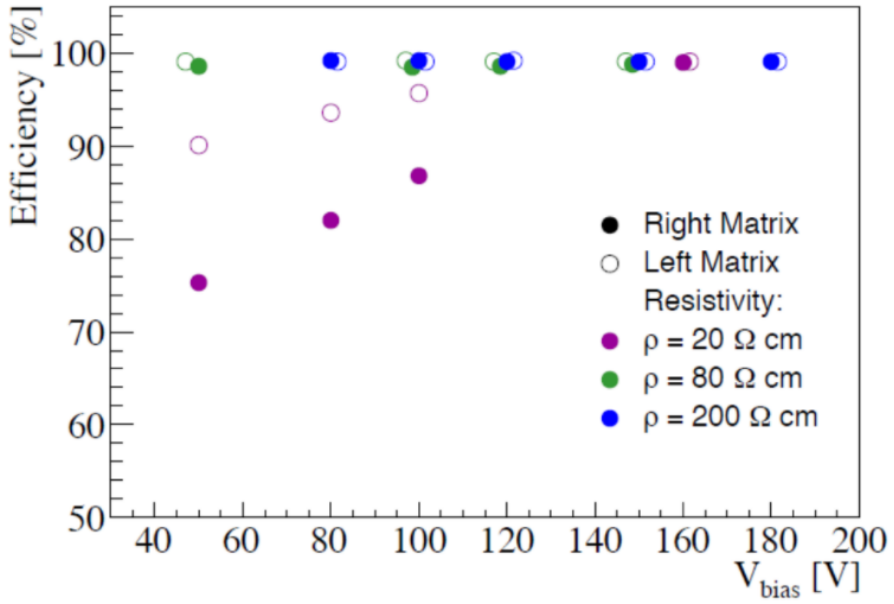
- H35demo **monolithic** matrices characterization
  - *R. Casanova et al., TWEPP 2017*

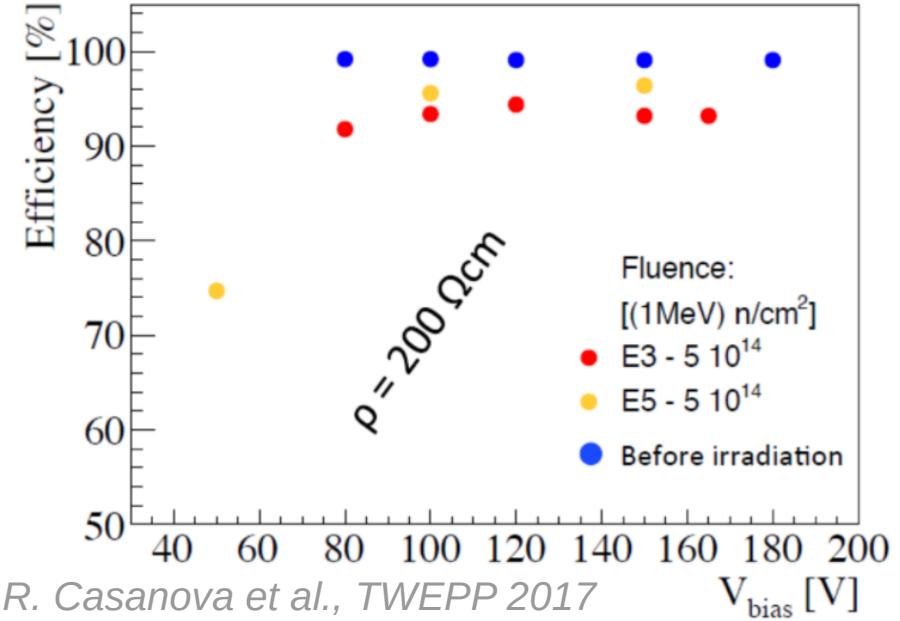


Hit reconstruction efficiency

- **Before** irradiation
  - Uniform efficiency
  - For low resistivity, large bias needed to achieve 99% (in large fill factor designs)
- **After** irradiation (5E14 n_{eq}/cm^2)
  - For ρ = 200 Ωcm: eff > 90% above 80 V
  - Other resistivities being studied
    - However: 350mW/cm2
    - Significantly lower in next generation (ATLASpix, aH18): 100mW/cm2

I. Peric, priv comm 2017



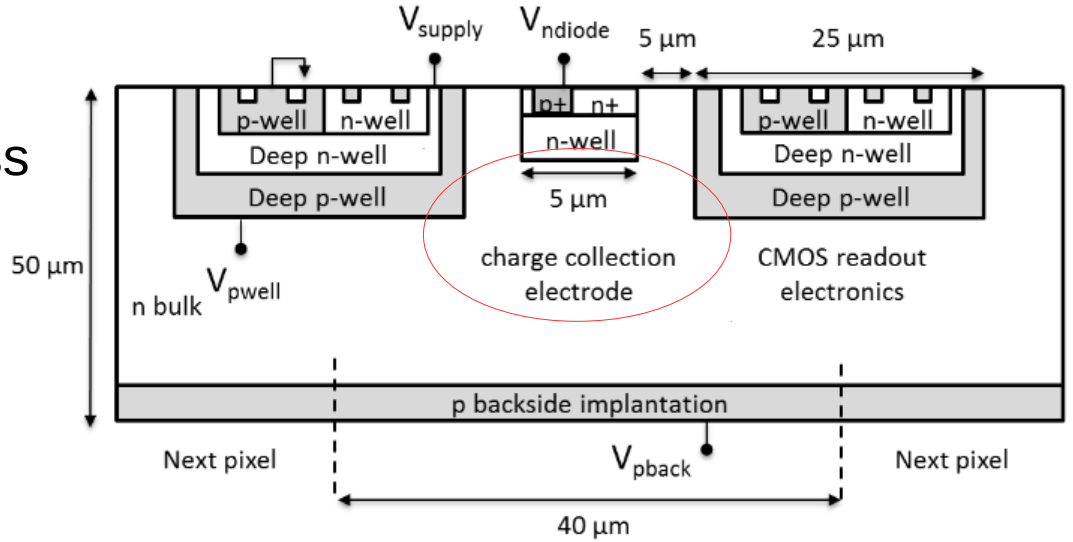


R. Casanova et al., TWEPP 2017

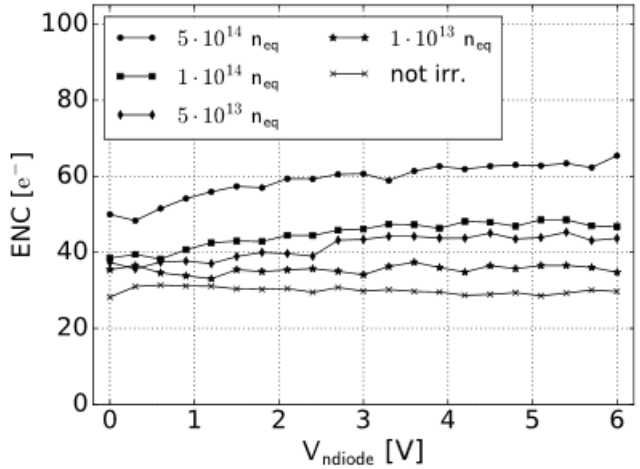
Depleted CMOS for ATLAS HL-LHC

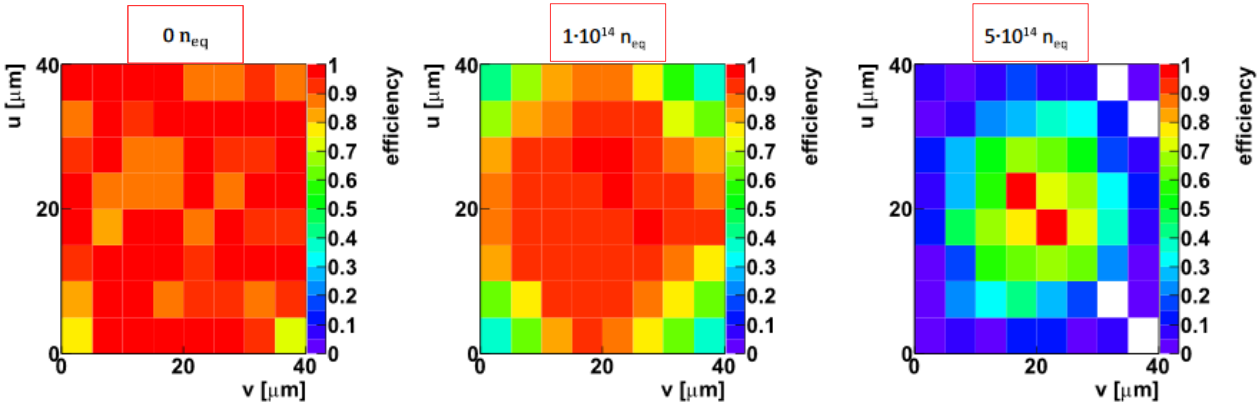
***Small fill factor** approach*

- ESPROS
  - 150nm CMOS, 6 metal layer process
  - Deep p-well, isolated full CMOS
  - Substrate: high-ρ **n-type bulk**
  - Backside implant
  - 40 x 40 μm^2 pixels
  - CSA and discr. + binary readout



T. Obermann et al., 2017 JINST 12 C01062



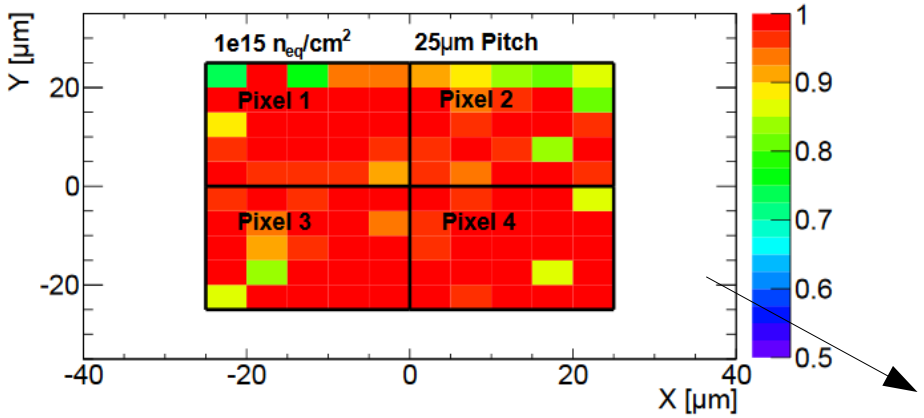


➢ Low noise performance… but significant efficiency degradation at 5E14 n_{eq}/cm^2

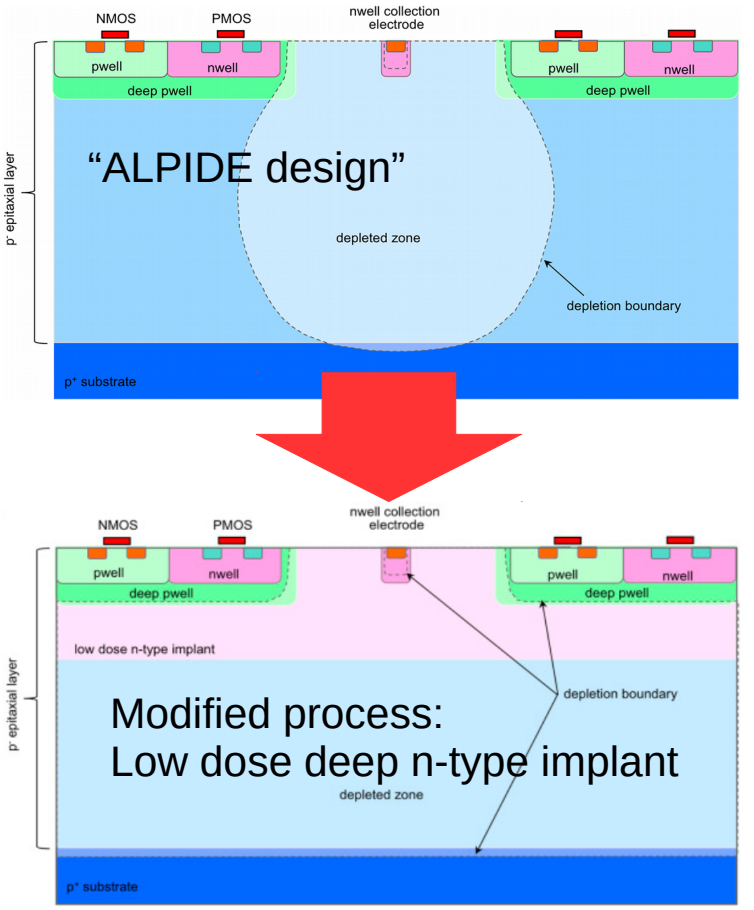
Depleted CMOS for ATLAS HL-LHC

***Small fill factor** approach*

- **TowerJazz ATLAS Investigator**
  - Based on ALICE developments
  - TJ 180 nm full CMOS ***modified process***
    - TJ-Monopix
  - epi p-type 25 µm on p-type substrate
  - ρ > 1kΩ cm
  - Various pixel sizes included
    - 25 x 25 to 50 x 50 µm^2
  - Pixel: CSA + discr + hit memory



H. Pernegger et al., 2017 JINST 12 P06008



W. Snoeys et al., NIM A 871, 1 (2017) 90

- Improved results after irradiation
- 97.4% for 30 x 30 µm^2 (1E15 neq/cm2)

➢ *See talk of **W. Snoeys** on this workshop*

SOI Devices

- **SOI: S**ilicon **O**n **I**nsulator (on SiO2)
  - Combine thin low ρ electronic layer with high ρ bulk:
    - Monolithic approach with good detector efficiency
  - *J. Marczewski et al., IEEE Trans Nucl Schi 51 1025 (2004) – SUCIMA project*

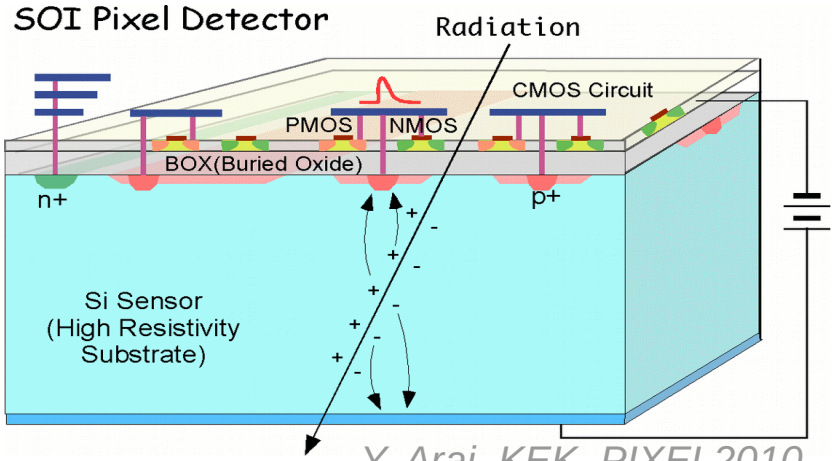
Pros

- Full CMOS process and depleted bulk
- Small pixels possible
- Now SOI CMOS available:
  - FD-SOI, OKI, LAPIS, KEK

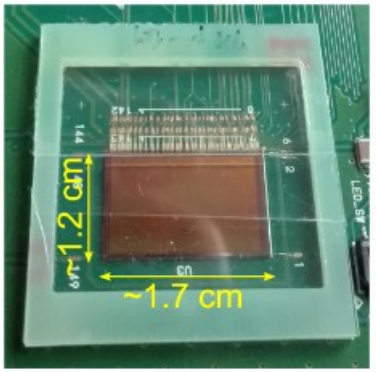
Cons

- Radiation limitation due to positive charge trapped in BOX
- Back gate effect: bulk bias affects electronics
  - Suppressed with buried p well
  - *R. Itimisha et al., 10.5170/CERN-2009-006.68*

➢ *See talk of **Y. Lu** on this workshop*



Y. Arai, KEK, PIXEL2010

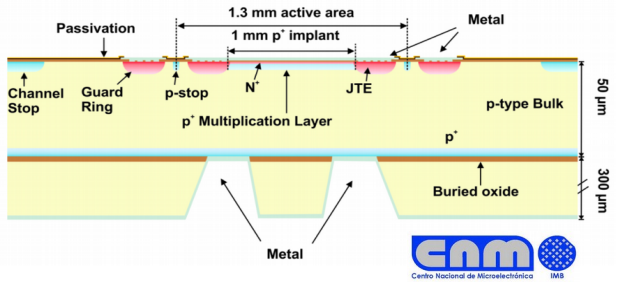


- INPTIX6, KEK/Lapis SOI CMOS technology
- Rad hardness 60krad

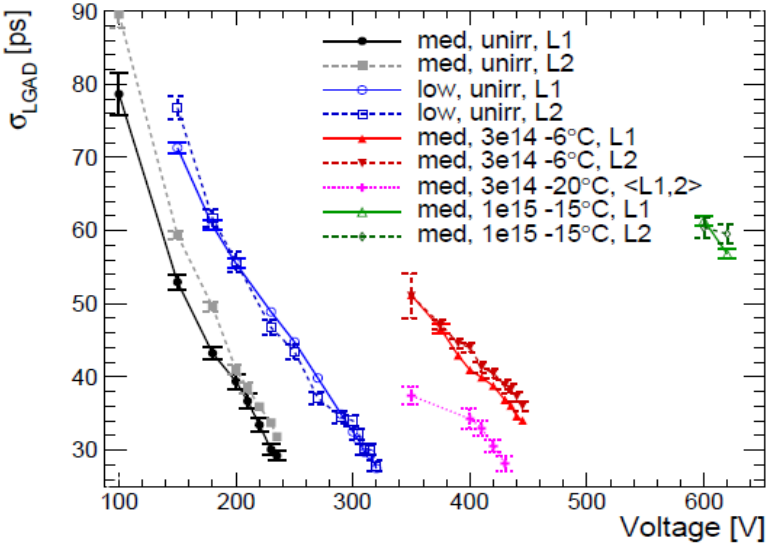
Y. Arai et al 2017 JINST 12 C01028

Other Issues: Timing

- **Timing detector for CEPC?**
  - Timing detectors being considered for HL-LHC upgrades at ATLAS & CMS
  - Performance gains in pile-up rejection impact b-tagging, jet-reconstruction, etc
    - Impact at CEPC?
- Integrated **timing on CMOS**-based technologies
  - Already achieved 100 ps resolution on 130 nm CMOS technology (NA62 GTK [1])
  - However, large pixel size and high power consumption needed for TDC/pixel
    - 300 x 300 μm^2 and 1mW/pixel
- **LGAD** technology developed at CNM (Barcelona) [2], proposed for timing [3]
- Multiplication layer increases signal slope which reduces jitter and time-walk



J. Lange et al., JINST 12 (2017) P05003



- Resolution <30 ps/layer/mip after 3E14n_{eq}/cm^2 !!
- But.. problem of small pitch LGAD sensors?
  - *E. Cavallaro et al., NIM A 796 (2015)136*

➢ *See talk of **A. Staiano** on this workshop*

[1] S. Garbolino and S. Martoiu, PRIME 2010
[2] G. Pellegrini et al., NIM A765 (2014) 12
[3] H.-W. Sadrozinski et al., arXiv: 1704.08666]

Conclusions

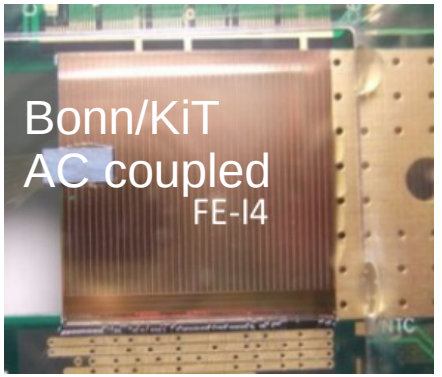
- **Pixel silicon detectors** will play a critical role in the **CEPC** experiments
- **CEPC** benefits from **synergies** with **ILC, ALICE, ATLAS, etc**
  - Already ongoing common efforts
- **Several sensor technologies** promise to satisfy pixel detector requirements
  - Radiation hardness requirements attainable
  - Challenge to fit functionality in small pixel size and moderate power consumption
- Important to keep **multiple sensor R&D lines** open
  - Avoid single failure point

Thank you

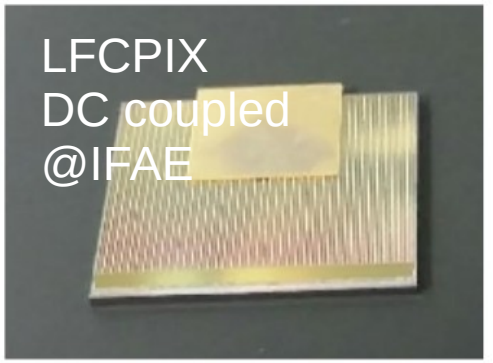
Backup Slides

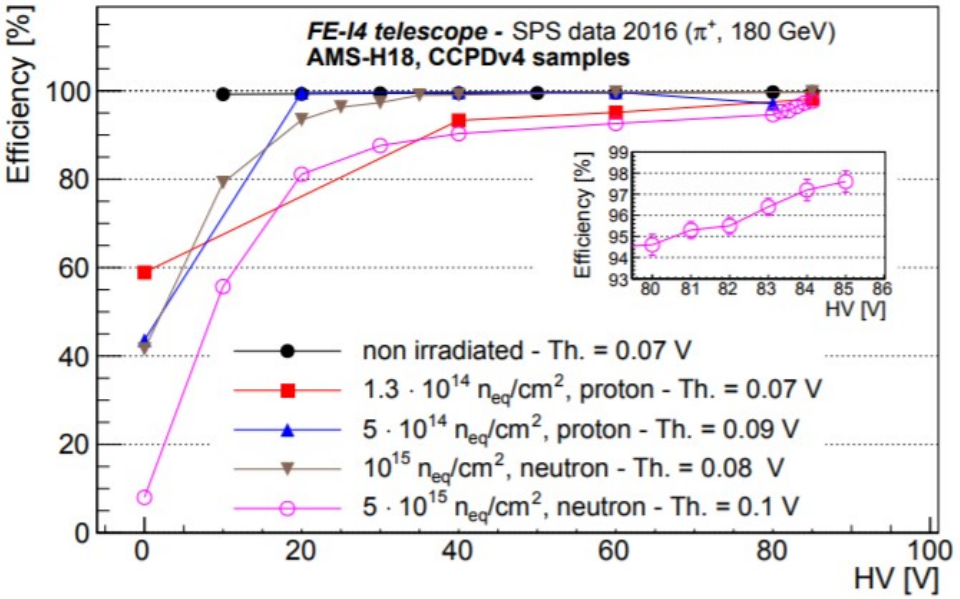
On AC Coupled CMOS Devices

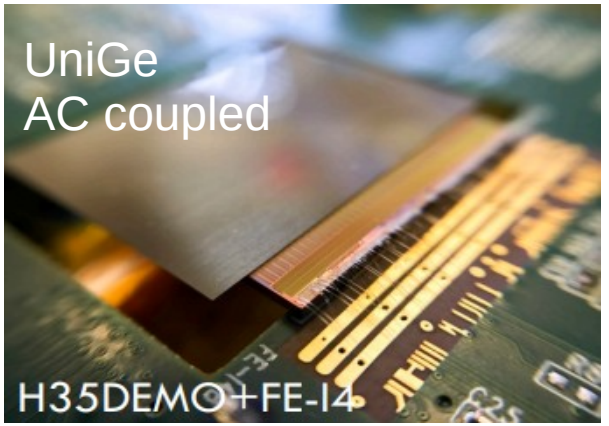
I. Peric et al., NIM A 765(2014)172



- **Initial** R&D focused on AC coupled CMOS devices
- Motivation was radiation hardness and timescale to develop fully monolithic ASIC
- However, “glueing” more challenging that expected
  - Uniformity & planarity complicated to achieve
  - No clear cost effectiveness





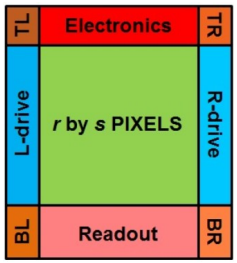


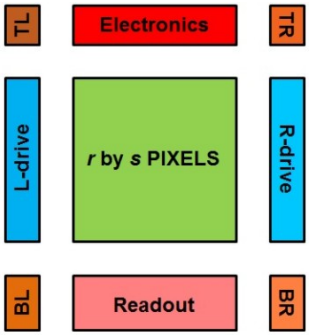
Proven radiation hardness

M. Benoit et al., arXiv:1611.02669v2

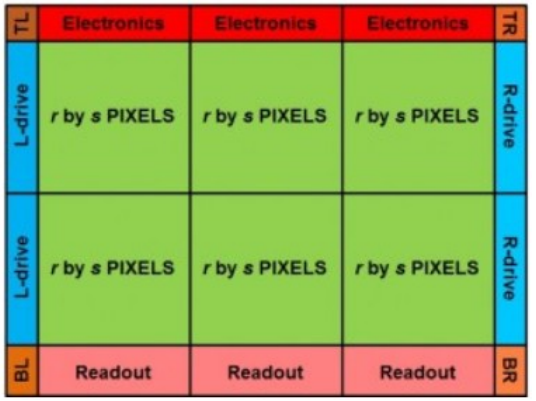
Other Issues: Large Area Coverage

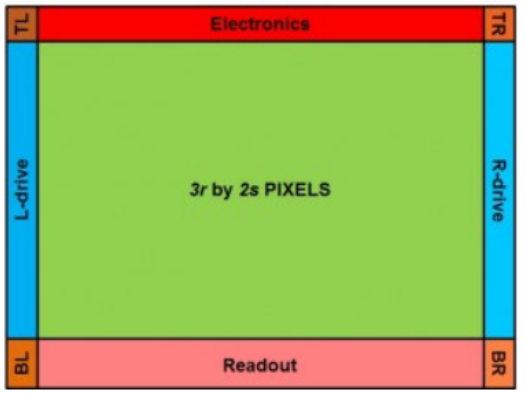
- Largest device size is currently ~2.5x2.5 cm^2
- **Butting** and **stitching** may overcome this limitation
  - Butting commonly used in HEP
  - Stitching available only on certain foundries/processes
    - Should not be an after thought…
    - Cost implications, need very good yield



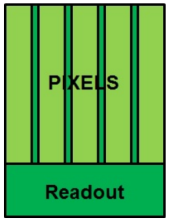


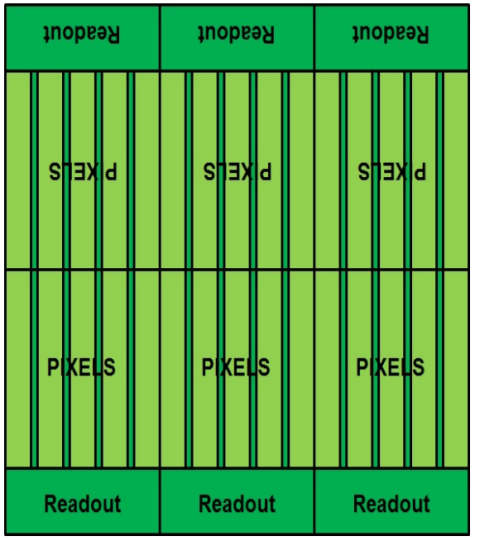
Stitching





Butting





LFoundry Development Line

Uni Bonn et al.

CCPD_LF (PROTO)

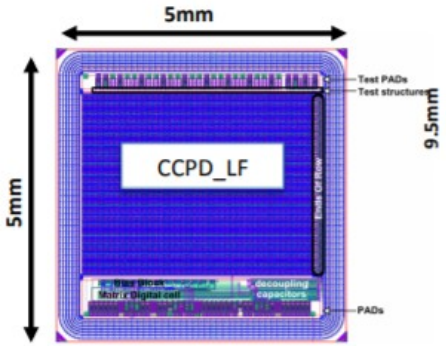
- Subm. in Sep. 2014
- 33 x 125 µm² pixels
- **Fast R/O coupled to FE-I4**
- Standalone R/O for test
- ***(Almost) Fully characterized***

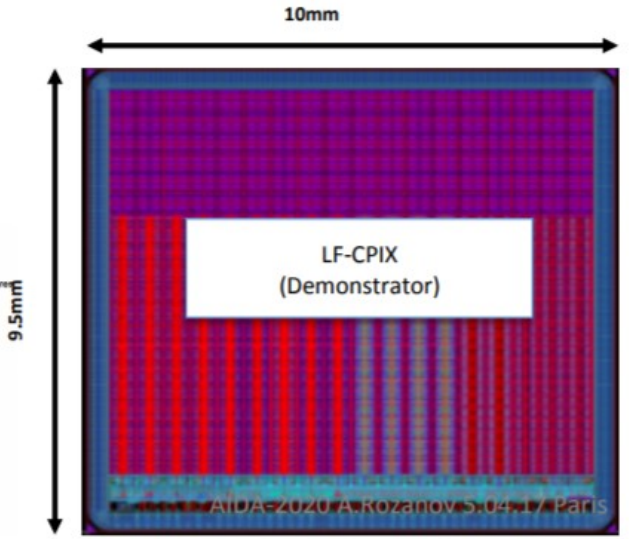
LF-CPIX (DEMO)

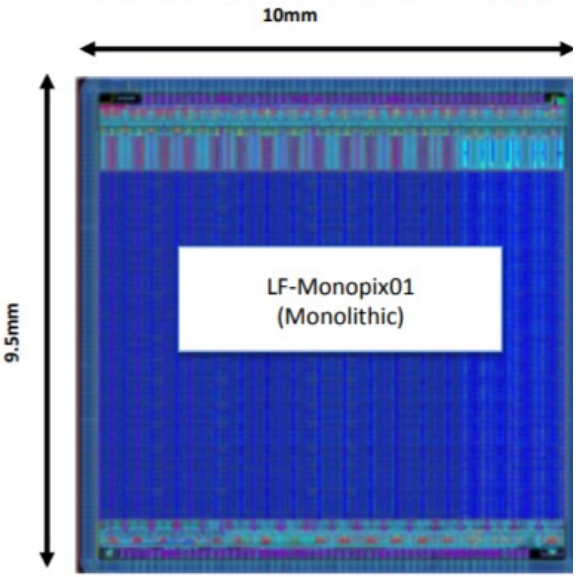
- Subm. in Mar. 2016
- ***CPIX demonstrator in LF***
- 50 x 250 µm² pixels
- 34 col of 168 pixels
- **Fast R/O coupled to FE-I4**
- Standalone R/O for test
- ***Many meas. available***

LF-Monopix01 (monolithic)

- Subm. in Aug. 2016
- "Demonstrator size"
- 50 x 250 µm² pixels
- 142x36 pixel matrix
- ***Fast standalone R/O***
- Standalone R/O like LF-CPIX
- **Just started measurements**







A. Rozanov AIDA 2020 meeting Paris 2017.