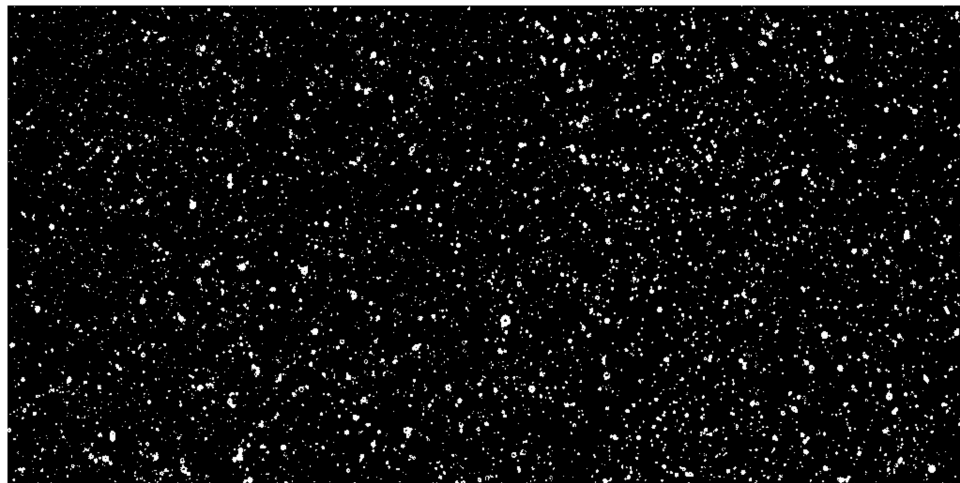
IHEP, Beijing, November 7th, 2017

The ALPIDE CMOS Pixel Sensor development for the ALICE ITS upgrade and further monolithic pixel developments for HEP in TJ 180nm CMOS

W. Snoeys, CERN, for the ALICE & ATLAS collaborations



p-ALPIDE3 chip: 200 MeV p at PSI

Acknowledgements

- The workshop organizers
- G. Aglieri, G. Anelli, F. Anghinolfi, P. Aspell, R. Ballabriga, S. Bonacini, M. Campbell, J. Christiansen, R. De Oliveira, F. Faccio, P. Farthouat, E. Heijne, P. Jarron, J. Kaplon, K. Kloukinas, A. Kluge, T. Kugathashan, X. Llopart, A. Marchioro, S. Michelis, P. Moreira, K. Wyllie, L. Musa, P. Riedler, M. Mager, M. Keil, D. Kim, A. Dorokhov, A. Collu, C. Gao, P. Yang, X. Sun, H. Hillemanns, S. Hristozkov, A. Junique, M. Kofarago, M. Keil, A. Lattuca, M. Lupi, C. Marin Tobon, D. Marras, M. Mager, P. Martinengo, G. Mazza, H. Mugnier, L. Musa, H. Pernegger, H. Pham, J. Rousset, F. Reidt, P. Riedler, J. Van Hoorne, P. Yang, D. Gajanana, A. Sharma[a], B. Blochet[a], C. Sbarra, C. Solans Sanchez, C. Riegel, C. Buttar, D. Michael Schaefer, D. Maneuski, I. Berdalovic, K. Moustakas, M. Dalla, N. Wermes, N. Egidos Plaja, R. Bates, R. Cardella, T. Wang, T. Hemperek, W. Wong, G. Iacobucci, M. Barbero, P. Pangaud, A. Habib, S. Bhat …

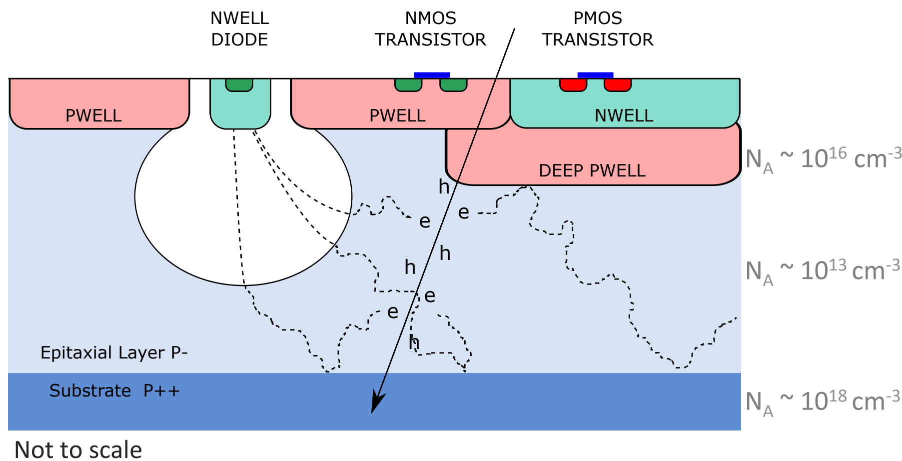
and other collegues from CERN and the ALICE ITS upgrade and ATLAS ITk

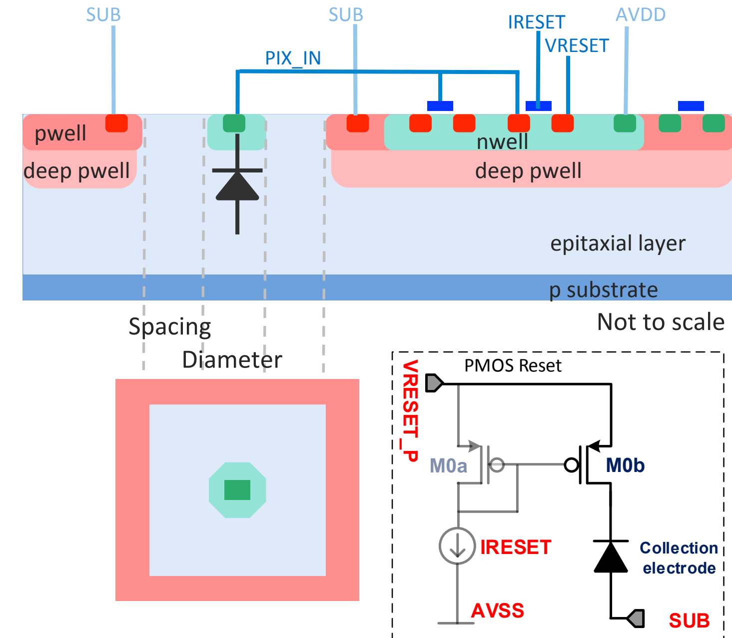
Outline

- The ALPIDE development for the ALICE ITS upgrade
- Process modification for full depletion of the sensor volume and improved radiation tolerance and timing
- The ATLAS CMOS development using this process for the outer pixel layer
- Outlook and further perspectives

Standard Pixel Sensor imaging Process (TowerJazz)

CMOS 180nm
3 nm thin gate oxide, 6 metal layers





- High-resistivity (> 1kΩ cm) p-type epitaxial layer (18 μm to 30 μm) on p-type substrate
- Deep PWELL shielding NWELL allowing PMOS transistors (full CMOS within active area)
- Small n-well diode (2 μm diameter), ~100 times smaller than pixel => low capacitance (2fF) => large S/N
- Reverse bias can be applied to the substrate to increase the depletion volume around the NWELL collection diode and further reduce sensor capacitance for better analog performance at lower power

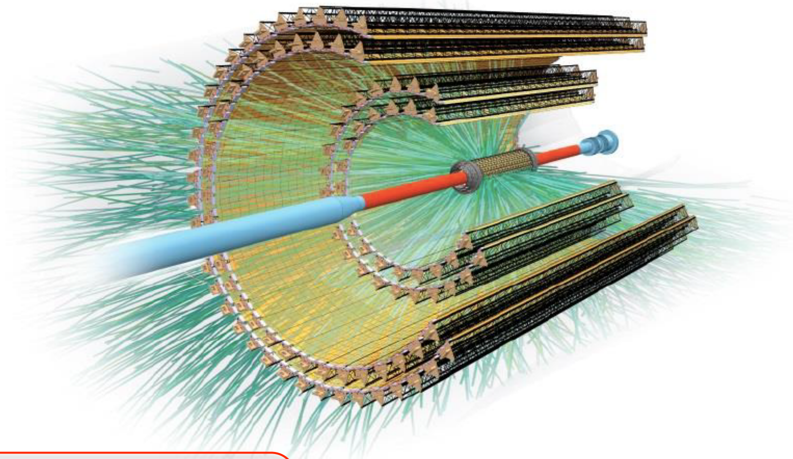
The ALICE Inner Tracking System Upgrade

Replace the inner tracking system with an entirely new detector in 2019-2020

Objectives

1. Improve impact parameter resolution by a factor ~3
   - Get closer to IP (radius of first layer): 39 mm -> 23 mm
   - Reduce pixel size: currently 50 μm x 425 μm -> O(30 μm x 30 μm)
   - Reduce x/X_0/layer from ~1.14% -> ~0.3% (inner layers)
2. Better tracking efficiency and p_T resolution at low p_T
   - Finer granularity: from 6 to 7 layers and all layers with pixels
3. Faster readout
   - Readout Pb-Pb interactions at 100 kHz
   - Readout pp interactions at >200 kHz
4. Design for fast removal and insertion
   - Maintenance during yearly shutdown

Technical Design Report for the Upgrade of the ALICE Inner Tracking System
J. Phys. G 41 (2014) 087002
CERN-LHCC-2013-024 ; ALICE-TDR-017



Thin sensors (50 μm), high granularity (~30 x 30 μm^2), large area (10 m^2)
moderate radiation (TID 2.7 Mrad & NIEL 1.7 10^{13} 1 MeV n_{eq}/cm^2

→ Monolithic Active Pixel Sensors

General requirements for the sensor chip

Parameter	Inner Barrel	Outer Barrel
Chip size (mm x mm)	15 x 30	
Chip thickness (μm)	50	100
Spatial resolution (μm)	5	10 (5)
Detection efficiency	> 99%	
Fake hit rate	< 10^{-5} evt^{-1} $pixel^{-1}$ (ALPIDE << 10^{-5})	
Integration time (μs)	< 30 (< 10)	
Power density (mW/cm^2)	< 300 (~35)	< 100 (~20)
TID radiation hardness (krad) (**)	2700	100
NIEL radiation hardness (1 MeV n_{eq}/cm^2) (**)	1.7×10^{13}	1.7×10^{12}
Readout rate, Pb-Pb interactions (kHz)	100	
Hit Density, Pb-Pb interactions (cm^{-2})	18.6	2.8

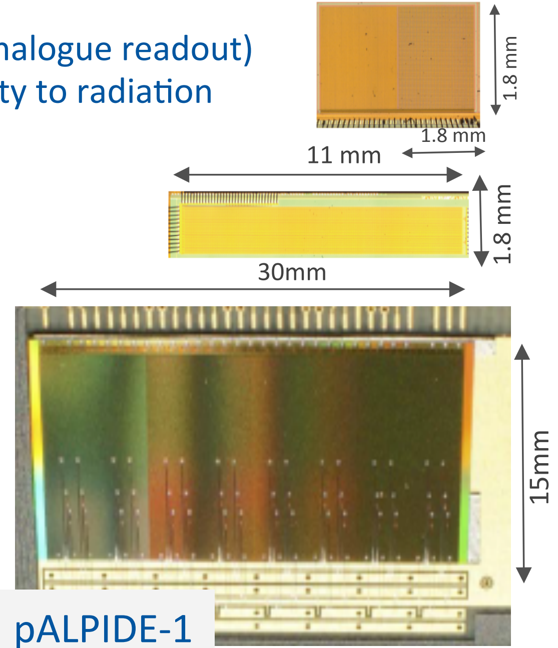
(*) In color: ALPIDE performance figure where above requirements

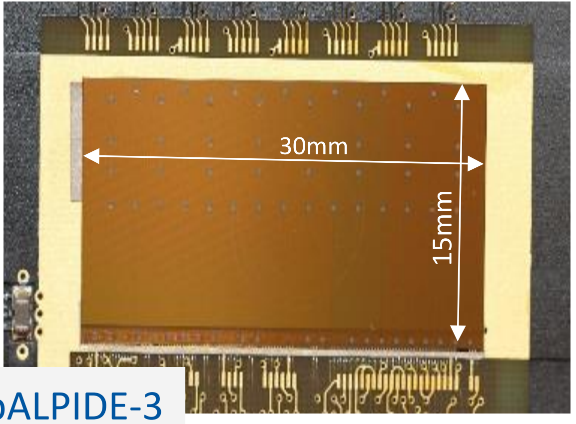
(**) 10x radiation load integrated over approved program (~ 6 years of operation)

ALPIDE Development

Design team: G. Aglieri, C. Cavicchioli, Y. Degerli, C. Flouzat, D. Gajanana, C. Gao, F. Guilloux, S. Hristozkov, D. Kim, T. Kugathasan, A. Lattuca, S. Lee, M. Lupi, D. Marras, C.A. Marin Tobon, G. Mazza, H. Mugnier, J. Rousset, G. Usai, A. Dorokhov, H. Pham, P. Yang, W. Snoeys
(Institutes: CERN, INFN, CCNU, YONSEI, NIKHEF, IRFU, IPHC) and comparable team for test

- **2012 — Explorer**
  - 20μm x 20μm and 30μm x 30μm pixels (analogue readout)
  - pixel geometry, starting material, sensitivity to radiation
- **2013 — pALPIDEss-0**
  - Matrix with 64 columns x 512 rows
  - 22 μm x 22 μm pixels
  - In-pixel discrimination and buffering
  - Zero suppression within pixel matrix
- **2014 — pALPIDE-1**
  - **First full-scale prototype**
  - Pixel pitch: 28 μm x 28 μm
  - 4 sectors with pixel variants
  - 1 register/pixel, no final interface
- **Apr 2015 — pALPIDE-2**
  - 4 sectors with pixel variants
  - Optimization of circuits
  - Allowing integration in ITS modules
  - No high-speed serial output
- **Oct 2015 — pALPIDE-3**
  - 8 sectors with pixels variant
  - **All Communication Features**
  - **(no ADC, no Temp Sens)**
- **Aug 2016 — ALPIDE**
  - **Single pixel variant**
  - **All features and optimization**





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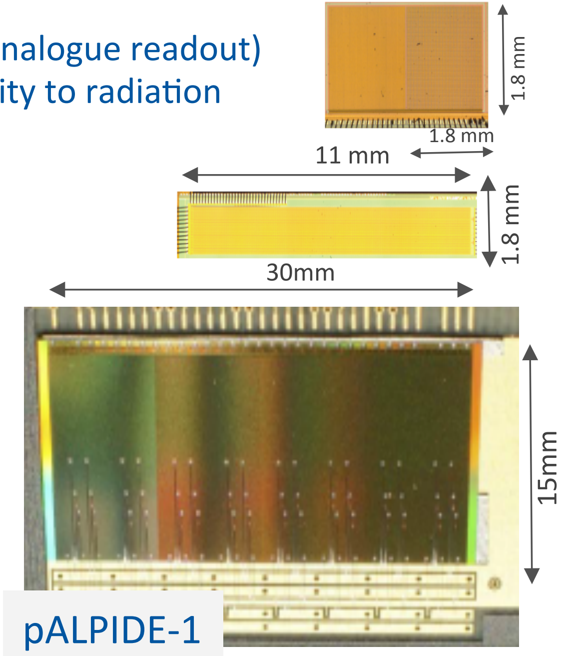
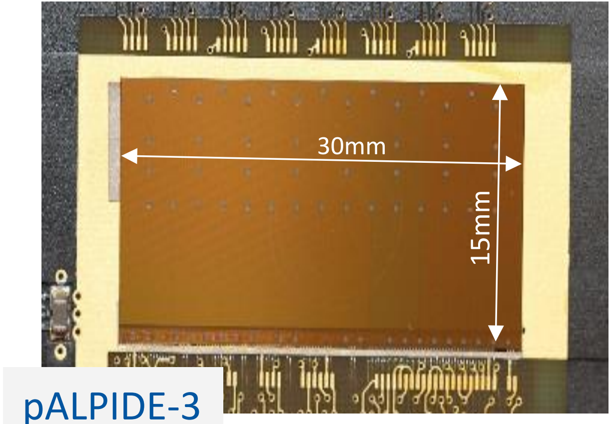




ALPIDE Architecture

1024 pixel columns

512 rows

Readout (zero suppression)

Readout (zero suppression)

Readout (zero suppression)

Readout (zero suppression)

Bias, Readout, Control

AMP

COMP

THR

In pixel:

Amplification

Discrimination

3 hit storage registers (MEB)

29 μm x 27 μm pixel pitch

Continuously active front-end

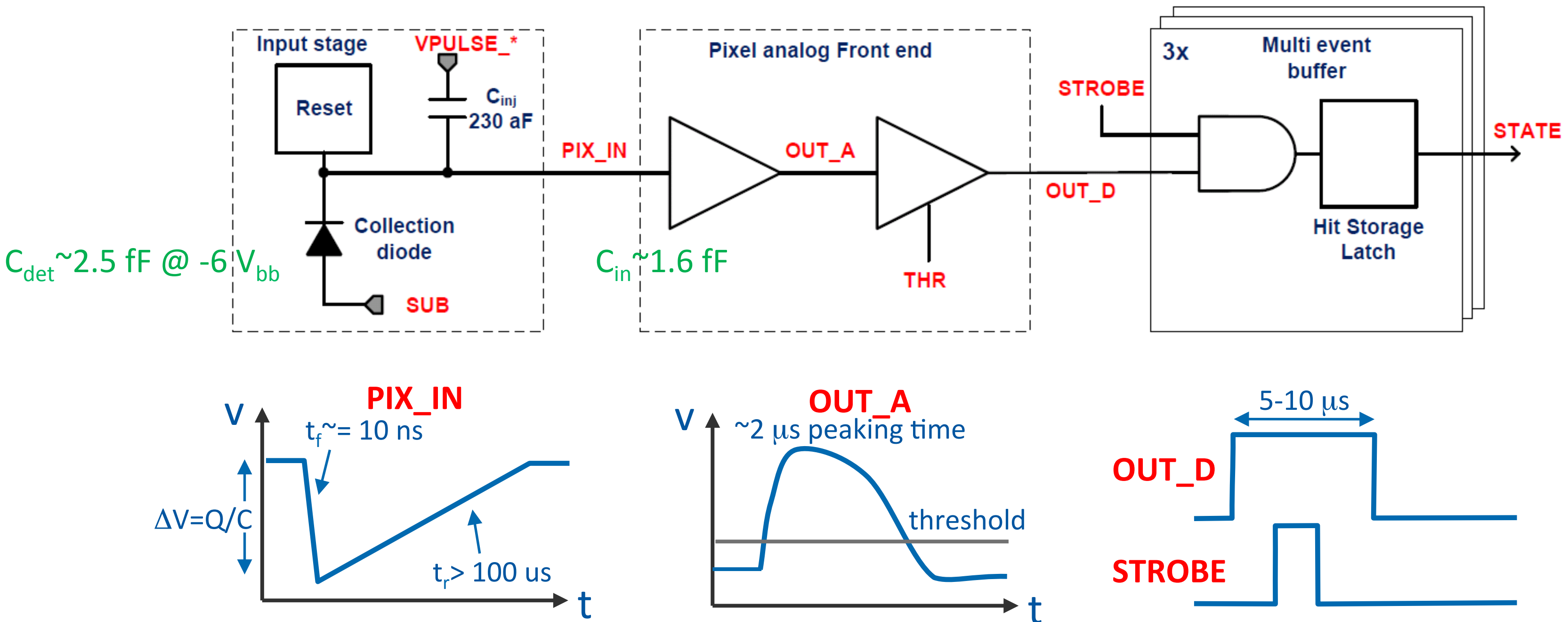
Global shutter

Zero-suppressed matrix readout

Triggered or continuous readout modes

No free running clock over the matrix

Pixel



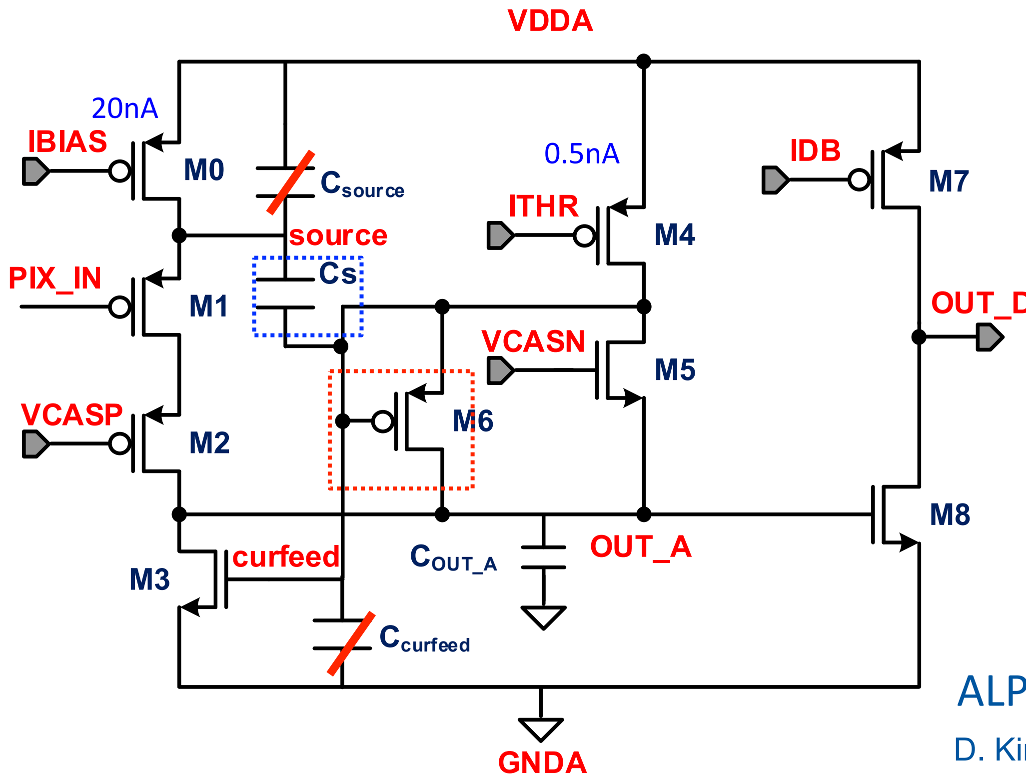
Analog front-end and discriminator continuously active

- Non-linear and operating in weak inversion. Ultra-low power: 40 nW/pixel
- The front-end acts as analogue delay line
- Test pulse charge injection circuitry
- Global threshold for discrimination -> binary pulse OUT_D

Digital pixel circuitry with three hit storage registers (multi event buffer)

- Global shutter (STROBE) latches the discriminated hits in next available register
- In-Pixel *masking* logic

Front end



Analog power ~ $(Q/C)^{-2}$ *

Q/C ~ 50 mV in ALPIDE

Conventional 300 μm thick strip detector: Q/C = 4fC/20pF = 0.2mV

*NIM A 731 (2013) 125

ALPIDE front end

D. Kim et al. –TWEPP 2015
DOI 10.1088/1748-0221/11/02/C02042

- Also used with increased current for ATLAS development

ALPIDE Layout features

Pixel layout

Matrix (detail)

Priority encoder

Collection Diode

Priority encoder

Front End

Digital Pixel Section

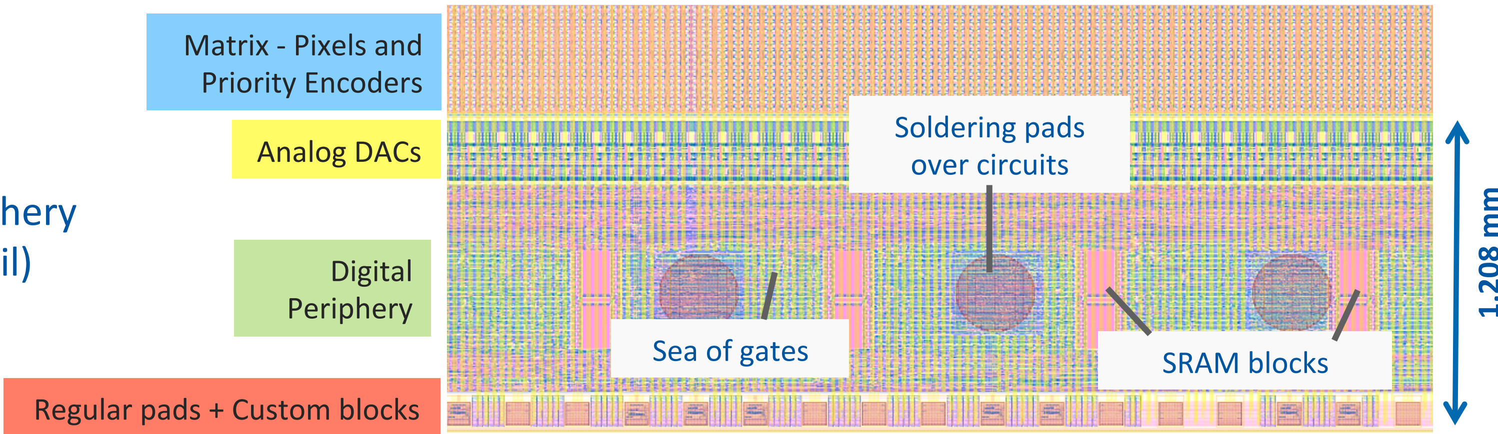
26.88 µm

9.66µm

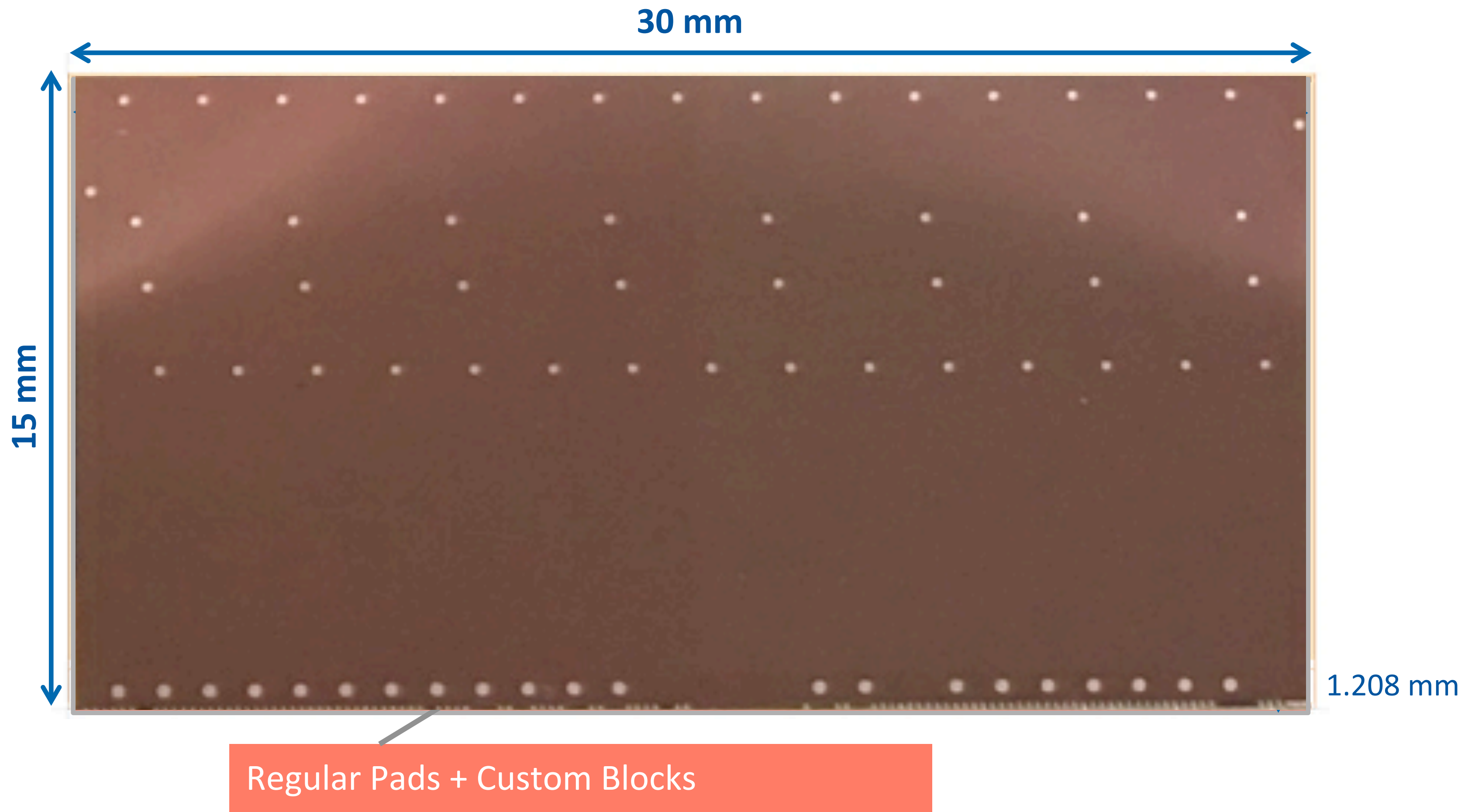
19.58 µm

29.24 µm

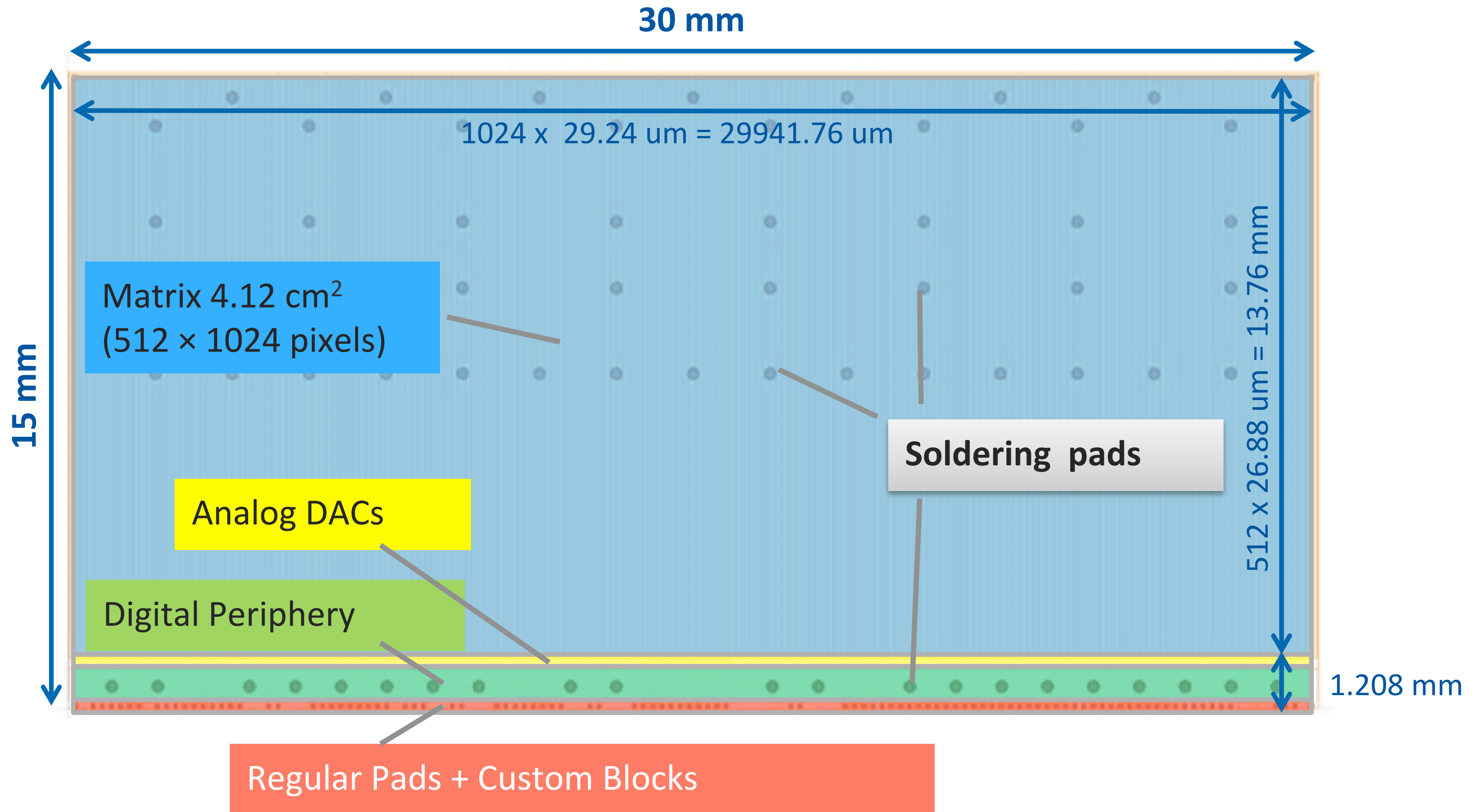
Periphery (detail)



ALPIDE Floorplan



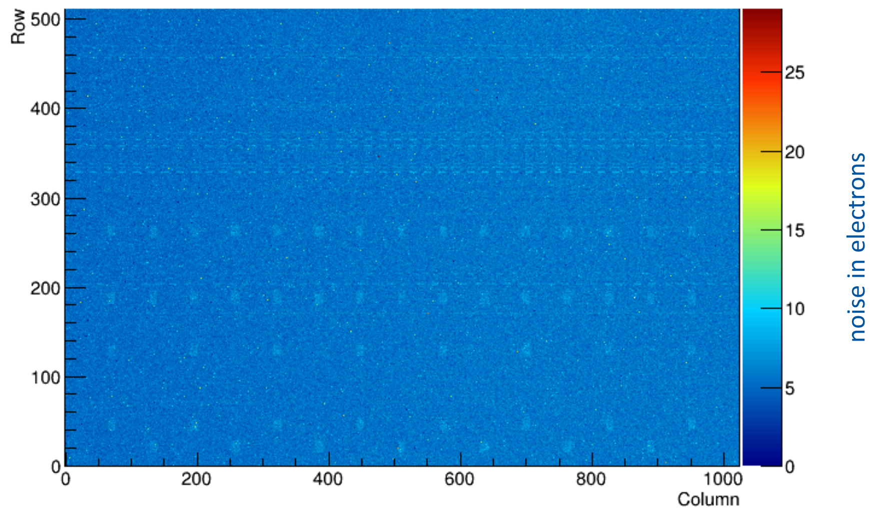
ALPIDE Floorplan

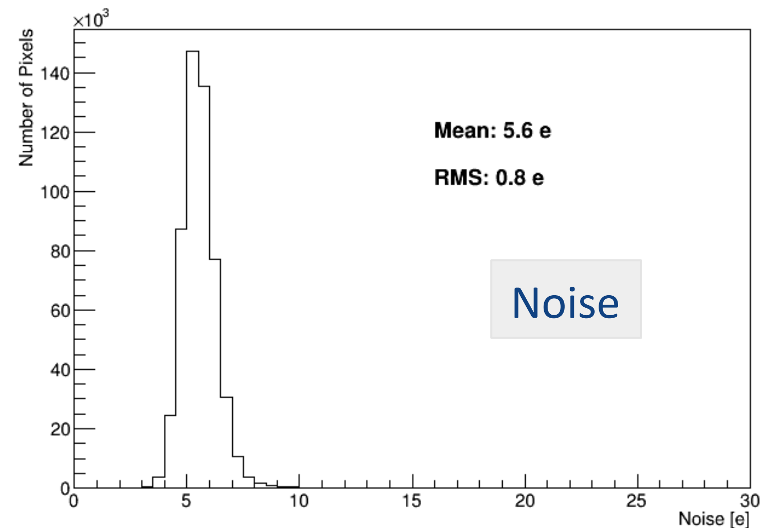


ALPIDE – Some Results

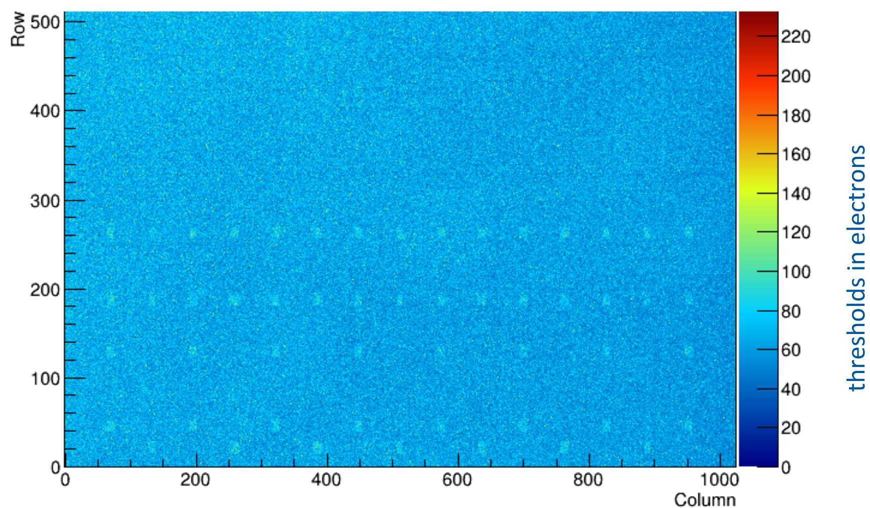
Charge threshold and Noise

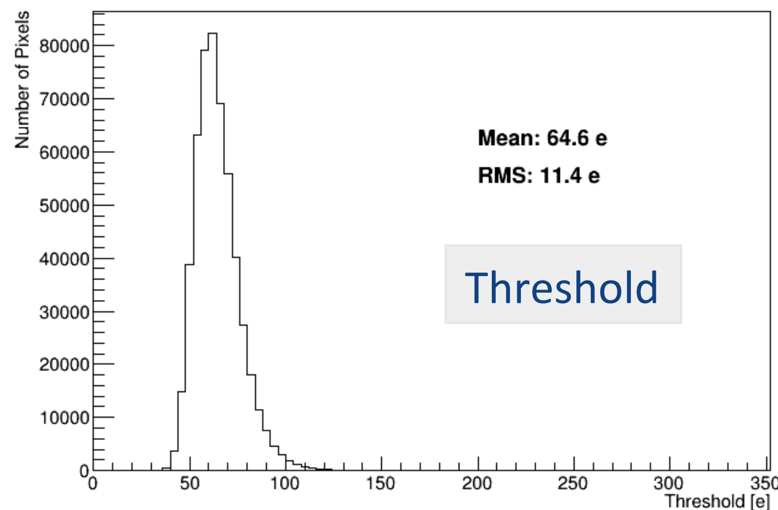
Noise Map





Threshold MAP





Detection Efficiency and Fake Hit Rate

Detection Efficiency (%)

Fake-Hit Rate/Pixel/Event

Threshold (e^-)

NIEL/TID

V_{BB}=-3V

10x lifetime NIEL

non-irradiated

Sensitivity Limit

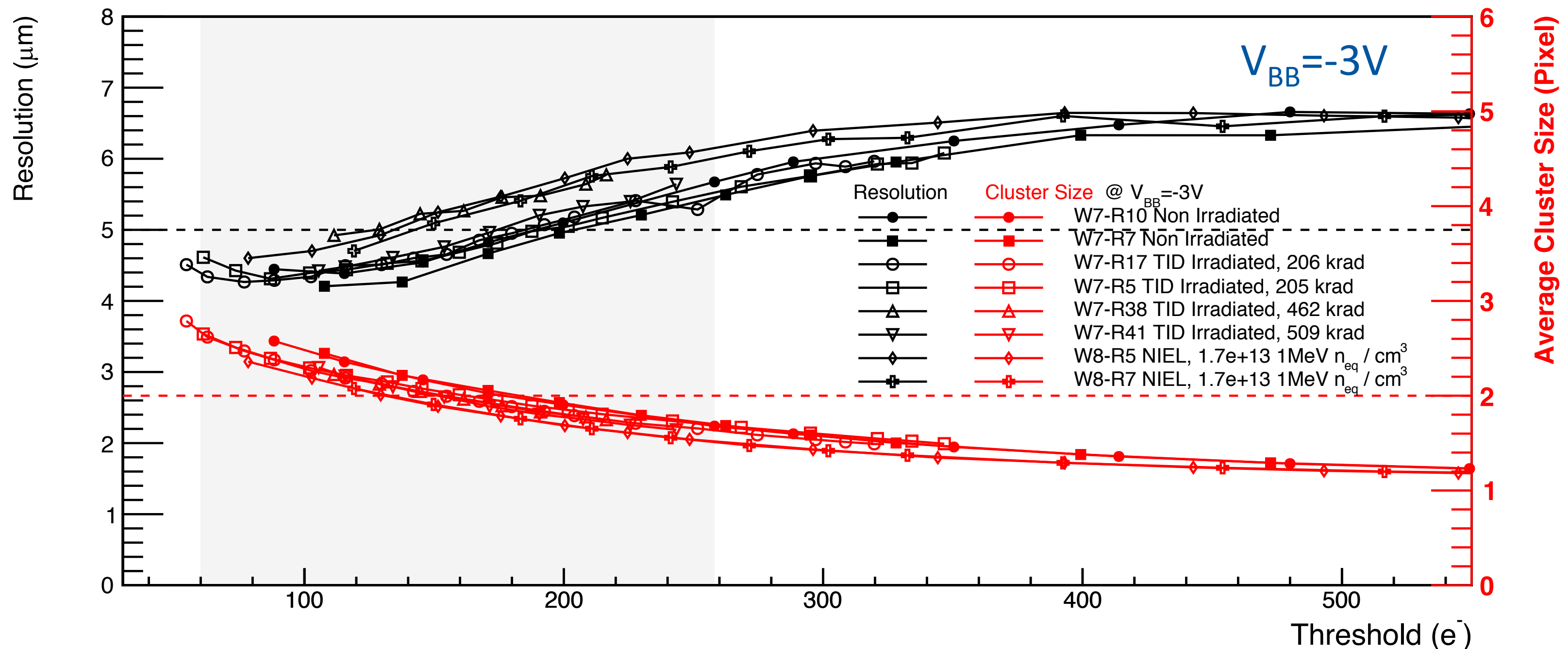
10 Pixels masked

Efficiency | Fake-hit Rate @ V_{BB}=-3V

- W7-R10 Non Irradiated
- W7-R7 Non Irradiated
- W7-R17 TID Irradiated, 206 krad
- W7-R5 TID Irradiated, 205 krad
- W7-R38 TID Irradiated, 462 krad
- W7-R41 TID Irradiated, 509 krad
- W8-R5 NIEL, 1.7e+13 1MeV n_{eq} / cm^3
- W8-R7 NIEL, 1.7e+13 1MeV n_{eq} / cm^3

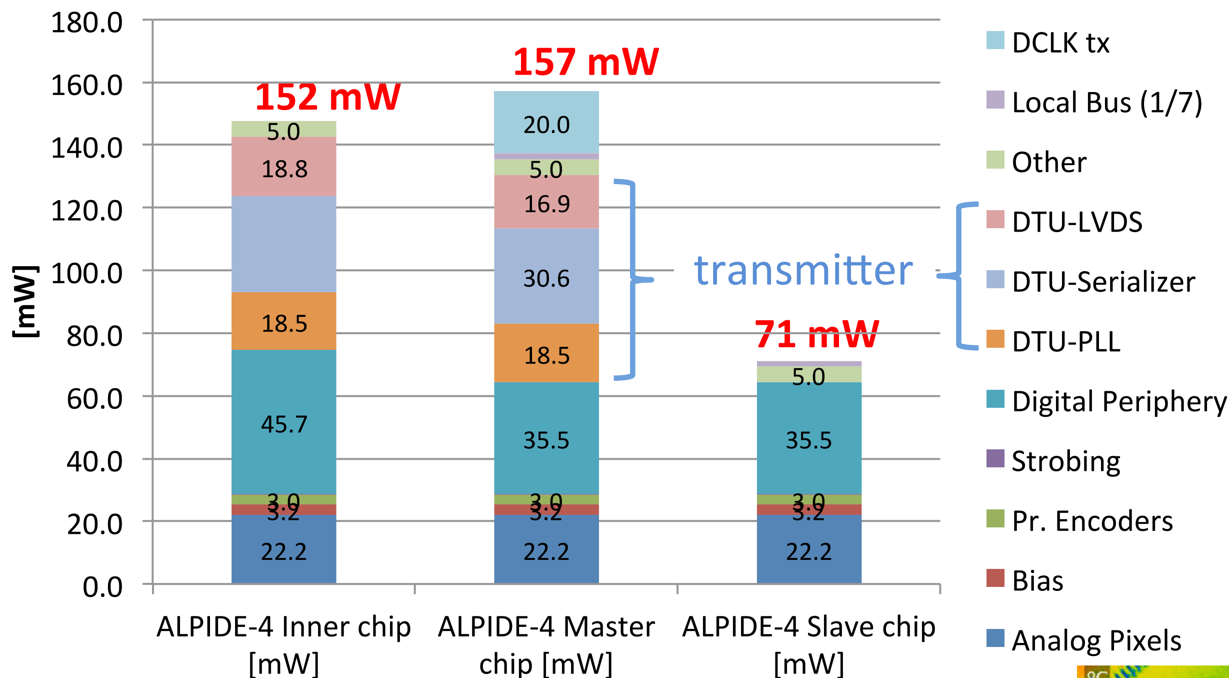
- Large operational margin with only 10 masked pixels (0.002%)
- Chip-to-chip fluctuations negligible
- Non-irradiated and NIEL/TID chips show similar performance
- Sufficient operational margin after 10x lifetime NIEL dose

Position resolution and cluster size



- Chip-to-chip fluctuations negligible
- Non-irradiated and TID/NIEL chips show similar performance
- Resolution of about 6μm at a threshold of 300 electrons
- Sufficient operational margin even after 10x lifetime NIEL dose

ALPIDE Power consumption



Sensitive area: 4.12 cm^2

Inner Barrel: 36.9 mW/cm^2

Outer Barrel: 20.2 mW/cm^2

In the matrix:

(analog + digital)/area

(22.2 + 3.2)/4.12

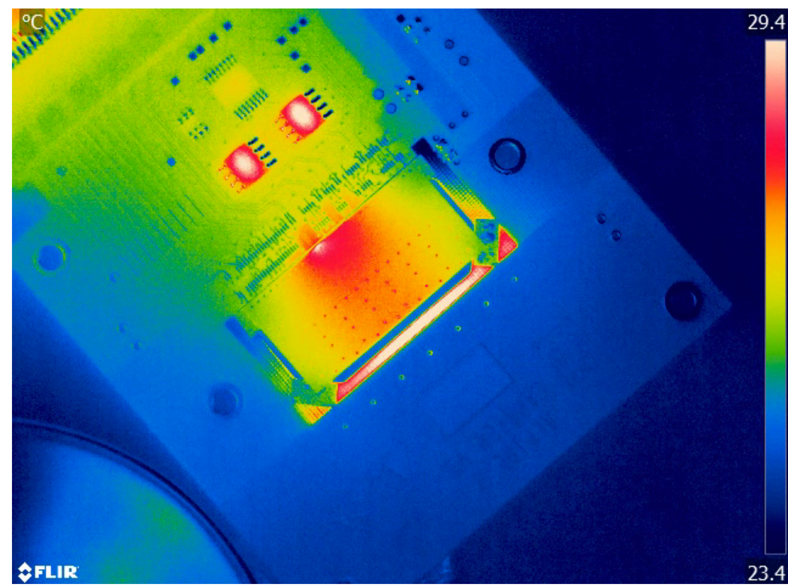
= 6.2 mW/cm^2

With 40 nW front-end and Q/C ~ 50 mV analog power consumption still dominant within the matrix

Matrix readout only active if hit present

Clock gating in the digital periphery

For the future more work needed on Q/C, architecture periphery and transmitter for overall power consumption



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ALPIDE & ITS Upgrade status

ALPIDE – production readiness review 25/11/2016

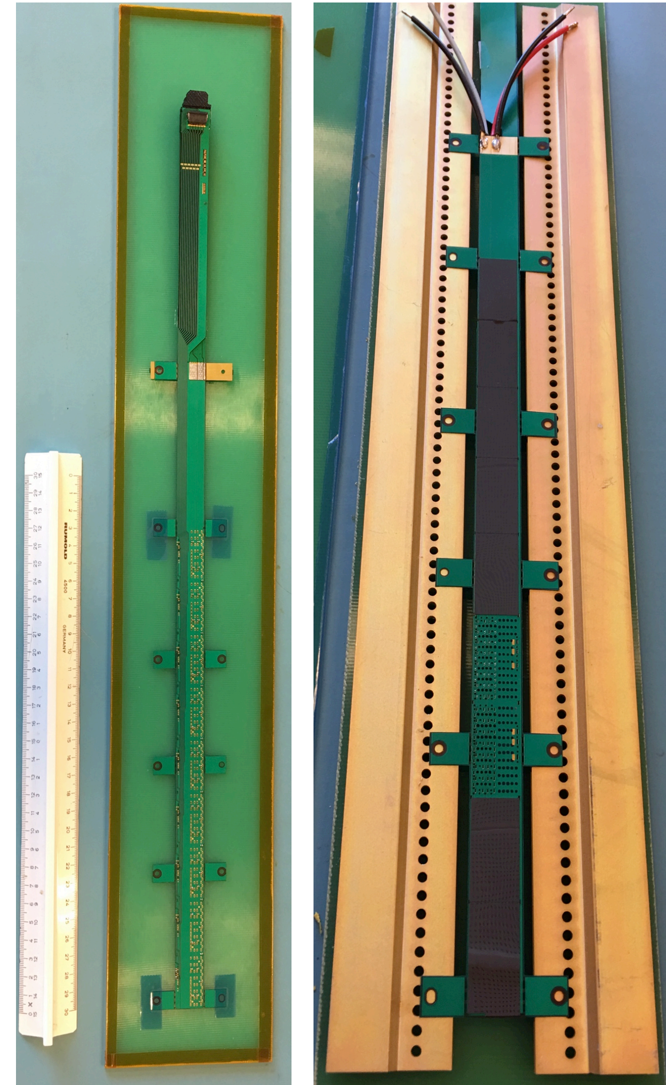
Production now launched

More than 500 wafers produced

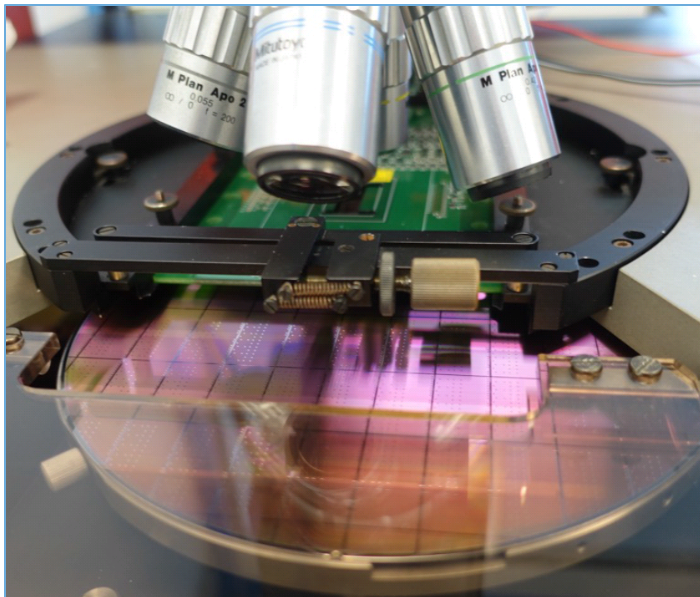
Several chip testing and module assembly centers,

including one in CCNU (Wuhan)

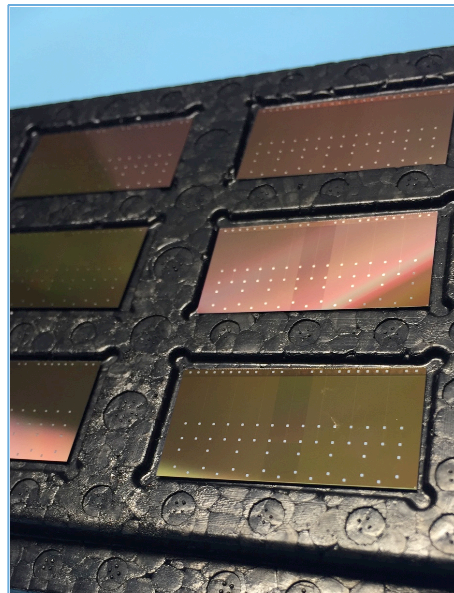
Inner Barrel Module (9 chips)



Wafer probe testing

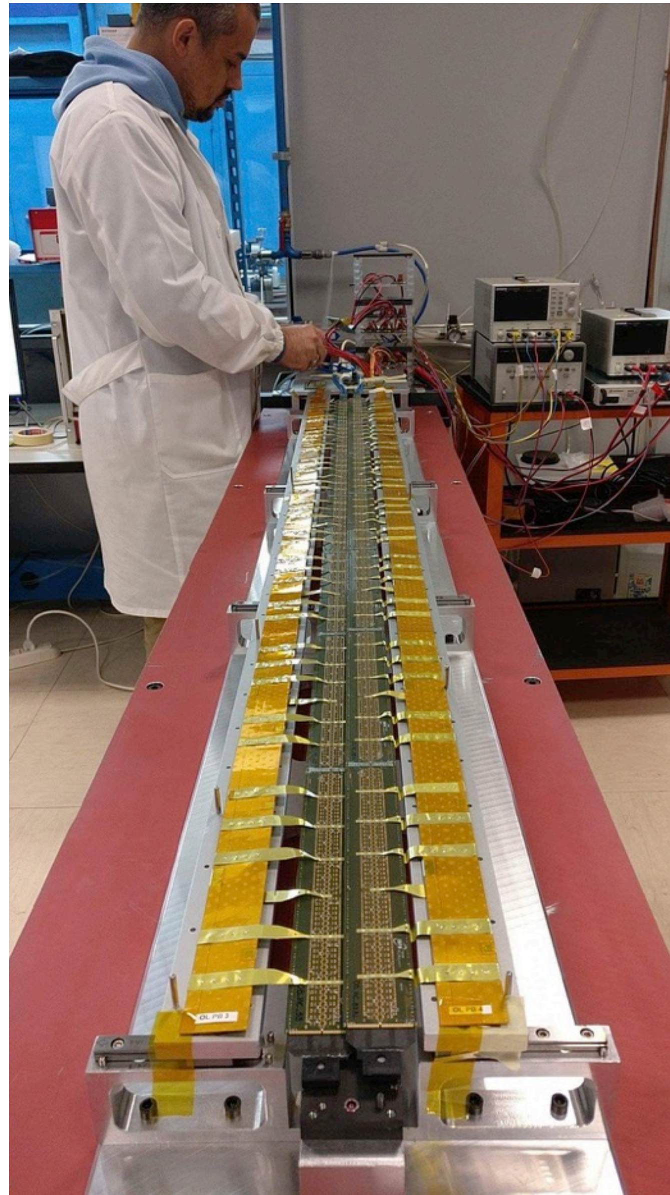


Single chips after thinning & dicing



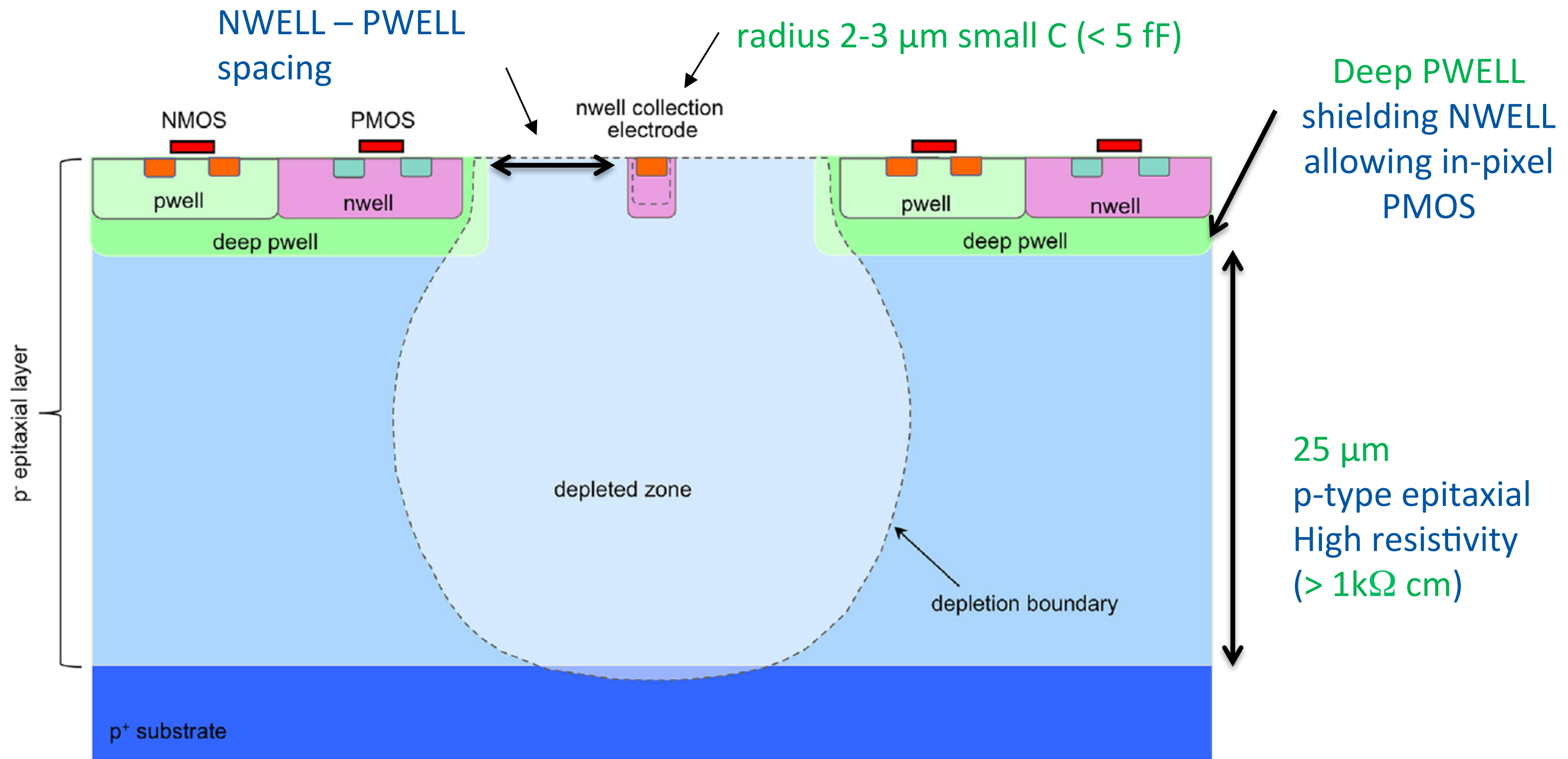
Outer barrel stave

ALICE



Standard process

- 180nm CMOS imaging sensor process
- Electronics outside the collection electrode: small electrode (low C), large circuit area, no signal coupling



- Reverse bias to increase depletion volume (-6 V, the sensor is not fully depleted)

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Modified process

- Novel modified process developed in collaboration with the foundry
- Adding a planar n-type implant significantly improves depletion under deep PWELL

NMOS
PMOS
nwell collection electrode
pwell
nwell
deep pwell
pwell
nwell
deep pwell
low dose n-type implant
p⁻ epitaxial layer
depletion boundary
depleted zone
p⁺ substrate

25 μm
p-type epitaxial
High resistivity
(> 1kΩ cm)

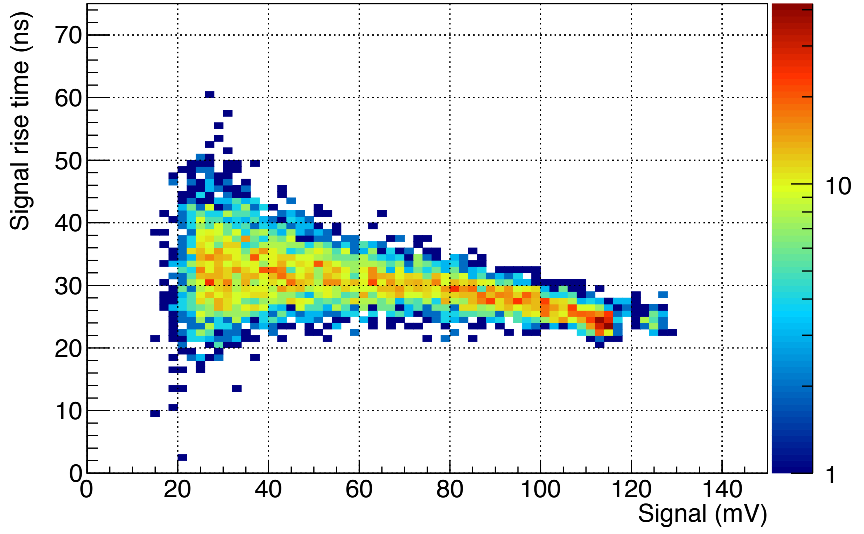
- Possibility to fully deplete sensing volume
- No significant circuit or layout changes required

W. Snoeys et al.
DOI 10.1016/j.nima.2017.07.046

^{55}Fe measurements before irradiation

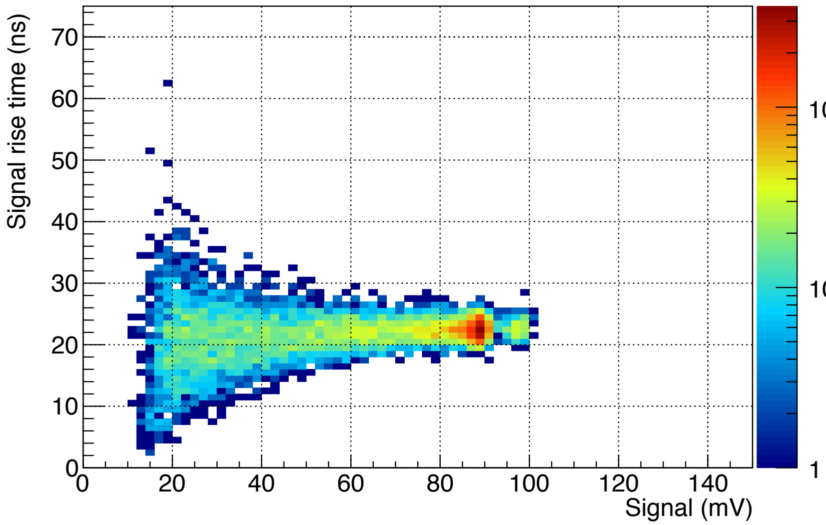
J. Van Hoorne

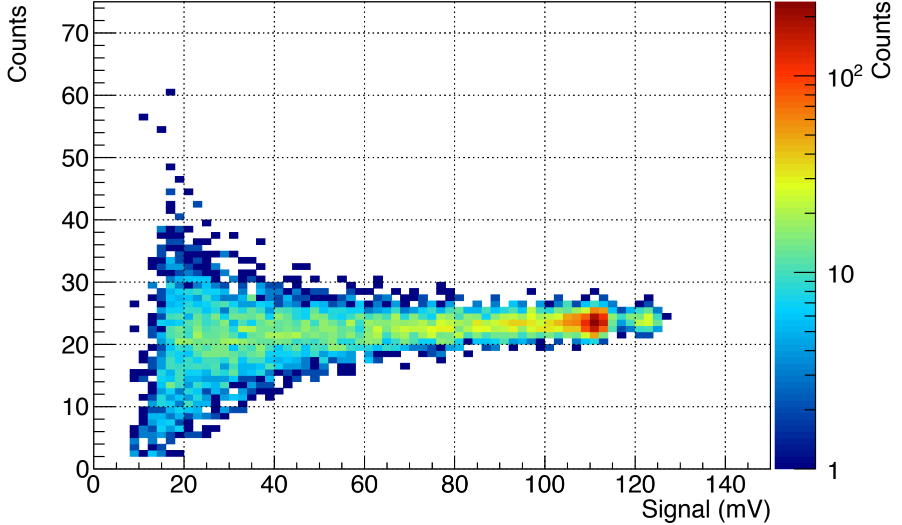
Standard process



Note: circuit contributes significantly to the signal rise time !

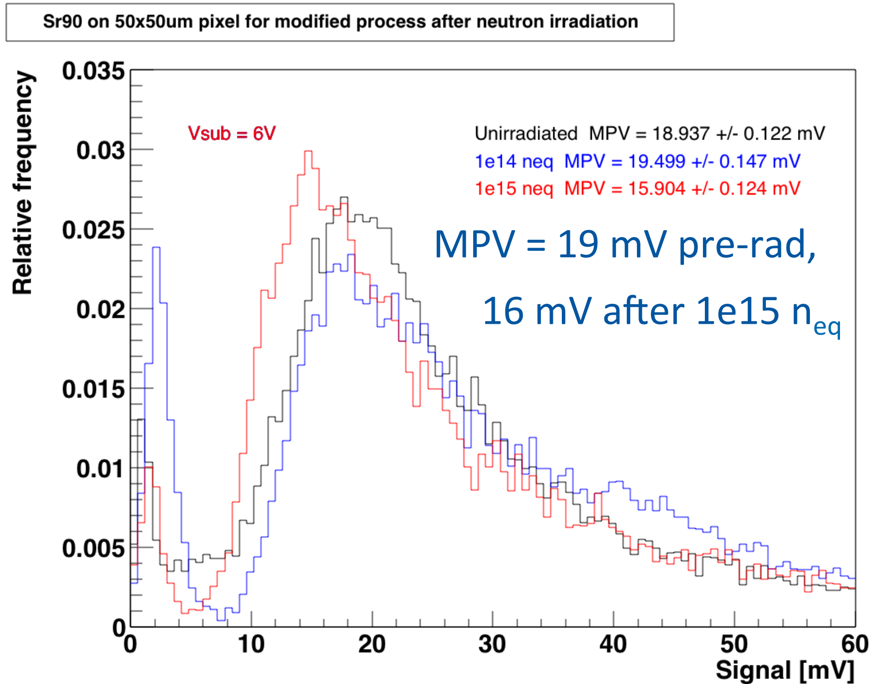
Modified process

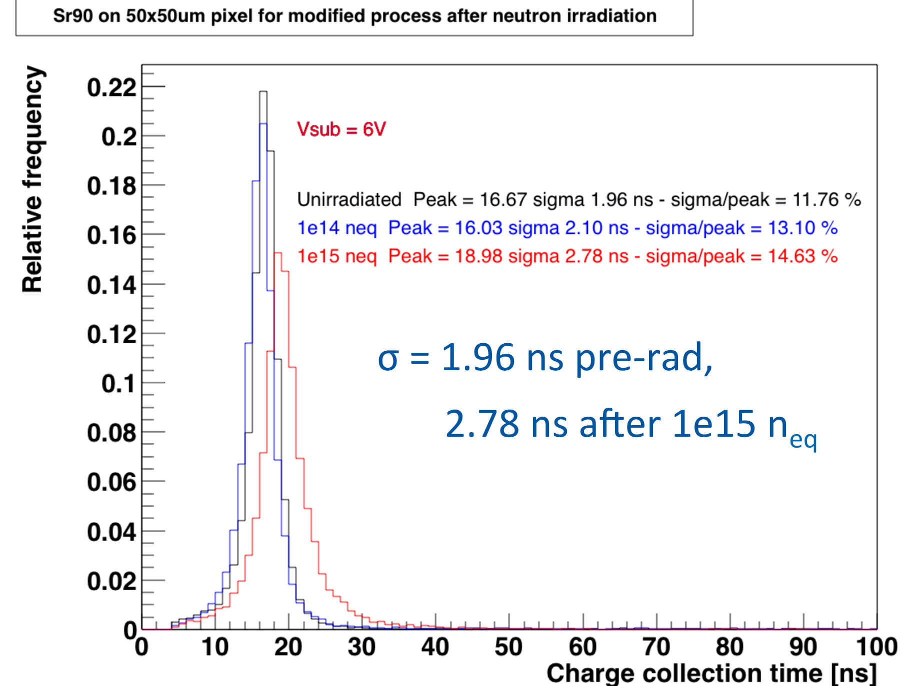




much less charge spread over different pixels and much more uniform in time response

Measurement results after irradiation





Courtesy H. Pernegger et al.

Results on detection efficiency after irradiation (1e15 n_{eq}/cm^2) also encouraging

Improvement of the radiation tolerance by at least an order of magnitude

Initiated development for the ATLAS ITK involving several groups

Monolithic pixel development for ATLAS outer pixel layer

- Large effort on many technologies
- Concentrating on depleted MAPS for radiation tolerance
- Large chips and very encouraging results become available

- 50 Mrad, 10^{15} n_{eq}/cm^2
- ~ 1 Mhits/mm^2/s
- Serial power

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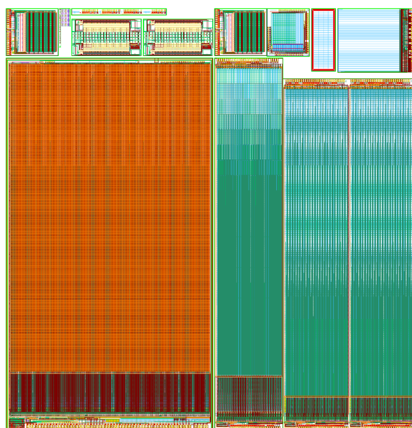
Large chips become available in several technologies

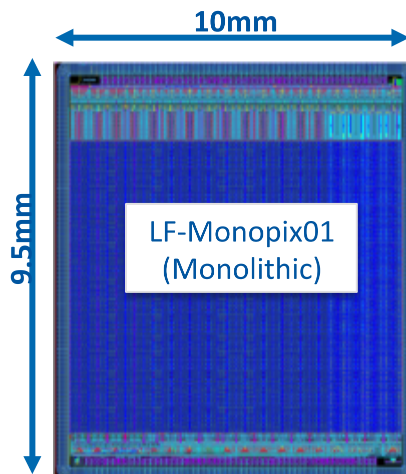
Chip name	Technology	CE Size*	Pixel size [μm²]	R/O architecture	Staust
aH18	AMS 180nm	Large	56 × 56	Asynchronous	Measurements
Malta	TowerJazz 180nm	Small	36 × 36	Asynchronous	Submitted
TJ Monopix		Small	36 × 40	Synchronous	
LF Monopix	LFoundry 150 nm	Large	50 × 250	Synchronous	Measurements
Coolpix		Large	50 × 250	Synchronous	
LF2		Large	50 × 50	Synchronous	

* CE Size = Collection Electrode Size



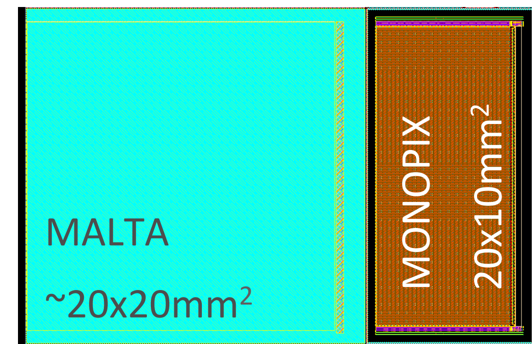
ATLAS Pix & MuPix

AMS 180 nm



MONOPIX, LF2 & COOLPIX

Lfoundry 150 nm

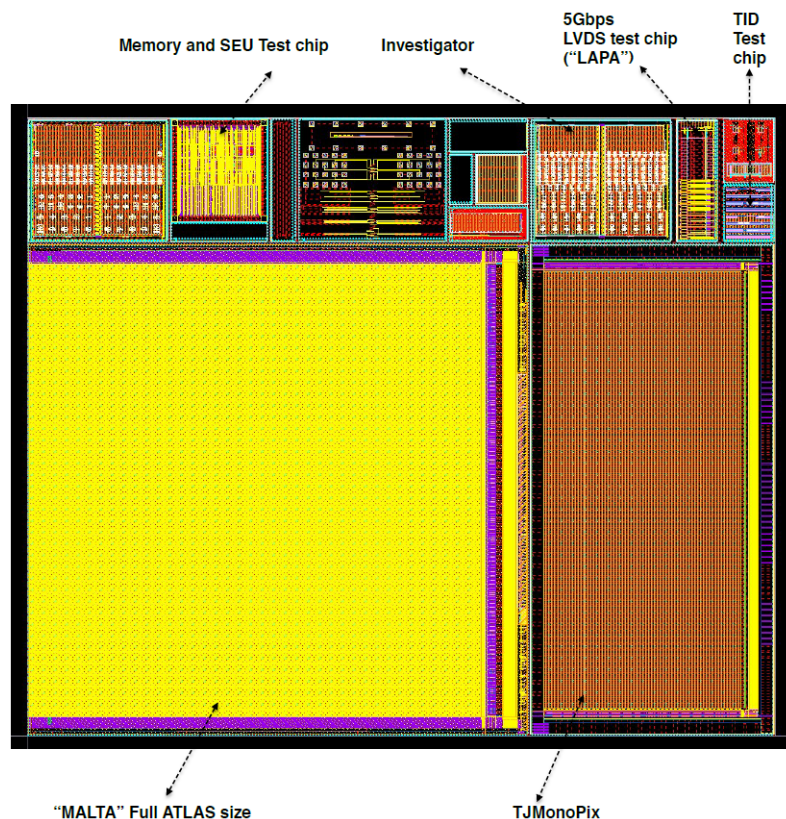


MONOPIX & MALTA

TowerJazz 180 nm

Note: MALTA= Monolithic from ALICE To ATLAS

TJ submission (back by the end of the year)



Design team for the first submission: Bonn & CERN, now expanding with interest of several other groups

(Also test chips by RAL & IPHC)

Cfr TWEPP 2017

T. Kugathasan[a], A. Sharma[a], B. Blochet[a], C. Sbarra[d], C. Solans Sanchez[a], C. A. Marin Tobon[a], C. Riegel[a], C. Buttar[c], D. Michael Schaefer[a], D. Maneuski[b], H. Pernegger[a], H. Mugnier[a], I. Berdalovic[a], J. W. Van Hoorne[a], J. Rousset [a], K. Moustakas[b], L. Musa[a], M. Dalla[d], N. Wermes[b], N. Egidos Plaja[a], P. Riedler[a], R. Bates[c], R. Cardella[a], T. Wang[b], T. Hemperek[b], W. Snoeys[a]

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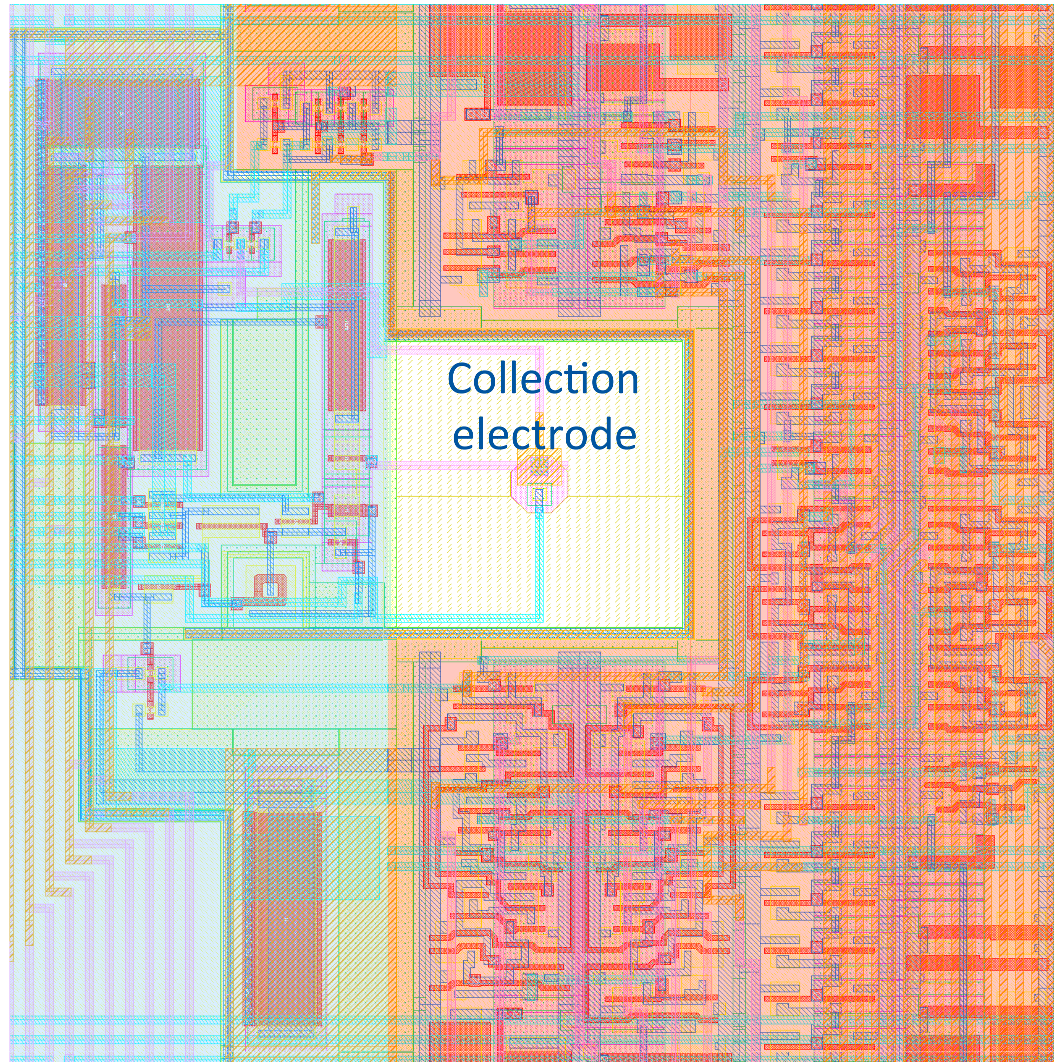
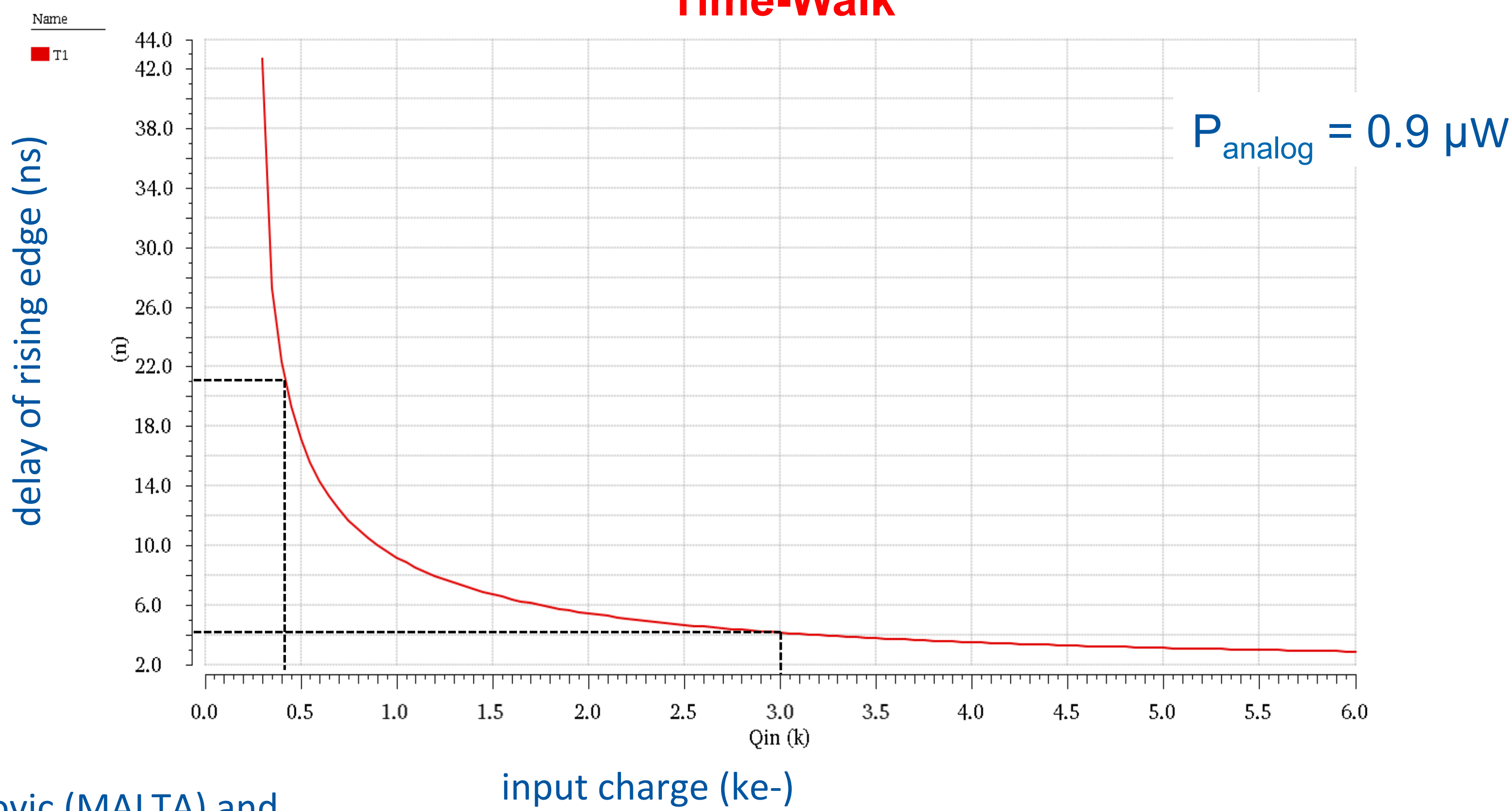
Pixel (MALTA)



Front-end simulation performance

Charge threshold Q_{th}	300 e	
Equivalent Noise Charge	7.1 e	threshold/noise > 10
Channel-to-channel RMS	10.2 e	good threshold uniformity, no need for in-pixel tuning



Ivan Berdalovic (MALTA) and
Kostas Moustakas (MONOPIX)

Synchronous vs Asynchronous: matrix power

- Assumptions: Matrix 2 cm x 2 cm
- Analog Power < 75 mW/cm^2 (36.4 µm x 36.4 µm pixel)
- Power for clock distribution (needed for synchronous design)
  - Energy per 1 cm toggled line at 1.8 V = 2 pF/cm x (1.8 V)^2 = 6.5 pJ
  - 137 lines per cm (1 per double column) for 36.4 µm pixel pitch:

    137 x 6.5 pJ x 40 MHz = 36 mW/cm^2 (in MONOPIX ~2x differential lines)

- Power for matrix readout (MALTA)

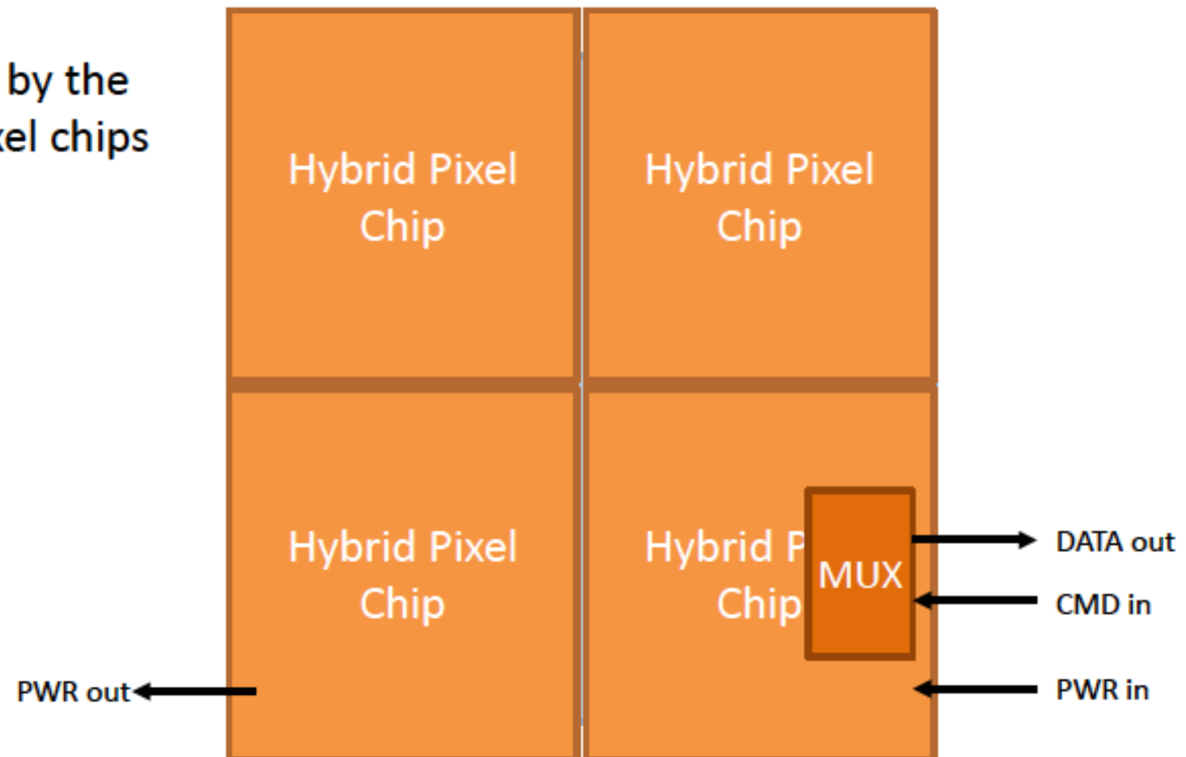
	pixel hit rate		Power/bit/cm^2 (H=2 cm)	Power (4.5 bit toggling)
Layer	hit/BC/mm^2	Mhit/mm^2/s	mW/cm^2	mW/cm^2
0	0.68	27.2	17.7	79.6
1	0.21	8.4	5.5	24.6
2	0.043	1.72	1.1	5.0
3	0.029	1.16	0.8	3.4
4	0.021	0.84	0.5	2.5

- Asynchronous much larger bandwidth

Note : need to add periphery power !!

Data Concentrator for Hybrid Pixel Modules

- Data concentrator (MUX) based on LP-GBT building blocks
- 65nm CMOS
- Serial powering supported by the shunt regulators on the pixel chips



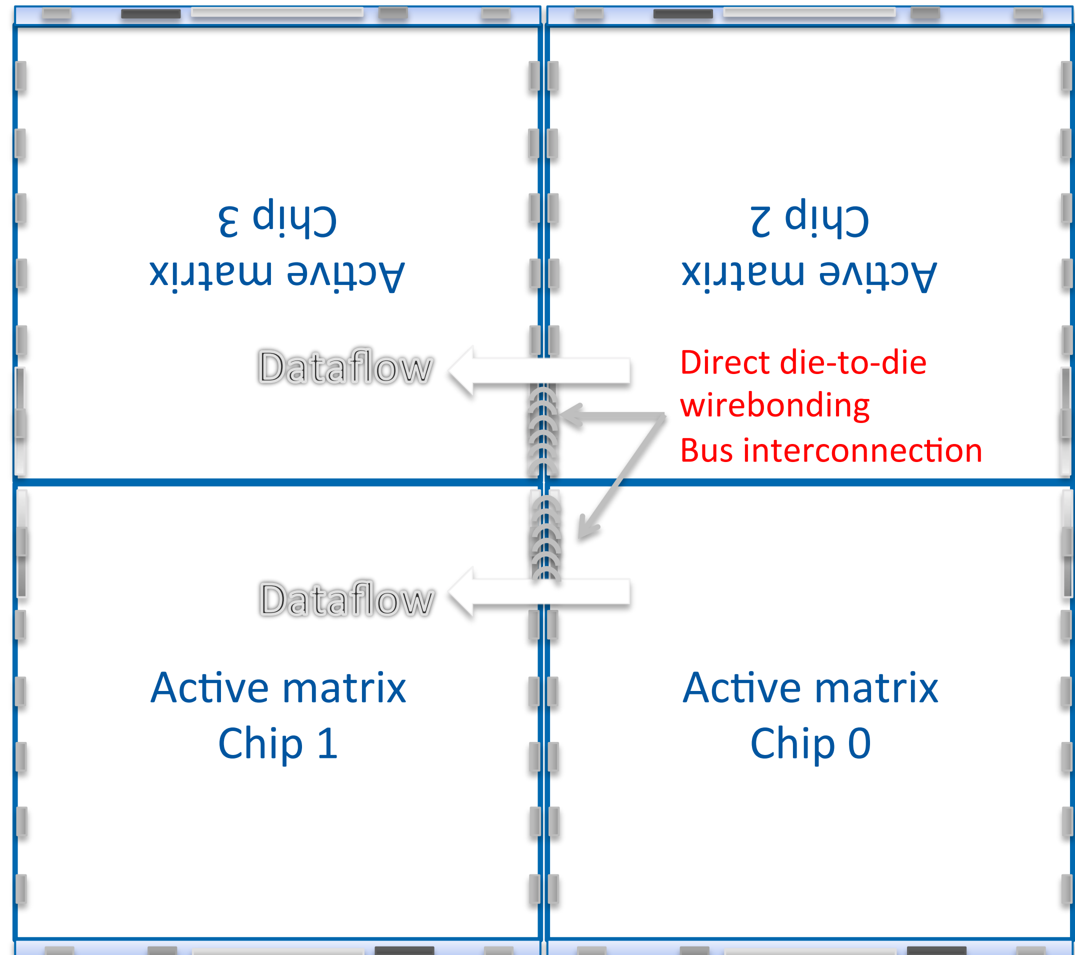
CMOS Quad Module

Important: establish path towards an ITK compatible module

4 CMOS chips chained to one CMOS Quad Module

Use direct die-to-die wirebonding to interconnect data IO between chips ->
All high speed chip signals routed in silicon (and not on flex to reduce flex mass and maintain signal integrity at high speeds)

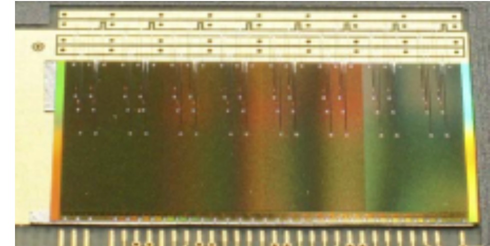
Adding aggregator chip also here guarantees compatibility with hybrid module



Summary

ALPIDE CMOS Pixel Sensor Chip for the ALICE ITS upgrade now in production

Used also for the new Muon Forward Tracker (MFT) detector in ALICE



Detection Efficiency > 99%

Fake hit rate << 10^{-5} /event/pixel

Position resolution < 5 μm

Process modification for better radiation tolerance and timing

Based on low dose blanket n-type implant

Radiation tolerance improvement by at least an order of magnitude

Maintains low capacitance

Monolithic pixel development for outer pixel layer in the ATLAS upgrade

Large prototypes and promising results become available in several technologies

Small collection electrode size offers significant advantages for the electronics design (power, speed, noise performance, in-pixel circuit complexity…)

Effort towards common design started with several groups committed and others joining
Concentrate on conceptual full module design, architecture and system issues trying fast path to full module (eg aggregator chip, same or very similar to one needed for hybrid pixels)

Outlook: R&D taking important steps in each iteration

Continued effort in the following areas:

Device optimization

low sensor capacitance for better analog performance

small collection electrode also makes more space available for readout electronics

process modification maintains low capacitance and improves timing resolution, speed and radiation hardness.

Readout architecture

ALPIDE is first CMOS sensor chip for HEP with sparsifying readout similar to hybrid pixels

ATLAS: trying to empty the matrix faster and at low power

System design

Essential to address larger areas

ALPIDE contains chip-to-chip communication for the outer barrel modules

Data transmission is crucial, continuous need for increased bandwidth, at low or acceptable power

ATLAS requires serial power, so chip-to-chip power distribution: special issues like sensor bias

Stitching !!

Outlook: R&D taking important steps in each iteration

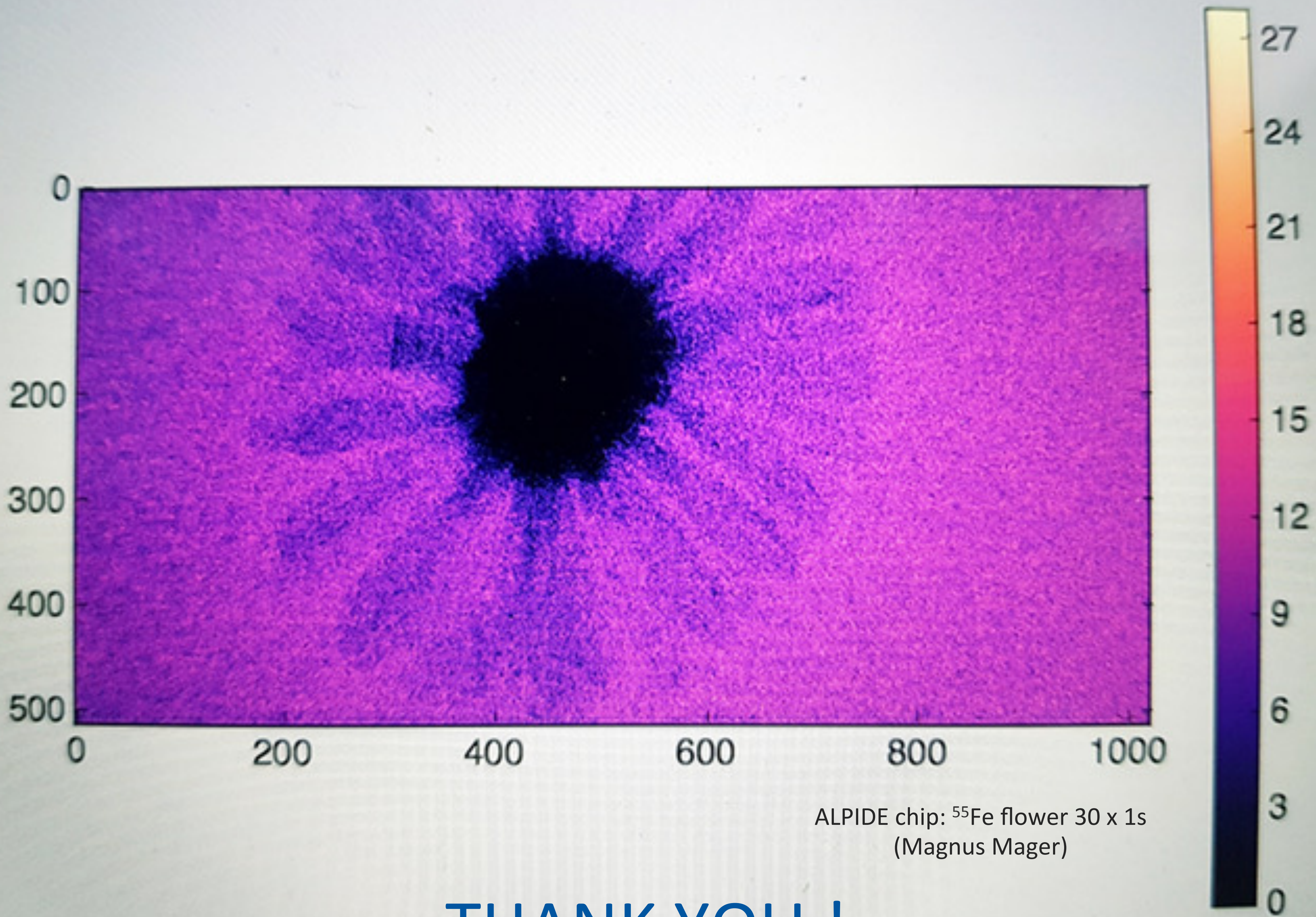
Need large teams

Build experience participating also in other projects (eg CCNU in ALICE)

Technology of tomorrow is different from today

Smaller line width technologies offer more bandwidth,
potentially better Q/C (lower power),
and higher granularity

Important technology and potential for collaboration with industry



ALPIDE chip: ^{55}Fe flower 30 x 1s
(Magnus Mager)

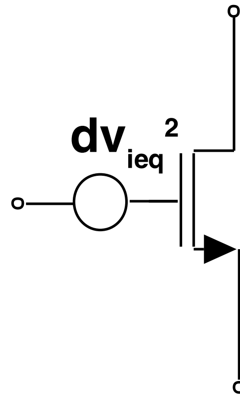
THANK YOU !

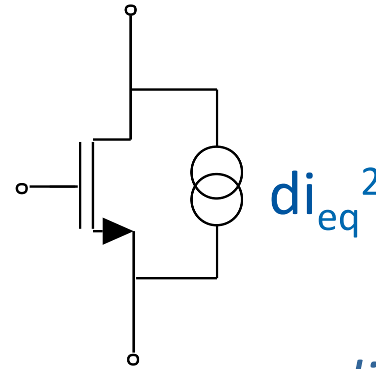
Backup

Analog Power Consumption:

Noise sources in a FET

EQUIVALENT WITH :





WHERE:

$$di_{eq}^2 = g_m^2 dv_{eq}^2$$

In weak inversion (WI): $g_m \sim I$

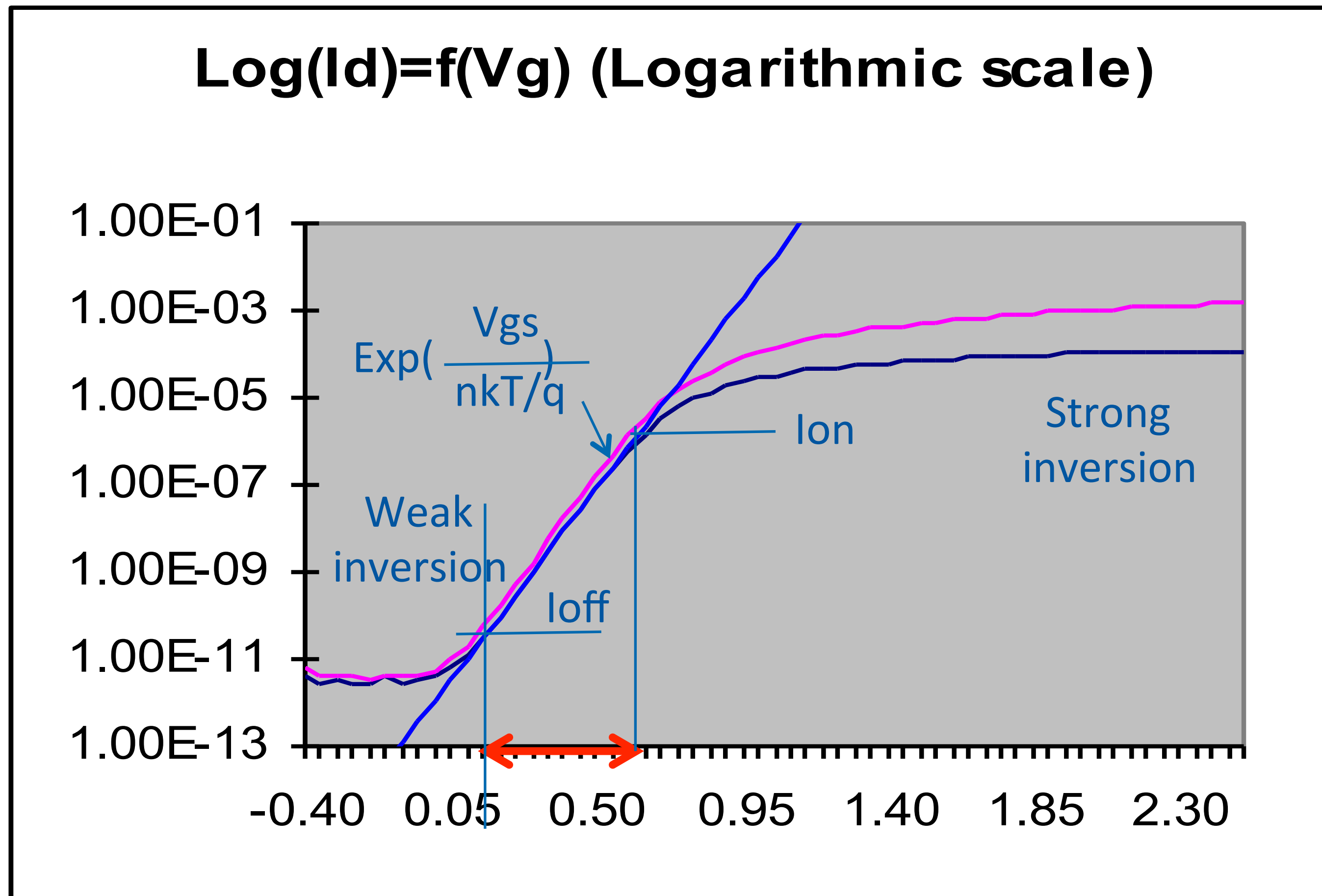
$$dv_{eq}^2 = (K_F/(WLCox^2 f^\alpha) + 2kTn/g_m)df$$

In strong inversion (SI) $g_m \sim \sqrt{I}$

$$dv_{eq}^2 = (K_F/(WLCox^2 f^\alpha) + 4kT\gamma/g_m)df$$

Transconductance gm related to power consumption

DIGITAL SIGNAL by further optimization ?



Slope in weak inversion 60-90 mV/decade,

for Ion/Ioff=10^4 on a single pixel => Q/C of 250-360mV

would practically eliminate analog power consumption

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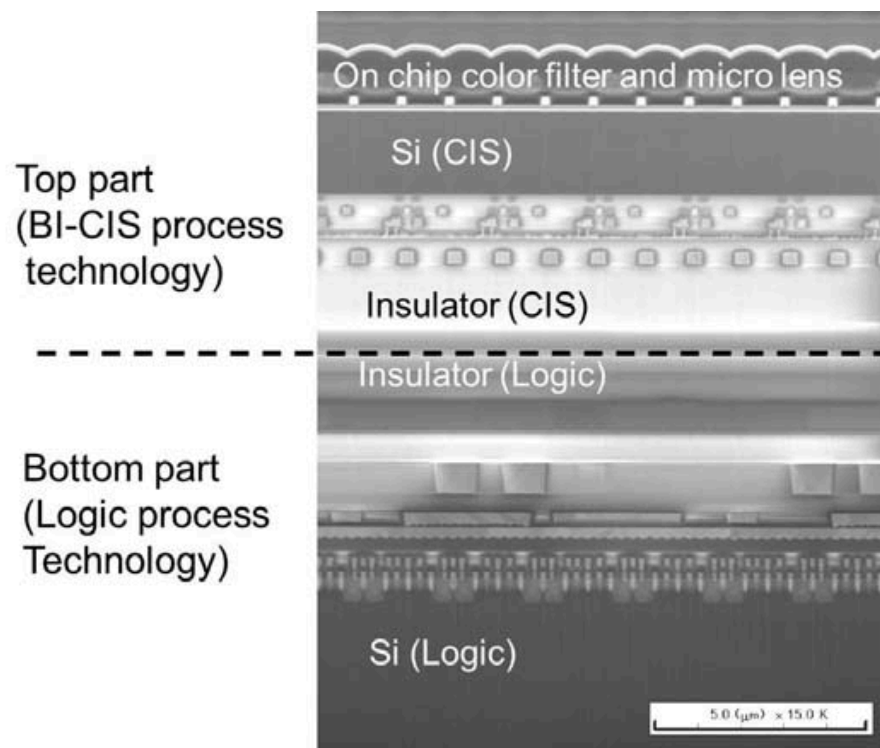
CMOS Monolithic Active Pixel Sensors

- CMOS MAPS have changed the imaging world, reaching:
  - less than 1 e^- noise

    (cfr S. Kawahito, PIXEL 2012)
  - > 40 Mpixels
  - Wafer scale integration
  - Wafer stacking
  - ...

- In High Energy Physics silicon has become the standard in tracking applications both for sensor and readout

- … and now CMOS MAPS make their way in High Energy Physics !

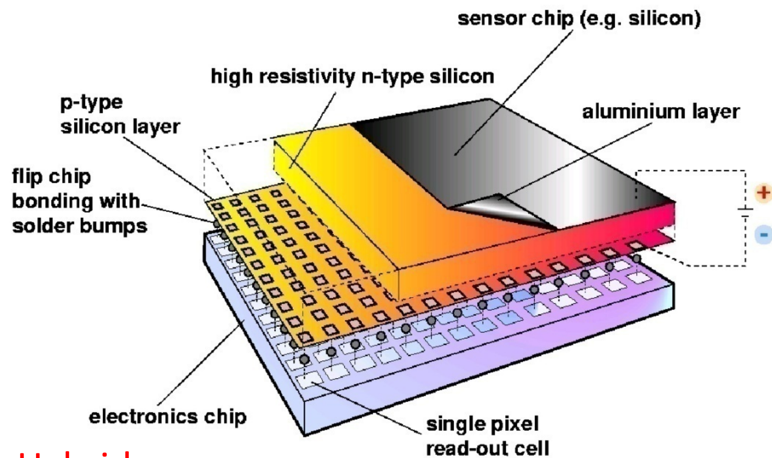


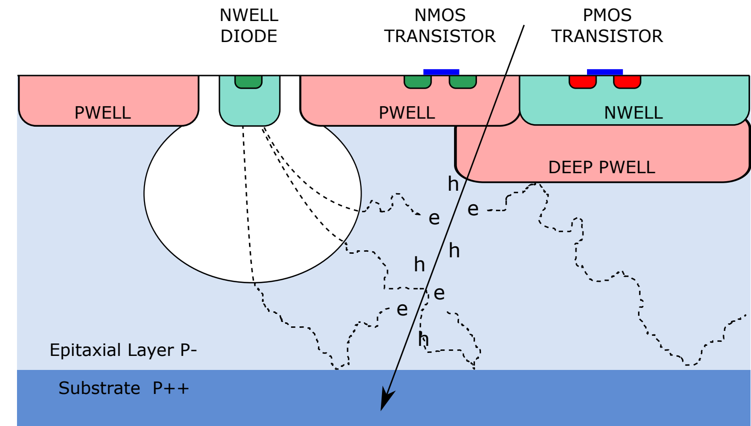
Backside Illuminated 8M Pixel Stacked Imaging Sensor

S. Sugawa et al. Sony Corp.

ISSCC 2013

Hybrid versus Monolithic





Hybrid

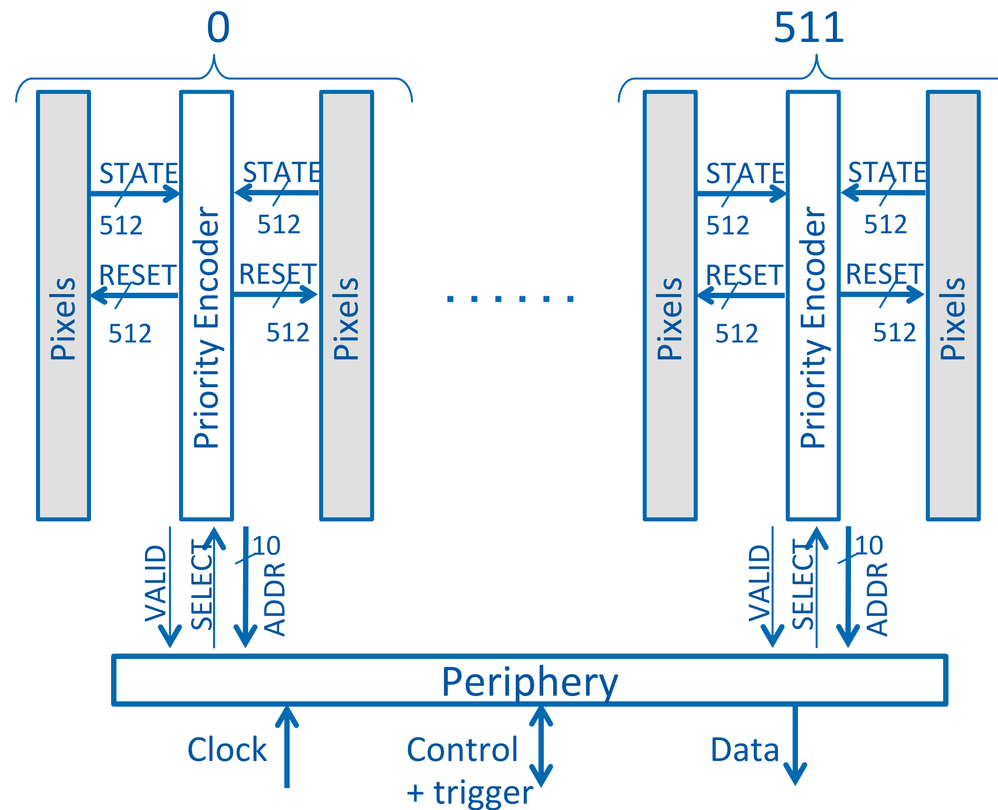
- Large majority of presently installed systems
- 100 % fill factor easily obtained
- Sensor and ASIC can be optimized separately
  - Sensor other materials
  - ASIC standard CMOS

Monolithic

- Easier integration, lower cost
- Promising not only for pixel detectors but also for full trackers
- Potentially better power-performance ratio and strong impact on material budget
- MAPS installed in STAR and adopted for ALICE ITS upgrade, considered for outer pixel layer in ATLAS ITk

New technologies (Through-Silicon-Vias, microbumping, etc) could make distinction more vague. Stacked CMOS imagers are available in industry, but usually not with per pixel connection. ATLAS & CLIC (I. Peric, R. Ballabriga et al.) are investigating capacitive coupling between sensor and readout chip.

Matrix readout



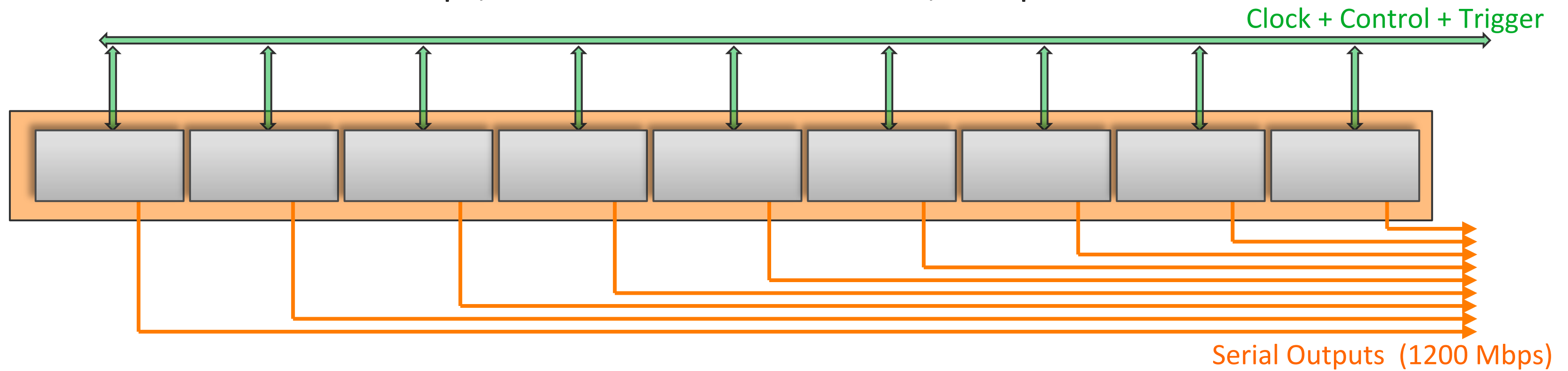
The Priority Encoder sequentially provides the addresses of all hit pixels in a double column

- Combinatorial digital circuit steered by peripheral sequential circuits during readout of a frame
- No free running clock over matrix. No activity if there are no hits
- Energy per hit: E_h ~= 100 pJ -> ~3 mW for nominal occupancy and readout rate
- Buffering and distribution of global signals (STROBE, MEMSEL, PIXEL RESET)

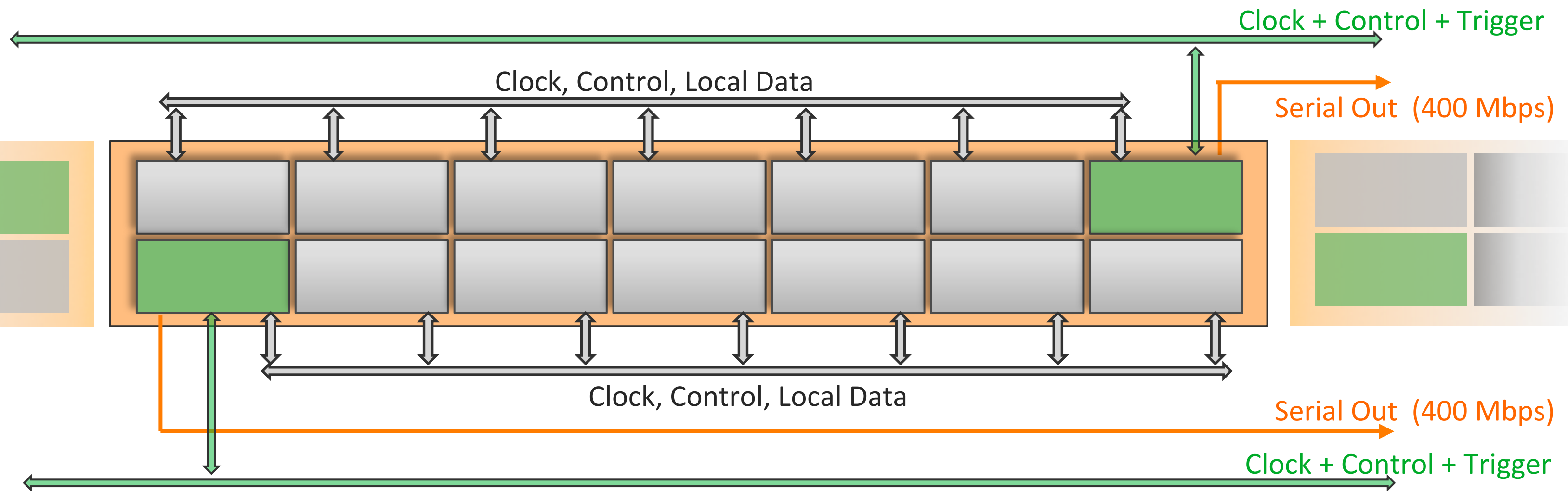
ALPIDE Readout and Control Features

Detector Modules with ALPIDE Chips

ITS Inner Barrel Module – 9 chips, common clock and control, independent data lines



ITS Outer Barrel Module – 2 groups of chips, Master + 6 Slaves
Only the Master interfaces to the external world and bridges control and data transfer



First CMOS Quad Module

- FPGA instead of MCC
  - Serializer
  - Cmd and Clk decoder
- Module bus interfaced to FPGA through LVDS chip output
- Serial powering testable