ATLAS R&D
CMOS SENSOR FOR ITK

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On behalf of the ATLAS R&D CPPM-ACC

CPPM / Atlas Chinese Cluster Collaboration

- CPPM / ACC collaboration for design and test of Front-End pixel electronics for ATLAS phase II upgrade.

- Scientific cooperation supervised by Pr. Xinchou LOU, Dr. Zheng WANG and Pr. Marlon BARBERO, derived from ATLAS CPPM / ACC project
(Pr. Shan JIN / Dr. Emmanuel MONNIER).

Use cases for ATLAS CMOS pixels

- Restricted here to pixel detector
- **Inner pixel** layers (R=3-6 cm). Strong radiation hardness demand to ~500 MRads. Use of FE-RD53 in 65nm technology with 50x50 um pixel size / or dedicated ROC. Four CMOS 25x25 um sub-pixels with thickness <50 um? "à la 3D elect." → Higher granularity!
- **Outer pixel layers** R> 15 cm. ~100 MRads. Use FE-Ix digital tier with HVCMOS pixels 50x250 um or smaller. Low cost bonding (gluing or C4 bumps) mandatory for cost reasons.
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Main target for TDR → ITk outer layer L4

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Most interesting from physics perspective → targets post-ITk

Specification of CMOS SENSOR for the ATLAS ITK upgrade

- A monolithic depleted CMOS sensor may be able to replace the diode sensor+FEIx of a hybrid module by incorporating this function in a single die CMOS monolithic chip. This replacement could offer several advantages, including finer pixel granularity, thinner charge collection layer for better 2-track separation, lower production cost and time, including savings by avoiding traditional bump bonding.

- Chip size = RD53 equivalent
- Pixel size < 50µm²
- Min. stable threshold setting <1000 e-
- Monolithic chip : digital bandwidth 160Mbps
  (number of bits transmitted per hit)
- Radiation level = 80 Mrad TID, and $1.5E^{15}$ n_{eq}/cm^2 NIEL at 4000 fb^{-1}

CMOS Sensor : Technology Overview

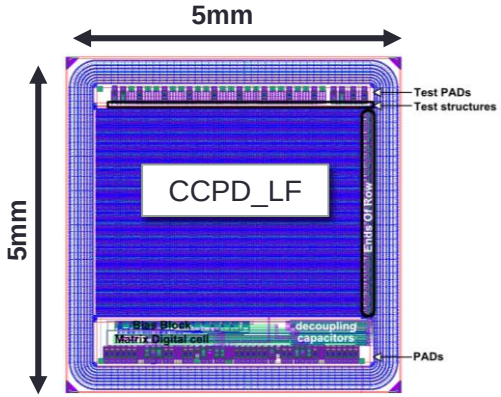
- AMS 350 nm
- AMS 180 nm
- **LFoundry 150 nm***
- Global Foundry 130 nm
- ESPROS 150 nm
- Toshiba 130 nm
- TowerJazz 180 nm
- STM 160 nm
- IBM 130nm
- XFAB 180 nm

* LFoundry 150 nm is now a SMIC Chinese technology

LFoundry development line

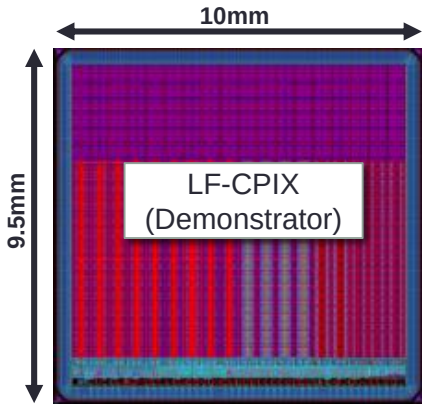
CCPD_LF (PROTO)

- Subm. in Sep. 2014
- 33 x 125 µm² pixels
- **Fast R/O coupled to FE-I4**
- Standalone R/O for test
- ***(Almost) Fully characterized***



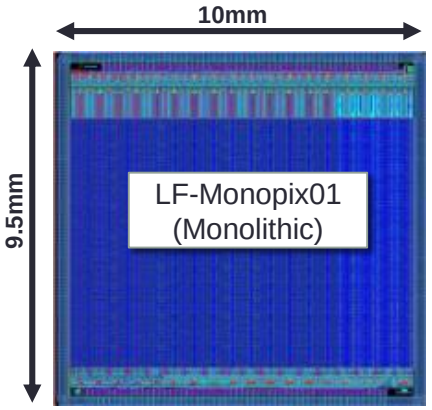
LF-CPIX (DEMO)

- Subm. in Mar. 2016
- ***CPIX demonstrator in LF***
- 50 x 250 µm² pixels
- **Fast R/O coupled to FE-I4**
- Standalone R/O for test
- ***First meas. available***



LF-Monopix01 (monolithic)

- Subm. in Aug. 2016
- "Demonstrator size"
- 50 x 250 µm² pixels
- ***Fast standalone R/O***
- Standalone R/O like LF-CPIX

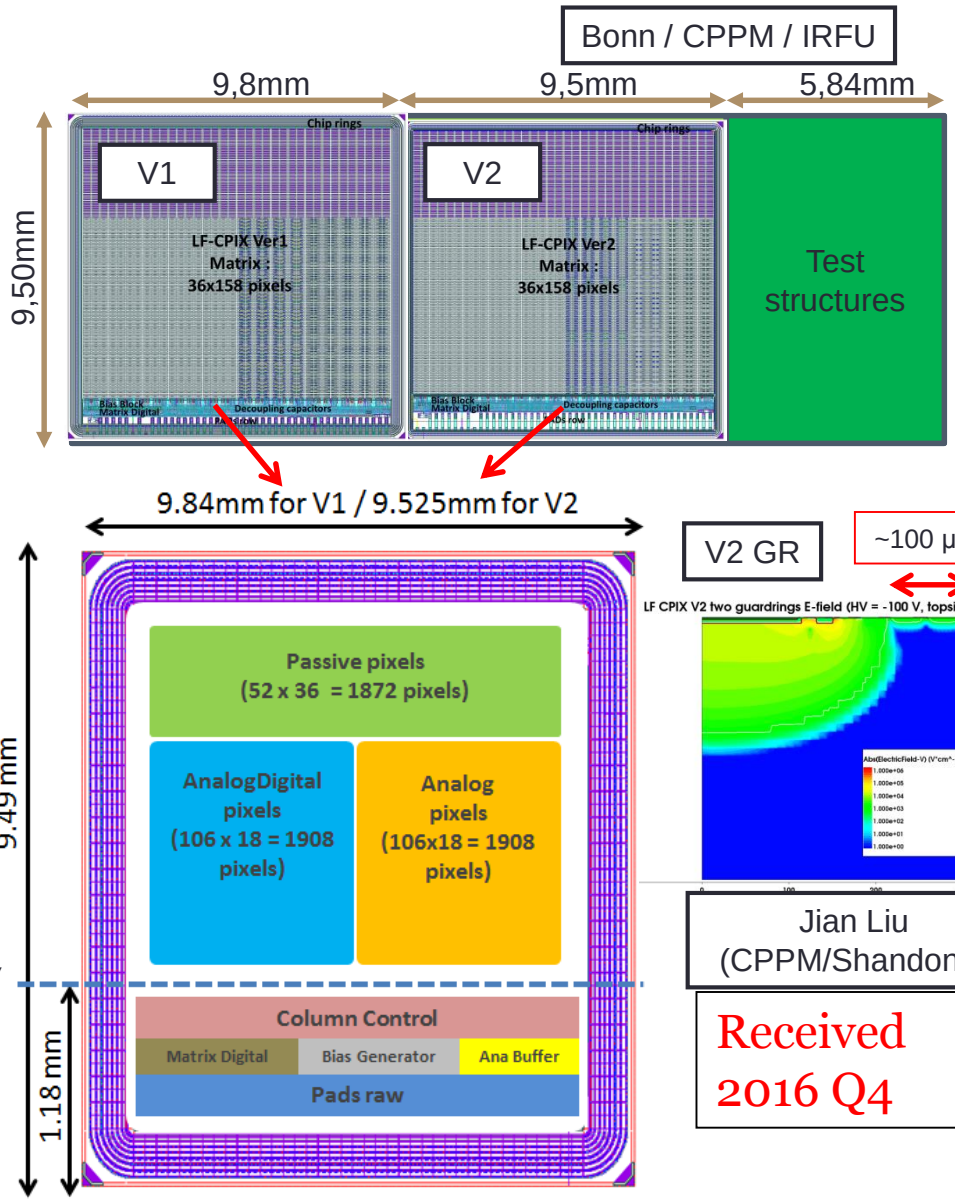


LFOUNDRY: LF-CPIX demonstrator

- Feb. 2016: 10×10 mm^2 chip size
- V2 = V1 + new guard ring strategy.

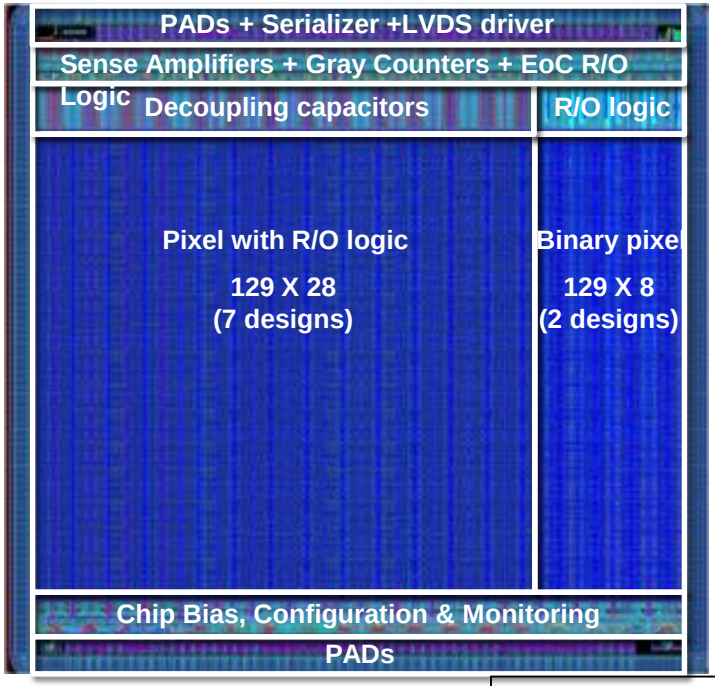
Pixel Matrix :

- Pixel 250µm×50µm (FEI4-like)
- All pixels have bond pad to FEI4
- 3 sub-matrices :
  - **Passive**: only DNwell sense diode
  - **AnalogDigital**: à la LF VA, 4 flavors (different diode bias, diff. input transistors NMOS and PMOS).
  - **Analog**: preamp with complementary input CMOS, and 8 flavors (diode polarization, outputs "linear", "saturated" or "digital"…).
  - Preamp out / hitOR available for all pix!



LFOUNDRY: MONOPIX demonstrator

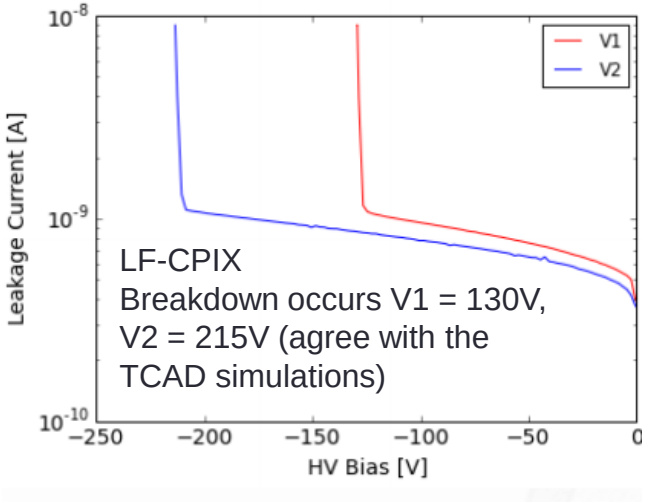
- Chip overview
- Large input from LF-CPIX: pixel, floor plan…
- 9 flavors for comparative studies => each 4 col.
  - Pixel with R/O logic (FE-I3 like pixel)
    - ❑ NMOS/CMOS pre-amp. ❑ Old/new discriminator
    - ❑ Different power domains for discriminator.
    - ❑ CS /CMOS token transmission
  - Binary pixel with R/O logic at column end
    - ❑ NMOS /PMOS source follower for “HIT” R/O

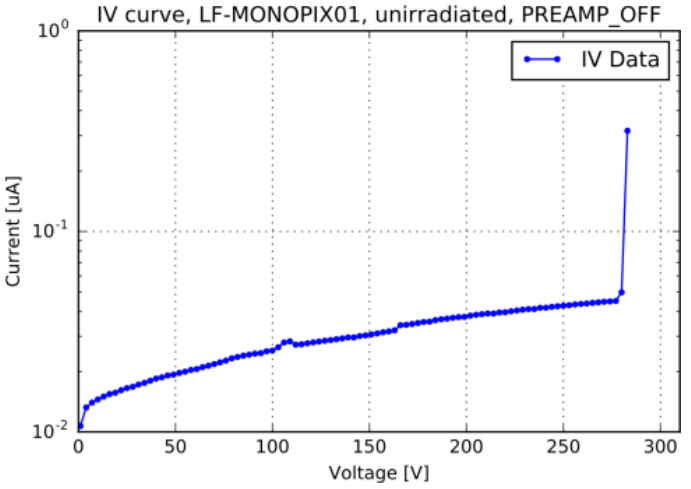


- Many design efforts to meet the challenges in terms of noise and timing
  - ❑ faster pre-amp. & discriminator ❑ careful layout and post layout sim.
  - ❑ full-custom in-pixel digital circuit & low noise digital block

Received 2017 Q1

First measurements (LFCPIX and MONOPIX)





LF-CPIX

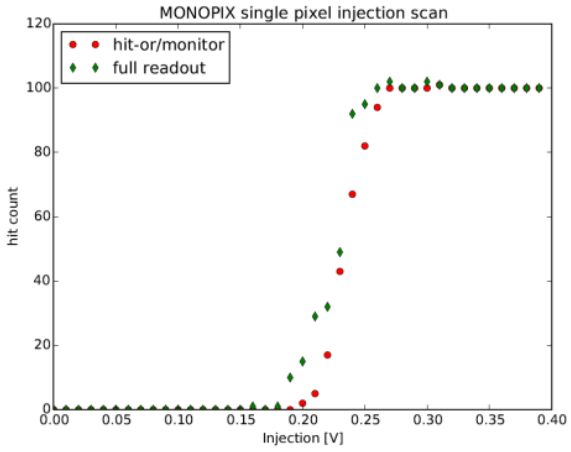
The test confirmed the new Break-Down voltage, simulated by TCAD.

The pixel electronic part give better results than the CCPD chip (Improved electronics performance and better charge collection efficiency)

Analog Gain degradation is reduced, the pixels dispersion are contained and the chip is Rad-Hard up to 50Mrads at the 1st test.

MONOPIX

The 1st tests show that the Monolithic chip is working with full depleted sensor and with real Read-Out communication from calibration signal



Conclusions and future plans

- CMOS SENSORS for ATLAS ITK can be produced in 10 different technologies. We have the choice…., but focus is made for ITK upgrade on 3.

- The 1st demonstrator LFOUNDRY chips are showing very good results on CCPD (see Jian Liu Talk) and the most advanced LFCPIX chip have very good results close to the TDR specifications. The time collection was improved (lower thresholds, higher signals with HR, time slewing corrections).
- And thanks to the TCAD simulation, to help on save time and money for that new HVCMOS technology approach.

- The ATLAS Pixels TDR should be written at the end of 2017, and the CMOS SENSORS chapter should be defined before this summer. Other CMOS monolithic SENSOR on Lfoundry, TowerJazz and AMS technologies are on design or test and should fit the TDR requirements

- The IHEP, SDU and CPPM have a very strong collaboration since many years, on ATLAS developments. We are willing to expand the partnership between Chinese institutes and CPPM on further HVCMOS, especially on new accelerator projects (CEPC, FCC…)