Hiroshima Conference HSTD 11

Okinawa, Dec 10 – 15, 2017

Pixel Detector Overview

Pixel Detectors ... where do we stand ?

in my very subjective opinion ... w/ apologies

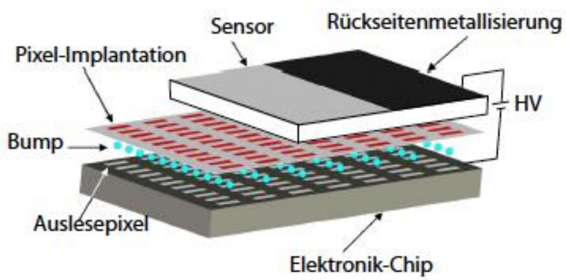
Norbert Wermes
University of Bonn

universitätbonn

SI LAB
Silizium Labor Bonn

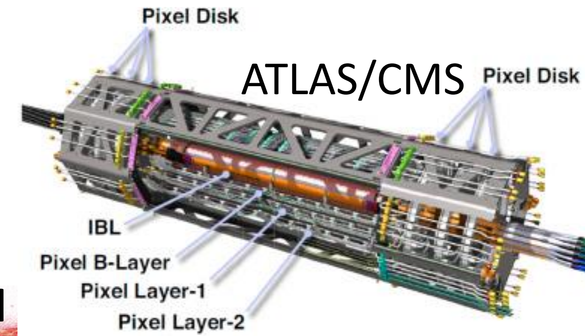
~1997

Hybrid pixel detectors



HEP tracking

LHC

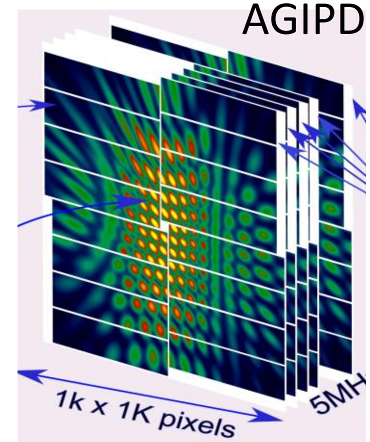


HI

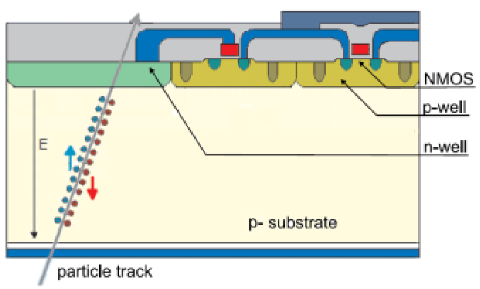
Imaging

biomedical

photon science

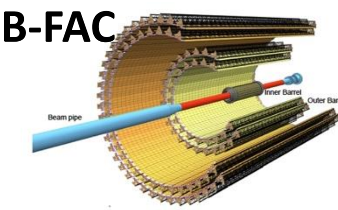


Monolithic pixel detectors



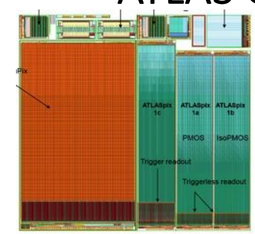
HEP tracking

HI, B-FAC

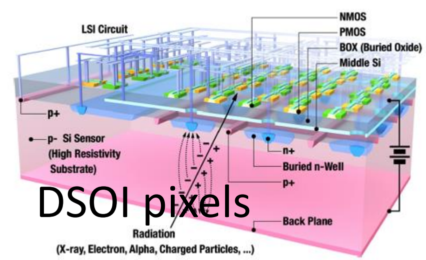


ALICE ITS

LHC



Imaging



2017

N. Wermes, HSTD11, OIST 12/2017

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Some early prejudices
... e.g. about HL-LHC radiation levels

- Tough for planar sensors ... !?
- There is no alternative, though ... !?
- Diamond will never become a pixel detector ... !?
- You have to use p-type material ... !?
- ...

talk by G. Kramberger

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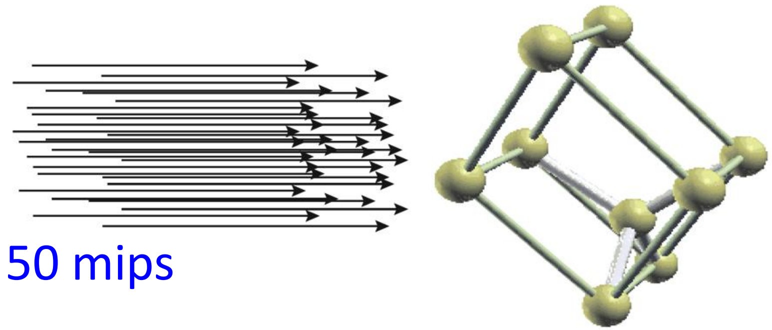
Radiation

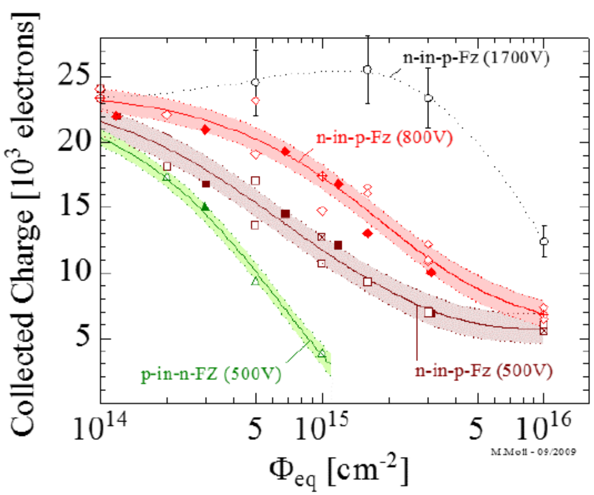


- HL-LHC fluence =>every Si lattice cell sees about 50 mips

Recipe

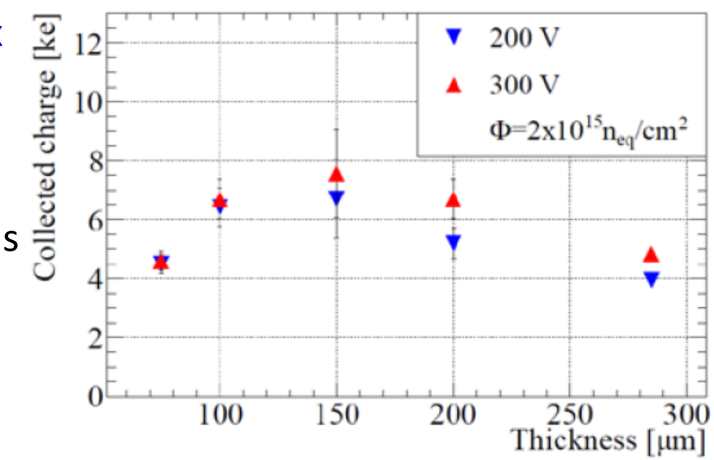
- Readout at n^+ electrodes (e^- collection)
- Operate at high bias voltages
- Carefully plan the annealing scenario
- Provide proper electrode design and guard rings
- Use p-substrates (rather than n-in-n) ... why?

evidence

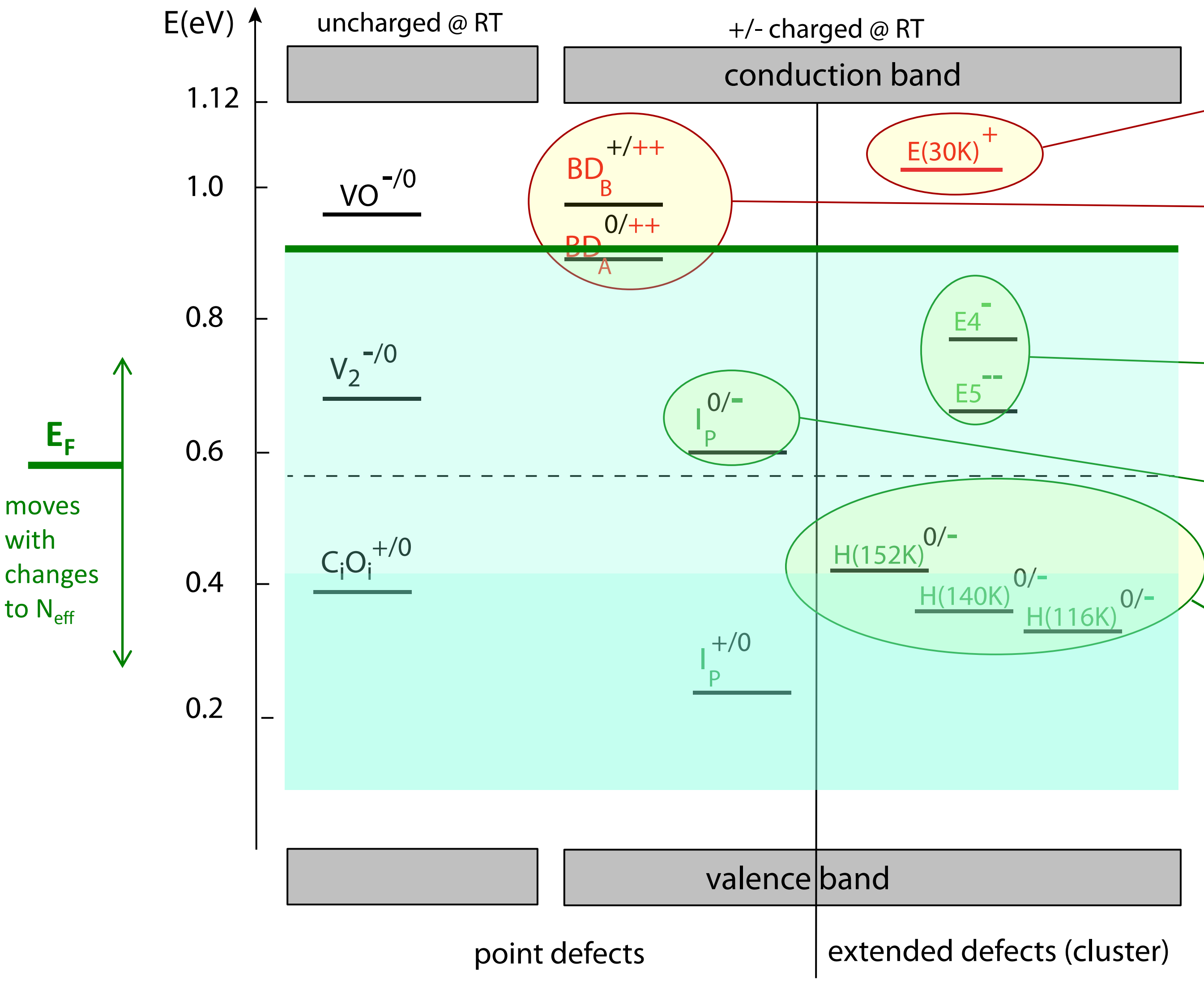


but more complex for pixels

- Q trapping
- structured weighting fields
- E-field after irradiation



What is actually different for p vs n bulk?



e- trap
positive space charge
higher conc. after proton than neutron irradiation
depends on oxygen content

BD=bistable donor (e- trap)
positive space charge
strongly produced in oxygen rich DOFZ material

triple vacancy, small cluster
negative space charge
-> **high leakage current**

V_2O complex (?)
negative space charge
causes **leakage current**,
strongly produced in oxygen lean STFZ

extended acceptor defects produced equally by n,p
negative space charge
-> **reverse annealing**

- most defects show linear fluence dependence
- cooling helps to keep I_{leak} and rev. annealing smaller
- N_{eff} changes

Radu et al., J. Appl. Phys. 117, 164503 (2015)
RD50, M. Moll et al., PoS (Vertex 2013) (2013) 026

n – bulk p - bulk

Donor removal/acceptor increase <-> acceptor removal

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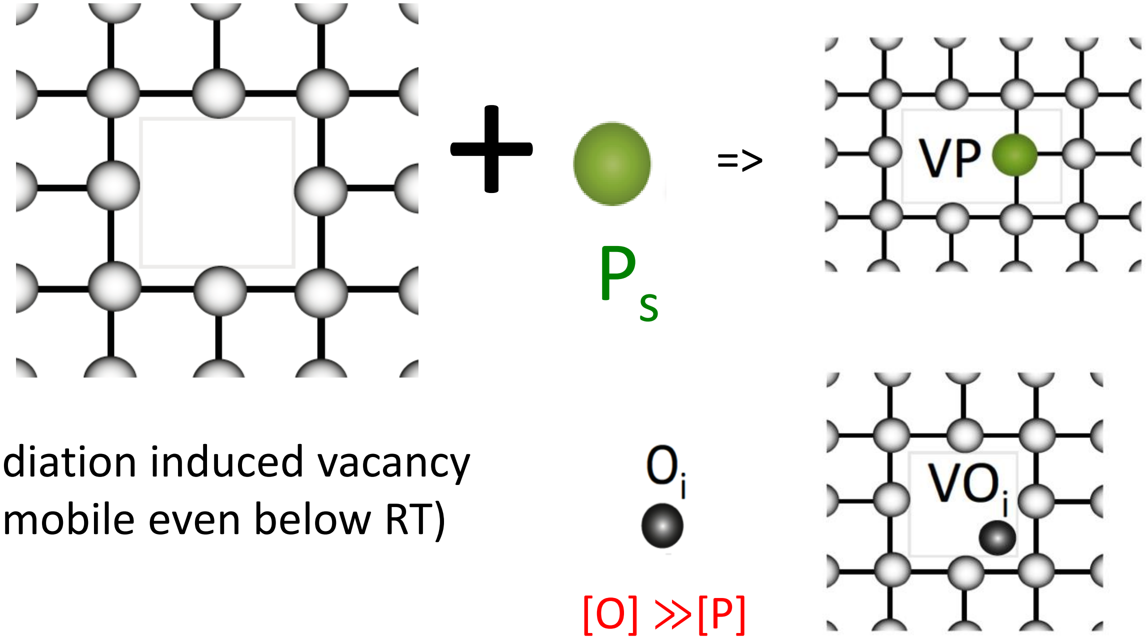


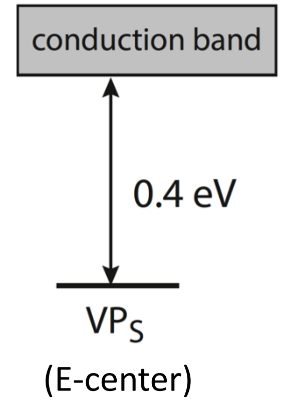
radiation induced vacancy
(mobile even below RT)

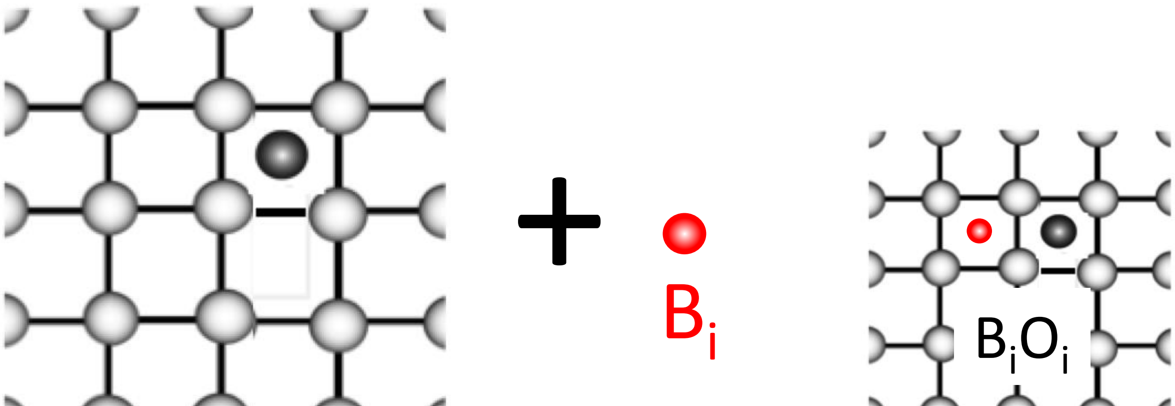
[O] ≫[P]

oxygen enriched silicon

<u>donor (P) removal</u>
decreases pos. ρ

<u>harmless</u>
VO_i defect

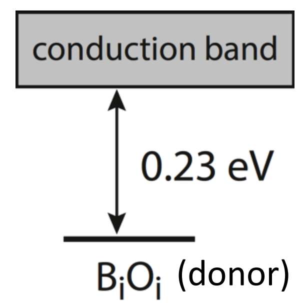




radiation induced oxygen interstitial

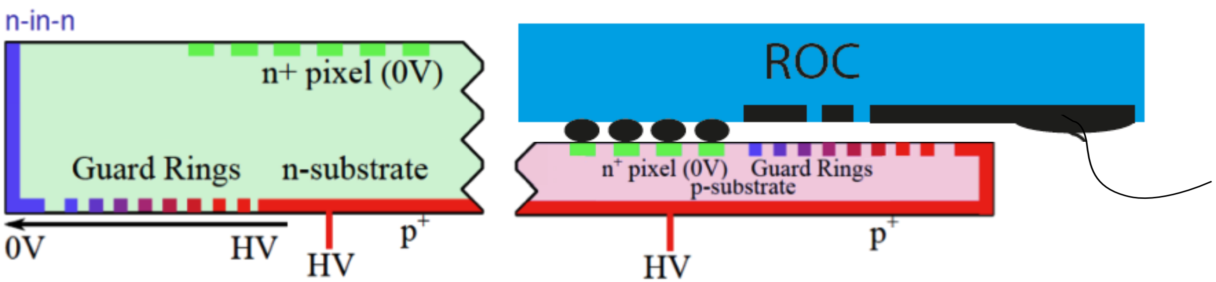
<u>acceptor (B) removal</u>
decreases negative ρ

Cure? C-enrichment?



A. Junkes, E. Donegani, C. Neunbüser, IEEE TNS (2014)
10.1109/NSSMIC.2014.7431260
E. Donegani, Thesis U Hamburg (2017)

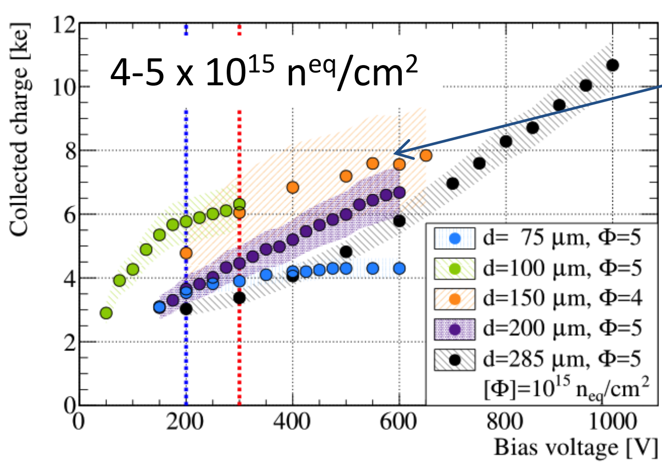
Radiation hard Si sensors -> (thin) planar pixel sensors

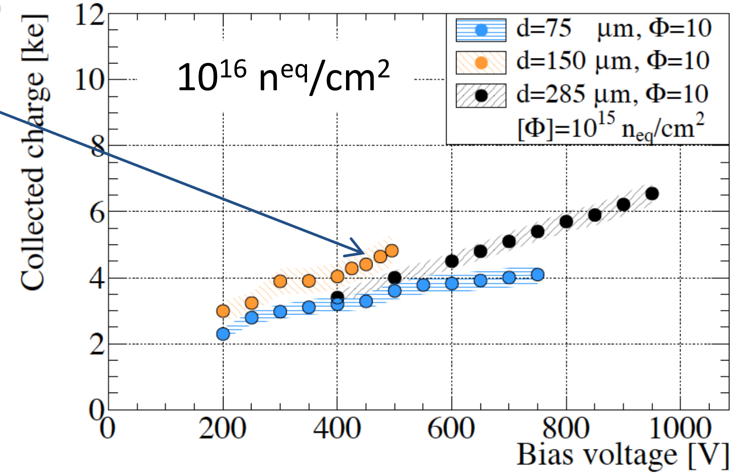


- thin **n+ in p** sensors after high fluences (neutrons)

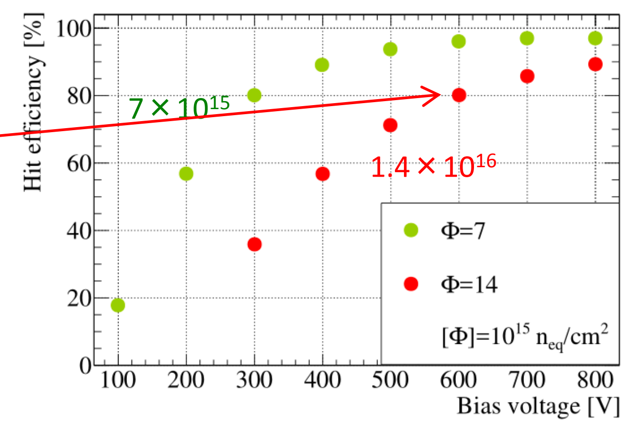
talk by K. Nakamura

best (100-150 µm)



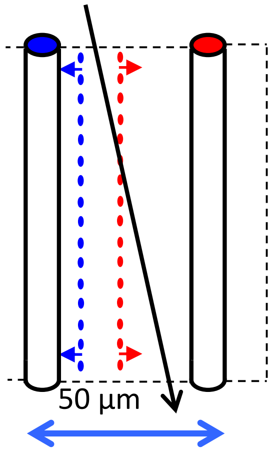


- **6000 – 7000 e-**
  for 100 - 200 µm sensors @ 300 V – 600 V bias
- hit efficiencies are still reasonable **at Φ > 10^{16}**



Macchiolo, Nisius, Savic, Terzo, NIM A831:111–115, 2016.
Terzo, Andricek, Macchiolo, Nisius et al, JINST 9 (2014) C05023
K. Kimura et al., NIM A831 (2016) 140-146
Y. Unno et al.,NIM A699(2013)72–77.

Radiation hard Si sensors -> 3D-Si sensors



- 3D sensors have been put to reality in ATLAS IBL detector since 2015 -> so far reliable and well performing

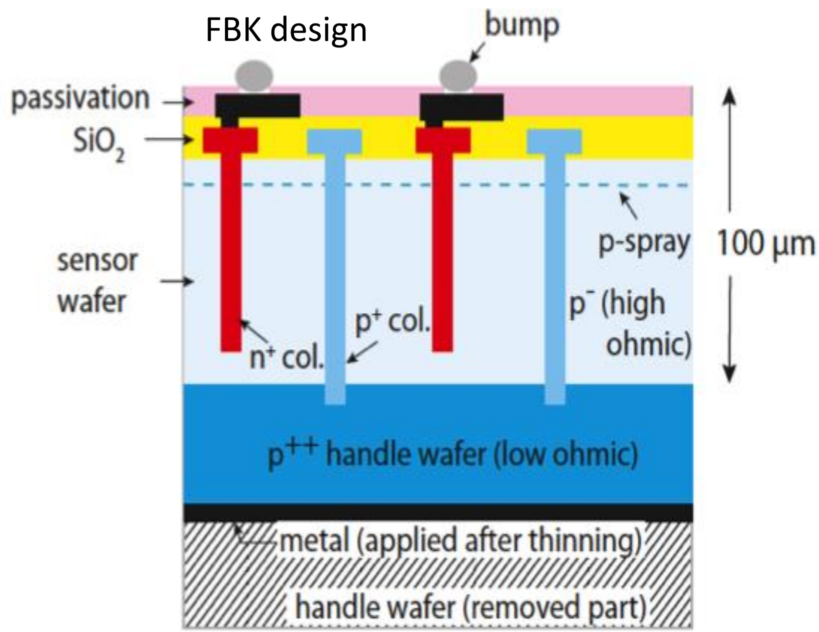
talk by C.B. Martin

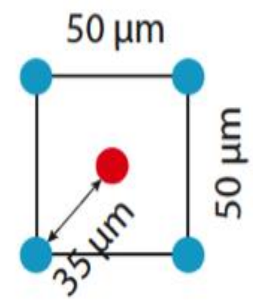
S. Parker, C. Kenney , J. Segal, ICFA Instr.Bull. 14 (1997) 30
C. Da Via, et al., NIM A49 (2005) 122-125,
NIM A 699 (2013) 18

- particle path (signal) different from drift path
- high field w/ low voltage

-> radiation tolerance
-> Q still 50% @ 10^{16} cm^{-2}

- slightly larger C_{in} (noise)
- now also in diamond, CdTe





Development for HL-LHC:
- thin (100 µm)
- 6” wafers
- electrodes thin (5µm) & narrowly spaced
- slim or active edges

G.F. Dalla Betta et al., NSSMIC.2015, arXiv:1612.00608,
J. Lange et al., arXiv:1707.01045

talks by H. Oide, J. Lange

Radiation hard Si sensors -> 3D-Si sensors

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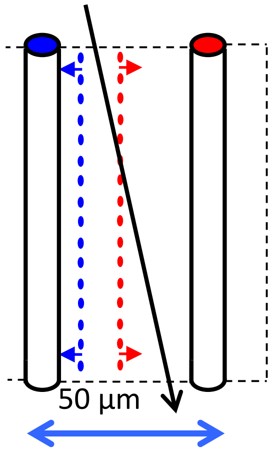

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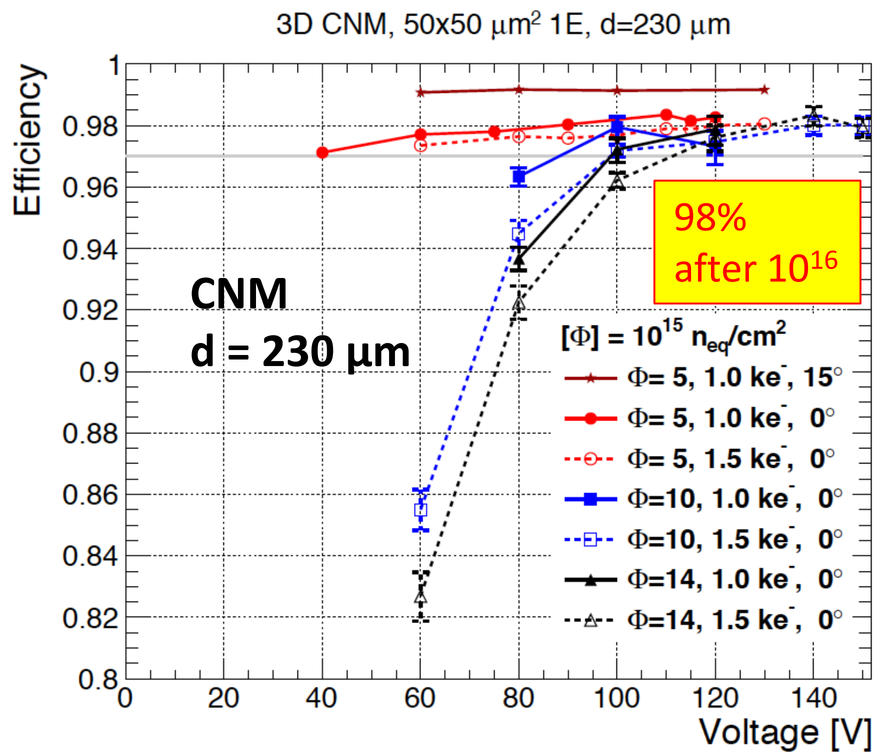

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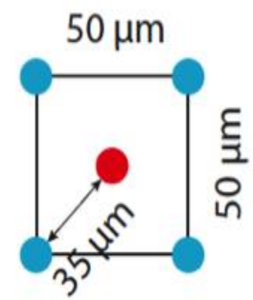

Development for HL-LHC:

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talks by H. Oide, J. Lange

Diamond ...

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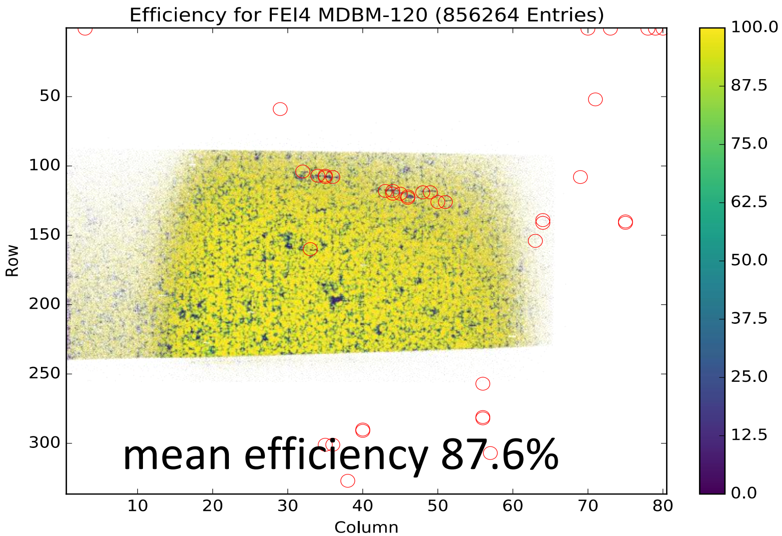
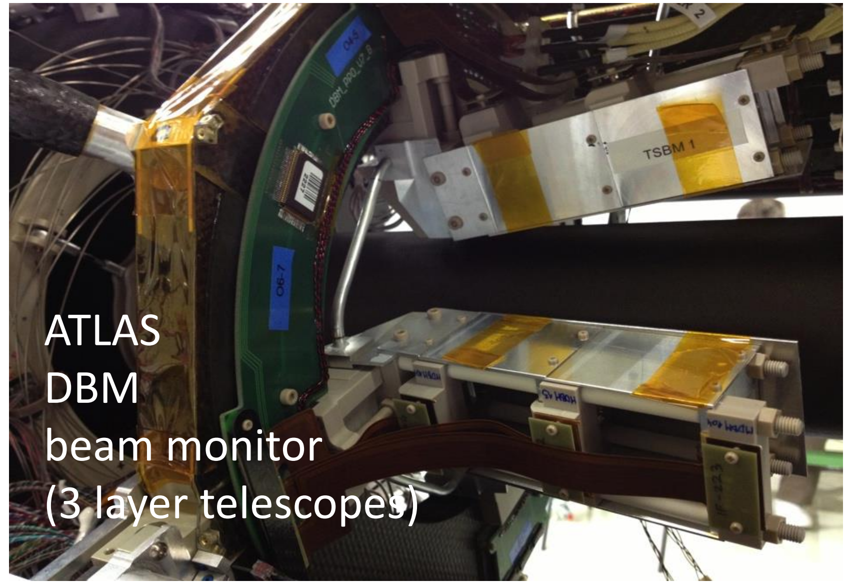
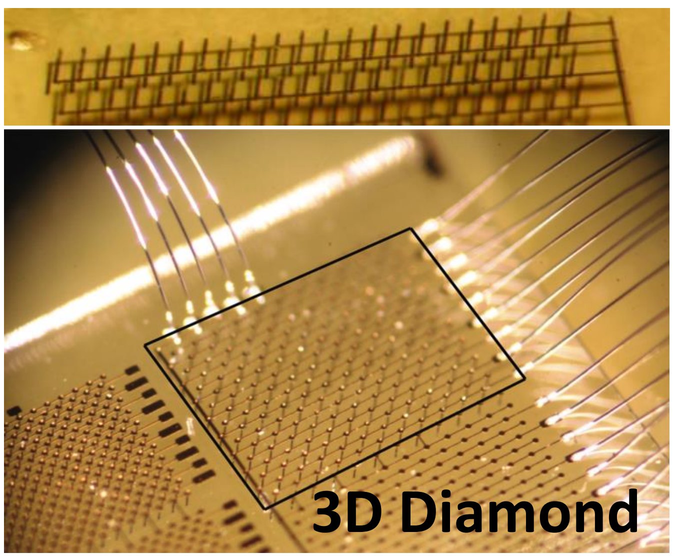
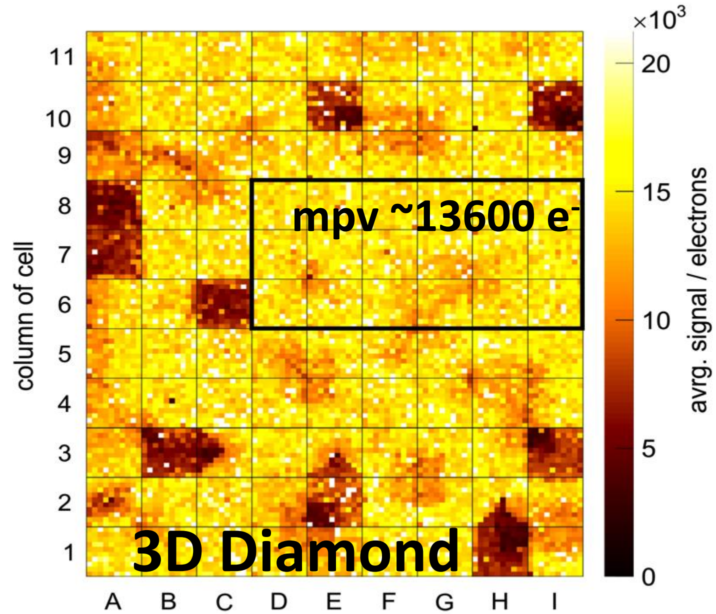
... has been made into a radhard "quasi" tracker









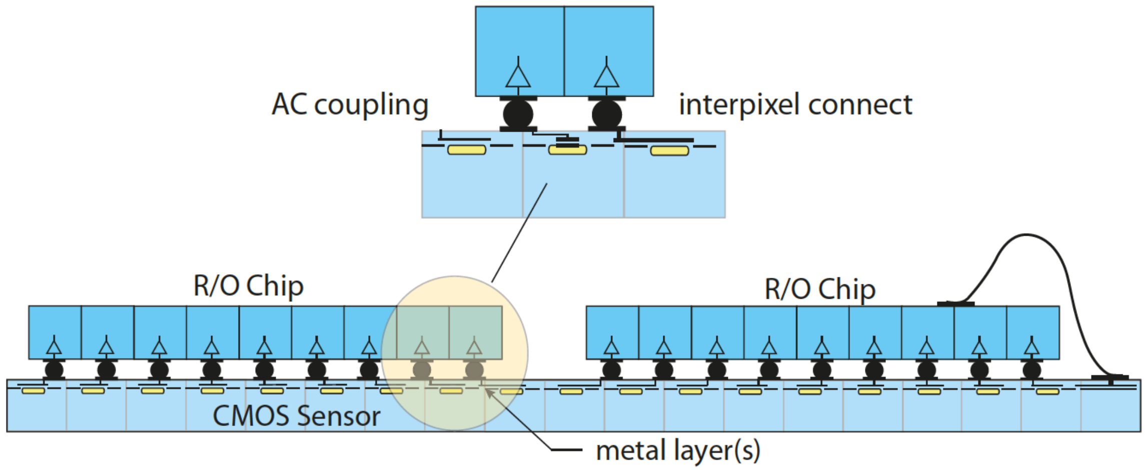
talks by
H. Kagan
N. Venturi

Kononenko et al., Diamond and Relat. Mater 18 (2009) 196

F. Bachmair, RD42-Coll., doi.org/10.1016/j.nima.2016.03.039

You cannot use CMOS (technologies for) sensors.
They do not have the same properties as "good" silicon sensors ... !?

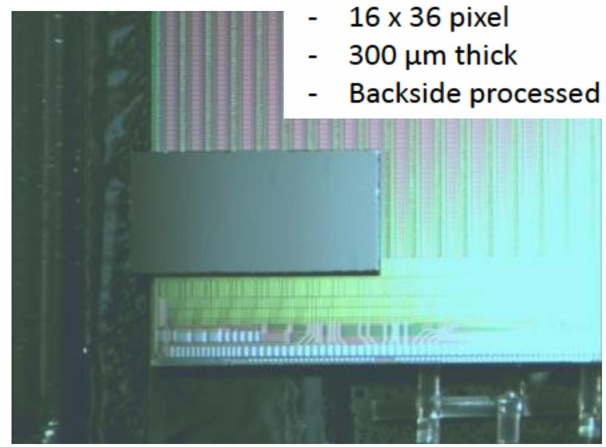
... passive CMOS sensors



- can have in-pixel **AC coupling**
- fancy **RDL** possibilities by metal layers

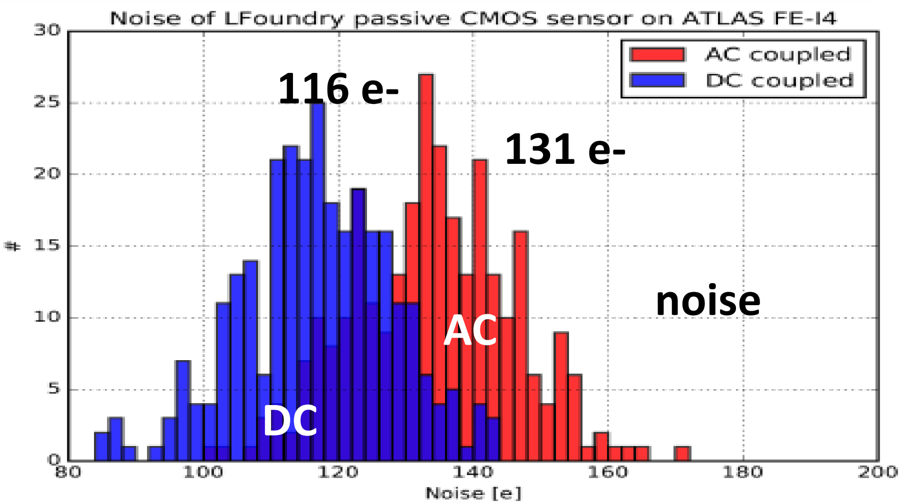
- **cheap** large feature size technology possible
- no extra bumping step, because bumps (**C4**) come with CMOS fabrication
- do flip-chipping in-house (large pitch)
- large sensors possible (→ reticule stitching)
- may be even wafer based flip-chipping (8“)

- LFounry 150 nm CMOS technology
- 2k Ωcm p-type bulk
- ATLAS FE-I4 pixel size (50 µm x 250 µm)
- 16 x 36 pixel
- 300 µm thick
- Backside processed

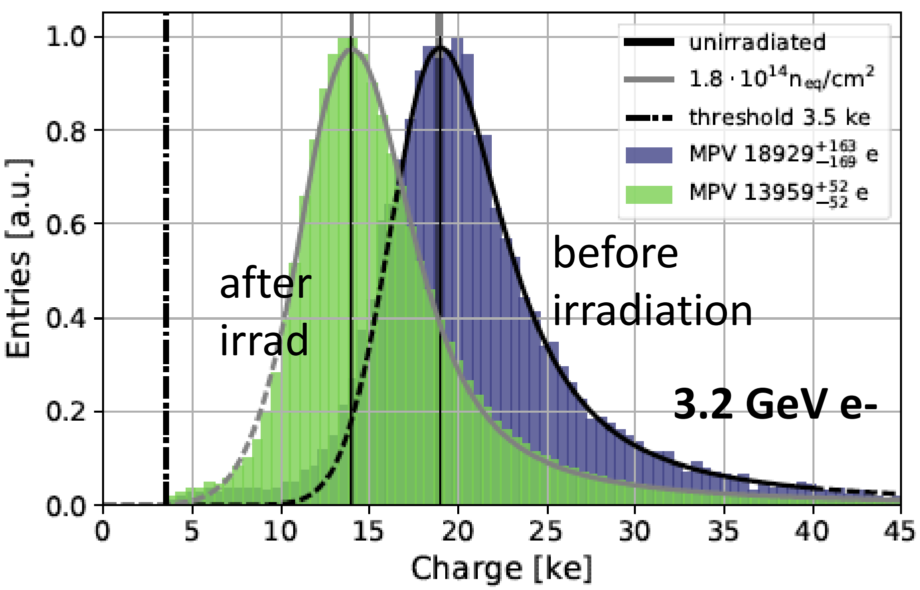


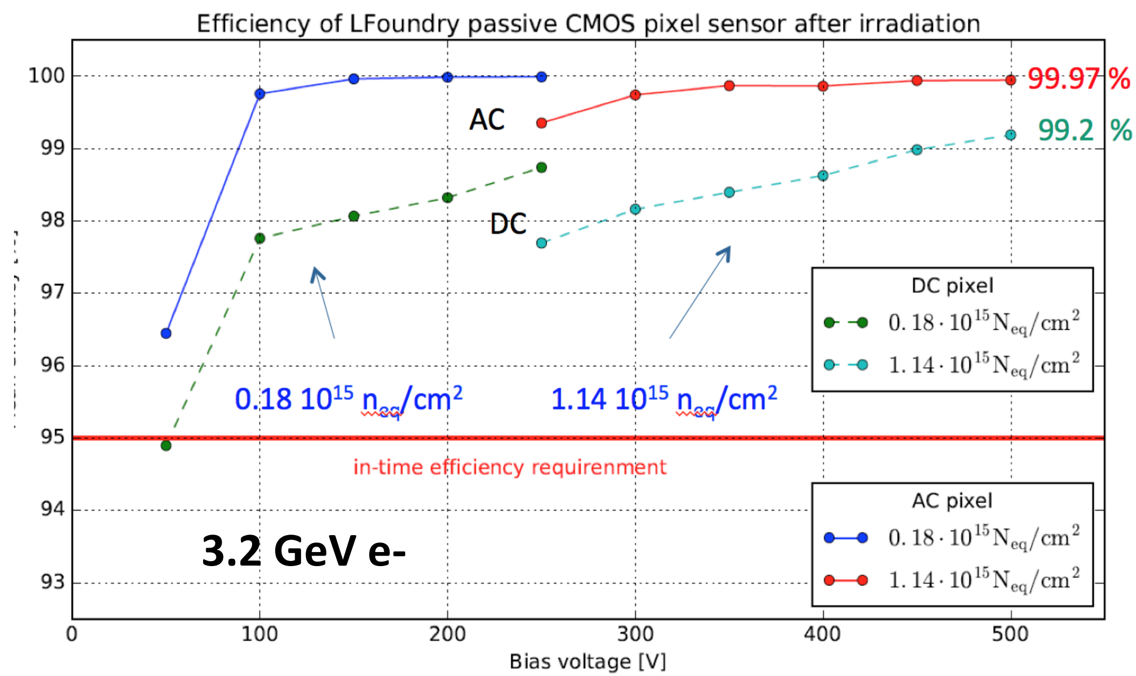
D.-L. Pohl et al., JINST 12 (2017) no.06, P06020

Performance of passive CMOS sensors



- **IV** curves of all samples ok (bias 120 V -> 500 V)
- about **220 µm** depletion depth
- leakage current **20 µA / cm³** (IBL: 15 µA/cm³)
- **noise** as in standard sensors
  - planar sensors (C_D = 117 fF): ENC = 120 e-
  - 3D-Si sensors (C_D = 180 fF): ENC = 140 e-
- **high efficiency after irradiation** (1 x 10^{15} n_{eq}/cm^2)





D.-L. Pohl et al., JINST 12 (2017) no.06, P06020

FE chip

- A complex chip (o(10^9) transistors) in general can only be done by industry and needs many years of development ... !? ... and is too expensive ... !?
- 250 nm technology was radhard => 65 nm technology is even better ... !?

Pixel R/O-Chip for HL-LHC rates (and radiation)

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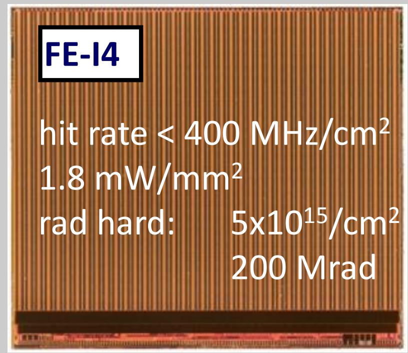
- Effort and costs so large that joint approach (cross experiments) is needed -> **RD53** (20 Institutes)
- High hit rate (not smaller pixel size) requires high logic density **-> 65nm TSMC**

250 nm technology

pixel size 400 × 50 μm²

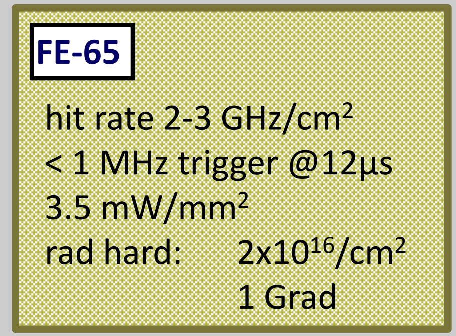
3.5 M. transistors



130 nm technology

pixel size 250 × 50 μm²

70 M transistors

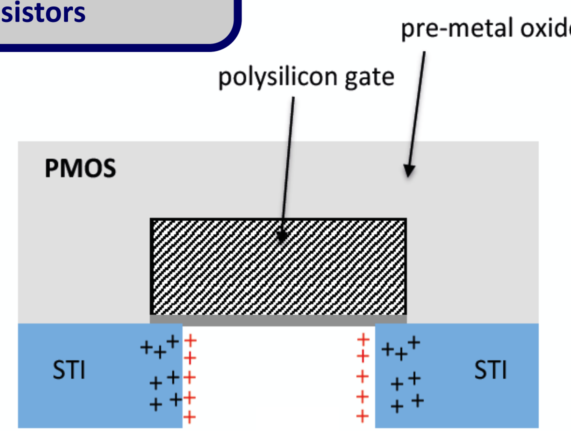


65 nm technology

pixel size 50 × 50 μm²

~ 1000 M transistors

- FE-65 prototypes (2016) -> RD53A (full size chip) -> back from foundry
- Deep submicron (250 nm & 130 nm) saved LHC pixel R/O chips
- 65 nm has its own – geometry induced – radiation effects to deal with
- Requires long and tedious study program ...

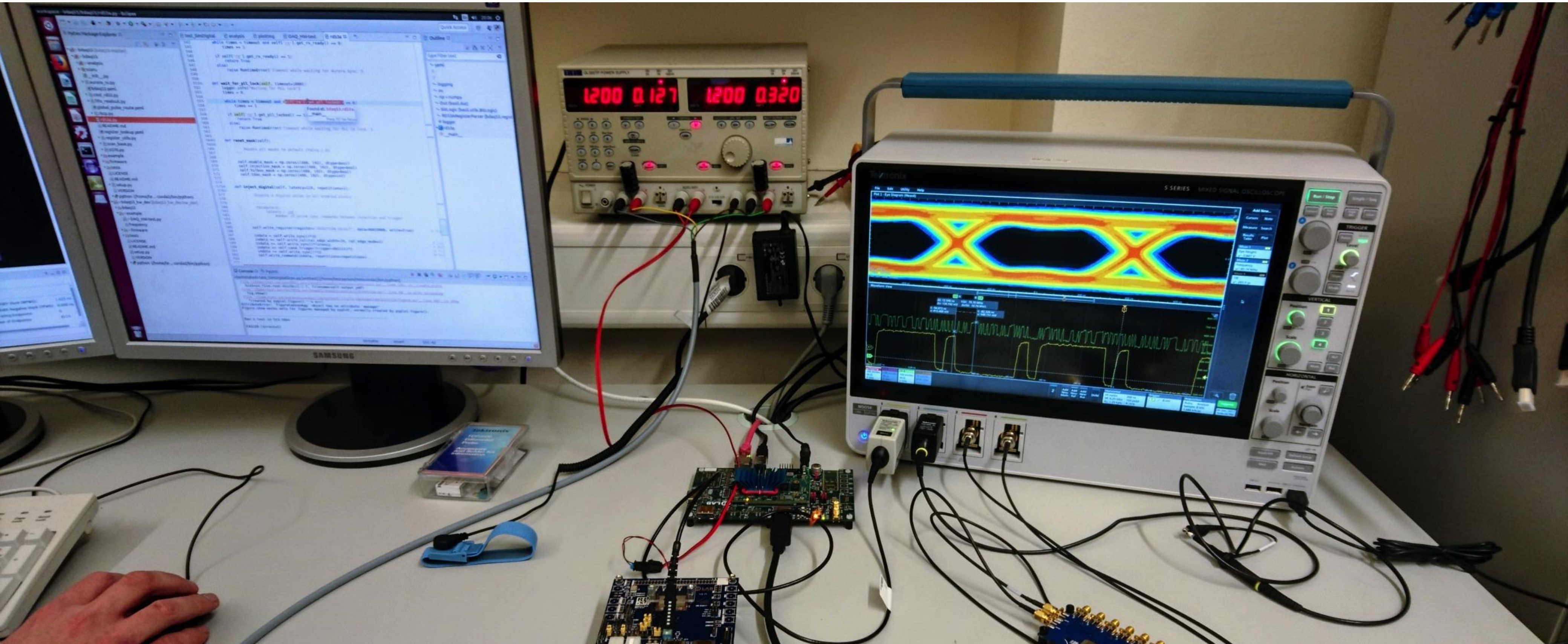


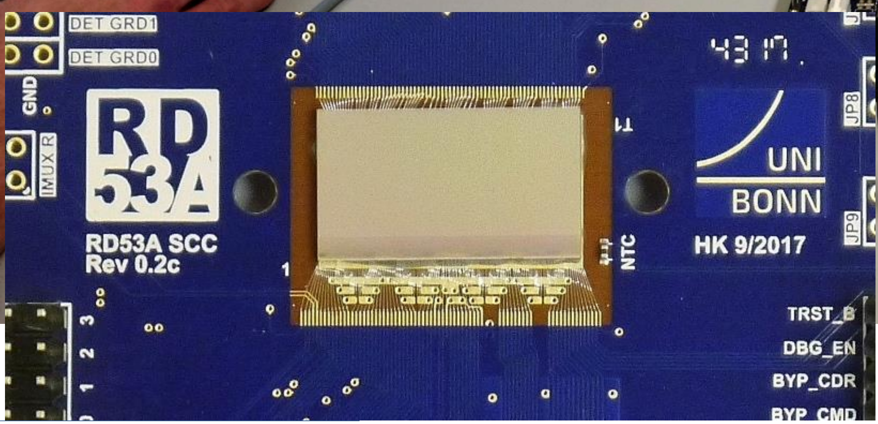
RINCE = Radiation Induced Narrow Channel Effects

RISCE = Radiation Induced Short Channel Effects

talk by F. Faccio ... "radiation strikes back"

RD53A alive ... (received last Wednesday)





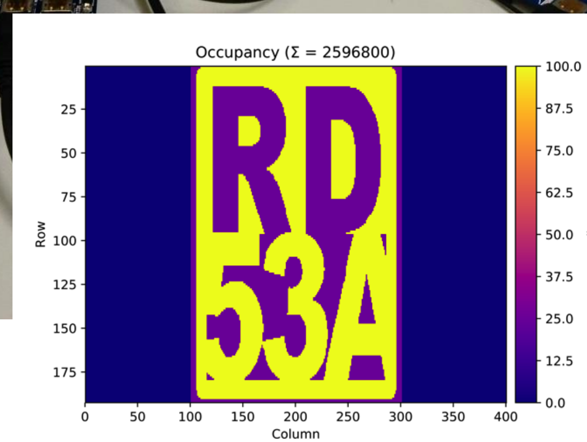
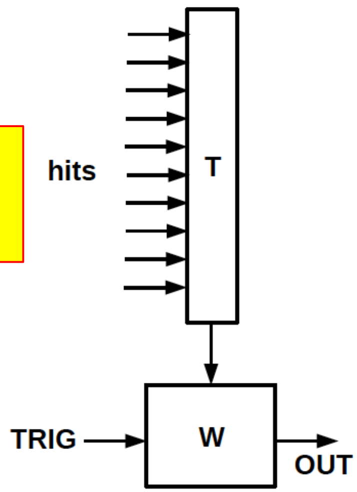


image produced by selective injections

Pixel R/O philosophy changes -> better architectures

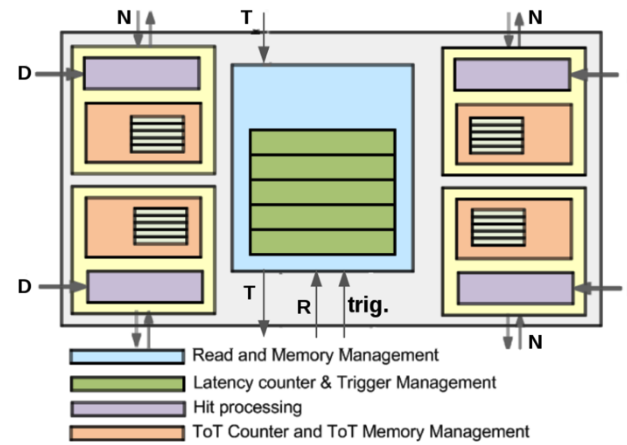
1st generation

- column drain R/O
- FE-I3 like



2nd generation

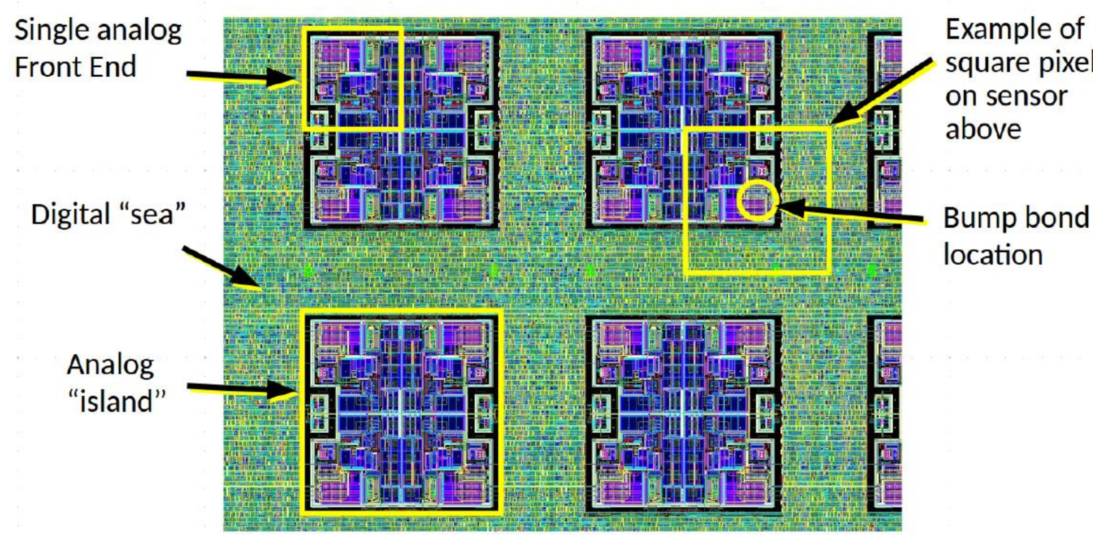
- 4-pixel region logic
- efficient for clusters
- FE-I4 like



talk by M. Garcia-Sciveres

3rd generation

- region architectures with grouped logic -> regional hit draining
- surrounded by synthesized logic ("digital sea")
- RD53A like



"analog islands in digital sea"

... complex designs can be made much faster now than in the early LHC days.

Current favorite large system layouts ...

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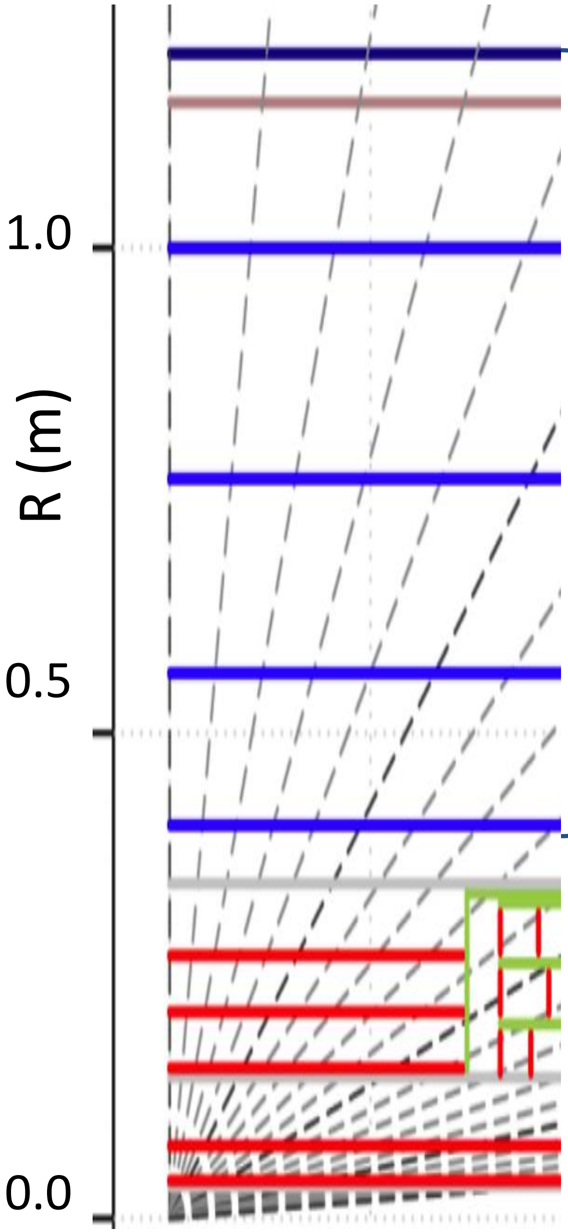
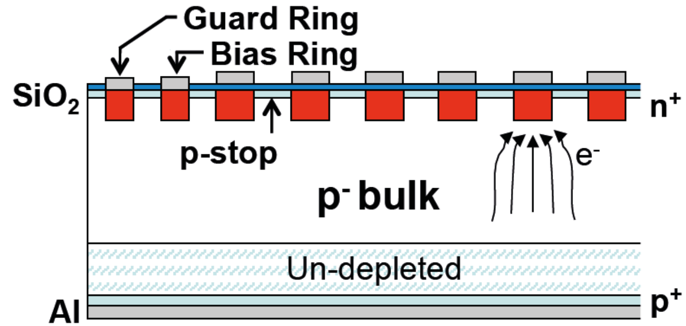


strips

outer pixel

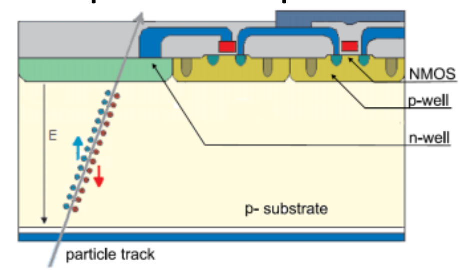
inner pixel

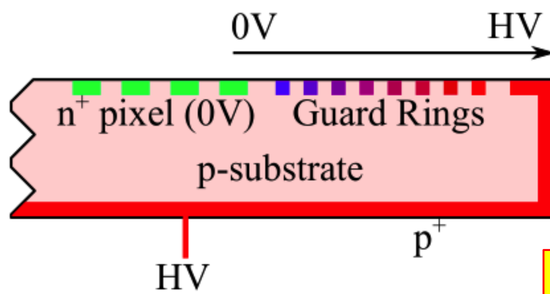
innermost pixel



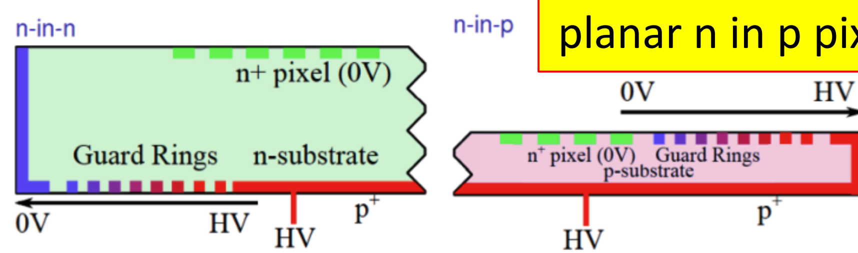
n in p
strip modules

depl. CMOS pixels

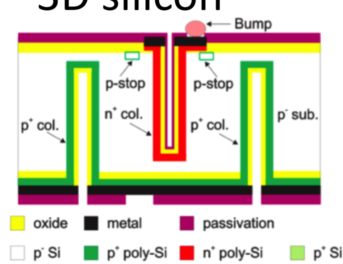




large modules
planar n in p pixels / CMOS?



3D silicon



dedicated
rad.-hard
detectors

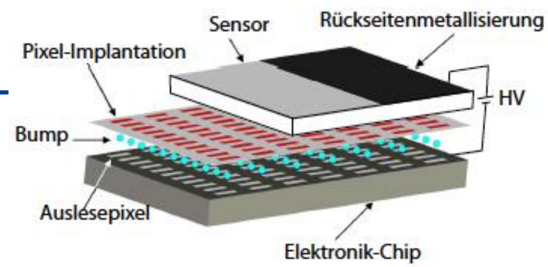
talks by
L. Rossi
J. Schwandt
B. Agkun

Monolithic pixel modules

- Monolithic pixels will never stand the LHC rates and radiation environment ... !?

- SOI pixel technology is fine, but it is difficult to get around the many challenges ... !?

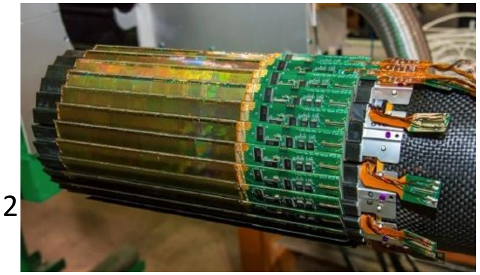
Hybrid Pixel Detectors



- **PROs** (split functionality)
  - complex signal processing in readout chip
  - zero suppression and hit storage during L1 latency
  - radiation hard chips and sensors to $>10^{15}\ n_{eq}/cm^2$
  - high rate capability (~MHz/mm^2)
  - spatial resolution ≈10 – 15 µm
  - **NEXT:** 3D integration (TSVs) ... from C2W to W2W assemblies
- **CONs**
  - relatively large material budget: >1.5% X_0 per layer
  - sensor + chip + flex kapton + passive components
  - support, cooling (-10°C operation), services
  - resolution could be better
  - complex and laborious module production
  - bump-bonding / flip-chip
  - many production steps
  - expensive
- hence: Monolithic pixels relying on commercial CMOS processes have come in focus (first outside LHC-pp -> also **for HL-LHC**)

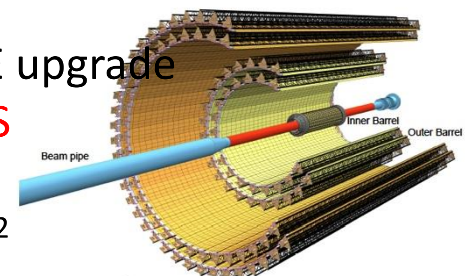
talks by W. Snoeys. H. Pernegger, I. Peric, T. Hirono, B. Hiti, D. Dannheim

STAR
MAPS
2014
0.16 m^2

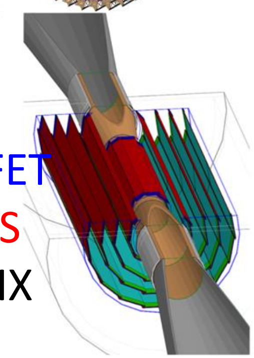


Belle II
DEPFET
2018
0.014 m^2

ALICE upgrade
MAPS
2021
10 m^2



ILC
DEPFET
MAPS
SOIPIX
20??



What is needed to realize (radhard) depleted CMOS pixels?

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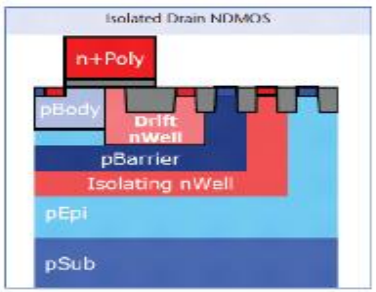
$$d \sim \sqrt{\rho \cdot V}$$

I. Peric, NIM A582 (2007) 876-885

1 **“High” Voltage add-ons to apply 50 – 200 V bias**

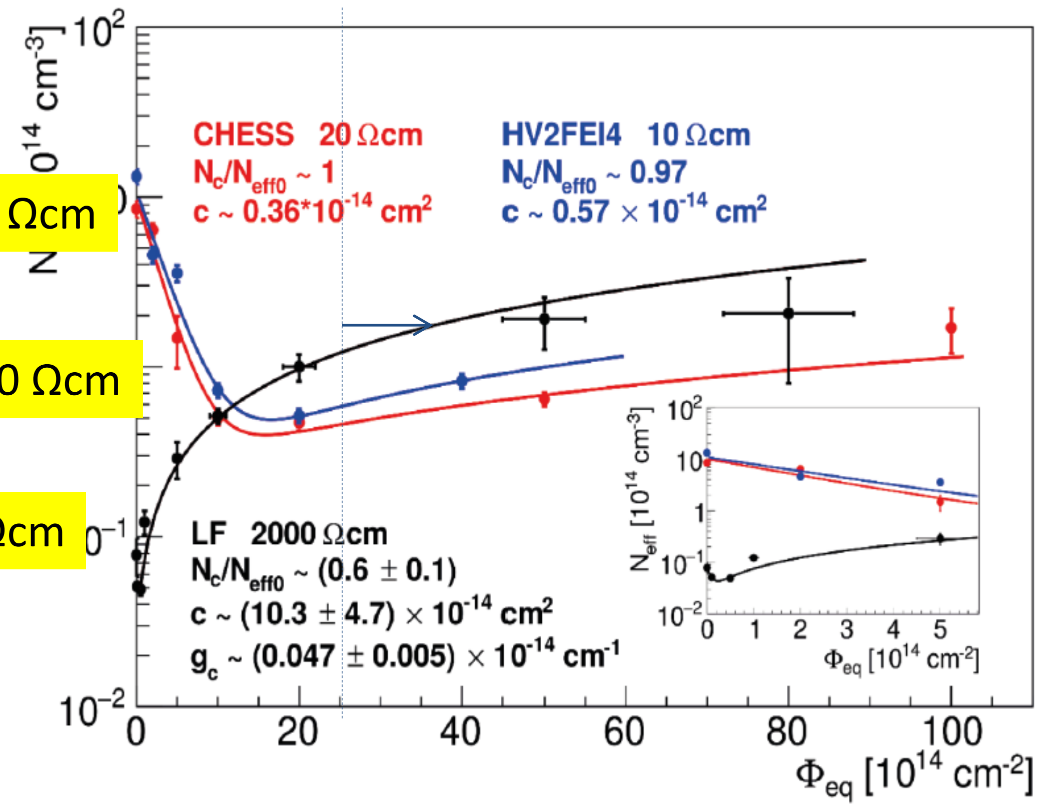
2 **“High” Resistivity Substrate Wafers (100 Ωcm – kΩ cm)**



from: www.xfab.com

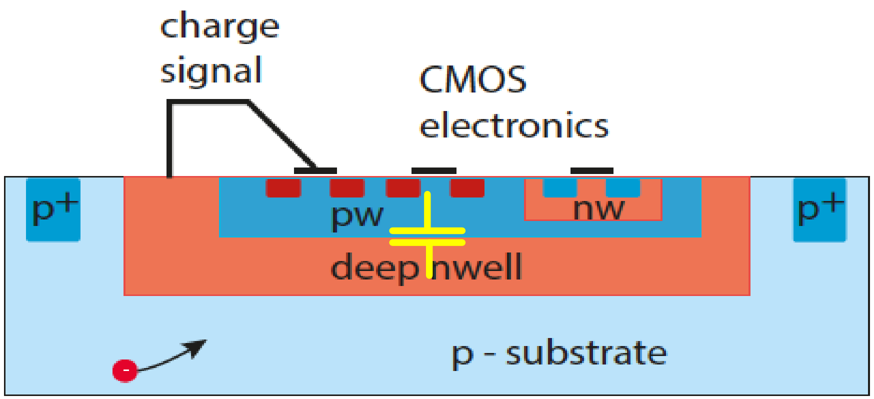
3 **Multiple (3-4) nested wells (for shielding and full CMOS)**

4 **Backside Processing (for thinning and back bias contact)**

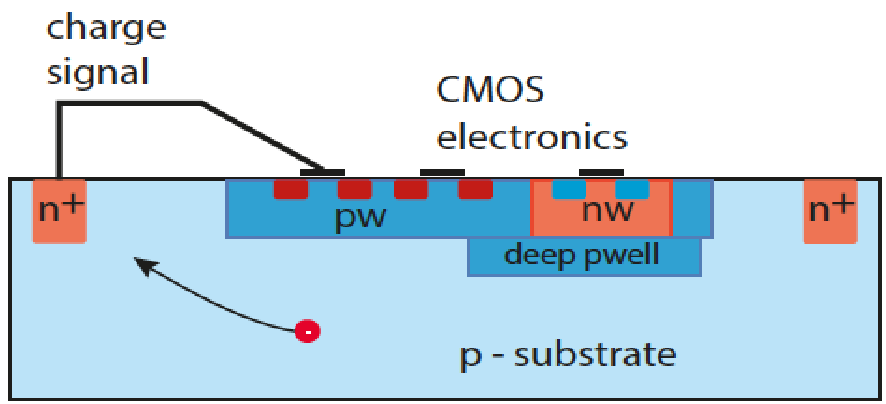


I. Mandic et al., JINST 12 (2017) no.02, P02021

The question of the fill-factor / electrode geometry



(a) Large fill-factor



(b) Small fill-factor

Electronics **inside** charge collection well

- Collection node with **large electrode**
  → no low field regions
  → on average **short(er) drift** distances
  → more **radhard**
- **Full CMOS** with isolation between NW&DNW
- **Large (> 100 fF)** sensor **capacitance** (due to DNW/PW junction!)
  → noise & speed or power penalties
  → x-talk possible (from digital to sensor) needs dedicated IC design

Electronics **outside** charge collection well

- Very **small sensor capacitance (~5 fF)**
  → noise low, speed high, power low
- on average longer drift distances and low field regions
  → **radhard?**
- also **full CMOS** with addn'l deep-p implant

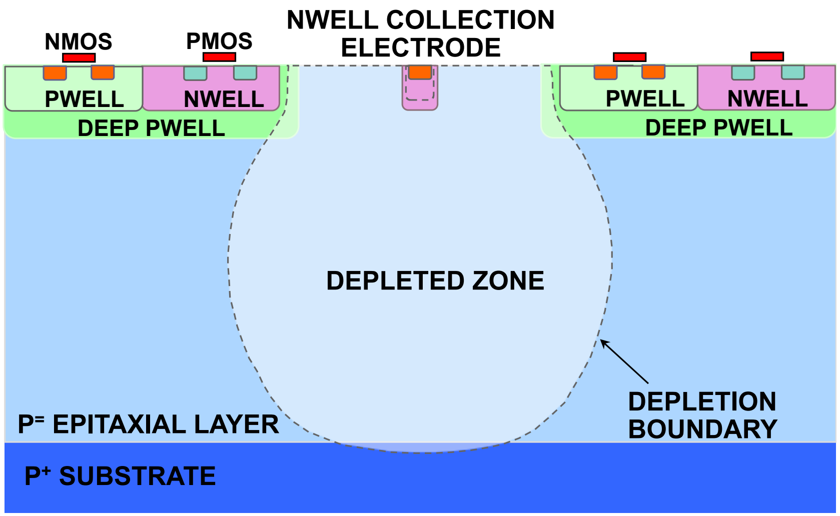
TJ Process modification of small electrode design

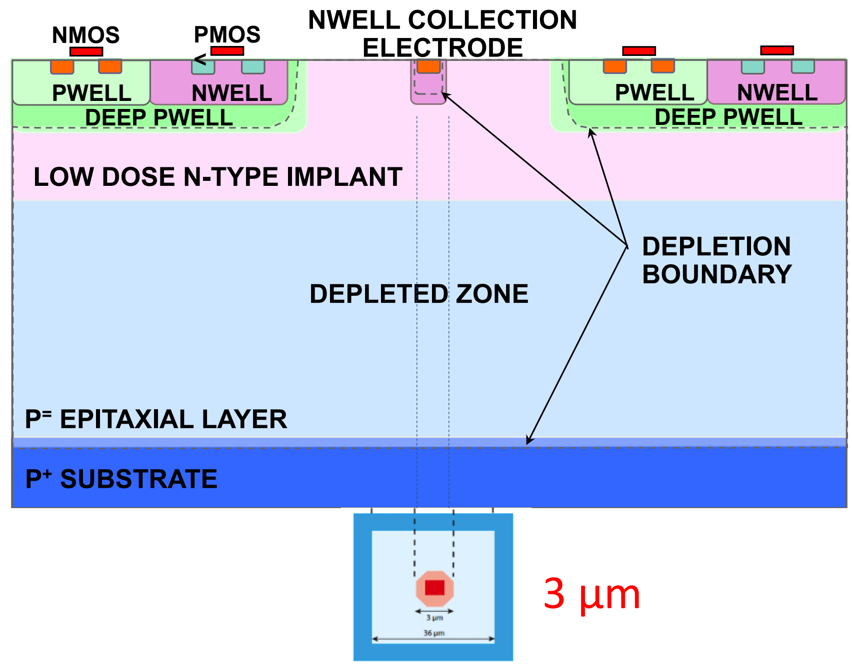
- **TowerJazz** 180 nm CMOS CIS
- deep PW full CMOS in pixel
- epi thickness: 18 – 40 μm
- Design derived from ALICE development
- **Modified process** to improve depletion & lateral E

W. Snoeys et al., NIM A871 (2017) 90 – 96.

Pixel dimensions:

- 36 x 42 μm^2 pixel size
- **3 μm diameter electrodes**
- Measured capacitance **<5fF**

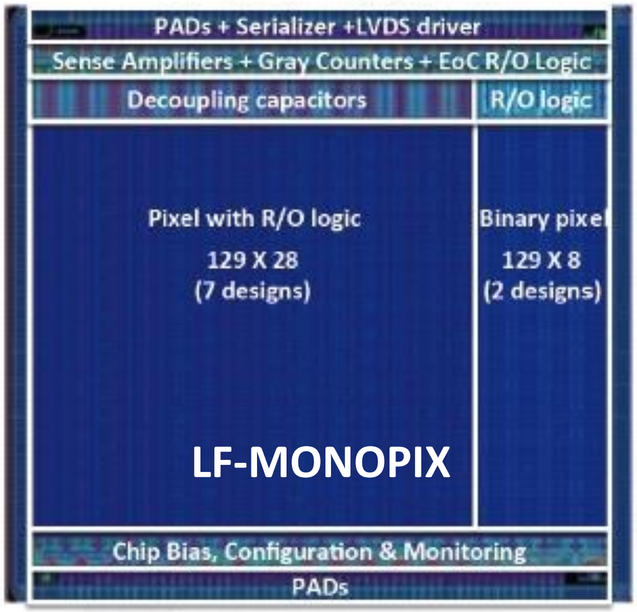


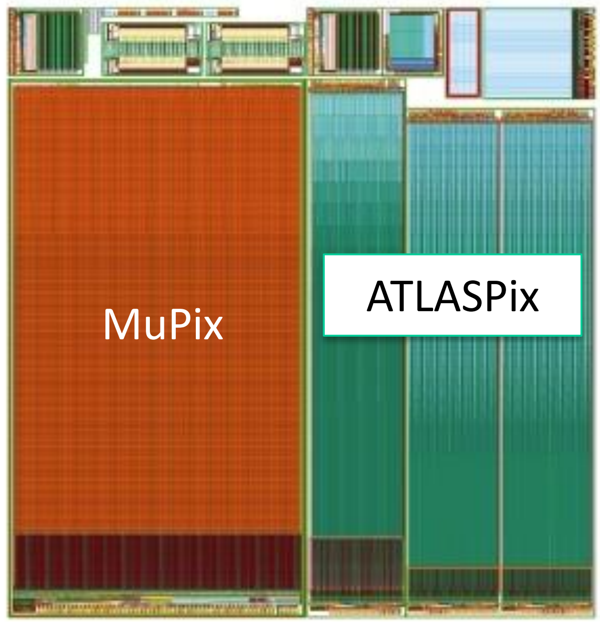


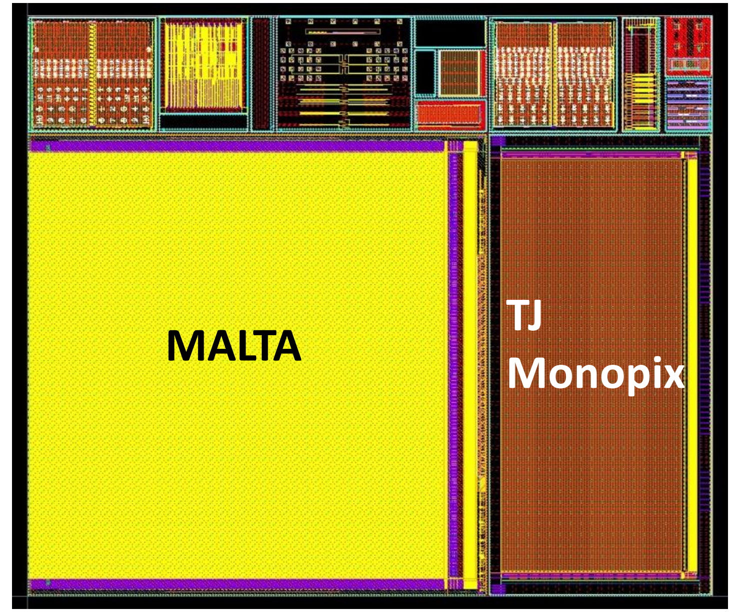
3 μm

36 μm

Large (~1 cm^2) full CMOS chips (=modules) w/ readout



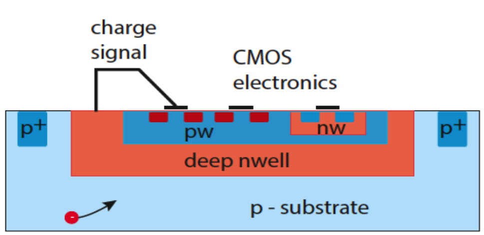




LFoundry 150 nm
substrate ρ > 2 kΩcm

ams 180 nm
substrate ρ ~ 0.08 - 1 kΩcm

TowerJazz 180 nm epitaxial (25 μm)
substrate ρ > kΩ cm



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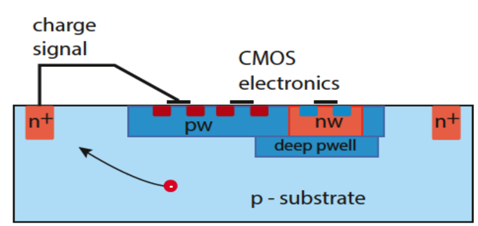
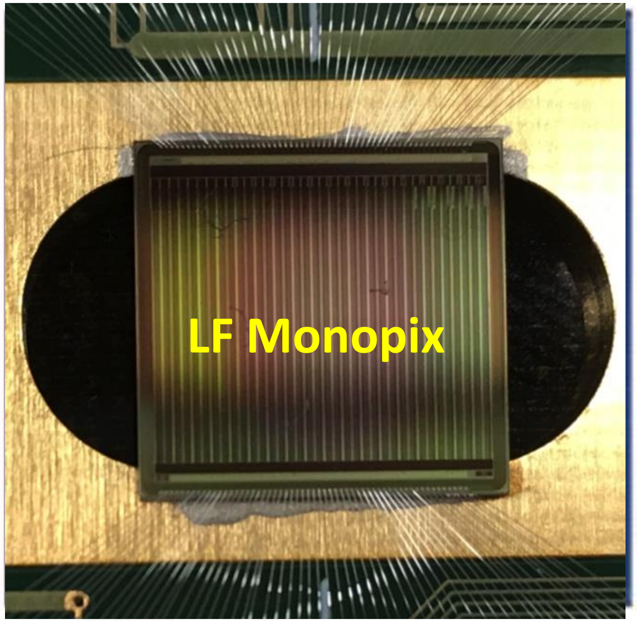
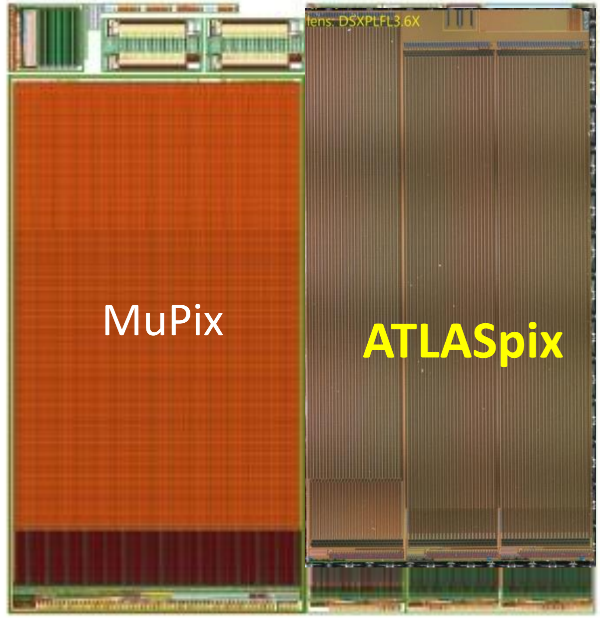


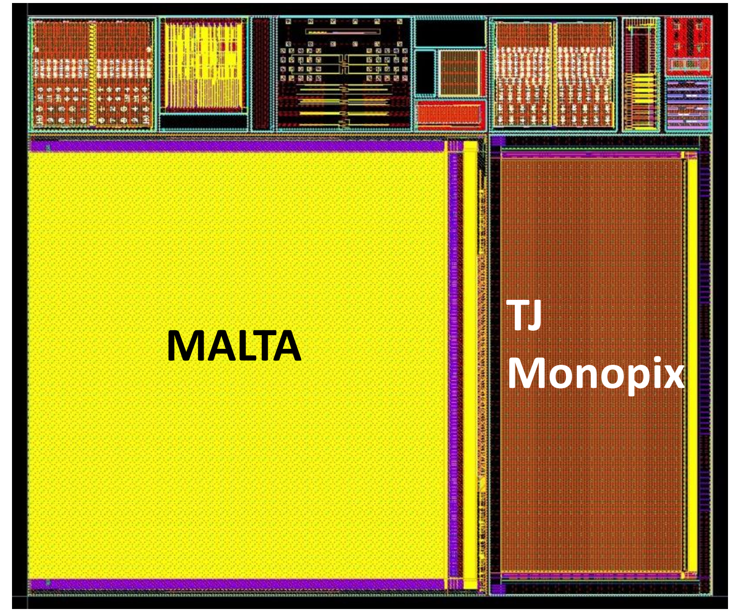
(b) Small fill-factor

talks by W. Snoeys. H. Pernegger, T. Hirono, I. Peric, D. Dannheim

Large (~1 cm^2) full CMOS chips (=modules) w/ readout







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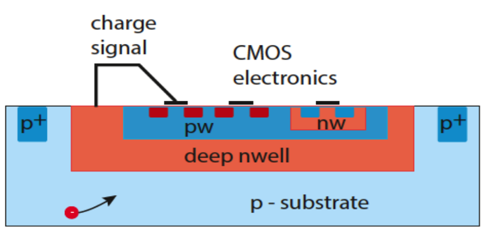

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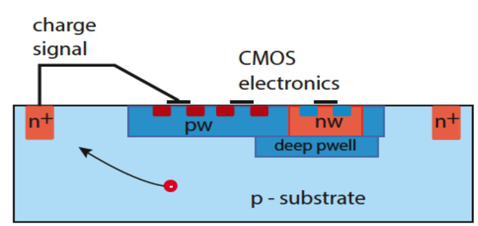

(b) Small fill-factor

talks by W. Snoeys. H. Pernegger, T. Hirono, I. Peric, D. Dannheim

Results extremely encouraging

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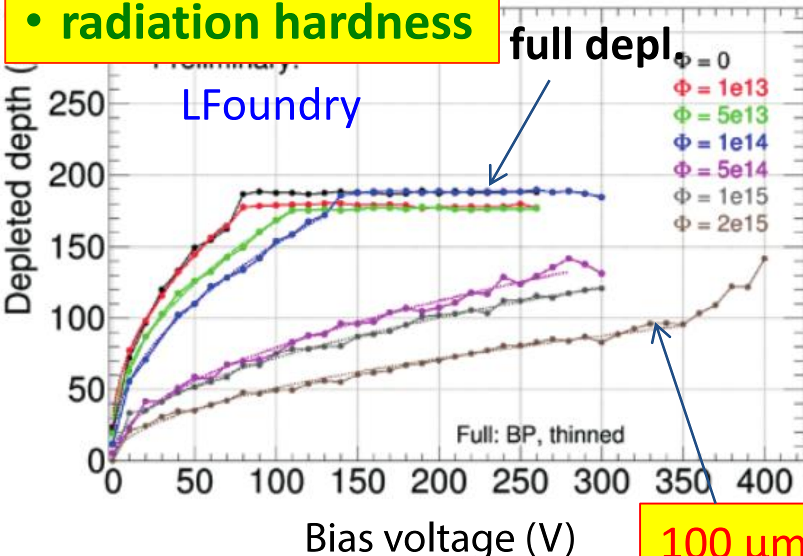
- **radiation hardness**

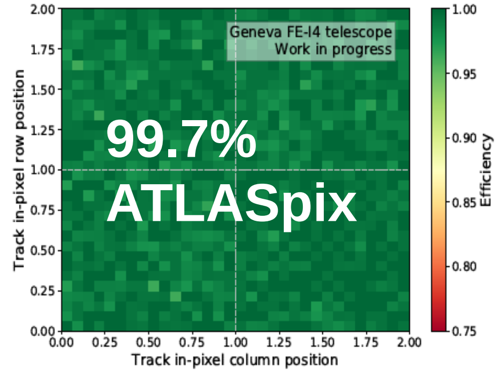
full depl.

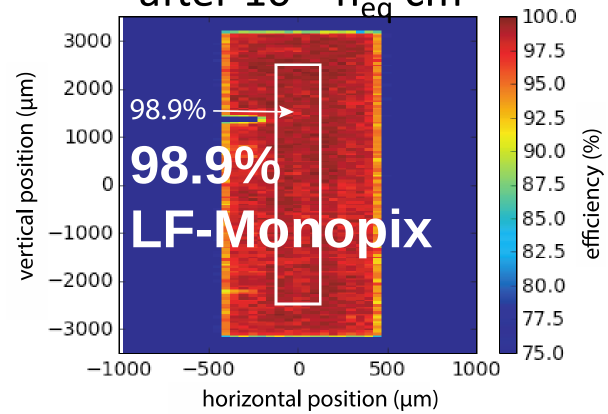


100 μm after 2x10^15

I. Mandić et al., JINST 12 (2017) no.02, P02021

- **efficiency**

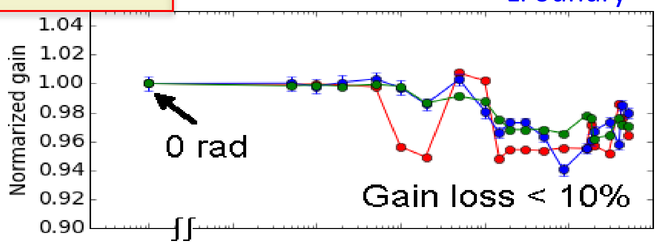




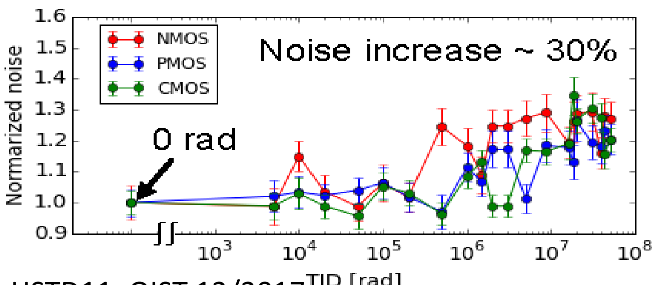
talks by H. Pernegger, T. Hirono, I. Peric

TID 1 MGy

gain



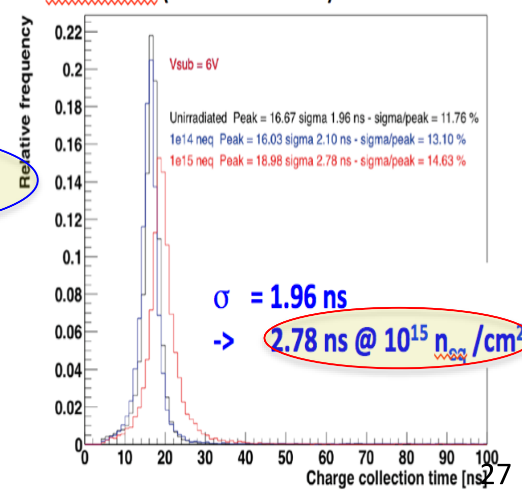
noise



- **timing**

ams180 after 1 x 10^{15} n_{eq}/cm^2

TowerJazz (small fill factor)

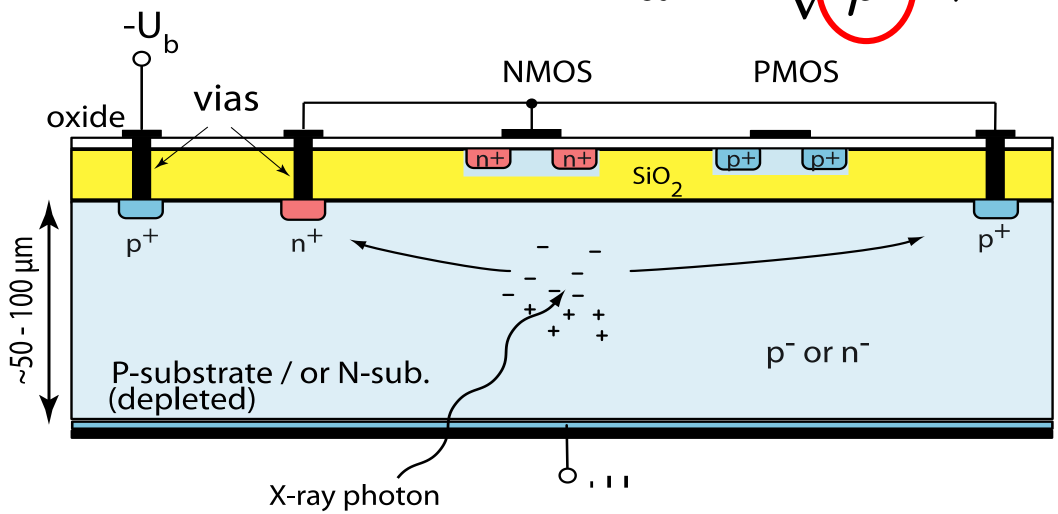


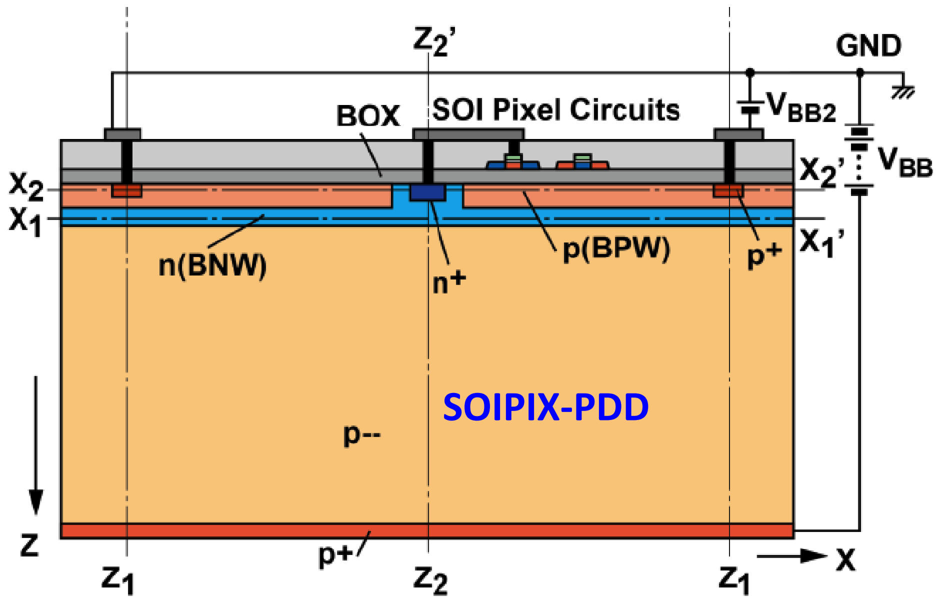
SOI pixels

Note again dedicated workshop included in this conference universitätbonn

FD CMOS on SOI

$$d \sim \sqrt{\rho \cdot V}$$





H. Kamehama et al., Sensors 2017

- **fully depleted SOI (thin film)** @ Lapis / KEK
- issues
  - back gate effect
  - coupling of sensor to circuit
  - radiation (TID) issues due to BOX
- cures developed in recent years
  - buried p-well, nested wells
  - "double SOI" structures

  => TID hard to 10 Mrad

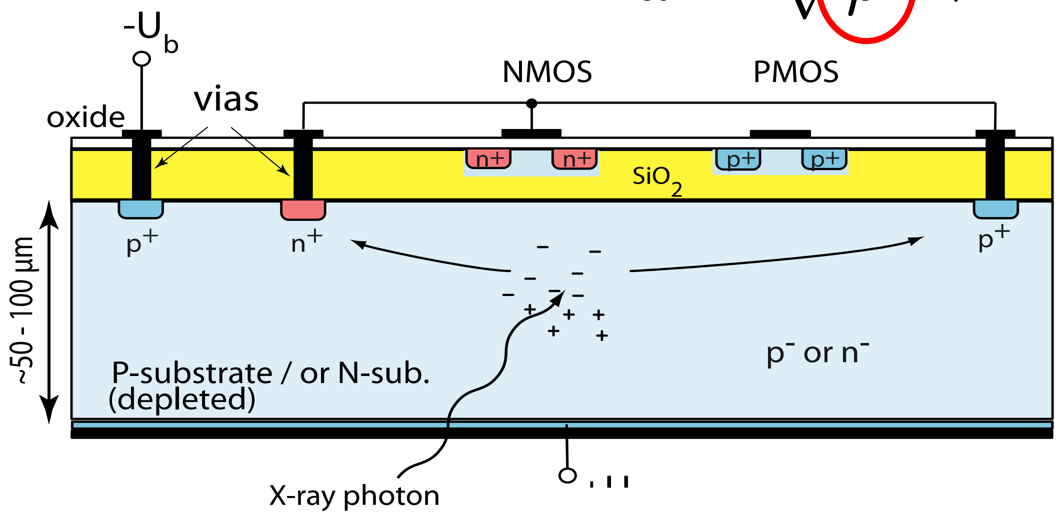
talks Y. Arai, K. Fukuda, S. Kawahito + SOI workshop

FPIX, SOFIST	particle tracking
INTPIX	X-ray
XRPIX, **SOIPIX-PDD**	X-ray astro
SOPHIAS	synchrotron rad.
cryogenic	far infrared
CNTPIX	counting -> biomed
MALPIX	ion spectroscopy

SOI monolithic pixels

FD CMOS on SOI

$$d \sim \sqrt{\rho \cdot V}$$



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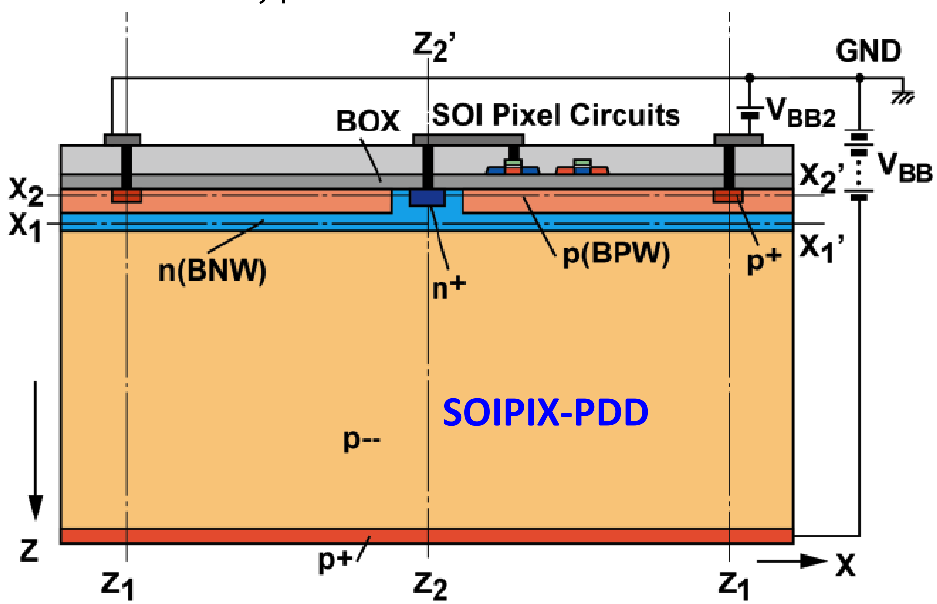

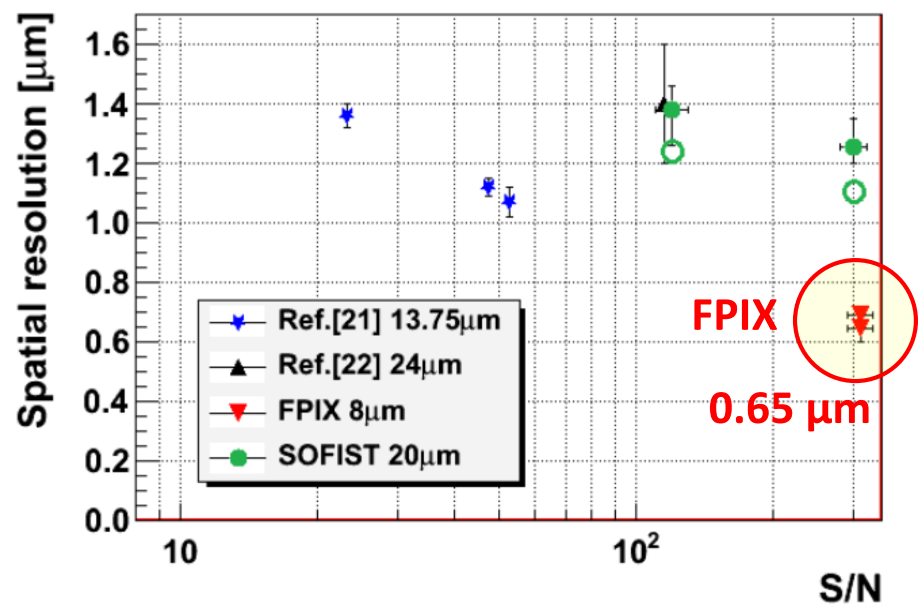

H. Kamehama et al., Sensors 2017

SOI monolithic pixels

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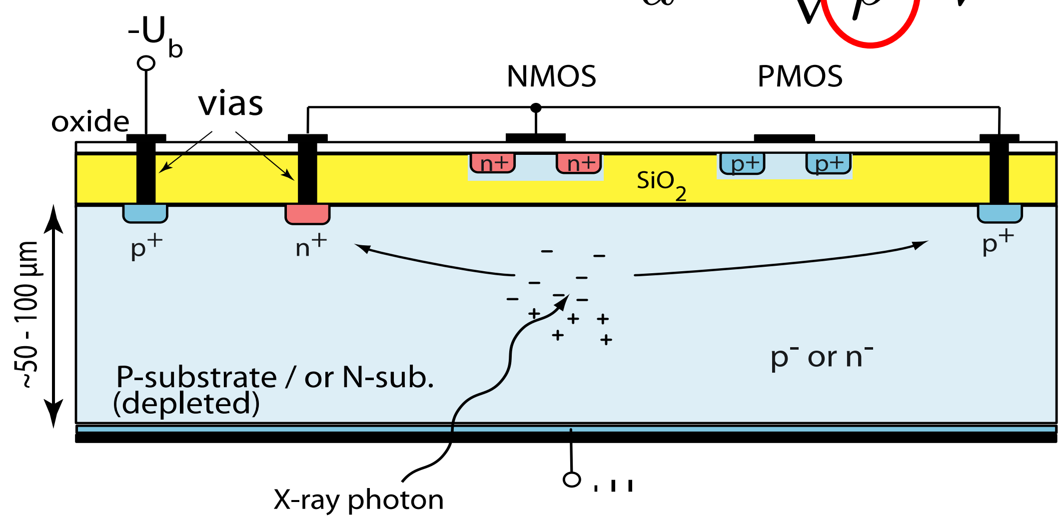
FD CMOS on SOI

$$d \sim \sqrt{\rho \cdot V}$$



- **fully depleted SOI (thin film)**
  @ Lapis/KEK
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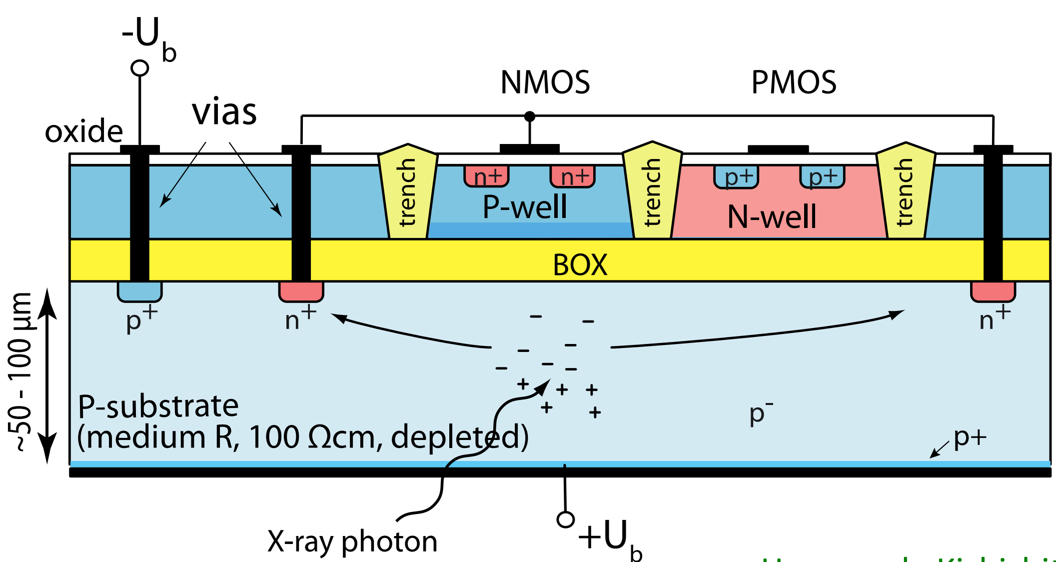


- **HV-SOI (thick film)**
- a promising alternative
- doped, non-depleted P- and N-wells prevent back gate effect and increase the radiation tolerance

Hemperek, Kishishita, Krüger, Wermes, NIM A796 (2015) 8-12

Time measurement with Si detectors

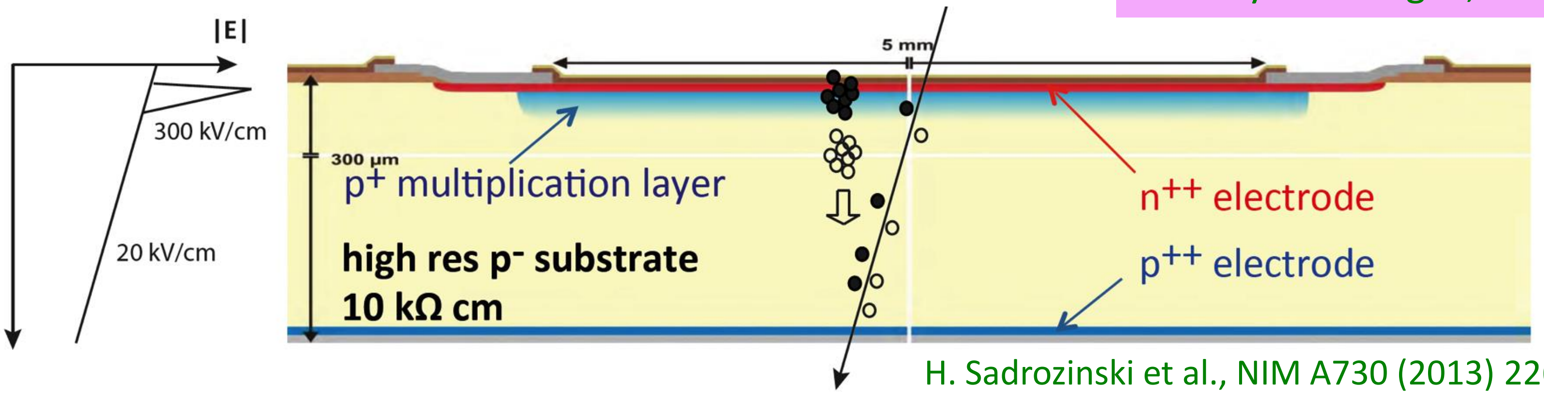
- Sub-ns timing with Si detectors is not possible ...!?
- Not with pixel detectors ...!?

4D tracking ... Δt = 30 ps <-> Δx = 1cm

Exploit charge amplification

- in "Geiger Mode" fashion (like in gas RPCs or in SiPMs)
  => σ_t governed by avalanche fluctuations
- OR .... in "linear mode" fashion -> Low Gain Avalanche Detectors (LGADs)

talks by N. Cartiglia, H. Sadrozinski, G. Pellegrini



H. Sadrozinski et al., NIM A730 (2013) 226-231, NIM A831 (2016) 18-23
N. Cartiglia et al., NIM A796:141–148, 2015; NIM A845 (2017) 47-51
H. Sadrozinski, A. Seiden, N. Cartiglia, arXiv:1704.08666

- Separate the "collection" of charge from the signal gain
- Figure of merit for σ_t is the "slew rate" dV/dt ≈ Signal/τ_{rise}

Need: fast drift + large S/N

$$\sigma_t^2 = \underbrace{\left(\frac{V_{th}}{dV/dt}\bigg|_{rms}\right)^2}_{\sigma^2_{\text{time walk}}} + \underbrace{\left(\frac{\text{Noise}}{dV/dt}\right)^2}_{\sigma^2_{\text{noise}}} + \sigma^2_{\text{arrival}} + \sigma^2_{\text{dist}} + \sigma^2_{\text{TDC}}$$

arrival fluct.   distortion low w-field

- thin (!!)
- HV
- intr. amplification
- (small electrodes)
- broad-band amplifier

LGAD – successes so far ... and current challenges

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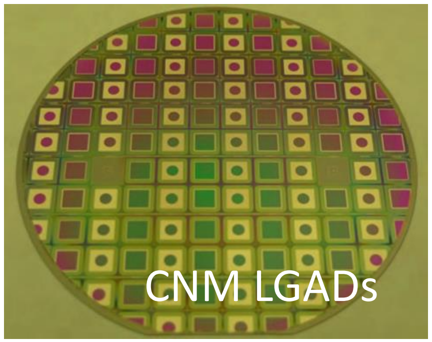
- ❑ Ultimate Goal: simultaneous space (~10µm) AND time resolution (< 50 ps) ... no pixels yet !
- ❑ Concrete application: ATLAS (HighGranularityTimingDetector; Forward) -> pile-up killer
  CMS-TOTEM (in Roman Pots)



LGAD
pad (~1 mm²)
detectors

G. Pellegrini et. al, NIM A 765 (2014) 12–16.
G. Pellegrini et al., HSTD 2015, arXiv:1511.07175

H. Sadrozinski et al., NIM A730 (2013) 226-231,
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N. Cartiglia et al., NIM A796:141–148, 2015;
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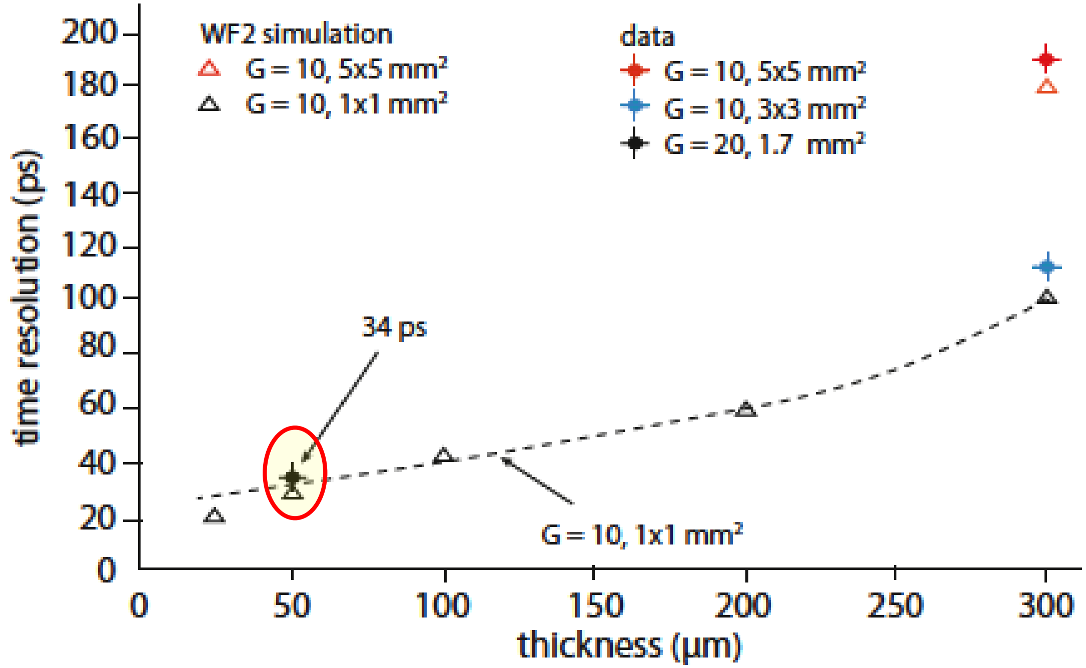
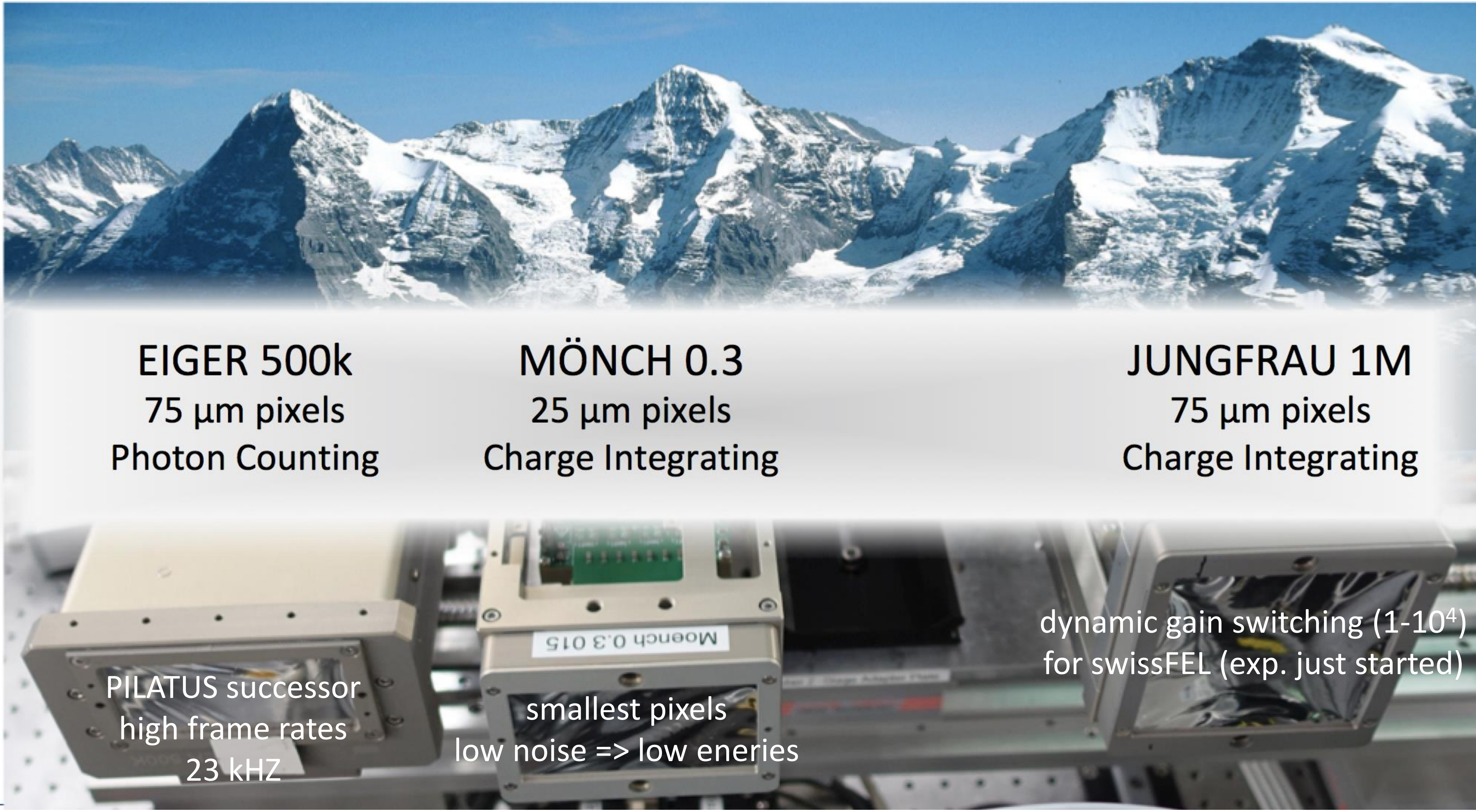


- ❑ main problem: gain variation with fluence (due to high doping of amplification region)
  (especially annoying in varying radiation fields)
  also: amplification no longer in metallurgical p-n junction only (so what!)
- ❑ current directions:
  (1) substitute B with Ga as acceptor dopant -> ?
  (2) Carbon-enriched p-silicon wafers ... ?

Pixel Imaging SYSTEMS (!!)

Hybrid Pixels for SLS @ PSI



talk by G. Carini

Hybrid Pixels for SLS @ PSI

mask made from photo

EIGER 500k	MÖNCH 0.3	JUNGFRAU 1M
75 µm pixels	25 µm pixels	75 µm pixels
Photon Counting	Charge Integrating	Charge Integrating

- ❑ 25 x 25 µm^2 bumped (!) pixels
- ❑ 320 eV energy resolution FWHM -> interpolation possible -> 1 µm res.
- ❑ Large dynamic range

AGIPD (adaptive gain) ... EU XFEL Pixel Detector

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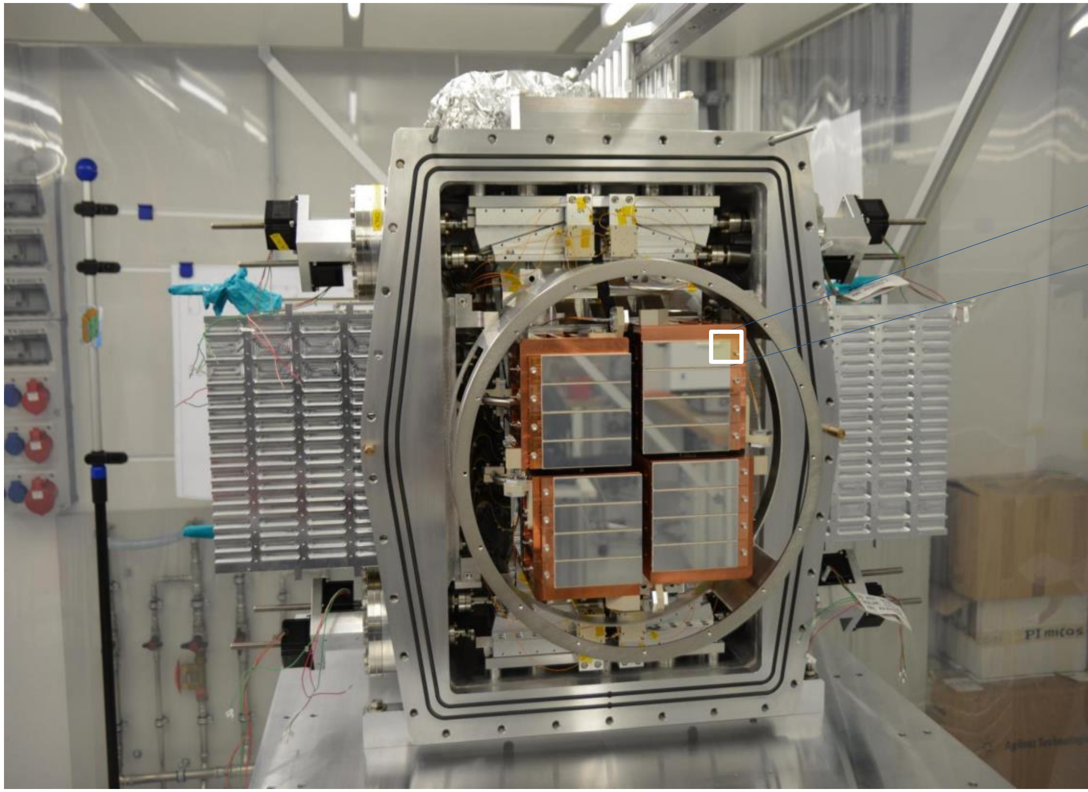
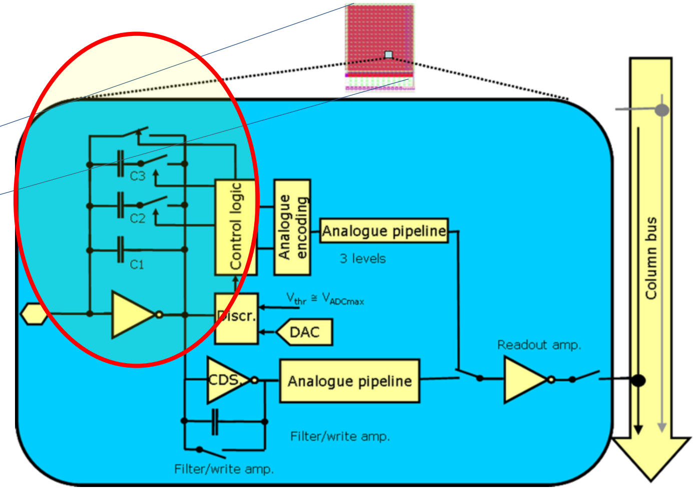
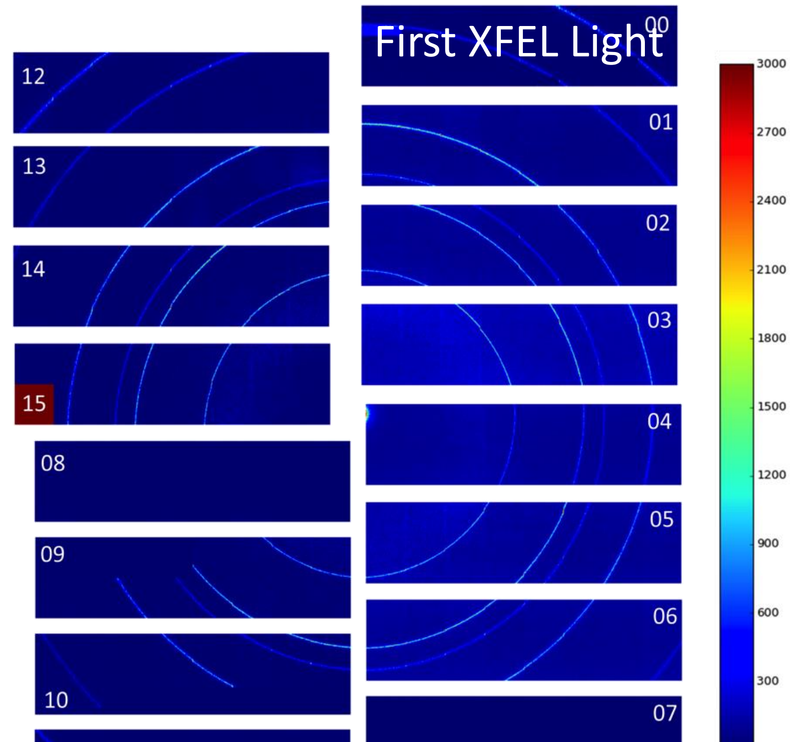
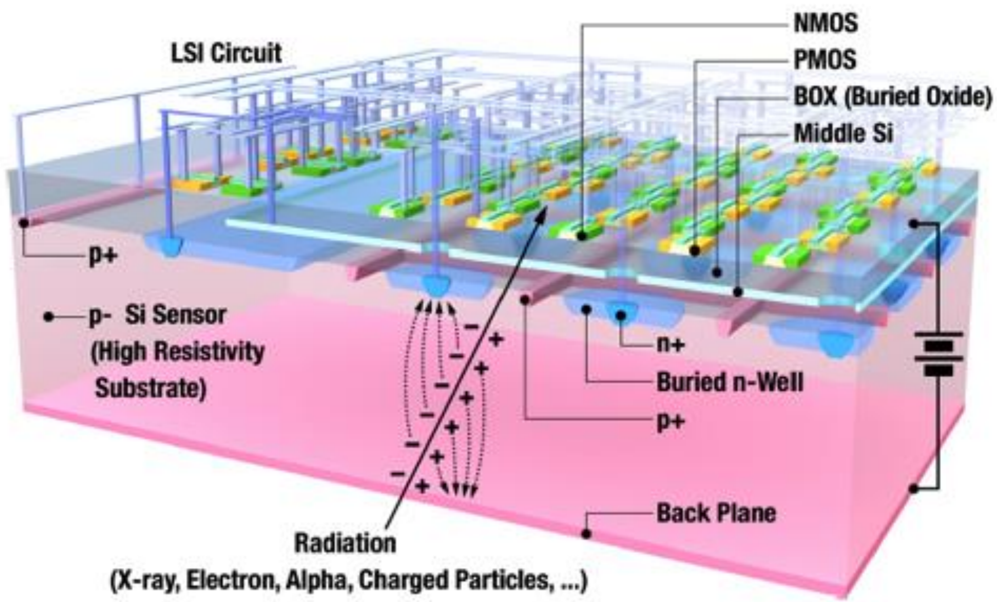






- addressing >10^4 dynamic range @ EU XFEL
- by "adaptive gain stages" (as JUNGFRAU)
- first XFEL Light has been seen ...

X-ray imaging with Monolithic SOI Pixels



Double SOI pixel detector
with > 10 Mrad TID tolerance

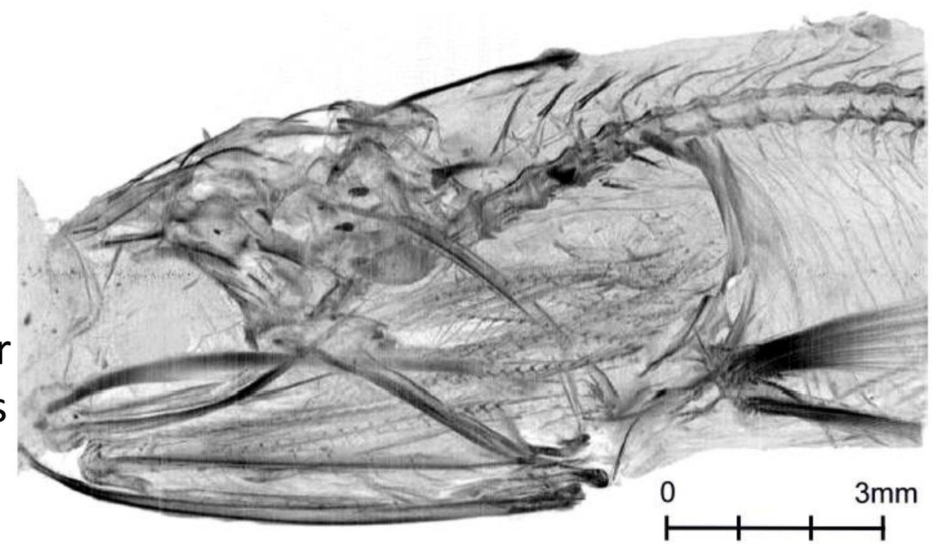


Image taken with single SOI pixel detector
17 x 17 μm^2 pixels, **500 µm** bulk thickness

Conclusions

- Silicon detectors remain the working horse for tracking and imaging detectors, especially in high rate and/or high radiation environments.
- This HSTD11 (2017) Conference is an excellent forum presenting the current state of the art.

BACKUP

Radiation effects in 65 nm CMOS small channel devices

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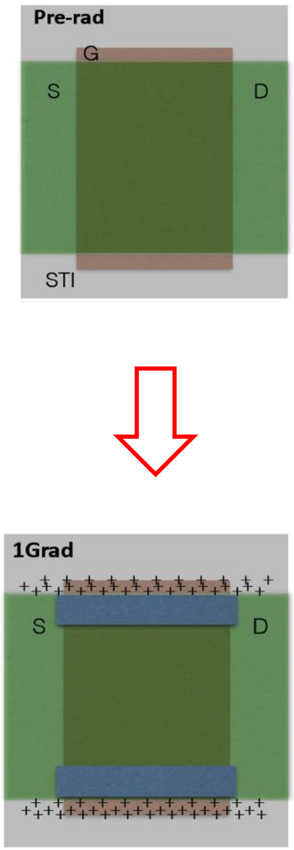
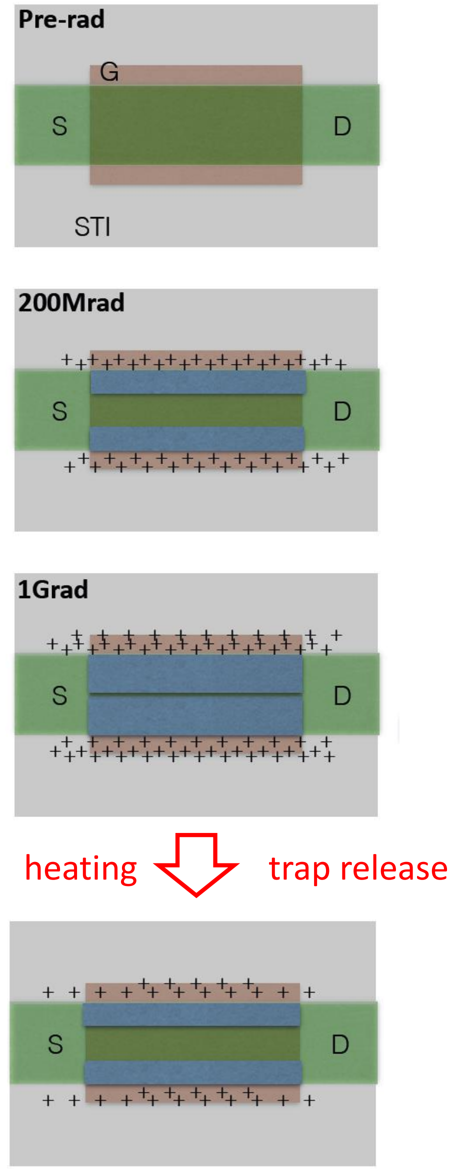
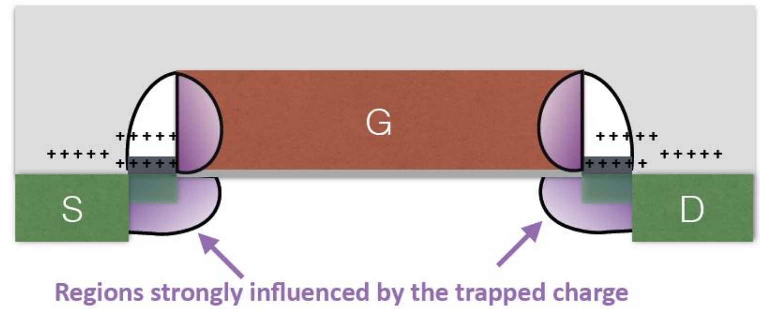
W = moderate size



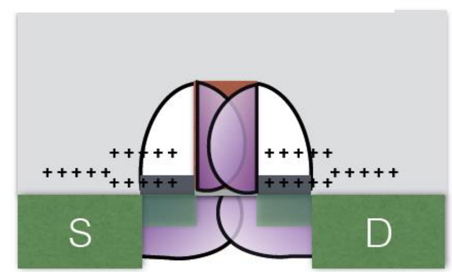
W = minimum size



L = moderate size



L = minimum size



cartoons: F. Faccio, TWEPP2015

Performance of sensor fabricated in CMOS

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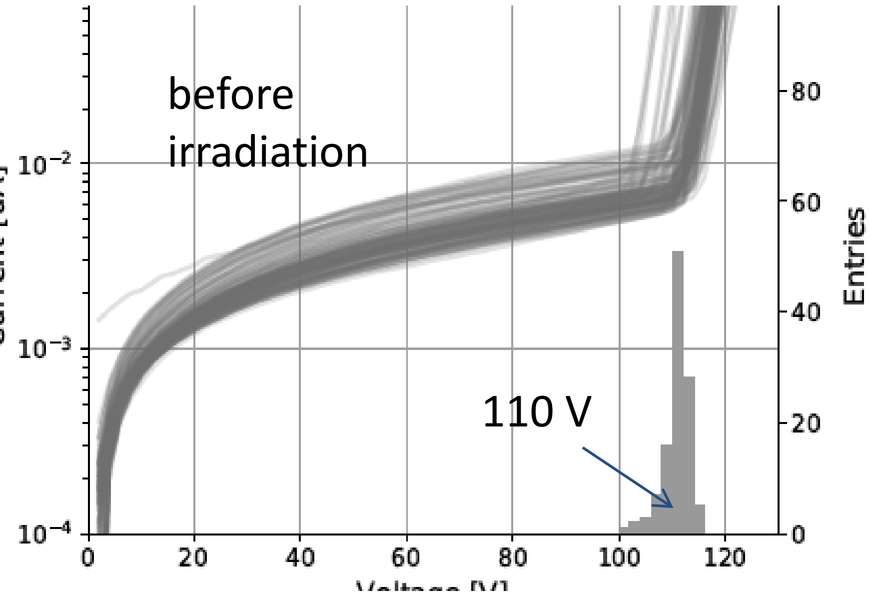
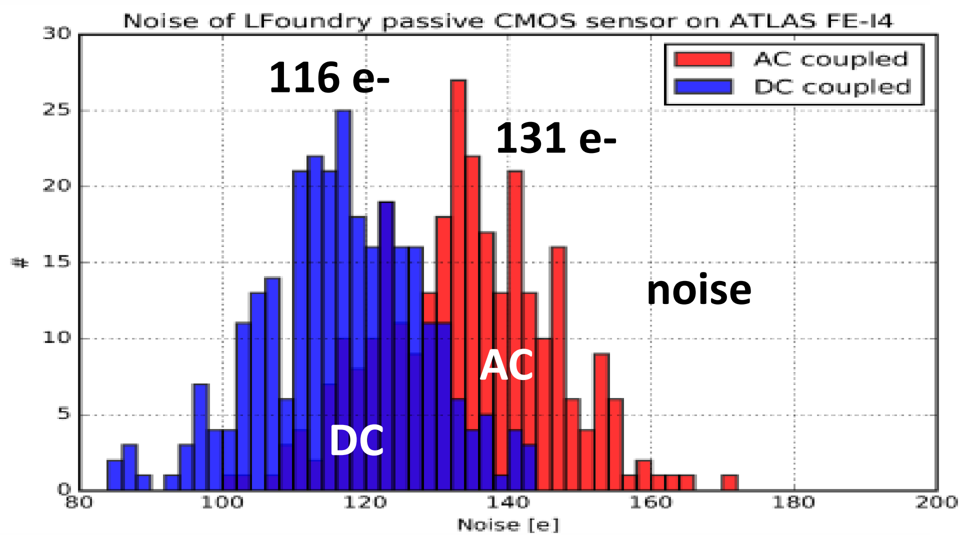
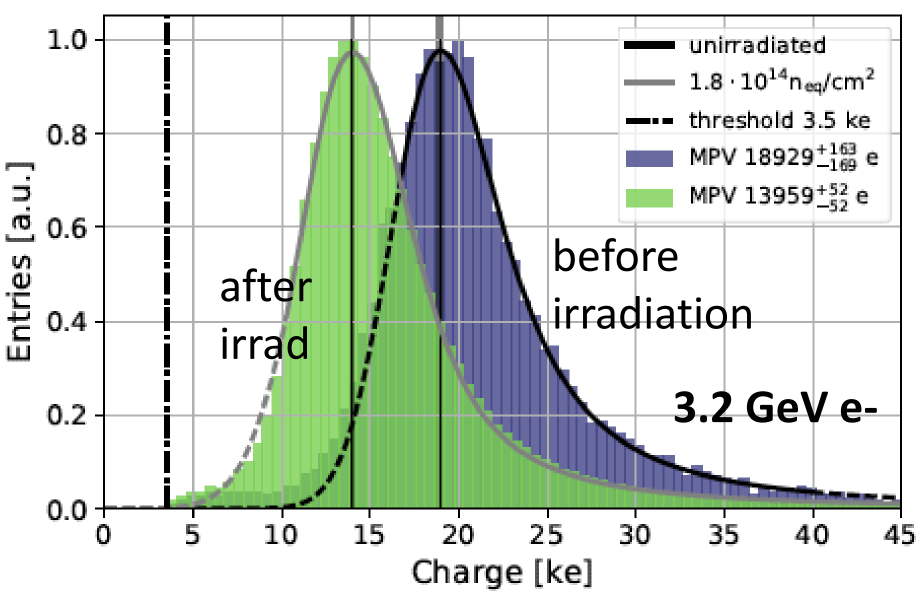


- **IV** curves of all samples ok (bias 120 V -> 500 V)
- about **220 µm** depletion depth
- leakage current **20 µA / cm³** (IBL: 15 µA/cm³)
- **noise** as in standard sensors
  - planar sensors (C_D = 117 fF): ENC = 120 e-
  - 3D-Si sensors (C_D = 180 fF): ENC = 140 e-
- **high efficiency after irradiation** (1 x 10^{15} n_{eq}/cm^2)





compare IBL
- planar sensors (C_D = 117 fF): ENC = 120 e-
- 3D-Si sensors (C_D = 180 fF): ENC = 140 e-

D.-L. Pohl et al., JINST 12 (2017) no.06, P06020