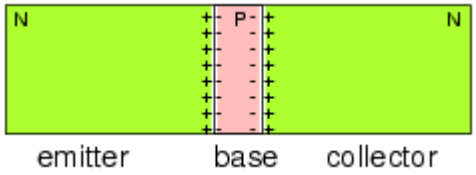
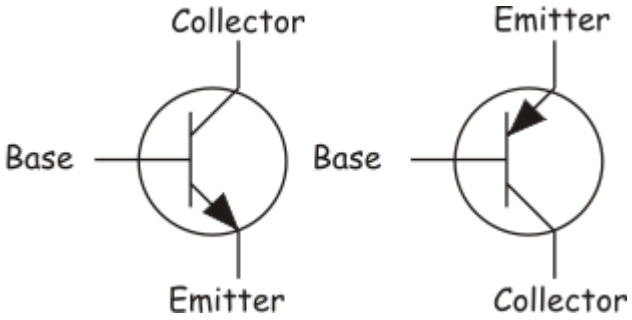
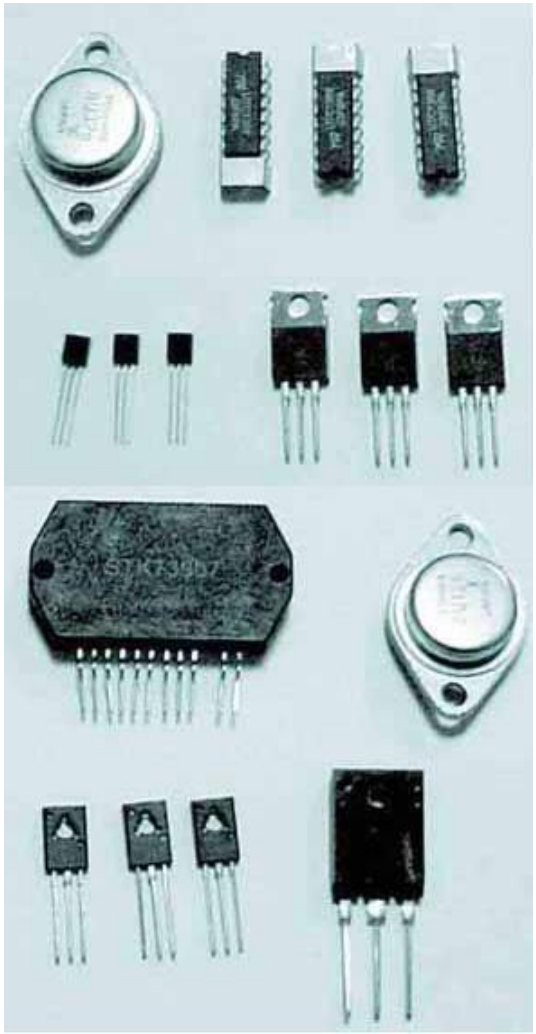
Short column around “Transistor”

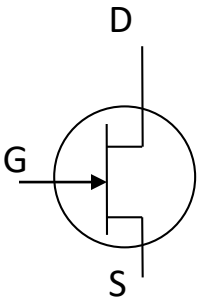
Transistor, FET, CMOS



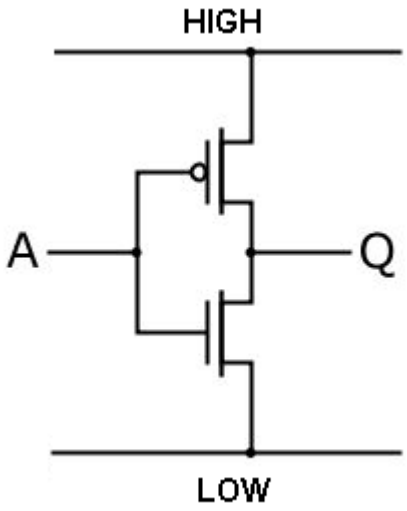


Transistor





FET

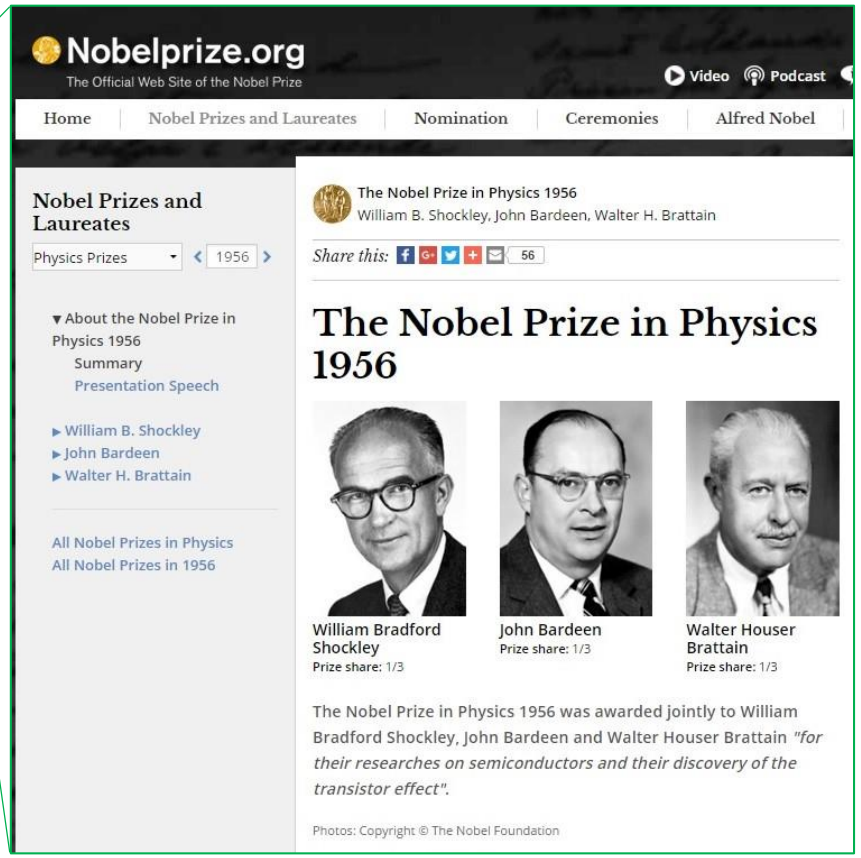


CMOS

You can refer, such as, https://www.allaboutcircuits.com/textbook/semiconductors/

Timeline

1925: Julius Edgar Lilienfeld's MESFET patent
1935: Oskar Heil's MOSFET patent
194?: Unpublished Bell Labs MESFET
1947: Ge BJT (Bardeen, Brattain, Shockley, Bell Labs)
1954: Si BJT (Teal, Bell Labs)
1960: MOSFET (Atalla&Khang, Bell Labs)
1961: Integrated circuit (Kilby, TI)
1963: CMOS (Sah&Wanlass, Fairchild)
1964: Commercial CMOS IC (RCA)
1965: DRAM (Fairchild)
1968: Poly-Si gate (Faggin&Klein, Fairchild)
1968: 1-FET DRAM cell (Dennard, IBM)
1971: UV EPROM (Frohman, Intel)
1971: Full CPU in chip, Intel 8008 (Faggin, Intel)
1974: Digital watch
1974: Scaling theory (Gänsslen&Dennard, IBM)
1978: Use of ion implanter
1978: Flotox EEPROM (Perlegos, Intel)
1980: Ion-implanted CMOS IC
1980: Plasma etching
1984: Scaling theory <0.25 **µ**m (Baccarani, U. Bologna)
1986: 0.1 **µ**m Si MOSFET (Sai-Halasz, IBM)
1991: CMOS replaces BJT also at high-end
1993: DGFET scalable to 30 nm (theory, Frank *et al*.)
2007: Non-SiO_2 (HfO_2–based) MOSFET (Intel)



Left list is taken from a slide made by M. Fischetti, "history of the MOSFET from a physicist's perspective"

Reference : Nobel Prize List awarded to scientists working at Bell Laboratories
(from https://www.bell-labs.com/our-people/recognition/)

Nobel Prize in Physics

total 7

2009
Willard S. Boyle and George E. Smith
Invention of the charge-coupled device (CCD), for electronic memory, which made the Charge Coupled Device (CCD) image sensor possible.

1998
Horst Störmer, Daniel Tsui, and Robert Laughlin
Discovery and explanation of a new form of quantum fluid with fractionally charged excitations (the Fractional Quantum Hall Effect.)

1997
Steven Chu
Development of methods to cool and trap atoms with laser light. (Prize shared with Claude Cohen-Tannoudji and William D. Phillips.)

1978
Arno A. Penzias and Robert W. Wilson
Discovery of the cosmic microwave background radiation that in turn provided clear substantiation of the "big bang" theory of how the universe began.

1977
Philip W. Anderson
Fundamental theoretical insights into the electronic structure of magnetic and disordered systems". (Prize shared with Sir Nevill Francis Mott and John Hasbrouck van Vleck.)

1956
John Bardeen, Walter H. Brattain and William Shockley
Research on semiconductors that led to the invention of the transistor in 1947.

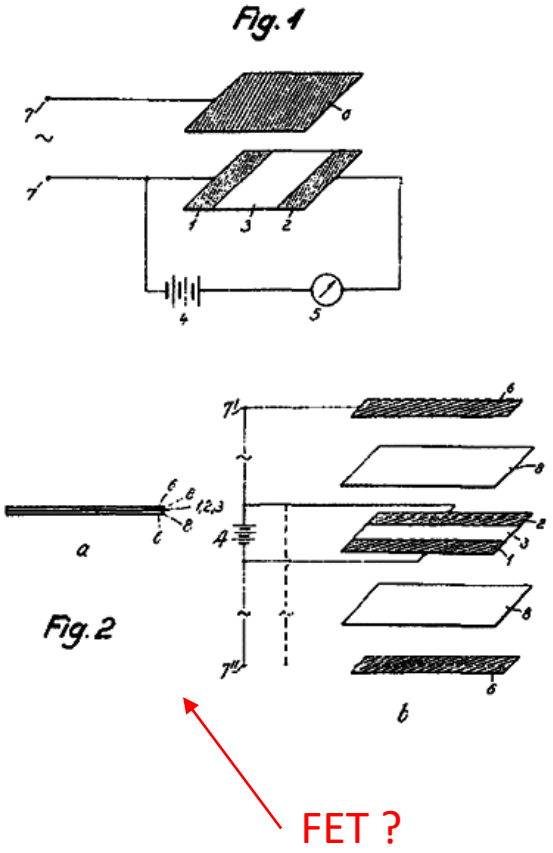
1937
Clinton J. Davisson
Discovery of the diffraction of electrons by crystals and demonstrated the wave nature of matter. (Prize shared with George Paget Thomson.)

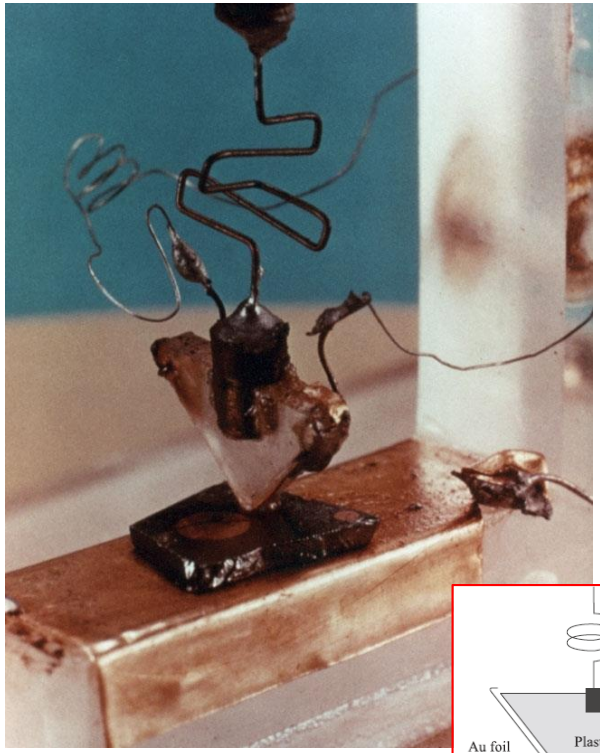
Nobel Prize in Chemistry

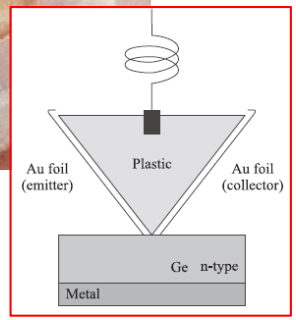
total 1

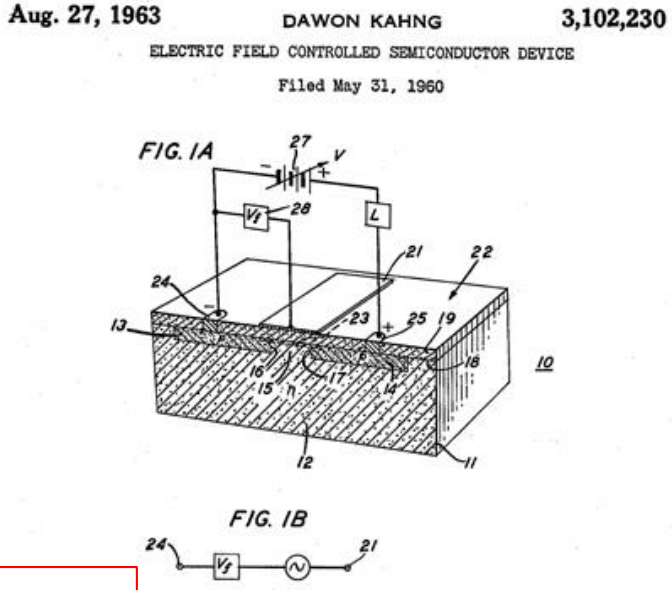
2014
Eric Betzig
Eric Betzig was awarded 2014 Nobel Prize in Chemistry “For the Development of Super-Resolved Fluorescence Microscopy” which is capable of measuring images of molecules from within living cells.

Transistor prehistory









1935 Heil's patent

1947 First BJT
Bardeen, Shockley, Brattain (Bell Labs)

1960 Atalla's MOSFET

#Figures are taken from a slide made by M. Fischetti, "history of the MOSFET from a physicist's perspective"

. . . World without semiconductor (transistor) is outside of our imagination now …

Everyday Life


Television

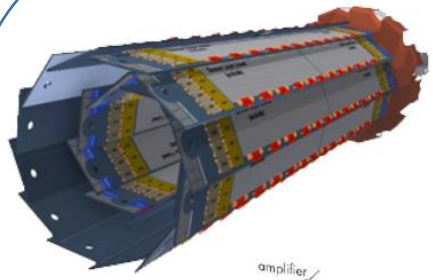

Advanced Medical Care

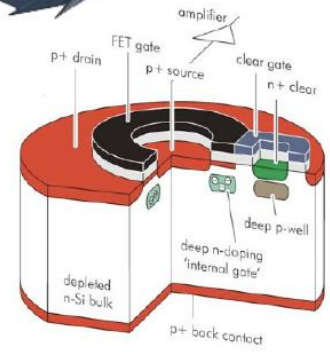

Personal Computer


Mobile Phones / Smart Phones

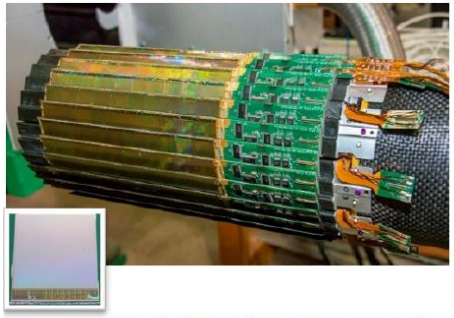

Automobile

Science

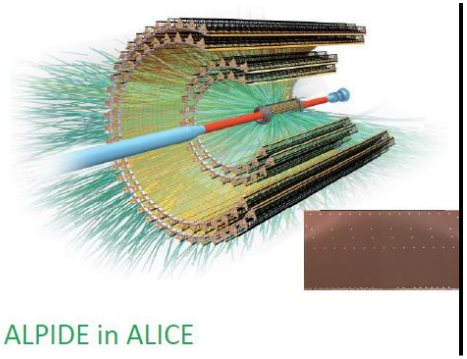




DEPFET in Belle

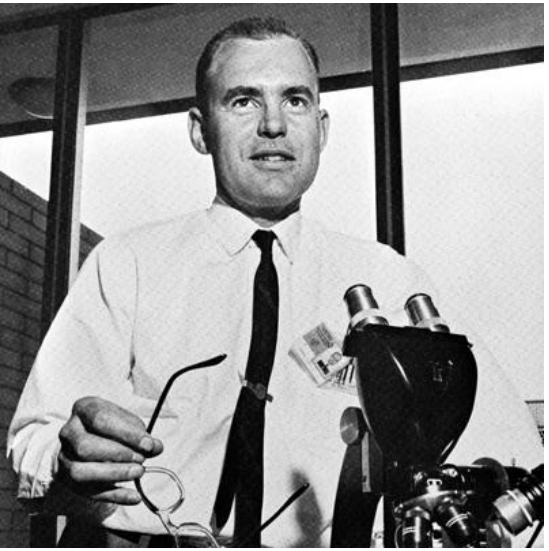


MIMOSA28 (ULTIMATE) in STAR

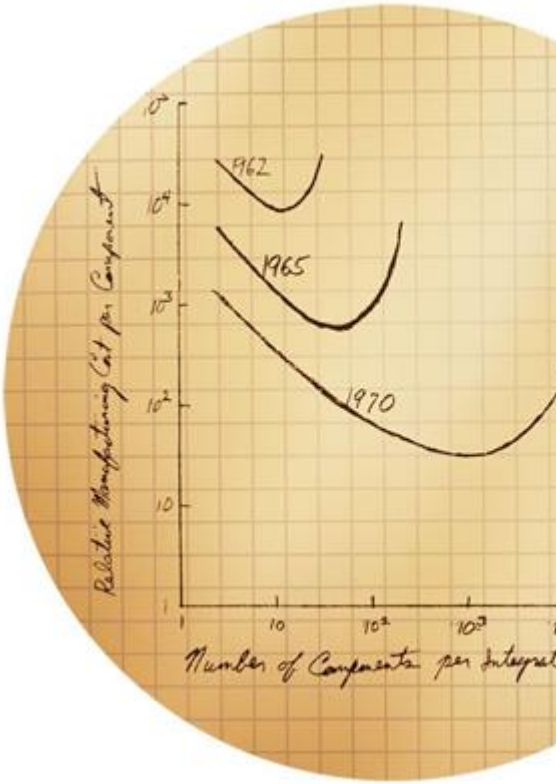


ALPIDE in ALICE

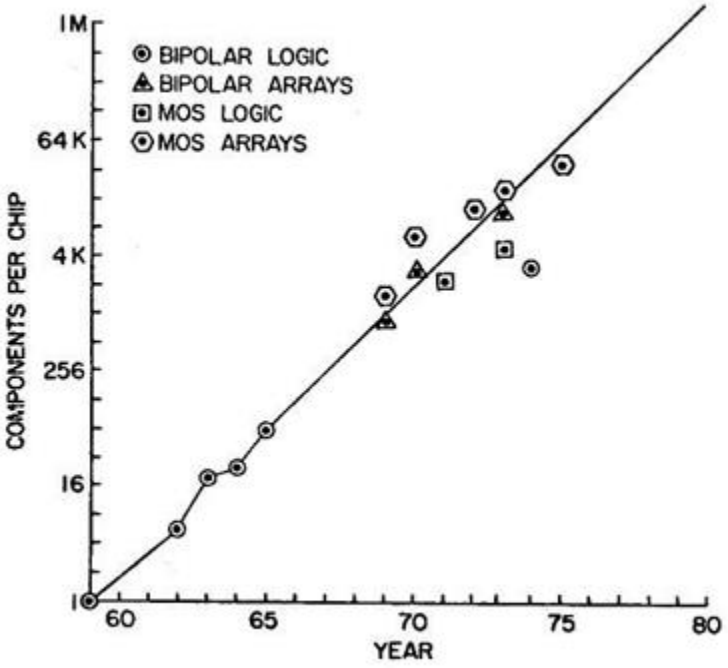
Moore's law



Gordon Moore



1965: Cost vs time



Moore's law 1960-1975

"Moore's law" = number of transistors in an IC has been increasing exponentially with time (usually, the rate is "double" within 2-3 years.)

Plot's with Moore's law

#1 "Transistors" are almost replaced with CMOS

#2 The (minimum) size/scale of the first generation transistor is 10 μm

#3 Gradually, "feature" size and the minimum size do not coincide. But "feature" size is still a good benchmark.

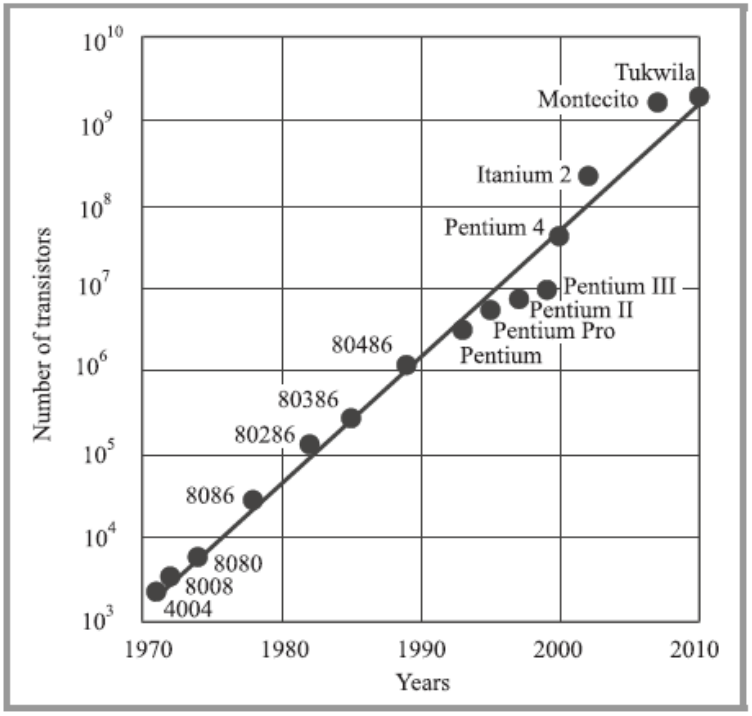


Fig. 7. Number of transistors in successive Intel processors as a function of time (data after [44]).

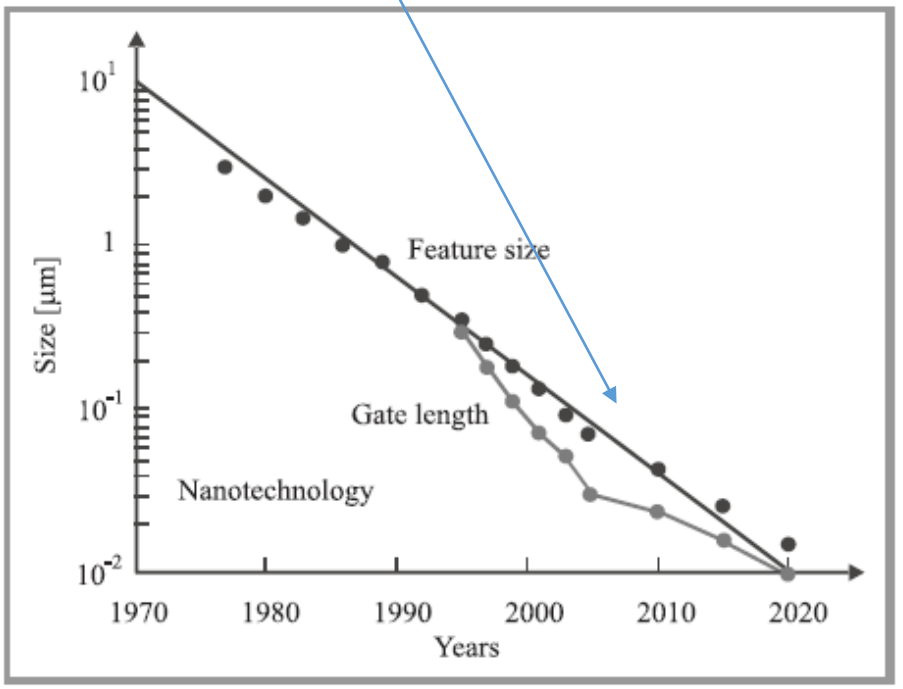


Fig. 8. Feature size as a function of time (data after [45]).

From Lidia Lukasiak and Andrzej Jakubowski, "History of Semiconductors"

IEEE Advancing Technology for Humanity

International Roadmap for Devices and Systems

IRDS: a committee to make a roadmap for semiconductor

1. IRDS More Moore mission

See https://irds.ieee.org/reports

System scaling enabled by Moore's scaling is more and more challenged with the scarcity of resources such as power and

.....

- Ground rule scaling slows down and saturates around 2024. EUV (extrame-ultraviolet) technology now started to slow down this saturation trend by having the cost under control thanks to process complexity reduction. Transition to 3D integration and use of beyond CMOS devices for complementary System-on-Chip (SoC) functions are projected after 2024.
- Ground-rule scaling need to also enable design-technology-co-optimization (DTCO) constructs that accommodate the area reduction as well as tighten the critical design that limits for overall SoC area scaling.
- Main challenge in 3D integration is how to partition the system to come up with better utilization of devices, interconnect and sub-systems such as memory, analog, and I/O. Parasitics improvement will become the major knob for performance improvement for nodes spanning between 2017 and 2024.
- SiGe and Ge channels are gaining importance as the high-mobility channels. IIIV channel faces challenges of variability, band-to-band tunneling, and large investments in fab infrastructure.
- Interconnect technology sees the use of non-Cu options, particularly in addressing the electromigration risks of Cu. On the other hand, metal resistance exponentially increases in both Cu and non-Cu options, which makes a careful selection of BEOL stack for SoC not to face performance loss due to the high resistance of tight-pitch layers.

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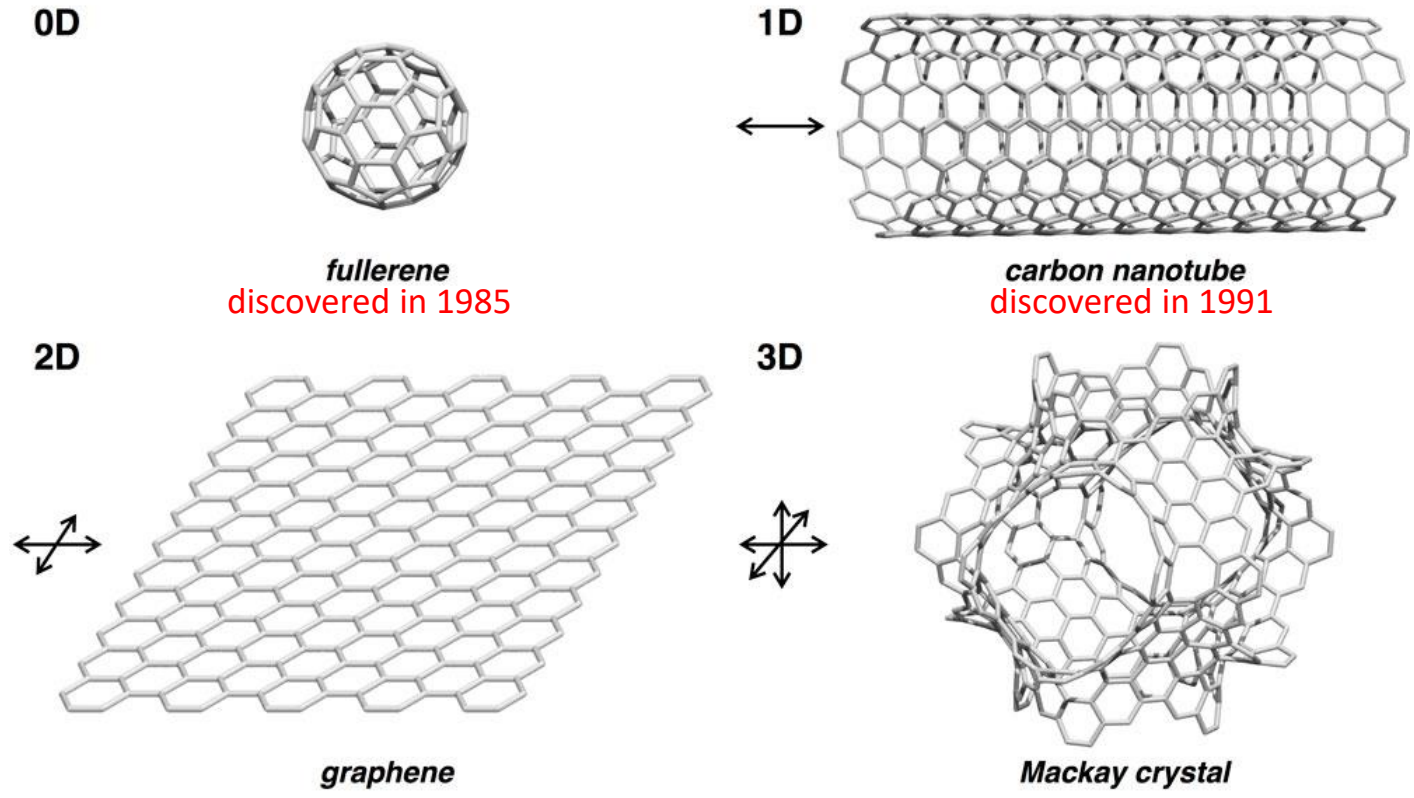
Personal attention -- Carbon material for future solution

Carbon is one of candidates for future material, and experts point out that it has huge advantages over current silicon base. However, practical application is expected 15~20 years later . . .



Advantage of carbon material for semi-conductor

Low Power operation:
Power = V^2 ~ 1/100 of current silicon base.

9B-3

Possibilities for V_{DD} = 0.1V Logic Using Carbon-Based Tunneling Field Effect Transistors

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Abstract- A systematic evaluation of the possibilities of low-voltage logic using carbon-based tunneling field effect transistors (TFET) is performed using the non-equilibrium green function (NEGF) formalism [1] for device simulation and ring-oscillator and load-driven inverter circuits. We found that the on-current is severely limited by quantum mechanical reflections due to wavefunction mismatch. The lower bound of subthreshold swing (SS) is limited by tunneling through the channel. Although the projected performance is well-below that of a recent prediction [2], we show that digital logic at V_{DD} = 0.1V is possible. Finally, we compare the TFET with its MOSFET counterpart and show that for V_{DD}=0.1V, the TFET out-performs the MOSFET.

Introduction: Carbon nanotube tunneling-based field effect transistors are being explored as possible candidates for next generation CMOS [3, 4], due to the potential for low operating supply voltage. With the recent discovery of the two-dimensional carbon [5], graphene nanoribbon (GNR) field effect transistors (FETs) have also emerged as a promising candidate for future technology. In this work, we performed a systematic study of the carbon-based TFET in order to understand its performance potential and how it compares to its MOSFET counterpart.

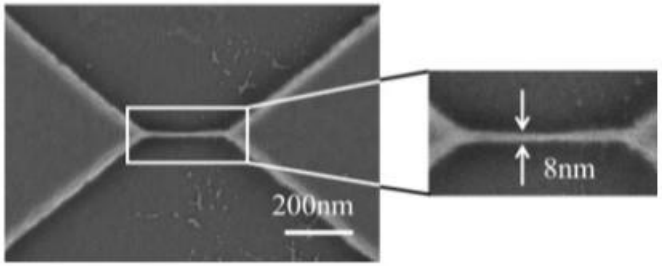
Methodology: We consider the following prototypical device, a zig-zag semiconducting nanotube with a bandgap of ~0.27eV, which, from a theoretical standpoint, is equivalent to an armchair graphene nanoribbon of 5nm width with the same bandgap [6]. Fig. 1 shows the device structure used in our simulation, which is the same as that in [2]. The source and drain are doped n-type and p-type respectively and the channel

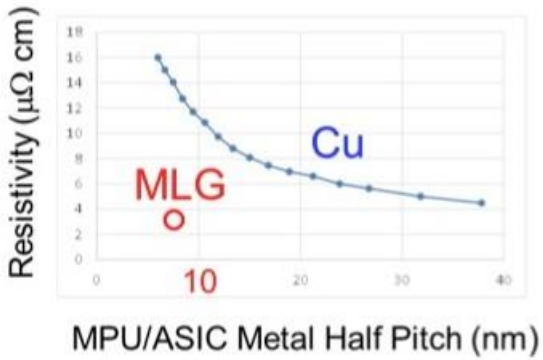
prediction. The on-current at V_{GS}= -0.1V computed using the WKB over-estimates the on-current by ~50%. Increasing the bandgap and the junction electric field would enhance WFM and would present a physical limit to the on-current of the TFET.

Off Current: As shown in Fig. 2(a), the off-current of the TFET is made up of two parts: 1) the band-to-band tunneling current across the whole channel (I_{BTBT}), and 2) the net current of thermionic emission over the source to drain barrier and minority carriers collection from drain to source (I_{THER}). I_{THER} is determined by the material's bandgap and set the lower bound for the off-current. Although increasing the bandgap would help to suppress I_{THER}, it might also compromise the on-current as previously discussed. On the other hand, I_{BTBT} can be reduced by simply increasing the channel length. Fig. 7 shows the off-current of the TFET as a function of channel length. At a channel length of ~100nm, one can approach the current limit set by I_{THER}. As shown in Fig. 8, the resulting benefit is an improved device SS. Note that both the 20 and 100nm channel length devices have a sub 60 mV/dec SS, but both are much larger that the projection of [2]. Our simulations assume ballistic transport, but upscaling of channel length would unavoidably make the device less ballistic. This example does, however, illustrate that channel down scaling might not be advantageous from an off-state consideration.

Circuit-Level Performance: Suppose we have a TFET operating at its performance limits, how would this device compare with its MOSFET counterpart? We address this question by circuit-level analysis, using the tool PETE [8]. As shown in Fig. 9, the TFET displays a reasonable voltage transfer characteristic at V_{DD} = 0.1V. As shown in Fig. 10 and

Low Resistivity when the size is closing to nano-scale.





最小抵抗率：3.2μΩcm

Summary

・Number/Size etc. of Transistor(semiconductor) follows so-called “Moore’s Law”

・It is expected that current Si technology is closing to the both of physical and technical limit. Many solutions are considered and tested.

・How about carbon materials ?

Transistor

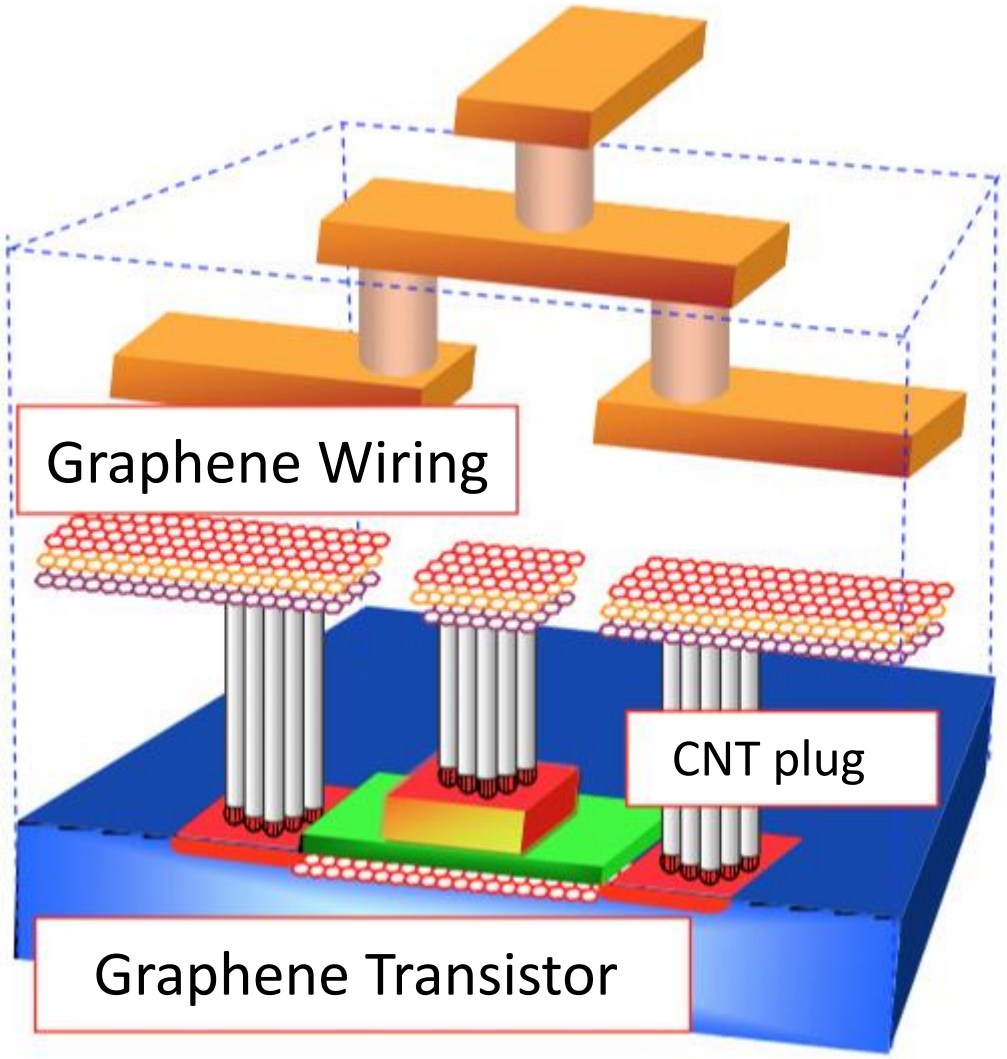
1947 (discovery) - 1971 (Intel 8008) ?
1980 (SSD at CERN) ?

33 years

nano carbon

1991 (discovery) - 20xx ?

if 33 years, , , = 2024



CNT: Carbon nano tube

Example Design: Application of nano-carbon material to the semiconductor

http://www.tel.co.jp/museum/magazine/material/150227_interview/02.html