ATLAS升级硅微条读出ASIC进展

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On behalf of the ITk ASICs Group

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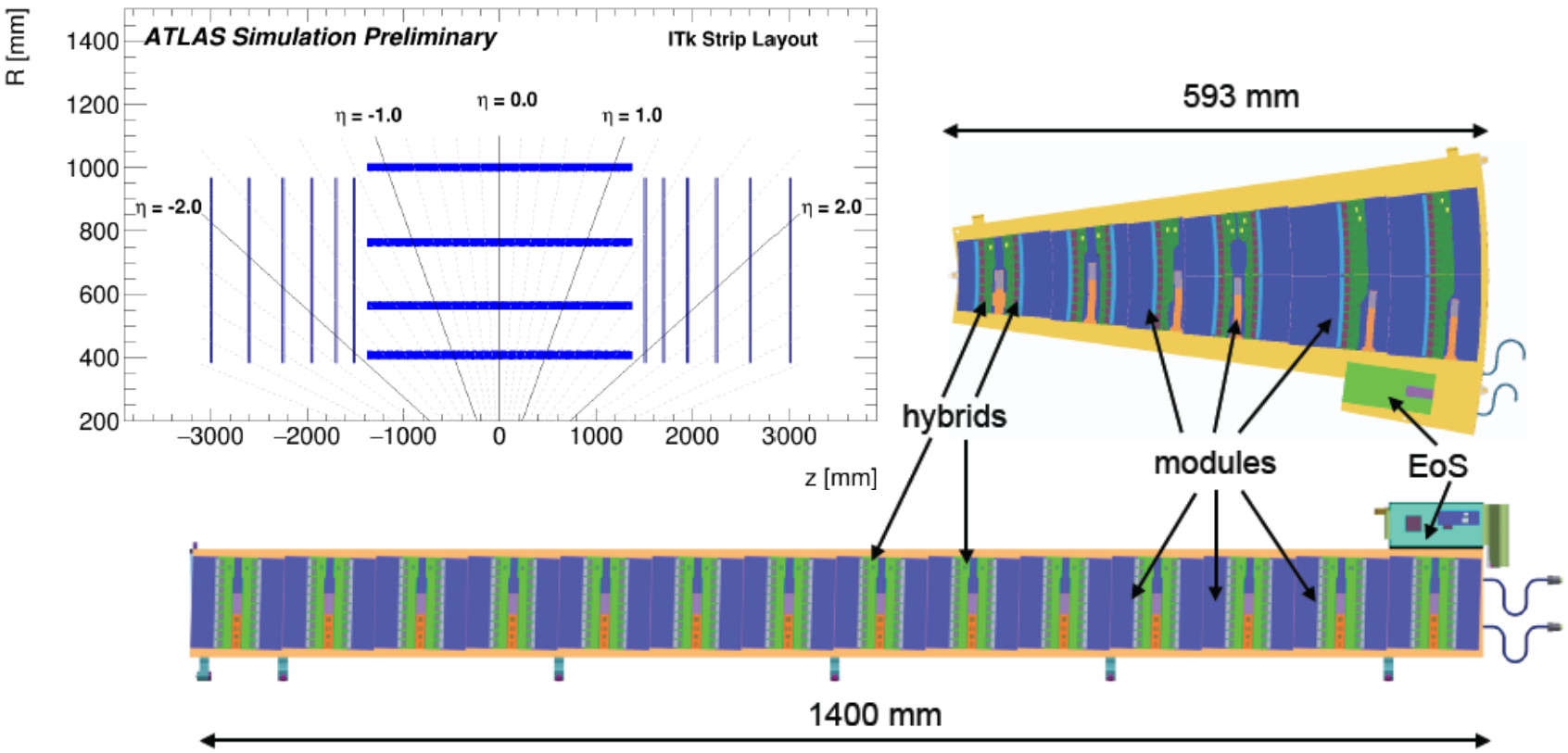
提纲

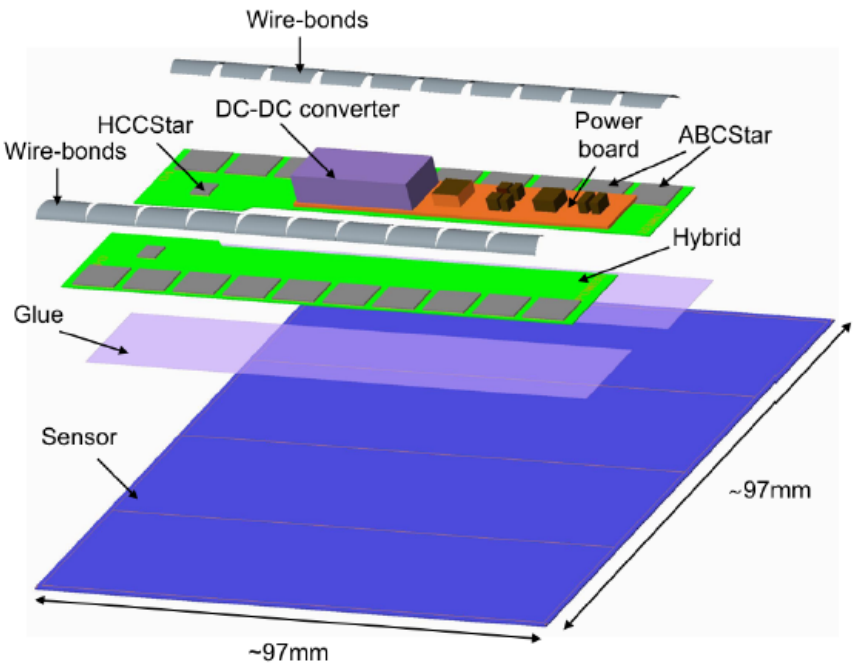
- **项目背景**
- ABCStar芯片设计及验证
- ABCN’进展

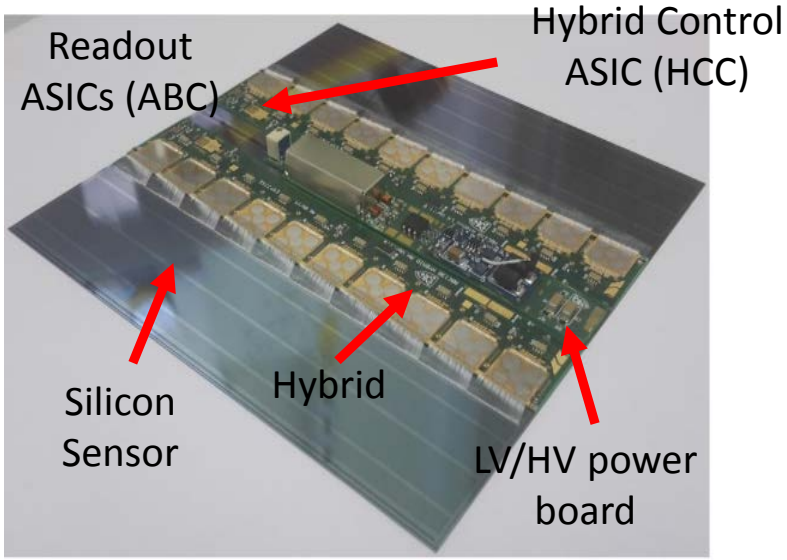
ITk硅微条探测器升级

- LHC—> ATLAS—> ITk—> Strip
- 粒度更细，规模更大，抗辐射要求更高



桶部短条模块

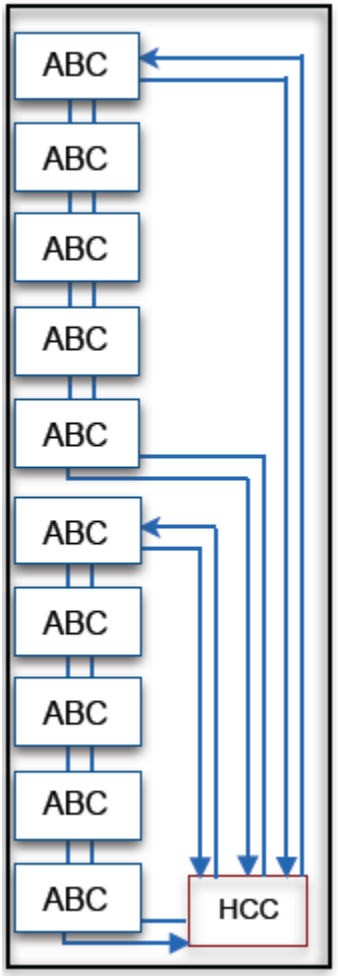


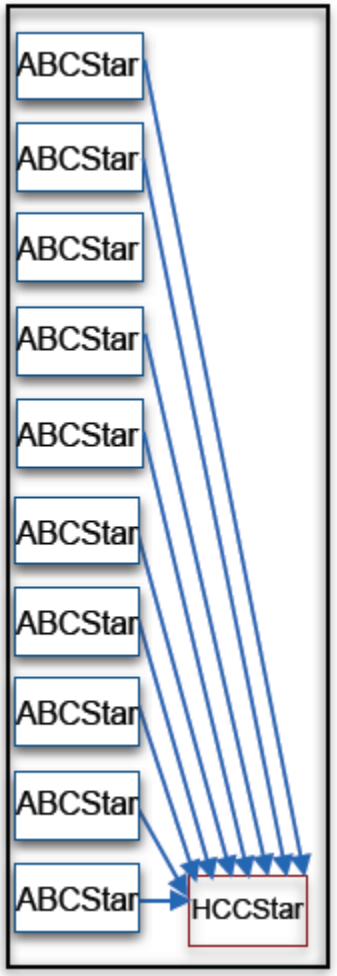


- Sensor， Hybrid， power board

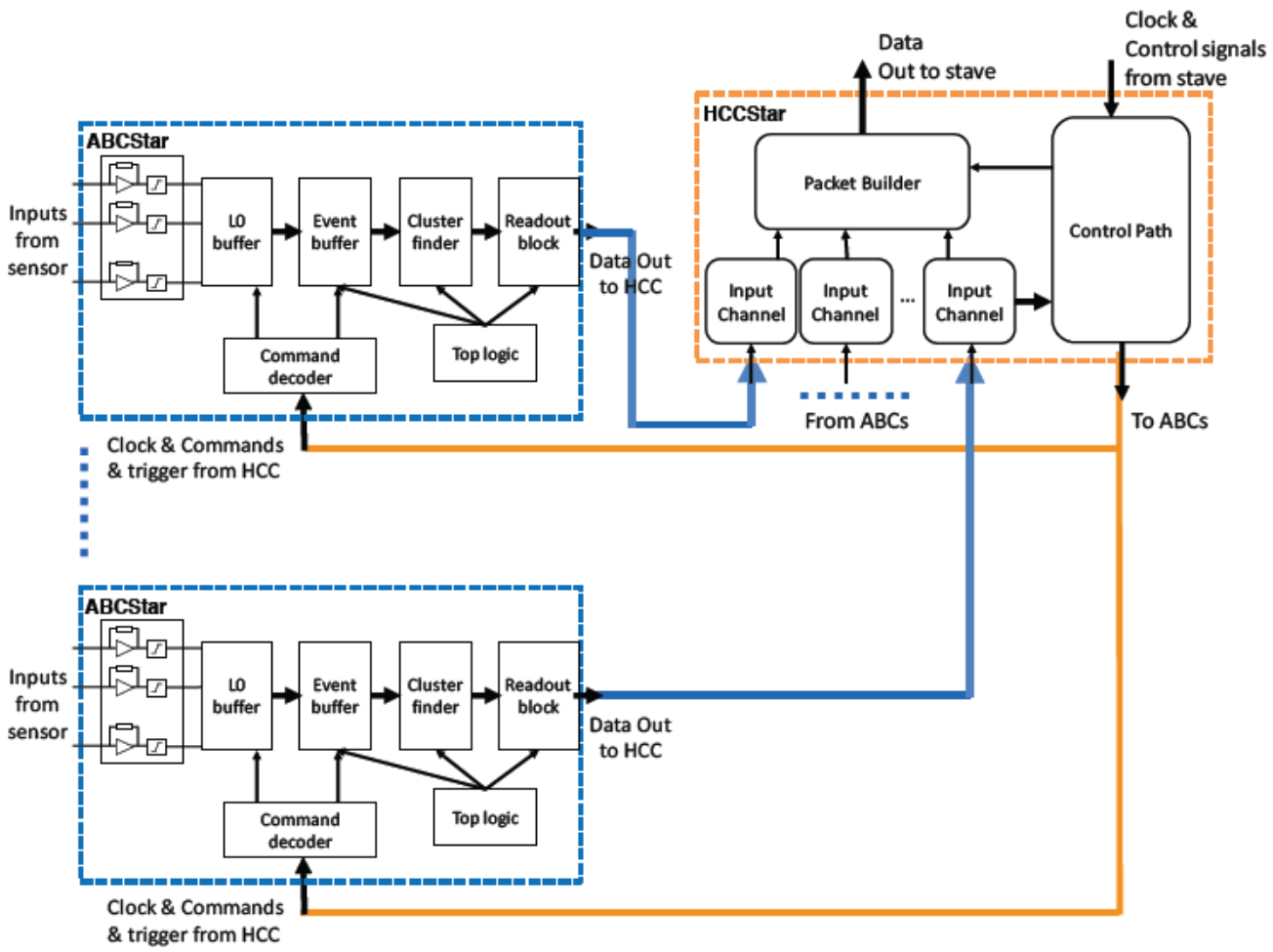
Motivation of ABCStar

- The ABCStar front-end ASIC
  - ABC--ATLAS Binary Chip
  - Star--Star readout with point to point connection
- From ABC130 to ABCStar
  - Change chip design to meet the requirement of increased trigger rate
  - Interface from ABCs to the HCC: Serial transfer of data to direct communication





Hybrid的star读出架构



参与人员

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- Mitchell Franck Newcomer, Paul Keener, Aditya Narayan (University of Pennsylvania (US))
- Joel Nathan De Witt (University of California, Santa Cruz (US))
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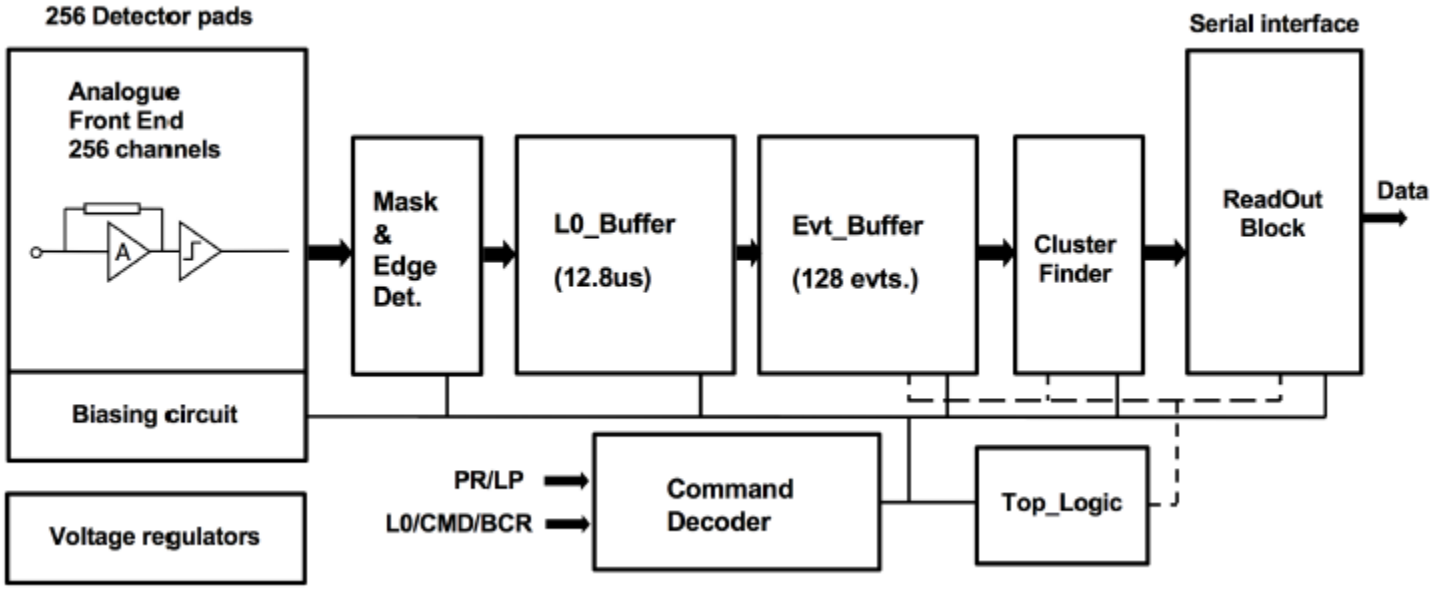
提纲

- 项目背景
- **ABCStar芯片设计及验证**
- ABCN’进展

ABCStar芯片架构

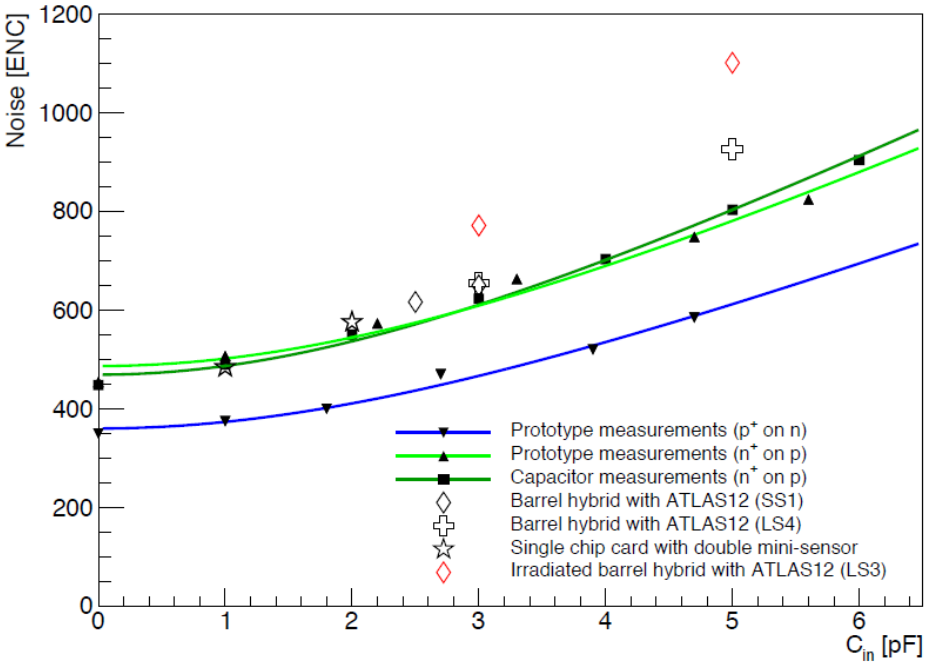


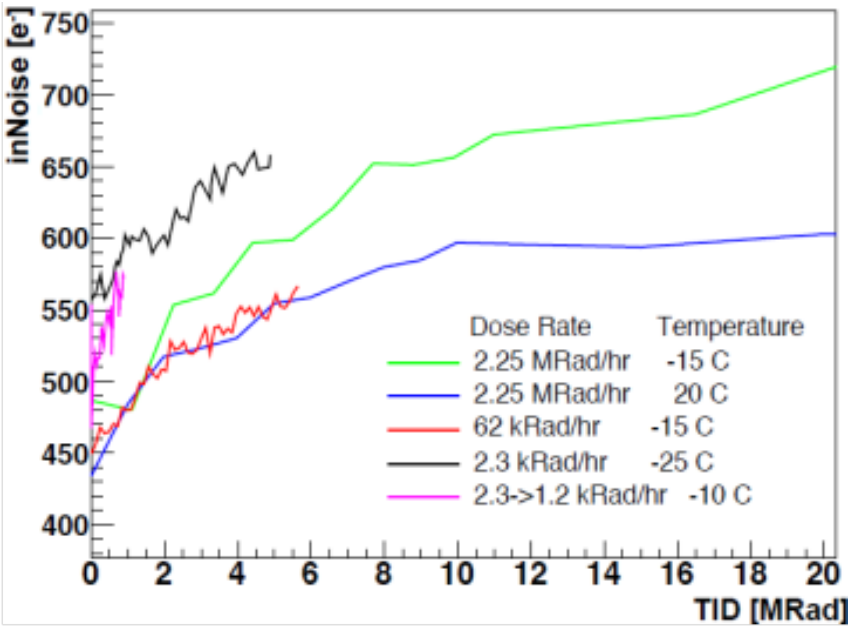
- It uses the standard binary readout architecture
- Data path: amplifier, discriminator, input register block, pipeline, event buffer and a cluster algorithm to compress data for output
- It is being designed to support various trigger modes
- It will be built in GF130nm technology

设计进展

Blocks/tasks Analog	status	Our contribution	Blocks/tasks Digital	status	Our contribution
FE	ongoing		InputRegisters	fixed	√
Voltage regulator	ongoing	interested	Two stage buffers	fixed	√
efuse	pending		Cluster Finder	fixed	
Analog monitor	pending	interested	Readout	fixed	
ESD	pending		TopLogic	fixed	√
			LCB and CommandDecoder	ongoing	
			hitsAccumulator	fixed	√
			Functional verification	ongoing	√
			SEU protection	pending	interested
			Digital backend	ongoing	interested

ABC130模拟前端测试

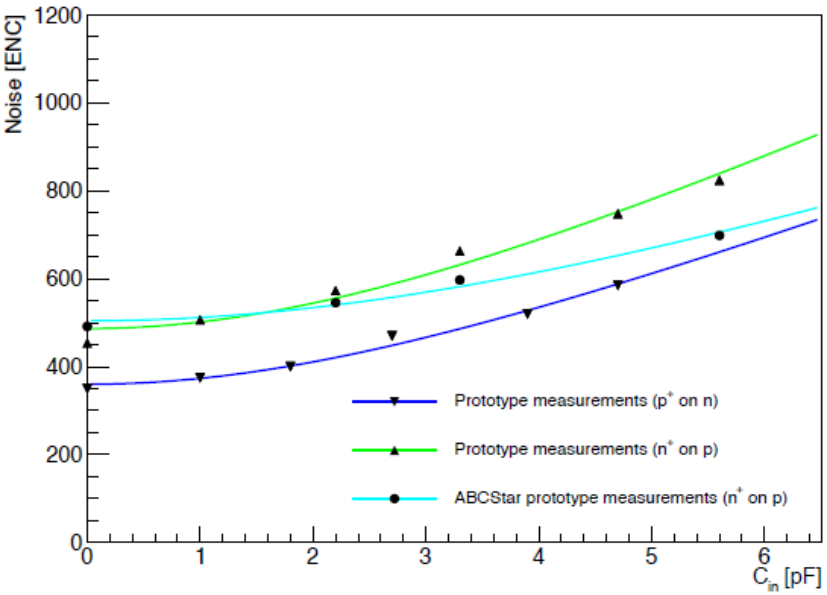


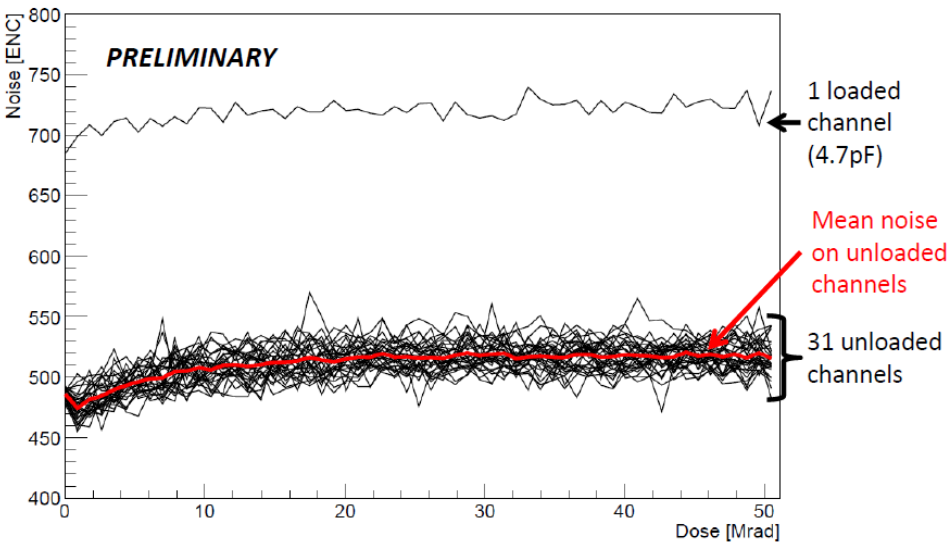


- A range of prototype: ABC130 front-end prototype, ABC130 single-chip test card, full barrel hybrid
- Connected to discrete capacitors: ENC for the prototype agrees well with hybrids and single chips
- Connected to sensors: noise increase due to strip resistance
- Noise increase for changed signal polarity → resistive feedback
- Excess noise after irradiation → Critical NMOS devices in enclosed geometry

ABCStar FE prototype

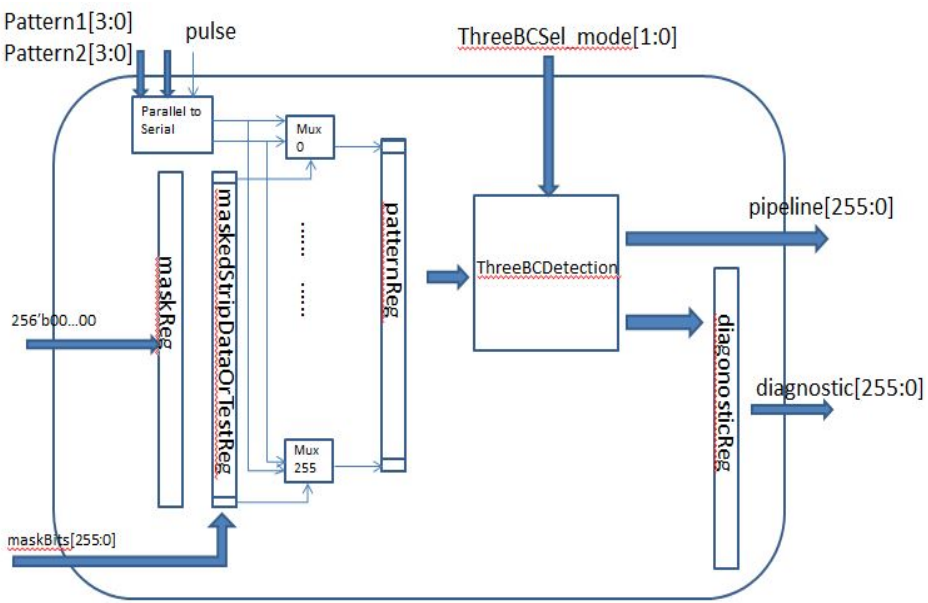
- Better noise slope w/o irradiation
- After irradiation
  - ~10% increase in the measured noise after 50.46 Mrad
    - X-ray，0.87Mrad/hr





Input Registers block

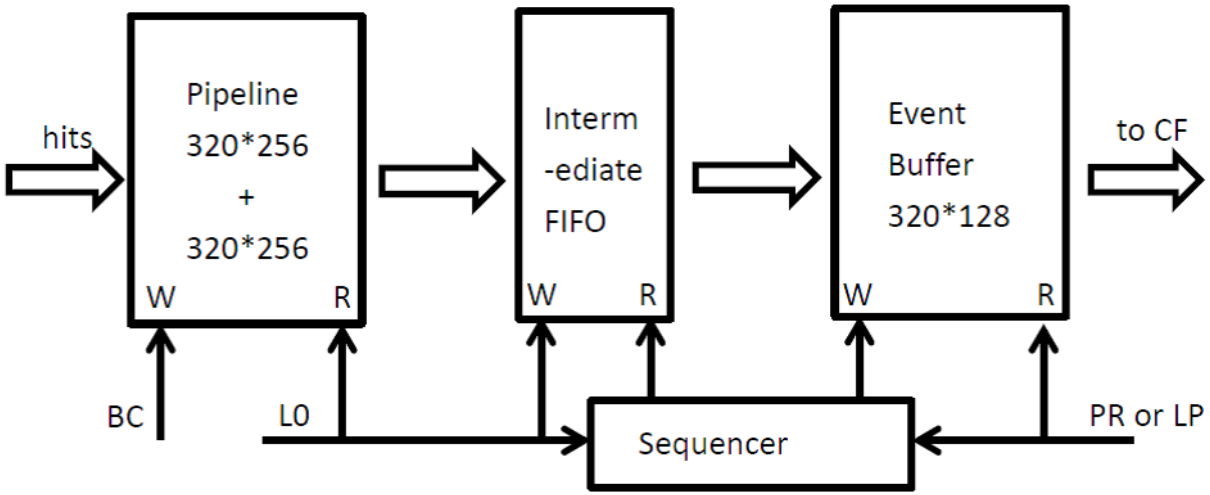
- Input register latches data with BC clock
- Mask/test registers for dual purpose
- Edge detection circuit with different selection criteria



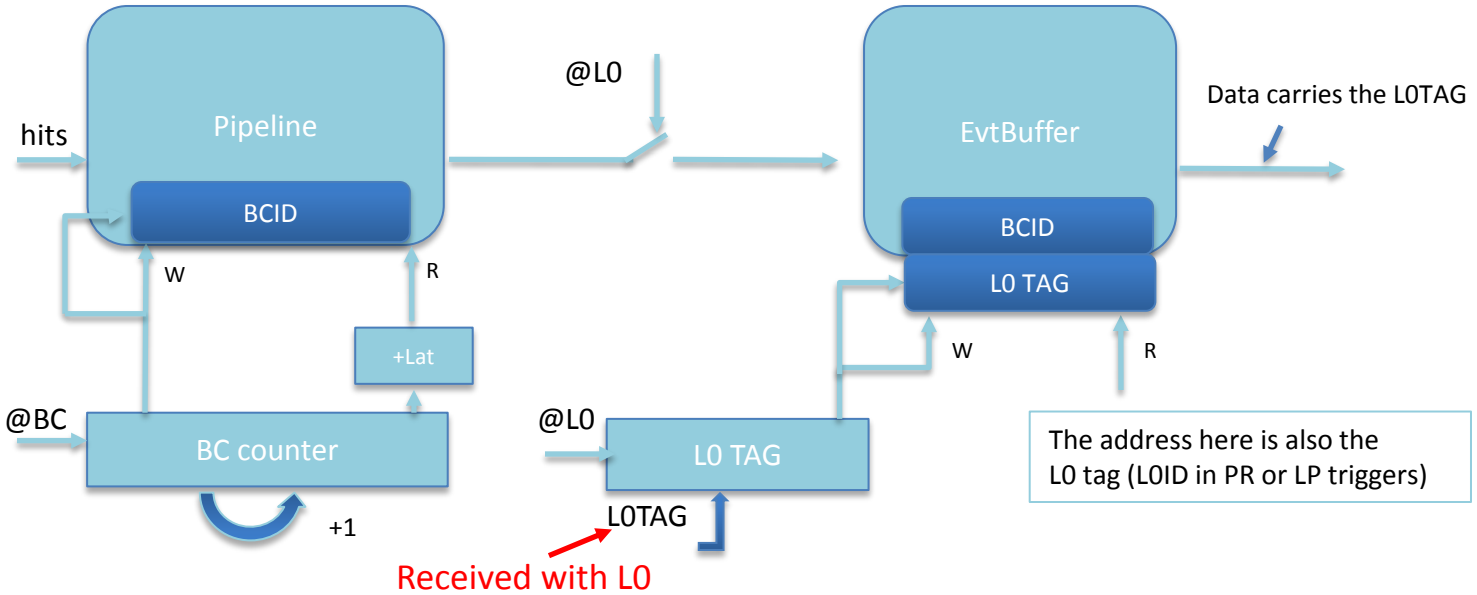
Det_mode (1:0)	Name of Selection Criteria	Hit Pattern (Oldest data bit 1st on the left)	Usage
00	Hit	1XX or X1X or XX1	Detector alignment
01	Level	X1X	Normal Data Taking
10	Edge	01X	Normal Data Taking
11	Clear	None	Special Mode

Two stage buffers

- The two stage buffers: Pipeline(L0Buffer) and EvtBuffer
- Basic memory IP: single port RAM
- Modification of buffer size
  - Pipeline(L0Buffer)extended to 512bit length
  - EvtBuffer reduced to 128bit length(128 events)
- Transfer 1 event per L0 from Pipeline to EvtBuffer(instead of 3)
- Intermediate FIFO to give the priority to EvtBuffer read operation, in case of consecutive L0s

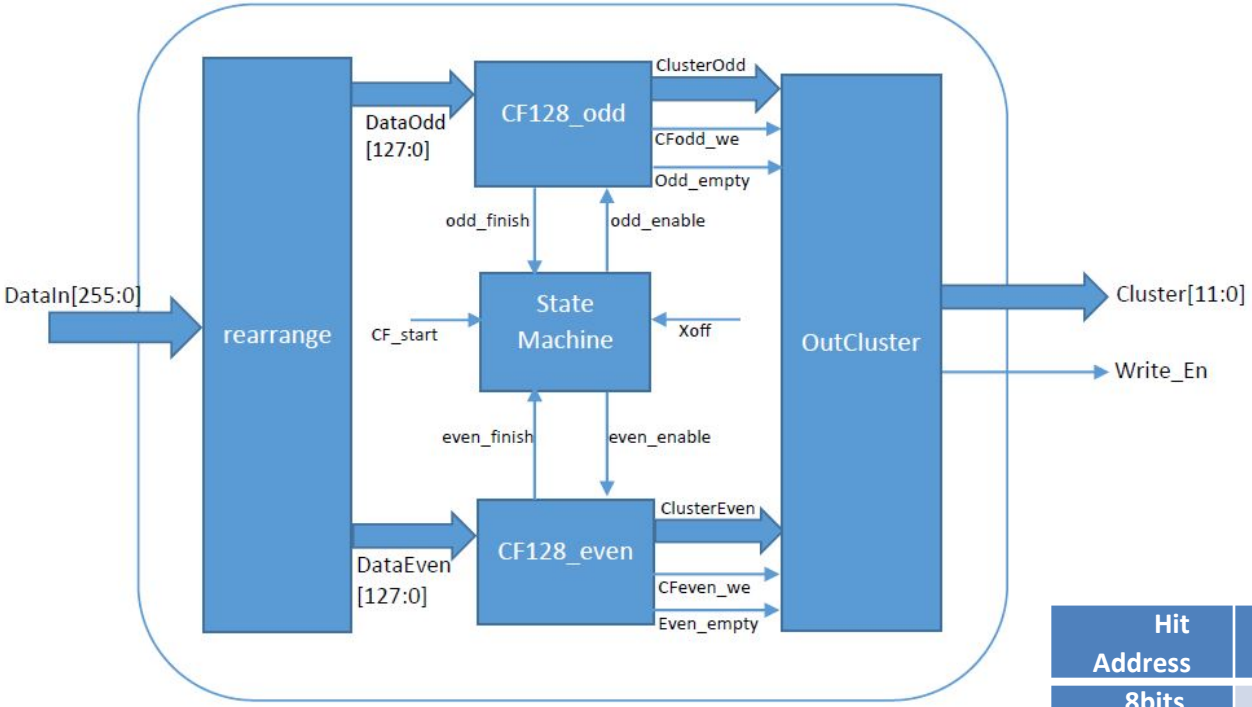


L0 tag insertion



- The L0ID counter is very sensitive and require synchronization regularly
- We will employ new scheme--sending a L0tag with L0
- This helps to improve the reliability

Cluster finder

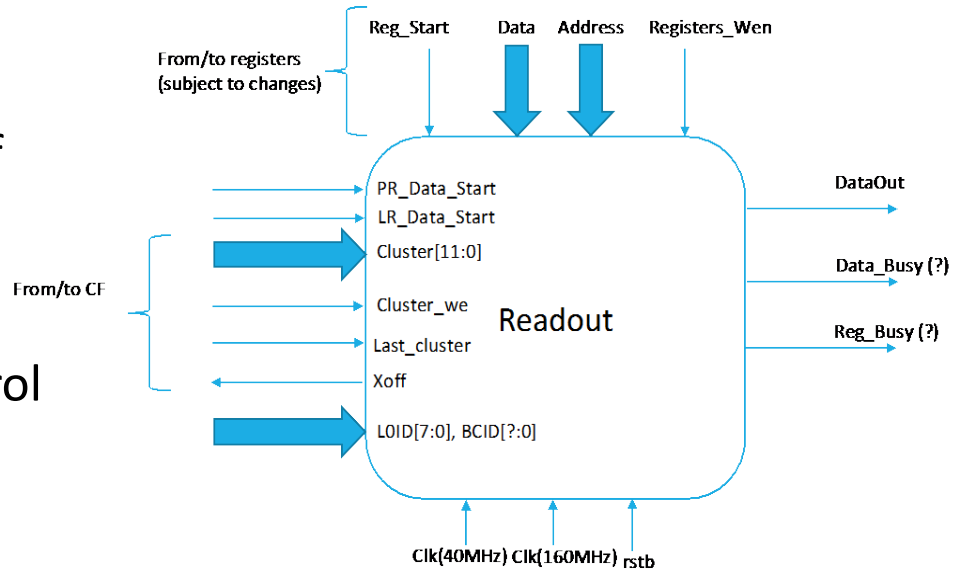


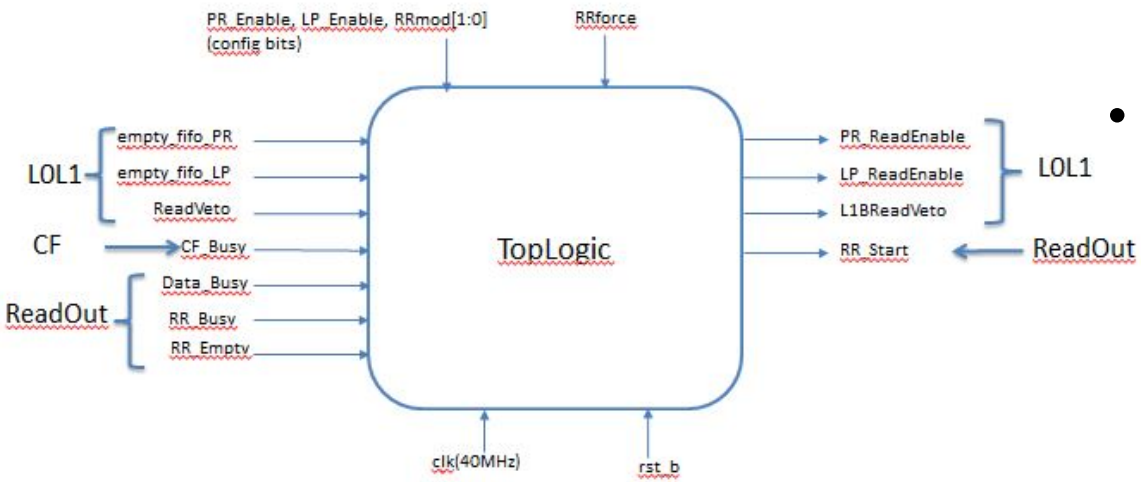
Hit Address	Following 3 strip values	Last cluster
8bits	3bits	1bit

- Data reduction circuit, creating a cluster byte for channels found with hits
- The cluster finder takes in 256 bits of strip data and reports out 12 bit clusters at 40MHz

Readout and TopLogic

- TopLogic
  - Sequencer for the control of EvtBuffer, ClusterFinder and ReadOut
  - Register readback control
  - PR/LP readout priority control

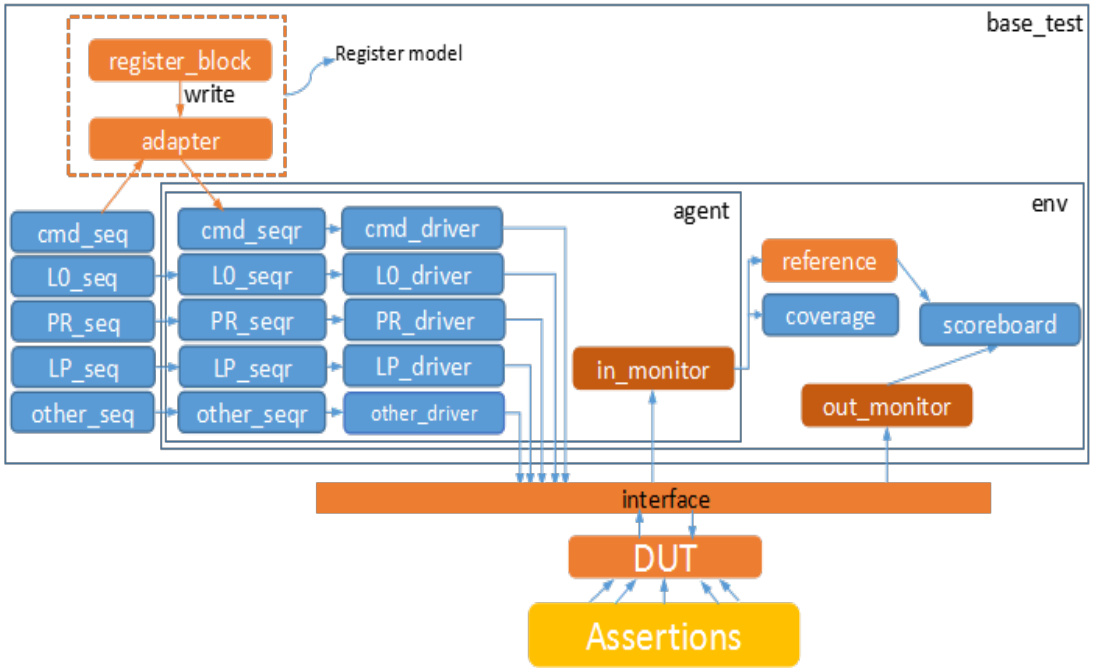




- Readout
  - Responsible for building data packets
  - A controller defines the order in which packets are formatted
  - Each packet is transmitted to the fast serializer

UVM setup for verification

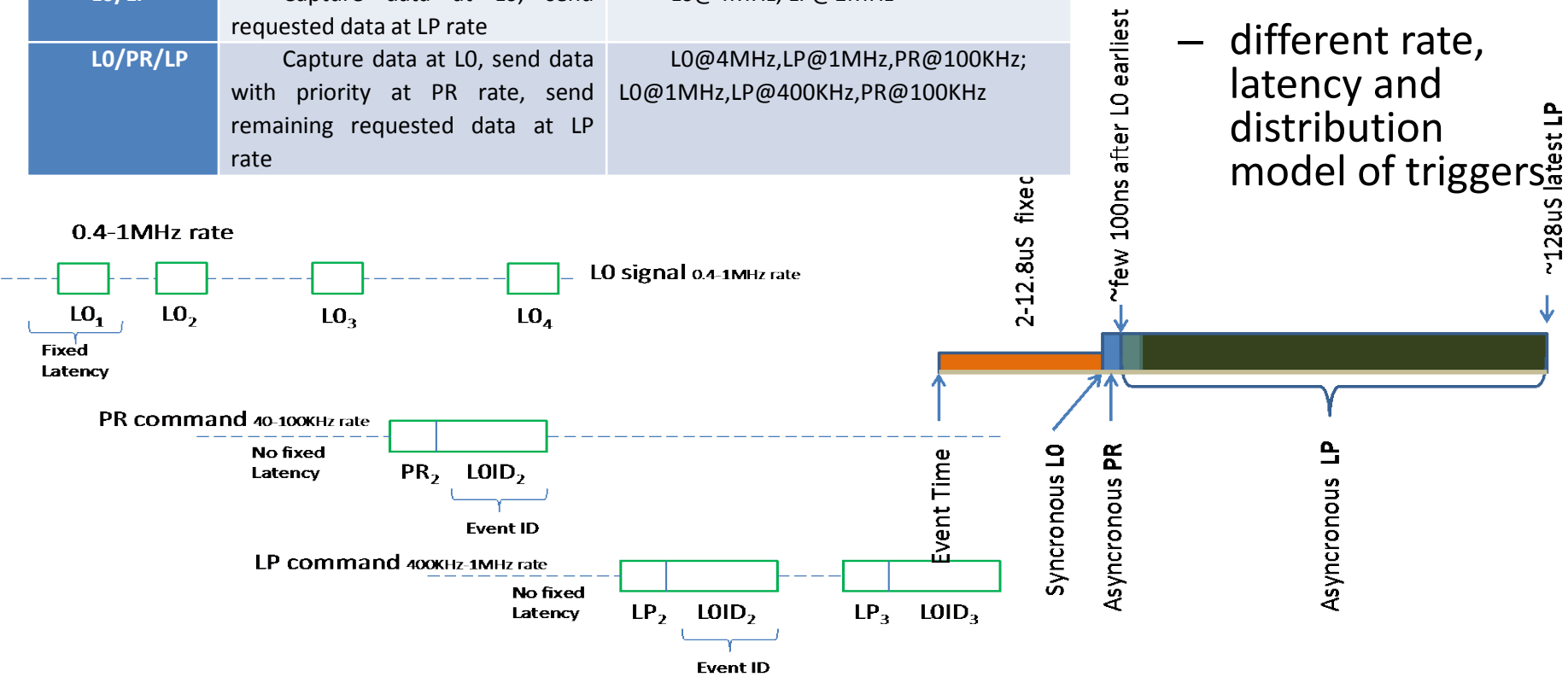
- A top verification setup based on (UVM)Universal Verification Methodology was built for the current design of ABCStar.
  - Functional coverage with customized random stimulus
  - Result comparison with reference model through scoreboard
  - SystemVerilog assertions for validating key design features



Trigger rates and latencies

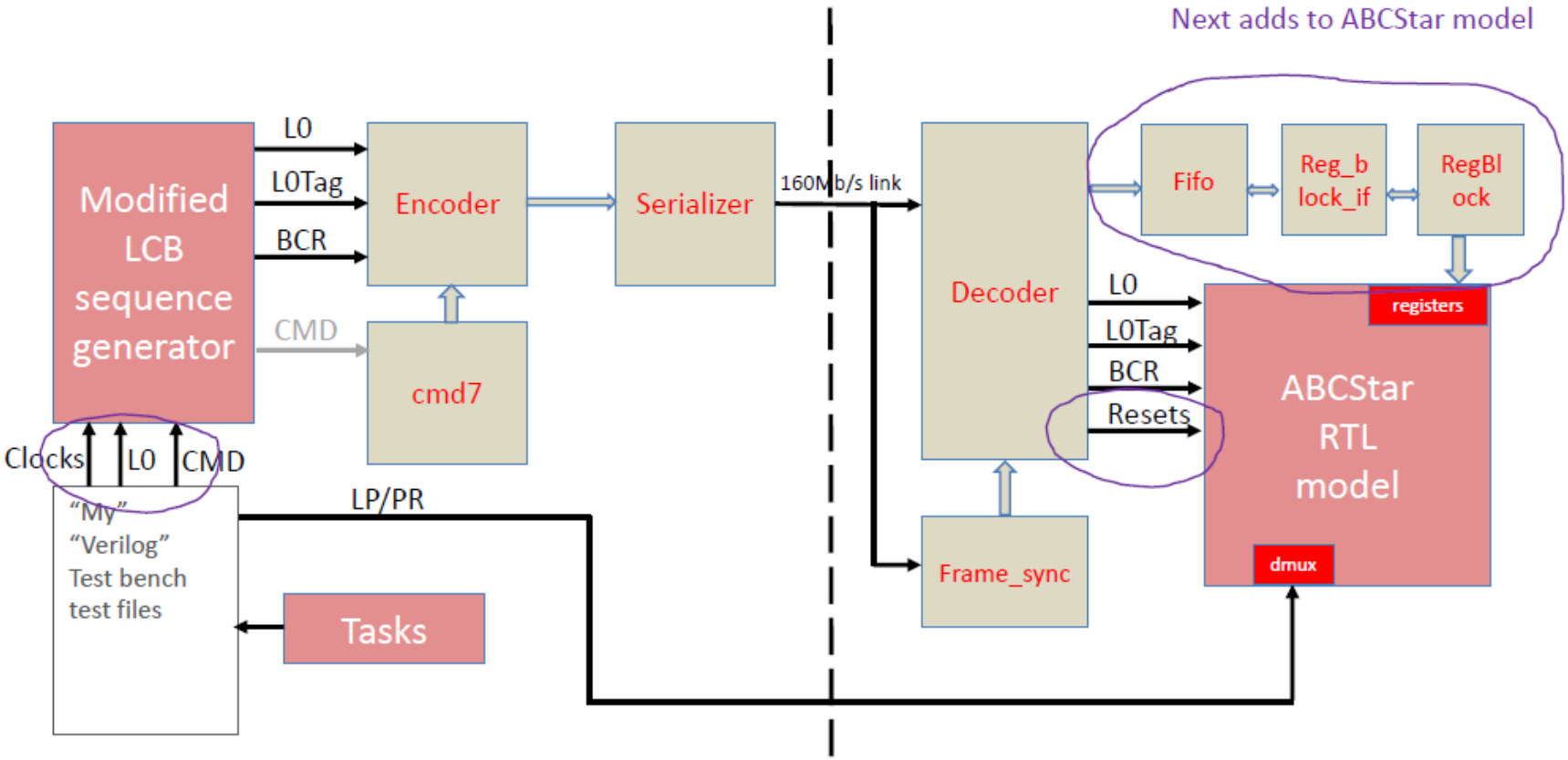
Trigger mode	description	Example tests with UVM setup
L0	Capture and readout at L0 rate	L0@1MHz, LP@1MHz
L0/LP	Capture data at L0, send requested data at LP rate	L0@4MHz, LP@1MHz
L0/PR/LP	Capture data at L0, send data with priority at PR rate, send remaining requested data at LP rate	L0@4MHz,LP@1MHz,PR@100KHz; L0@1MHz,LP@400KHz,PR@100KHz

- to verify the current design under several possible trigger conditions
  - different rate, latency and distribution model of triggers



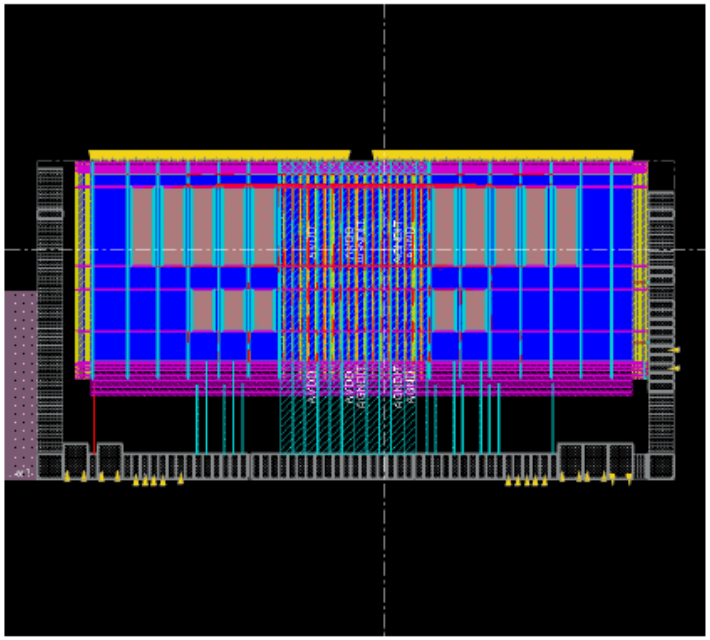
ABCStar verification

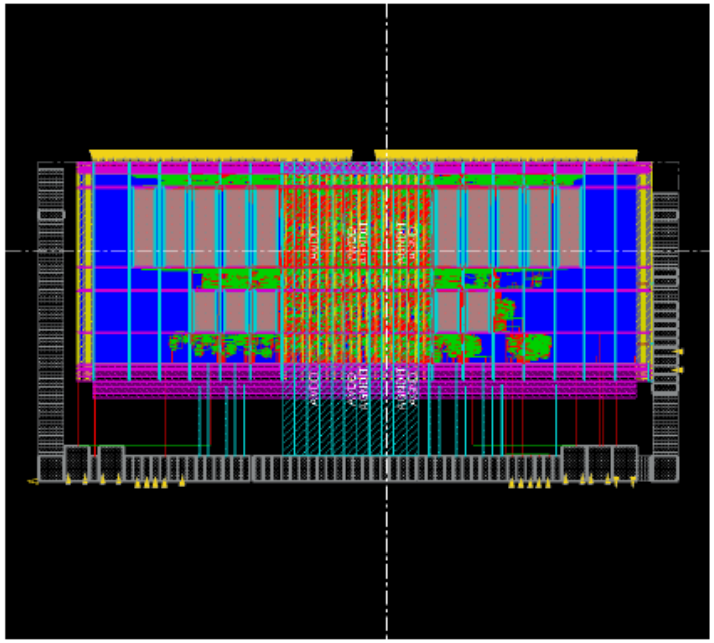
- LCB protocol updates



ABCStar layout

- Back-end progress
  - Digital only
  - All active pads on one side





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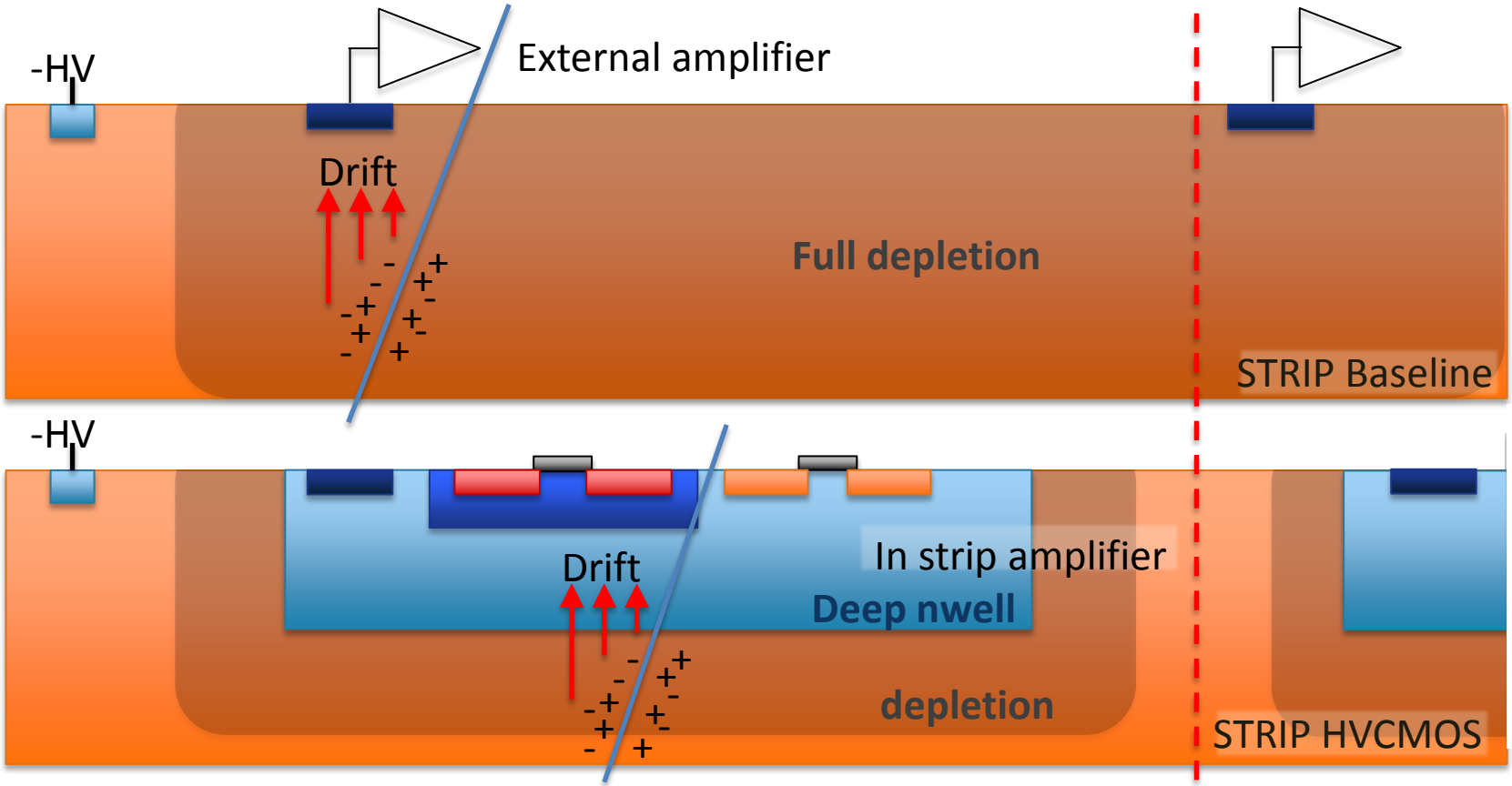
- **ABCN’进展**

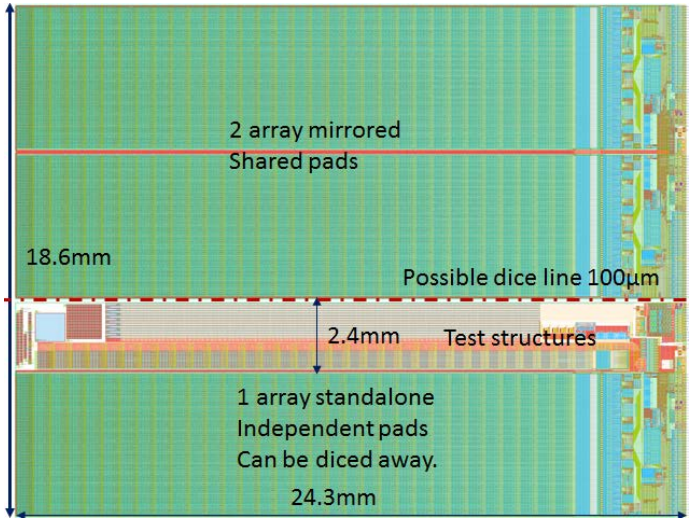
HV-CMOS硅微条

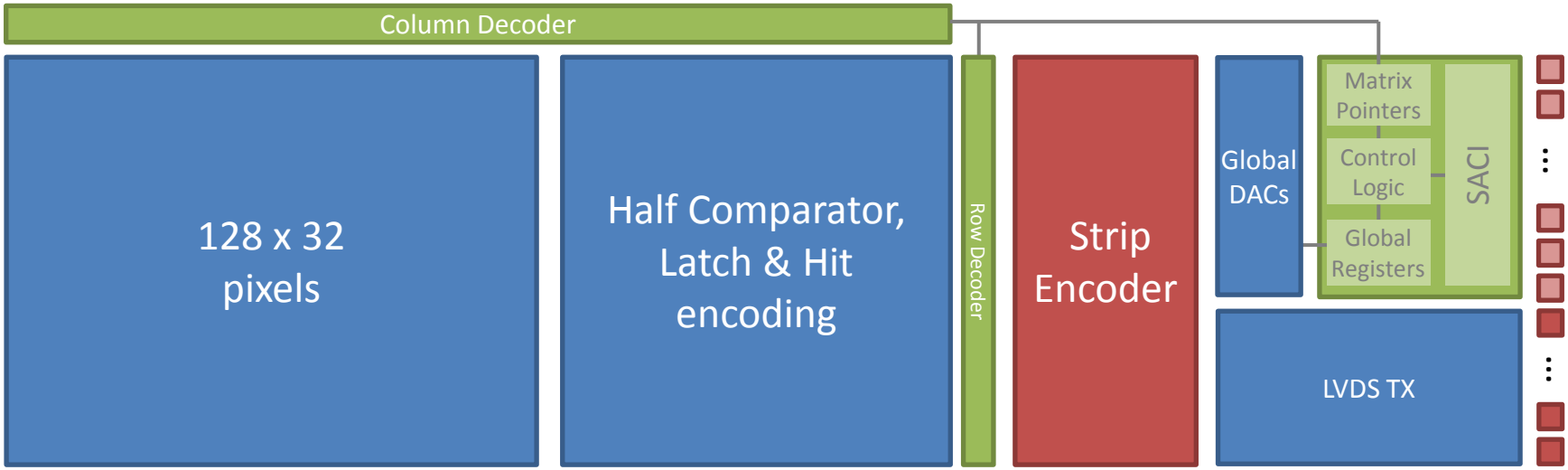


- HV-CMOS具有低成本，低物质量等优势，ITk升级备选方案

CHESS-2芯片

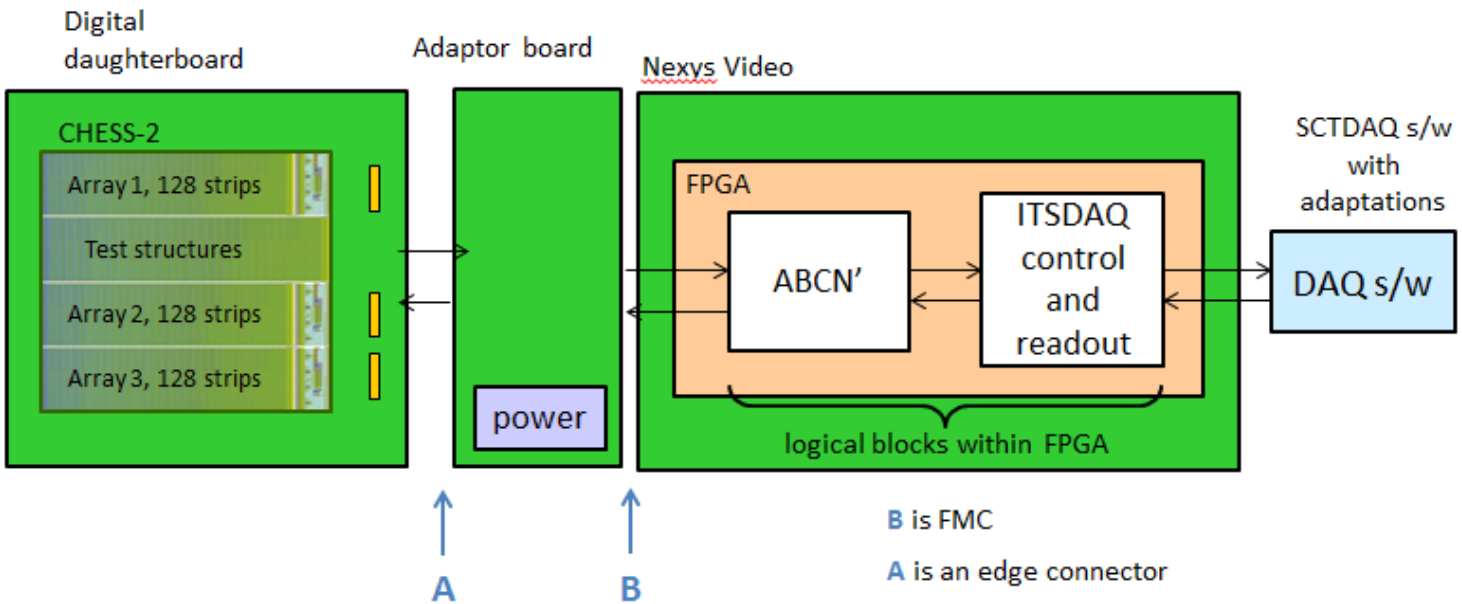
- CHESS-2芯片， AMS 0.35um HV工艺





ABCN’

- need CHESS2 chips and ABCN-like chip for evaluating module-level functionality and performance
- First step is to emulate ABCN’ in an FPGA



总结

- ABCStar芯片是复杂的数模混合芯片，目前指标已基本确定，将继续合作并做出更多贡献
- 采用HV-CMOS工艺的硅微条探测器具有显著优势，研发工作正在进行
- 通过ATLAS升级合作可以学习国外先进技术和经验，对国内相关领域发展具有积极意义