



# Study of Pixel Sensor for CEPC

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On behalf of CEPC vertex group

2017-4-27



# Outline

- *CEPC及探测器简介*
- *Pixel sensor的关键问题*
- *Pixel sensor的预研工作*
  - 研究思路
  - *CPS pixel sensor*
  - *SOI pixel sensor*
- *Summary*

## e<sup>+</sup>e<sup>-</sup> Higgs (Z) factory

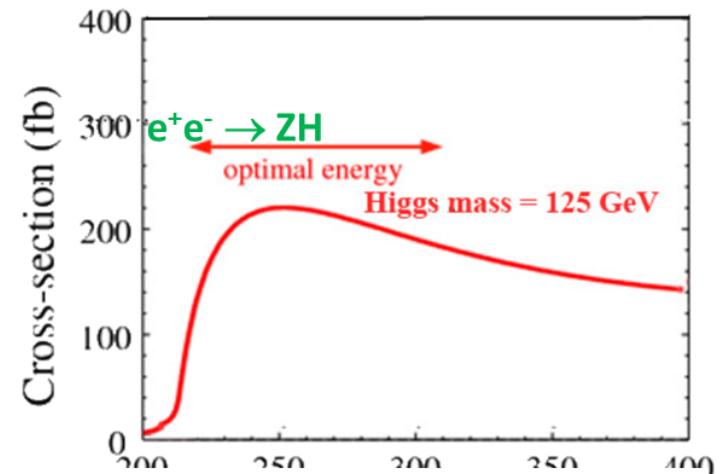
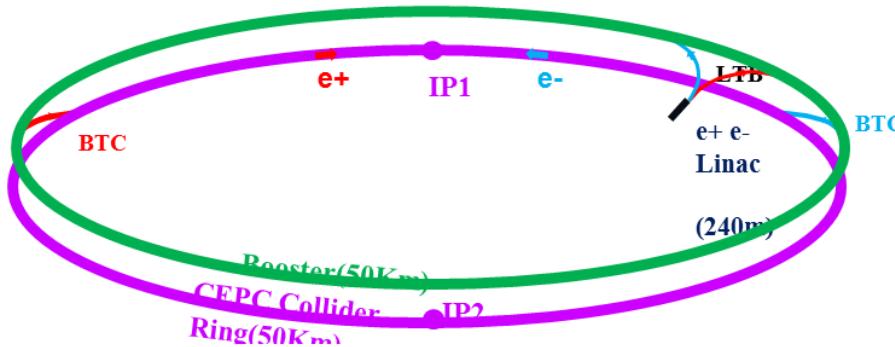
$E_{cm} \approx 240 \text{ GeV}$ , luminosity  $\sim 2 \times 10^{34} \text{ cm}^{-2} \text{s}^{-1}$ , 2IP, 1M H in 10 years  
can also run at the Z-pole

Higgs precision  
1% or better

Precision measurement of the Higgs boson (and the Z boson)

Upgradable to pp collision with  $E_{cm} \approx 50\text{-}100 \text{ TeV}$  (with ep, HI options)

A discovery machine for BSM new physics

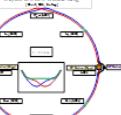


**BEPCII** will likely complete its mission ~2020s;

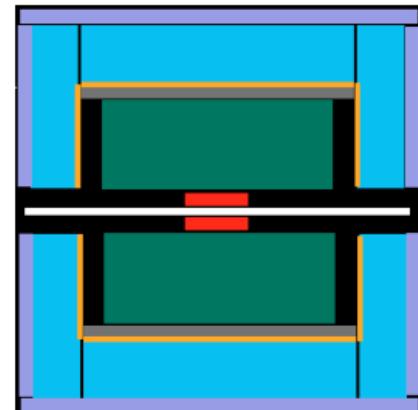
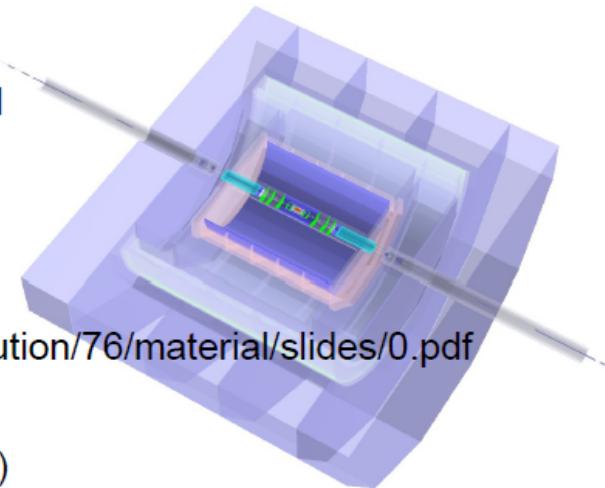
**CEPC** – possible accelerator based particle physics program in China after BII

April 19, 2017

# CEPC option characteristics comparison

Option	Pretzel	Sawtooth effect	Beam loading	Dynamic Aperture	Orbit Correction	H luminosity	Z-pole luminosity	AC power	SRF system compatible for H and Z
 Single Ring (SR)	Yes 	Very high 	Low 	Very small 	Very hard 	Low 	Very low 	High 	Difficult 
 Partial Double Ring (PDR)	No 	High 	Very High 	Medium 	Hard 	Medium 	Medium 	Low 	Difficult 
 Advanced Partial Double Ring (APDR)	No 	High 	High 	Medium 	Medium 	Medium 	High 	Low 	Difficult 
 Full Partial Double Ring (FPDR)	No 	Vey Low 	Low 	Large 	Easy 	High 	Very High 	Low 	Very good 

- The PFA Oriented Concept: Optimizing Via Sim-Reconstructions
  - Silicon/TPC + Ultra-high Granularity Calorimeter + 3 Tesla Field
  - Feasibility:
    - TPC: **OK** with the voxel occupancy & distortion
      - <https://arxiv.org/pdf/1704.04401.pdf>,  
<http://indico.ihep.ac.cn/event/6433/session/15/contribution/76/material/slides/0.pdf>
    - Passive cooling Calorimeter:
      - **OK** for Higgs physics (~% level degrading in reco. effi)
      - **May Severely degrade EW, tau physics performance: need further study**
  - Optimized Parameters recommended
- The Alternative Concept: To be implemented in Full Simulation
  - Wire Chamber + Dual Readout + 2 Tesla Field
  - Working gas optimization, occupancy & neutron flux tolerance
- Both concepts uses similar MDI/inner tracker system
  - *Radiation. Etc needs Xchecks*



# Physics driven requirements

**Table 2.1** Required performance of the CEPC sub-detectors for critical benchmark Higgs processes.

Physics Process	Measured Quantity	Critical Detector	Required Performance
$ZH \rightarrow \ell^+ \ell^- X$	Higgs mass, cross section	Tracker	$\Delta(1/p_T) \sim 2 \times 10^{-5}$
$H \rightarrow \mu^+ \mu^-$	$\text{BR}(H \rightarrow \mu^+ \mu^-)$	Tracker	$\oplus 1 \times 10^{-3} / (p_T \sin \theta)$
$H \rightarrow b\bar{b}, c\bar{c}, gg$	$\text{BR}(H \rightarrow b\bar{b}, c\bar{c}, gg)$	Vertex	$\sigma_{r\phi} \sim 5 \oplus 10 / (p \sin^{3/2} \theta) \mu\text{m}$
$H \rightarrow q\bar{q}, VV$	$\text{BR}(H \rightarrow q\bar{q}, VV)$	ECAL, HCAL	$\sigma_E^{\text{jet}} / E \sim 3 - 4\%$
$H \rightarrow \gamma\gamma$	$\text{BR}(H \rightarrow \gamma\gamma)$	ECAL	$\sigma_E \sim 16\% / \sqrt{E} \oplus 1\% (\text{GeV})$

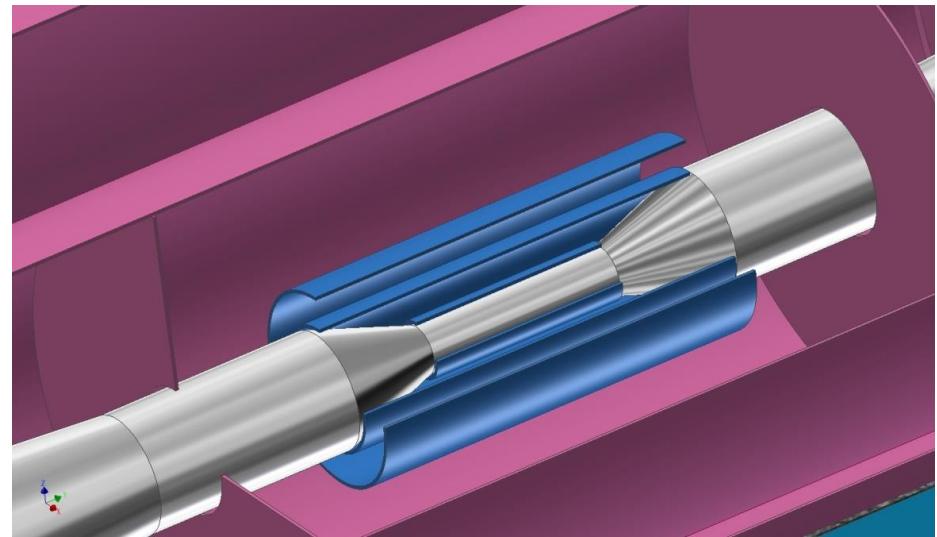
- excellent tagging capability of b-/c-quark jets and  $\tau$ -lepton
  - Impact parameter resolution,  $\sigma(r\phi) = a \oplus \frac{b}{p(\text{GeV}) \sin^{3/2} \theta} \mu\text{m}$
- Design constrains on vertex:
  - $\sigma_{s,p} = 2.8\mu\text{m}$  for the inner most layers;
  - Material budget less than **0.15%/layer**;
  - **r = 16mm** for the Inner most layer.

# Detector concept

## Baseline design for the pre-CDR

### Vertex detector:

- 3 layers of double-sided pixels
- $\sigma_{SP}=2.8\mu\text{m}$ , inner most layer
- readout time <20 $\mu\text{s}$



**VXD Geometry**

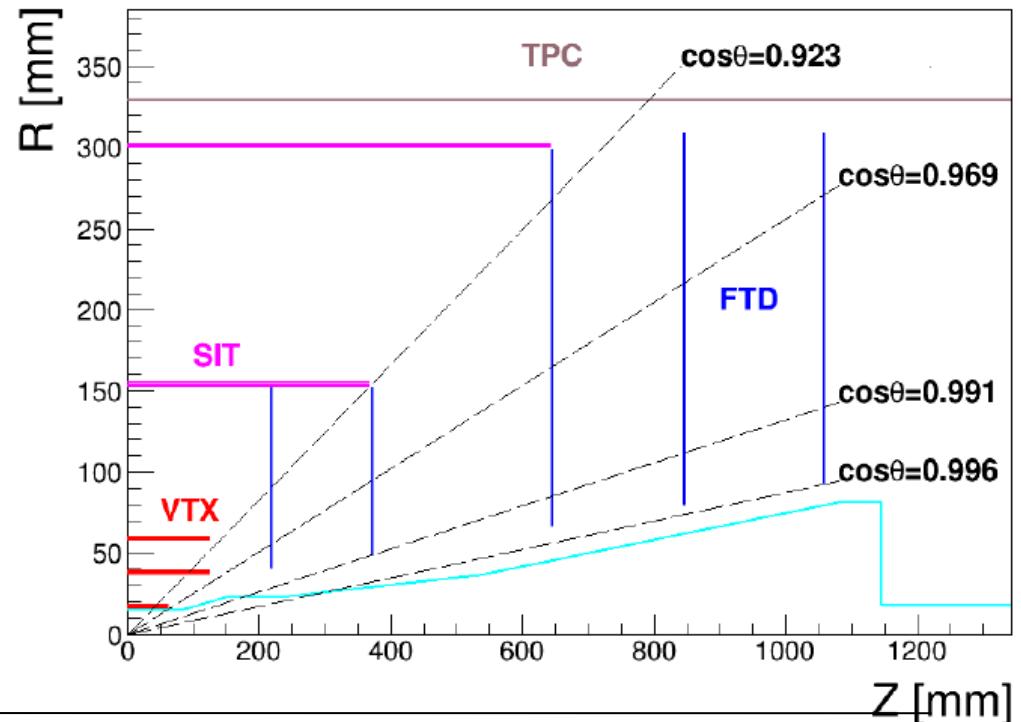
	R (mm)	z  (mm)	$ \cos \theta $	$\sigma_{SP}$ ( $\mu\text{m}$ )	Readout time ( $\mu\text{s}$ )
Layer 1	16	62.5	0.97	2.8	20
Layer 2	18	62.5	0.96	2.8	20
Layer 3	37	125.0	0.96	4	20
Layer 4	39	125.0	0.95	4	20
Layer 5	58	125.0	0.91	4	20
Layer 6	60	125.0	0.90	4	20

# Detector concept (Cont.)

## Si-tracker:

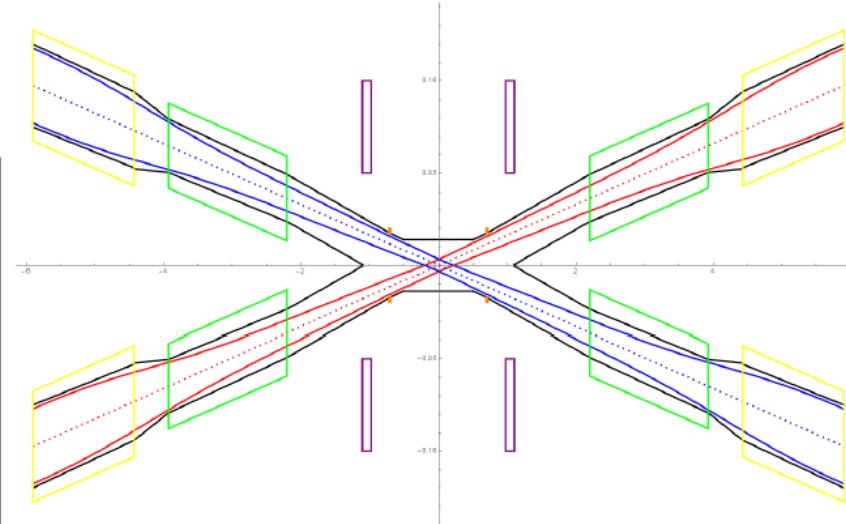
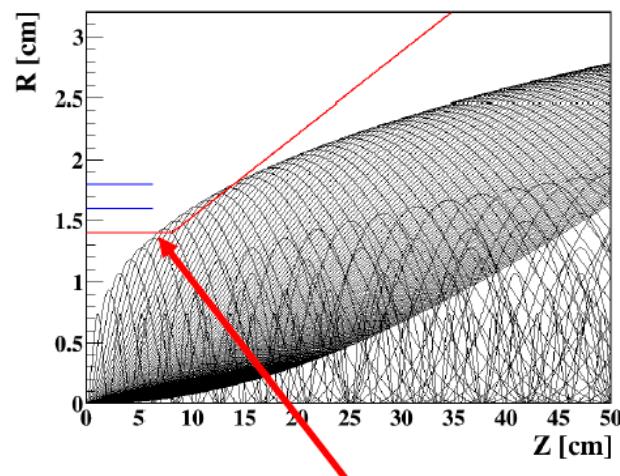
- Silicon Internal Tracker (SIT) – 2 inner layers strip detectors
- Forward Tracking Detector (FTD) – 5 disks (2 with pixels and 3 with Si strip sensor), comparing to 7 disks on ILD, due to smaller  $L^*$
- Silicon External Tracker (SET) – 1 outer layer Si strip detector
- End-cap Tracking Detector (ETD) – 1 end-cap Si strip detector on each side

Layout of strips (SET and ETD not shown)



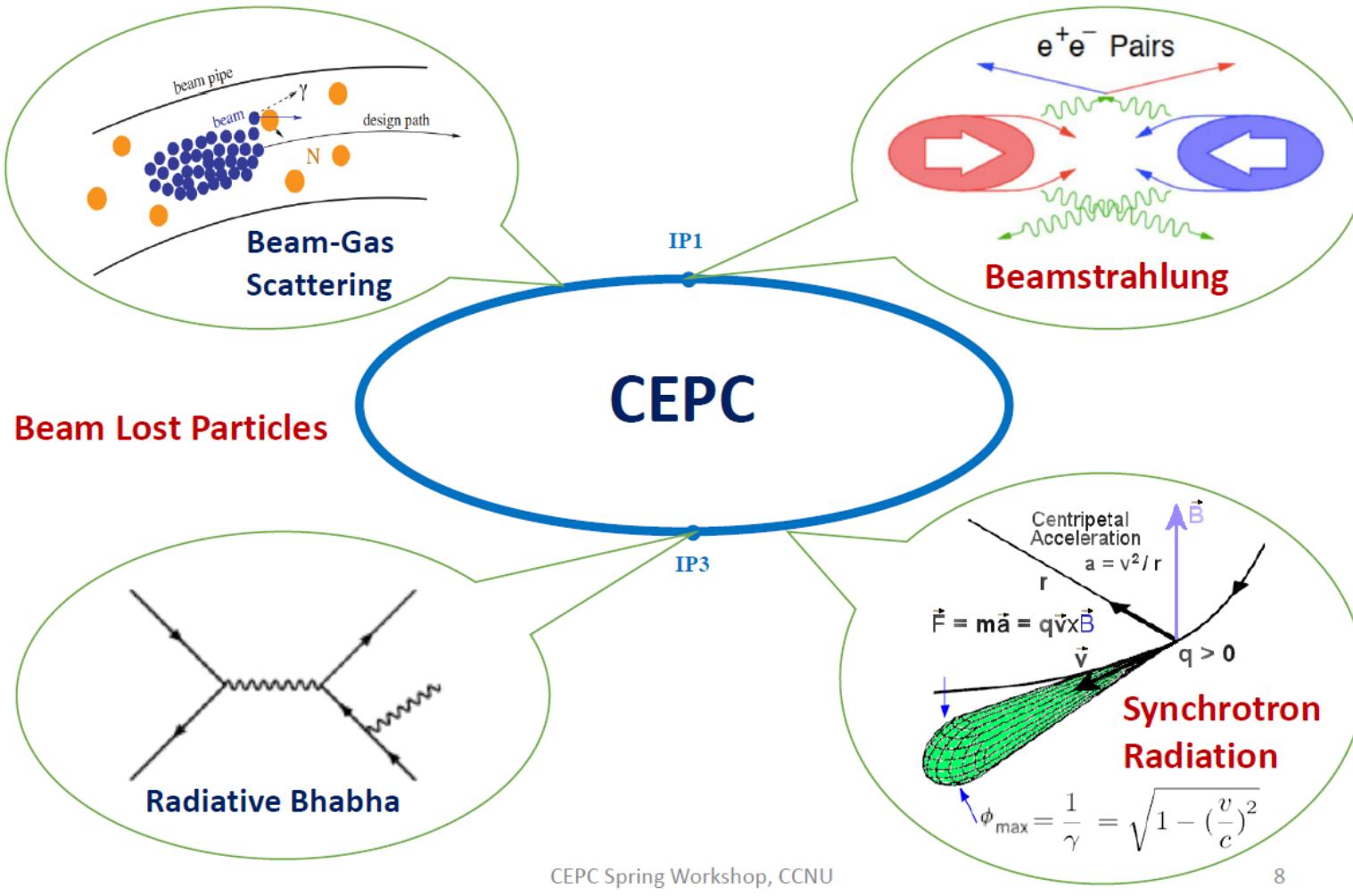
## Beam Pipe

*New beam pipe shape with beam clearance and HOM effects taken into account*



*Central area (Beryllium) to be tweaked and then be implemented together with the new beam pipe and magnets in detector simulation*

## Radiation Backgrounds





# Results of the Single Ring Scheme

Background Type	Generators	Sub-type	Particle Flux at VTX [ $cm^{-2}BX^{-1}$ ]	Particle Energy [GeV]	Priority
Synchrotron Radiation	Geant4; BDSIM	Dipole	$\sim 10^{10}$	$\sim 0.001$	★★★
		Quadrupole	$\sim 10^6$	$\sim 0.007$	
Beam Lost Particles	BBBrem; SAD	Radiative Bhabha	$\sim 10$	$\sim 120$	★★
		Beam Gas Scattering	↑	↑	
Beamstrahlung	Guinea-Pig++; PYTHIA6	Pairs	$\sim 10^{-2}$	$\sim 0.05$	★
		Hadrons	$\sim 10^{-5}$	$\sim 2$	

- The synchrotron radiation is the most important beam induced backgrounds in the single ring scheme
  - Require to reduce the critical energy and radiation power in the double ring scheme

# Pixel sensor challenges

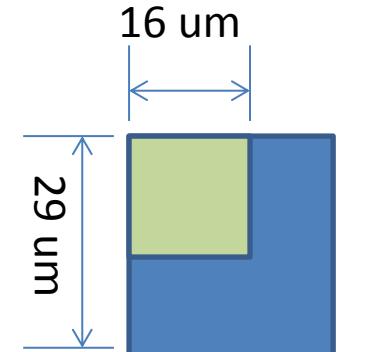
- To achieve S.P. resolution
  - Digital pixel  $\sim 16\mu m$
  - Analog pixel  $\sim 20\mu m$  (power pulsing mode in ILC)
- To lower the material budget
  - Sensor thickness  $\sim 50\mu m$
  - Heat load  $< 50 \text{ mW/cm}^2$  constrained by air cooling
- To tackle beam-related background
  - 20us/frame?
  - 300krad/year &  $3 \times 10^{12} n_{eq}/(\text{cm}^2 \cdot \text{year})$ ?

Physics driven requirements	Running constraints	Sensor specifications
$\sigma_{s.p.}$ <b>2.8um</b>		→ Small pixel <b>16um</b>
Material budget <b>0.15% <math>X_0/\text{layer}</math></b>		→ Thinning <b>50um</b>
	→ Air cooling	→ low power <b>50mW/cm<sup>2</sup></b>
r of Inner most layer <b>16mm</b>	→ beam-related background	→ fast readout <b>20us?</b>
	→ radiation damage	→ radiation tolerance <b><math>\leq 1 \text{ Mrad/ year ?}</math></b> <b><math>\leq 1 \times 10^{12} n_{eq}/(\text{cm}^2 \cdot \text{year}) ?</math></b>

# 前所未有的高指标要求

- 比ILD更苛刻的低功耗要求
  - ILD duty cycle 1ms/199ms
  - Reduction by a factor of 4
- 比ALICE/ITS upgrade更高的空间分辨率要求
  - 像素版图面积缩小为1/3

	Pixel sensor for CEPC vertex	ALPIDE for ALICE/ITS
S.P. resolution	2.8 um	5 um
Thickness	50 um	50 um
Power consumption	< 50 mW/cm <sup>2</sup>	35 mW/cm <sup>2</sup>
Integration time	20 us?	10 us with trigger
Radiation hardness	1 Mrad/ year $10^{12}$ neq/ (cm <sup>2</sup> year)	312 krad $1.7 \times 10^{13}$ neq/ cm <sup>2</sup>



Single pixel size

# Pixel Sensor的关键问题

- Sensing diode与front-end的设计优化
  - 空间分辨率
  - 模拟功耗
- Readout Architecture
  - 快速读出/时间标记
  - 数字功耗
  - 数据压缩与高速数据传输
- Radiation tolerance
  - 电离辐射
  - 非电离辐射
- Thinning
  - Backside processing

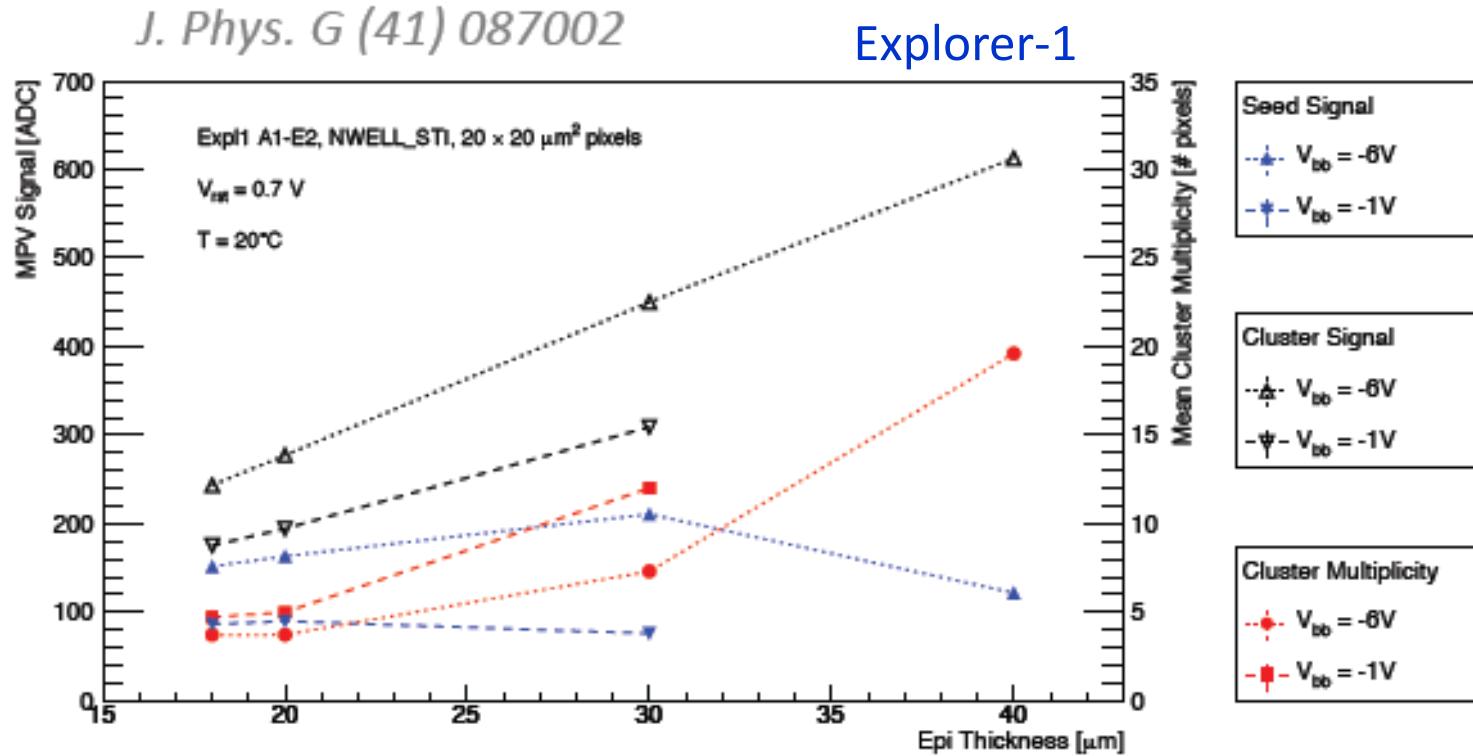


# Pixel sensor研究思路（1）： Biased diode and depletion

- Apply bias to thick HR epi.

- Larger seed signal
- Larger cluster signal
- Lower cluster multiplicity -> possibly degrade single point resolution

Christine HU-GUO, Yunpeng LU



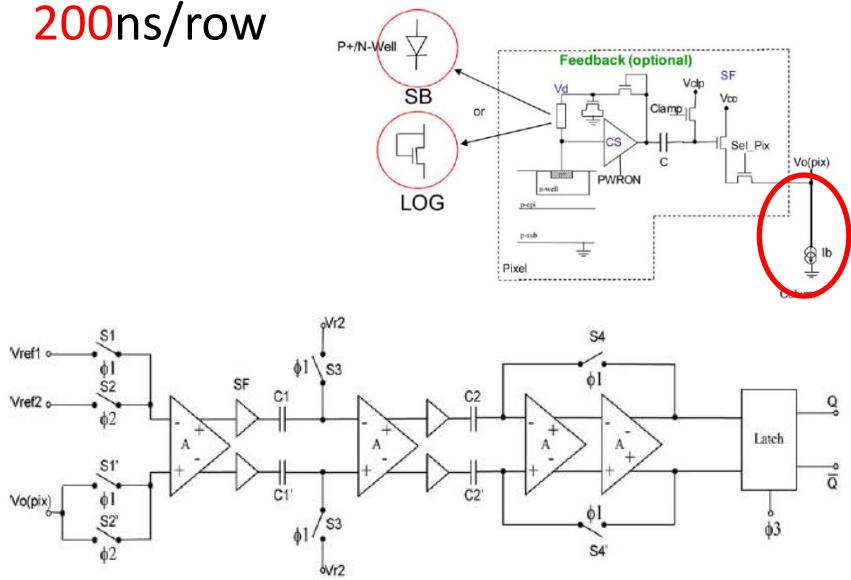
# Pixel sensor研究思路 (2) : In-pixel discrimination

Christine HU-GUO  
Yunpeng LU

- Much smaller current to drive a binary signal
  - and shorter settle time!
  - But require more area for layout.

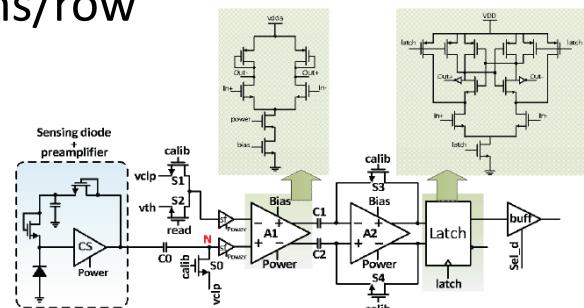
## MIMOSA32

- 55 $\mu$ A/pixel, dominated by the bias current of the output stage
- 65 $\mu$ A/column discriminator
- 200ns/row

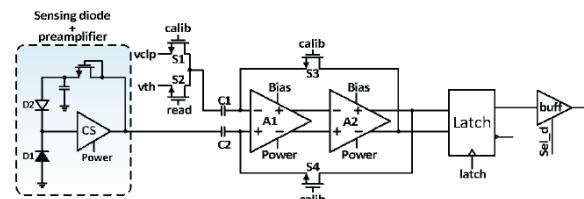


## AROM-0

- 11 $\mu$ A/pixel, in-pixel discriminator inclusive
- 100ns/row



(a) Version 1.



(b) Version 2.

# Pixel sensor研究思路（3）： Rolling shutter vs in-matrix sparsification

- Rolling shutter
  - Save on layout area
  - Conflicts between power and readout speed, and possible trade off

Christine HU-GUO  
Yunpeng LU

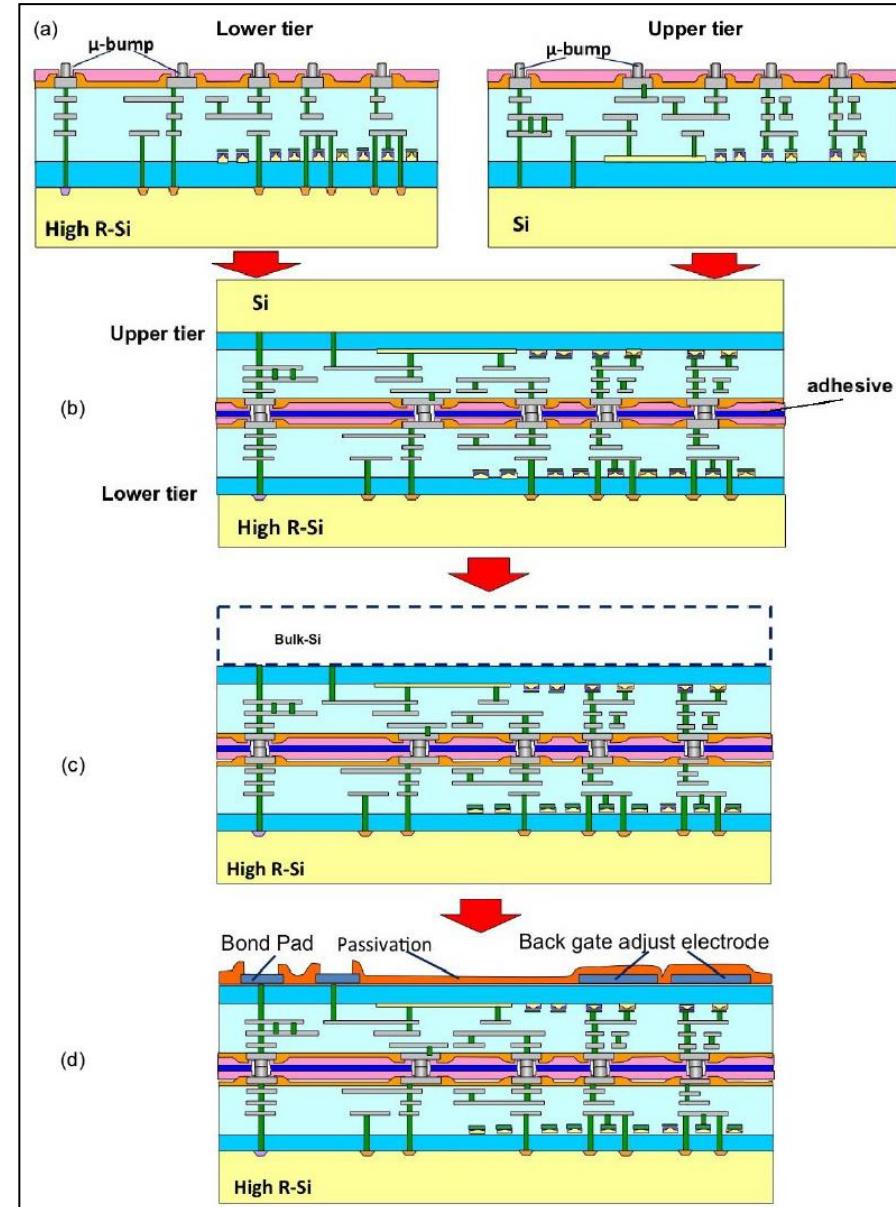
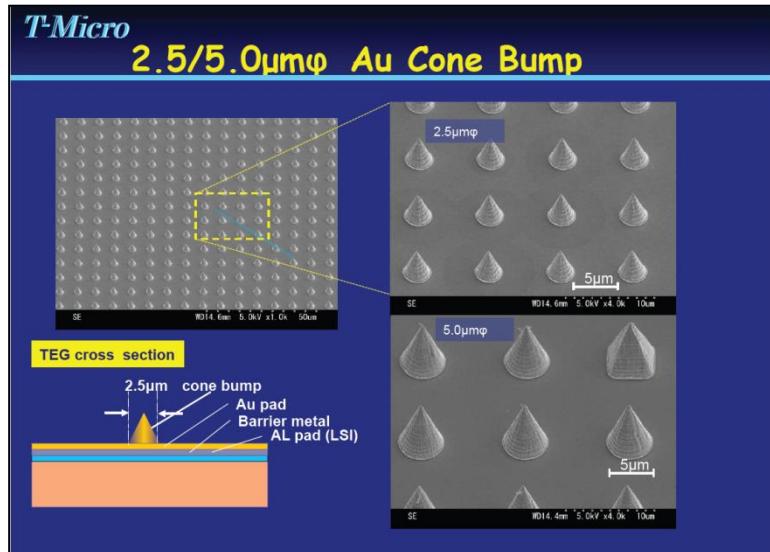
$$\begin{aligned} \text{Power} &\propto \text{N.of active rows} \\ \text{Readout interval} &\propto 1/\text{N.of active rows} \end{aligned}$$

- In-Matrix sparsification
  - Require extra area for address encoder
  - Fast and low power

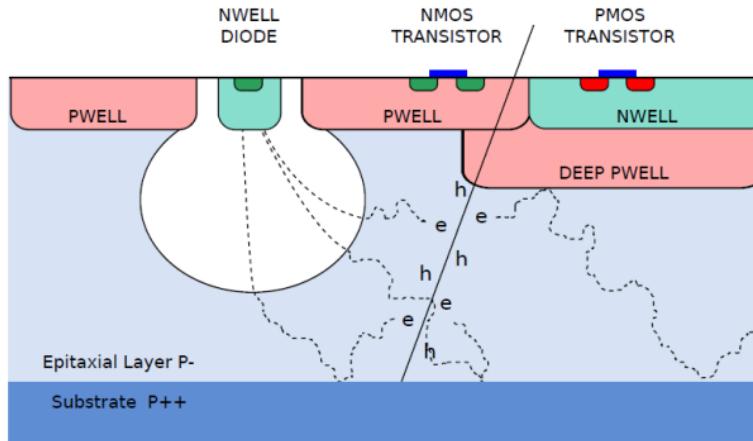
# Pixel sensor研究思路 (4) : 3D Integration

Yunpeng LU

- Pursued by SOIPIX collaboration
- Upper tier
  - SOI
  - digital readout
- Lower tier
  - SOI or CPS
  - Sensing diode and analog



# CPS pixel sensor相关的预研工作



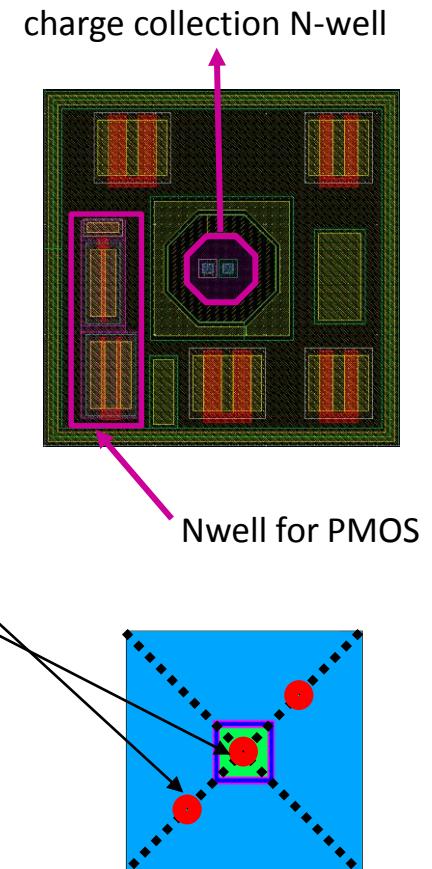
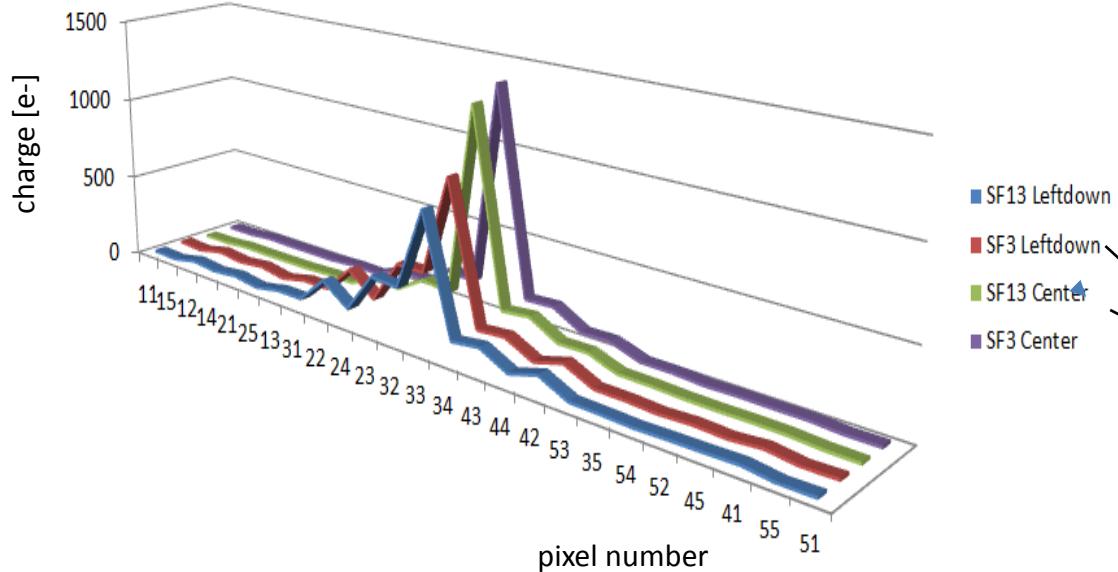
- TowerJazz 0.18um process
  - Quadruple well
  - HR epi
- First submission in Nov, 2015
  - Exploratory prototype, analog pixel
  - sensor optimization and radiation hardness study
- Second submission scheduled in May, 2017
  - Two digital prototype
  - Rolling shutter vs AERD logic

# TCAD simulation: Charge collection with competitive N-well

Ying ZHANG, Min FU, Liang ZHANG, Mei ZHAO

- To look at the effectiveness of deep P-well shielding

Sector	Diode area	Footprint area	Structure
SFB3	8 $\mu\text{m}^2$	20 $\mu\text{m}^2$	2T_nmos
SFB13	8 $\mu\text{m}^2$	20 $\mu\text{m}^2$	2T_pmos



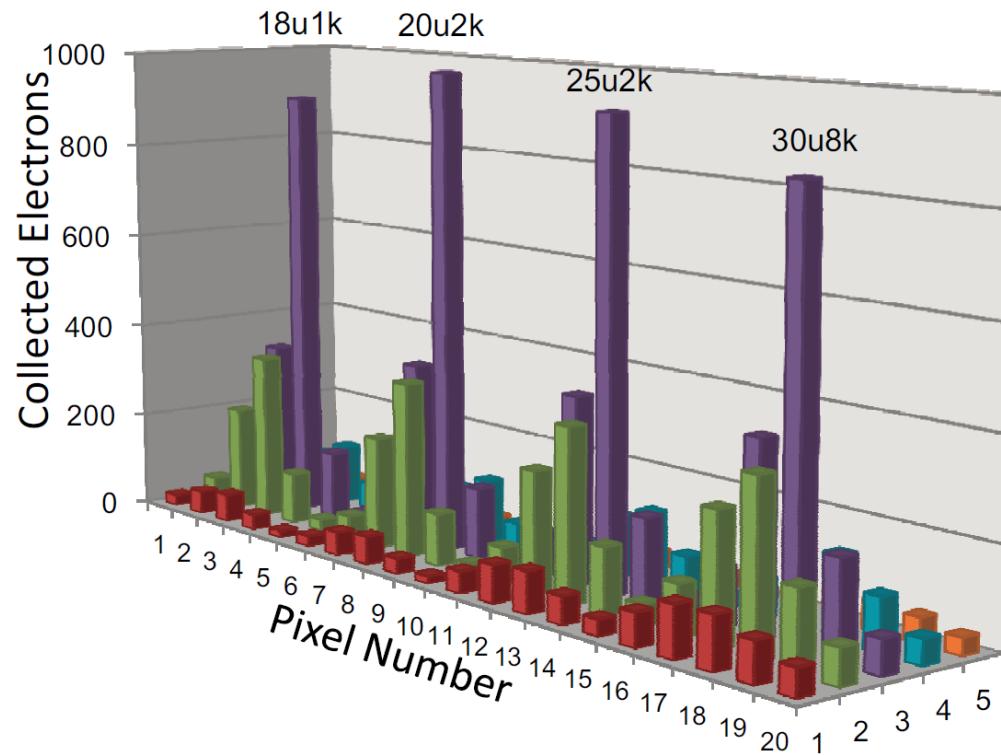
With the shielding of deep P-well, the competition of PMOS on charge collection is almost negligible → allow full CMOS within the pixel

hit position on the central pixel

# TCAD simulation: Charge collection with different epitaxial layers

Ying ZHANG, Min FU, Liang ZHANG, Mei ZHAO

- Pixel cluster with four different epitaxial layers
  - Optimization on diode geometry

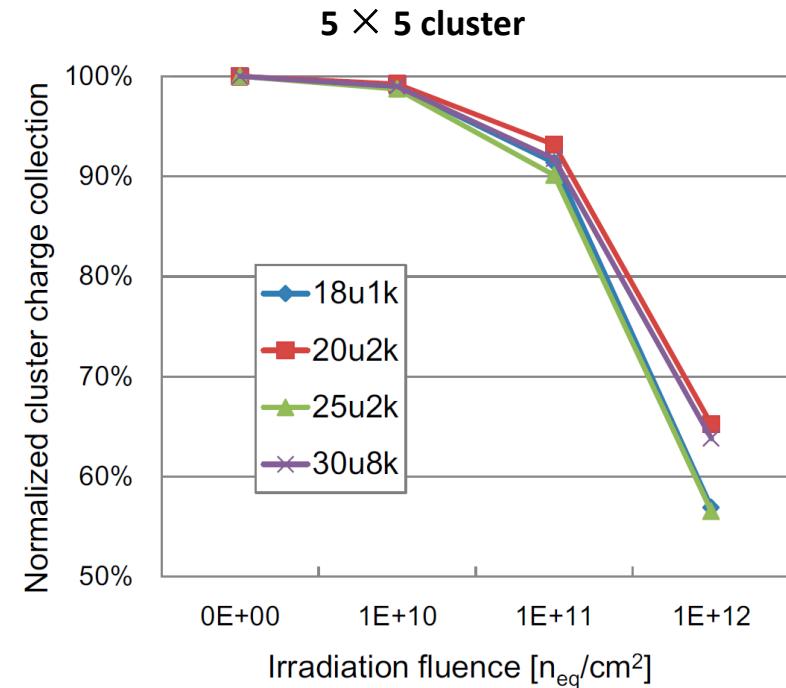
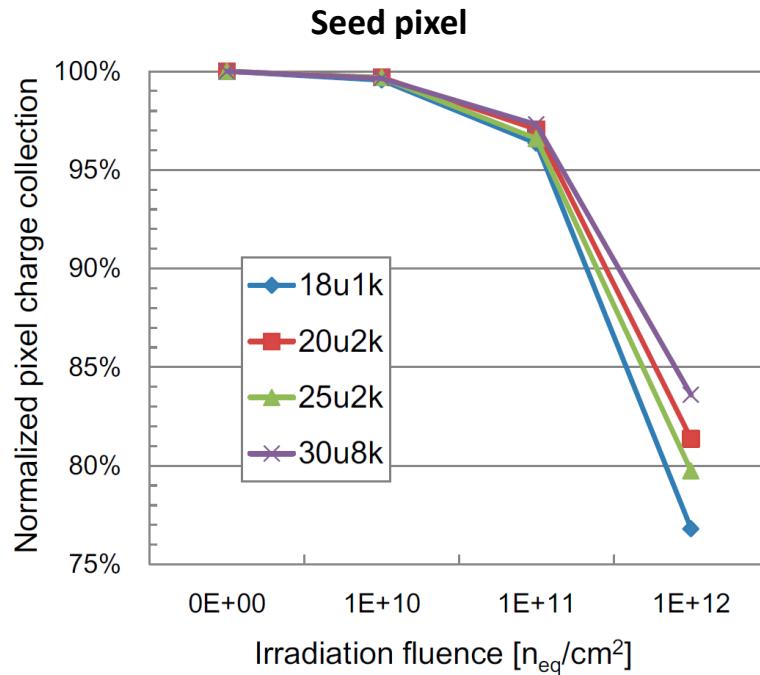


Total charge increases with the thickness and resistivity of the epi-layer, so does the charge sharing → **the 20 μm thick epitaxial layer could allow optimal charge collection**

# TCAD simulation: Charge collection with radiation damage

Ying ZHANG, Min FU, Liang ZHANG, Mei ZHAO

- 4 irradiation fluence with 4 epitaxial layer
  - Signals remain ~80% and ~60% respectively at CEPC annual fluence



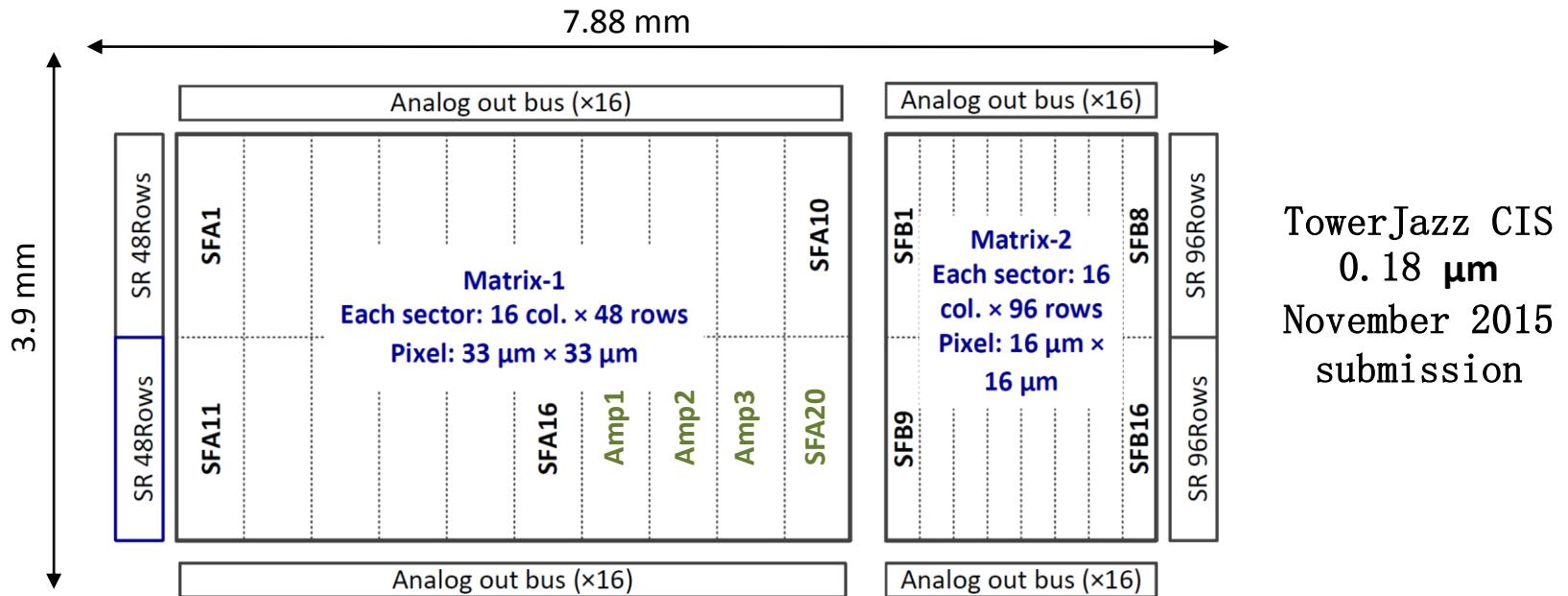
- Seed pixel: **higher resistivity → better radiation tolerance**
- Pixel cluster:
  - 25  $\mu m$  thick epi-layer worse than 20  $\mu m$  (same resistivity) → **charge sharing and radiation-caused-traps in a thicker epi-layer may degrade the performance**
  - 30  $\mu m$  thick one similar to the 20  $\mu m$  → **advantage of high resistivity can be partly neutralized by thicker epi-layer**

# First exploratory prototype

Ying ZHANG, Min FU, Liang ZHANG, Mei ZHAO

- **Goals: sensor optimization and radiation hardness study**
- **Floorplan overview:**

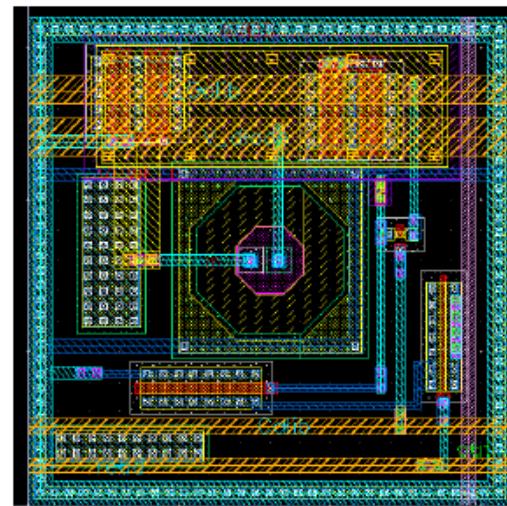
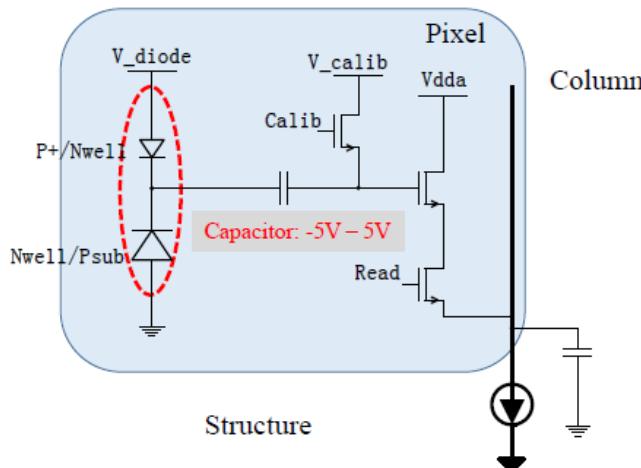
- Two independent matrices: Matrix-1 with  $33 \times 33 \mu\text{m}^2$  pixels (except one sector SFA20 with  $16 \times 16 \mu\text{m}^2$  pixels ), Matrix-2 with  $16 \times 16 \mu\text{m}^2$  pixels.
- Matrix-1: 20 sectors, each sector includes 48 rows and 16 columns
- Matrix-2: 16 sectors, each sector includes 96 rows and 16 columns



# Biased diode

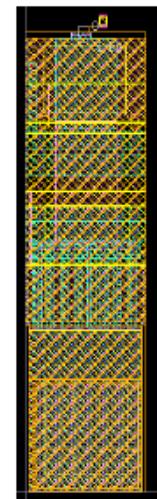
- Bias voltage up to 10 V
  - To measure seed/cluster signal versus  $V_{bias}$
  - To measure the cluster multiplicity
- Optimization of  $C_c$ ,  $V_{cal}$ , SF and noise
- Layout
  - 16um\*16um
  - Direct PAD for  $V_{diode}$

Yang ZHOU



Pixel Layout

- $16 \times 16 \mu\text{m}^2$ ;
- with transistors under  $MIM$  capacitor



Direct PAD layout: for  $V_{diode}$

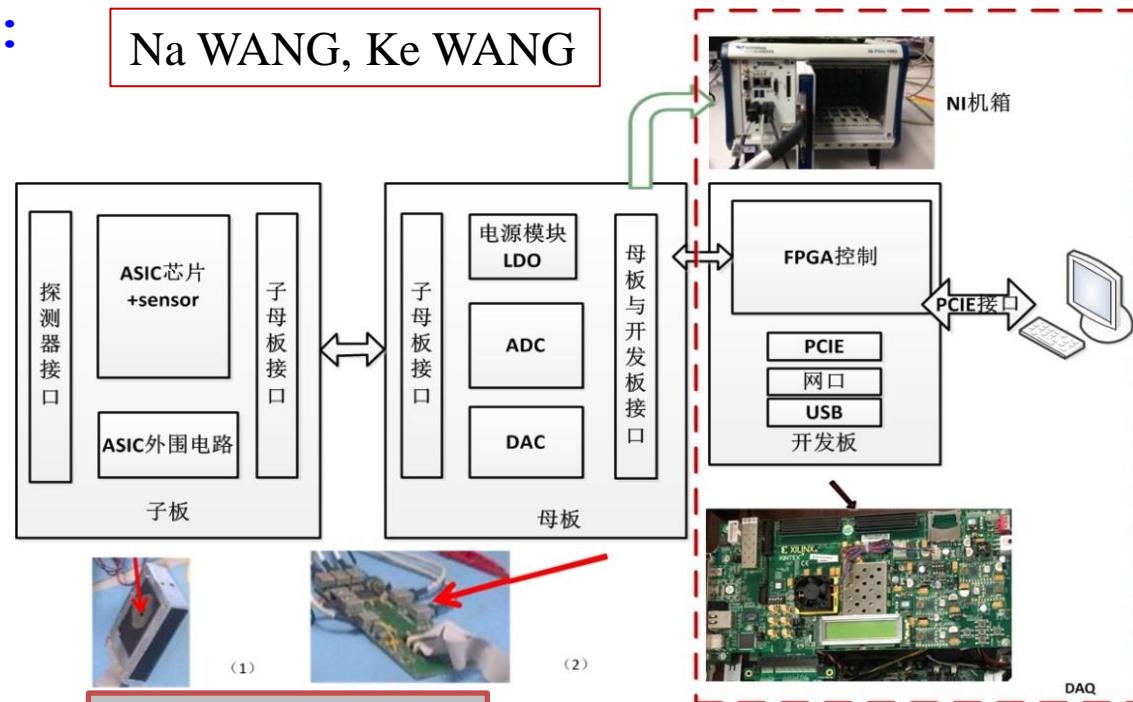
- $250 \times 65 \mu\text{m}^2$
- Without ESD
- Both sizes & power lines match with other PADs provided by foundry

# Hardware Test System for First CPS prototype

## Design structure include :

- Low noise data amplifier
- Data acquisition circuit design
- PCIE bus interface and data processing
- NI chassis interface

Na WANG, Ke WANG



## Design goals :

- low noise, high precision  
1 LSB: 20uV  
1 e- @7fF
- low cost large amount of data  
transmission > 1Gbit/s ( $16\text{bit} \times 16\text{ch} \times 4\text{MHz}$ )

**16-bitADC :**  
 $3 \times 65536 \approx 200000$ ,  
 $4\text{V}/200000 = 20\text{uV}$

- System feature :**
- PCIE records to transmit data in real time
  - SDD storage has been realized
  - **6Gbit/s real time data**

# Hardware Test System Structure

## The child motherboard :

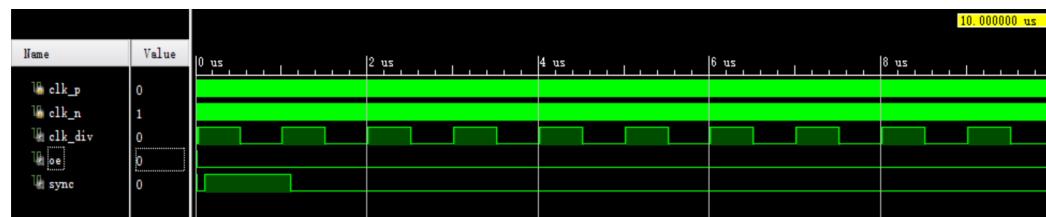
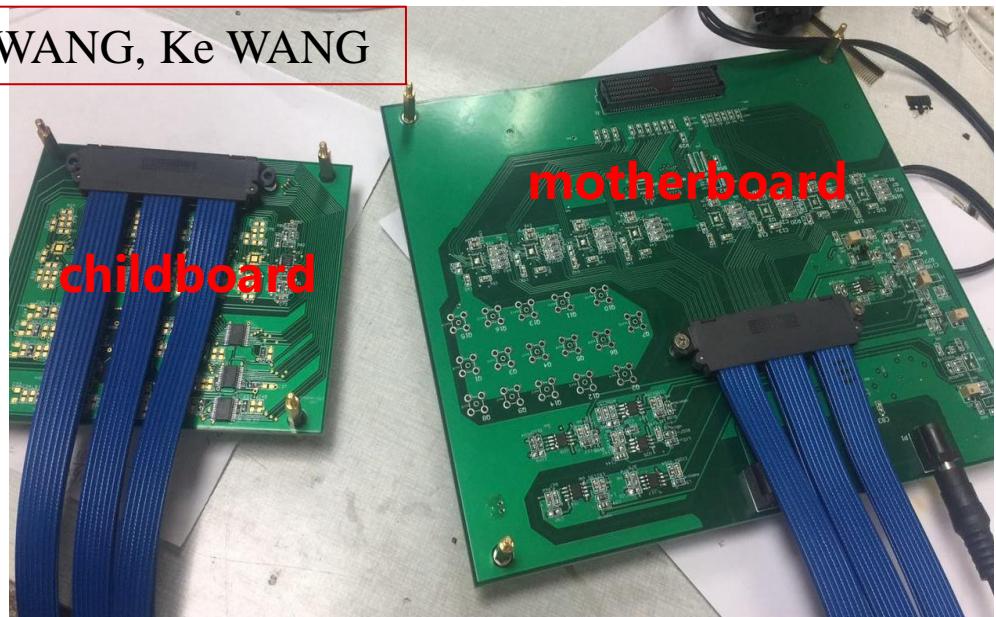
Na WANG, Ke WANG

childboard:

- process the analog signal from the chip to the motherboard
- Completed the part of the peripheral circuit welding, the next step to bond chip

motherboard :

- **16 channel ADC** to FPGA
- selftest finished:
  - provide power and bias
  - program control, clock, address by FPGA



# 第二次CPS流片的设计目标

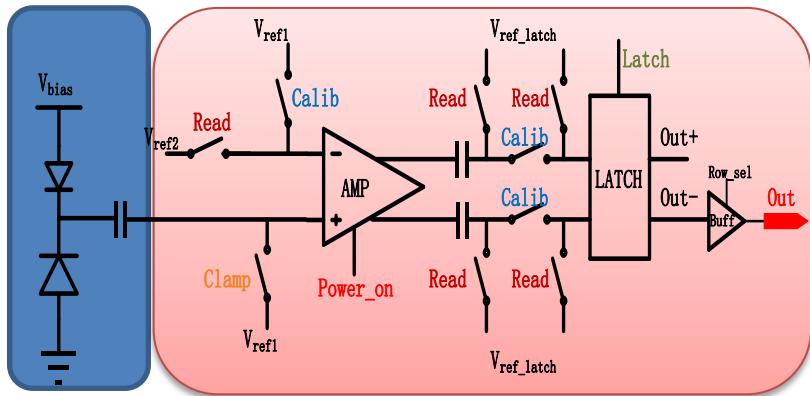
## ◆ CPS development context and the design goals of our attempt

Name	Structure	Pixel pitch	Integ.time	Power density	Spatial resolution
MISTRAL (IPHC)	Column-level comparator, Rolling-shutter	$22 \times 33$ (66) $\mu\text{m}^2$	30 $\mu\text{s}$	200 (100) $\text{mW/cm}^2$	
ASTRAL (IPHC)	In-pixel comparator, Rolling-shutter	$24 \times 31$ (IB) $\mu\text{m}^2$ $36 \times 31$ (OB) $\mu\text{m}^2$	20 $\mu\text{s}$	85 $\text{mW/cm}^2$ 60 $\text{mW/cm}^2$	$\approx 5\mu\text{m}$
ALPIDE (CERN, IN FN, CCNU, YONSEI)	In-pixel comparator, In-matrix zero compression readout	$27 \times 29$ $\mu\text{m}^2$	< 4 $\mu\text{s}$	< 39 $\text{mW/cm}^2$	
Attempt	Rolling shutter & AERD	More compact	< 10 $\mu\text{s}$	< 80 $\text{mW/cm}^2$	Higher resolution

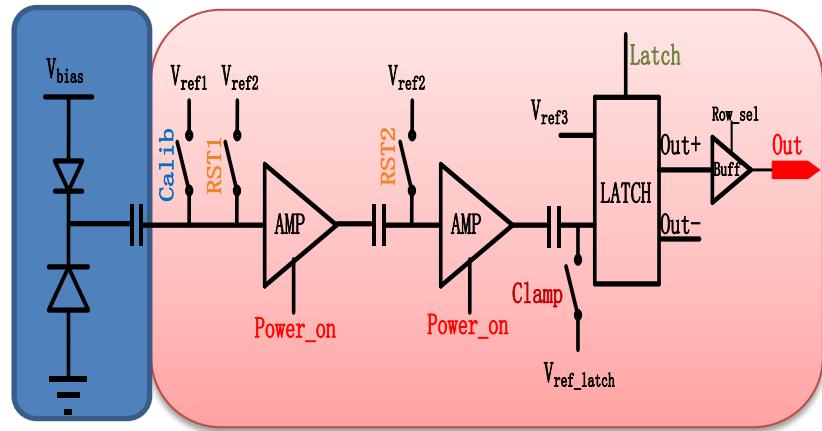
# Rolling shutter方案

Yang ZHOU

Digital pixels in rolling-shutter readout mode: 2 different versions

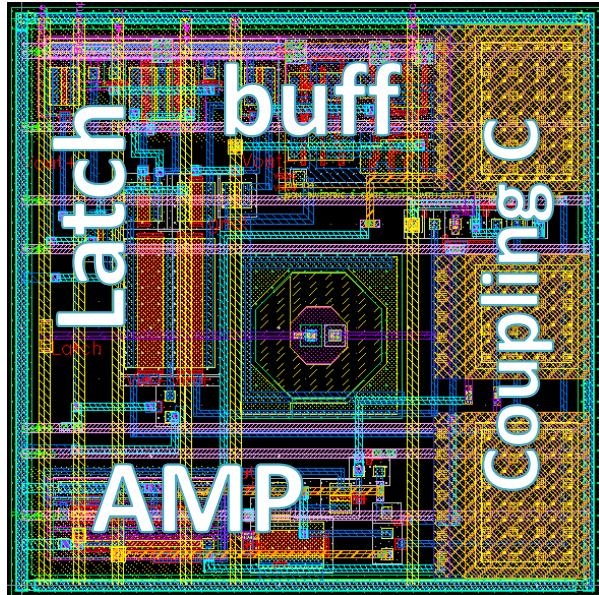


Version 1: differential amplifier + latch



Version 2: two stage CS amplifiers + latch

Pitch size: 22  $\mu$ m

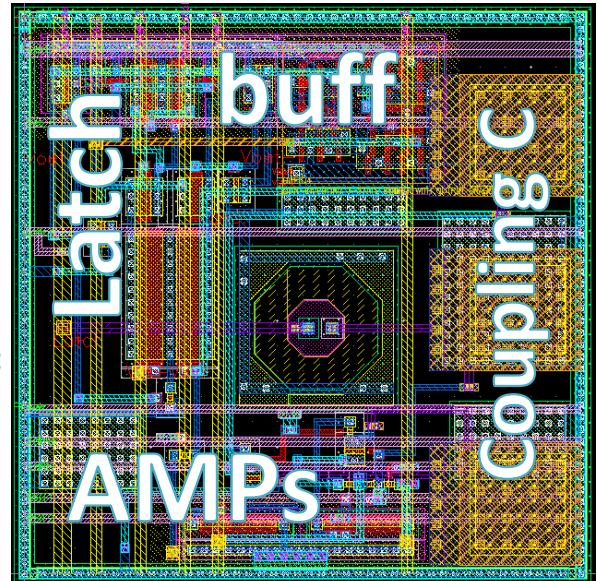


- Same amount of transistors;
- Offset cancellation technique;
- Version 2 has higher signal gain, but suffers “more” from “Latch” input voltage distortion.

Some key parameters in the design:

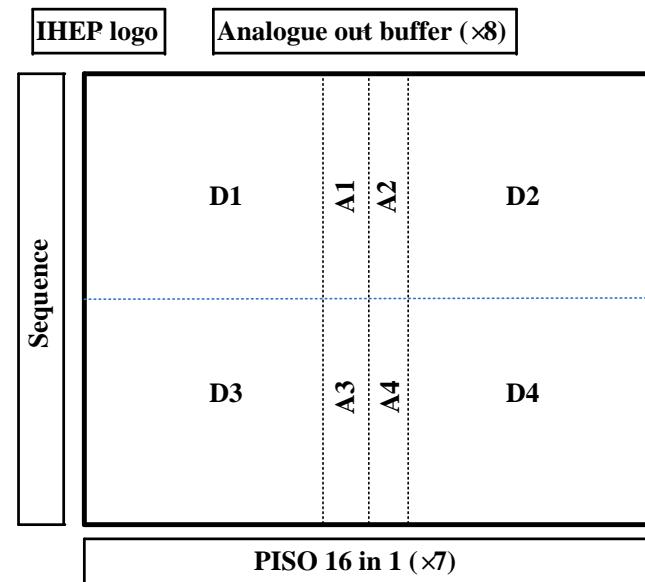
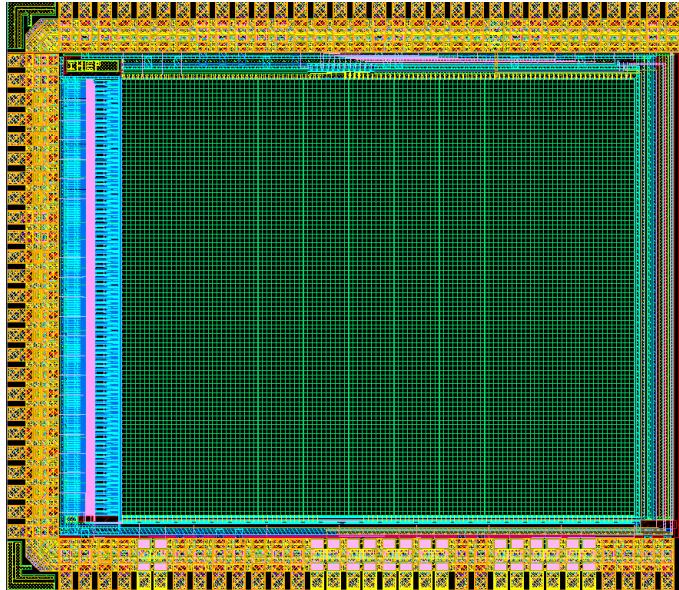
- Sensing point
- AMPs: noise/gain
- Latch: offset
- Timing: read out speed

Pitch size: 22  $\mu$ m



# Rolling shutter方案

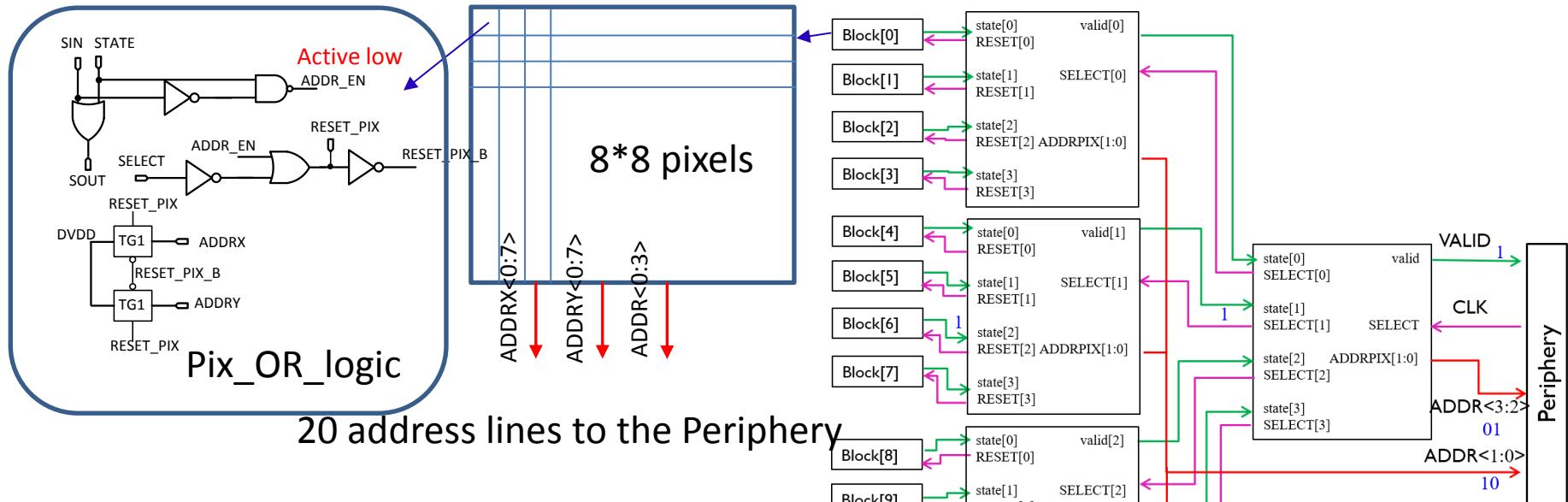
Yang ZHOU



- $3 \times 3.3 \text{ mm}^2$ ;
- $96 \times 112 \text{ pixels with 8 sub-matrix}$
- Processing speed:  $11.2 \mu\text{s/frame}$  for  $100 \text{ ns/row}$ ;
- Output data speed:  $160 \text{ MHz}$ ;
- Power:  $3.7 \mu\text{A/pixel}$ ;

# 基于AERD的MIC4方案

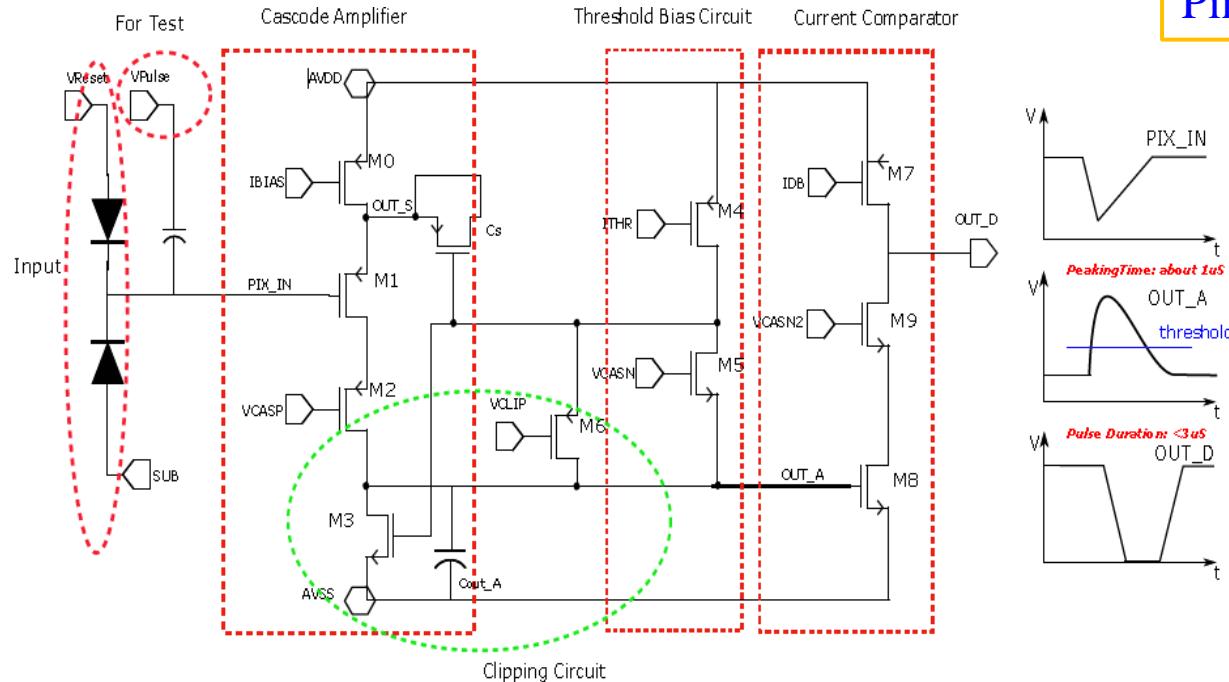
Ping Yang



- ALPIDE matrix readout circuit AERD has many connection lines occupy larger area than the logic circuit itself;
- OR gate chain: speed is limited with the number of the chain pixels;
- Combine these two solutions: 64 pixels as a group using OR gate chain, groups using AERD structure to readout

# MIC4 Front-end (1): current comparator

Ping Yang



- Signal charge creates negative voltage step  $\Delta V_{PIX\_IN}$  at input node(PIX\_IN).
- From OUT\_A baseline voltage to point where discriminated output OUT\_D flips when  $I_{M8} > I_{DB}$ .

$$\Delta V_{OUT\_A} \approx \frac{C_s \cdot \Delta V_{PIX\_IN}}{C_{OUT\_A}} = \frac{C_s}{C_{OUT\_A}} \cdot \frac{Q_{in}}{C_{PIX\_IN}}$$

## Simulation results

- ENC:  $8 e^-$
- Power cons.:  $61 nA/pixel$
- Threshold:  $140 e^-$
- Peaking time  $< 1 \mu s$
- Pulse duration  $< 3 \mu s$

# MIC4 Front-end (2): Charge-sensitive amplifier

Ying ZHANG

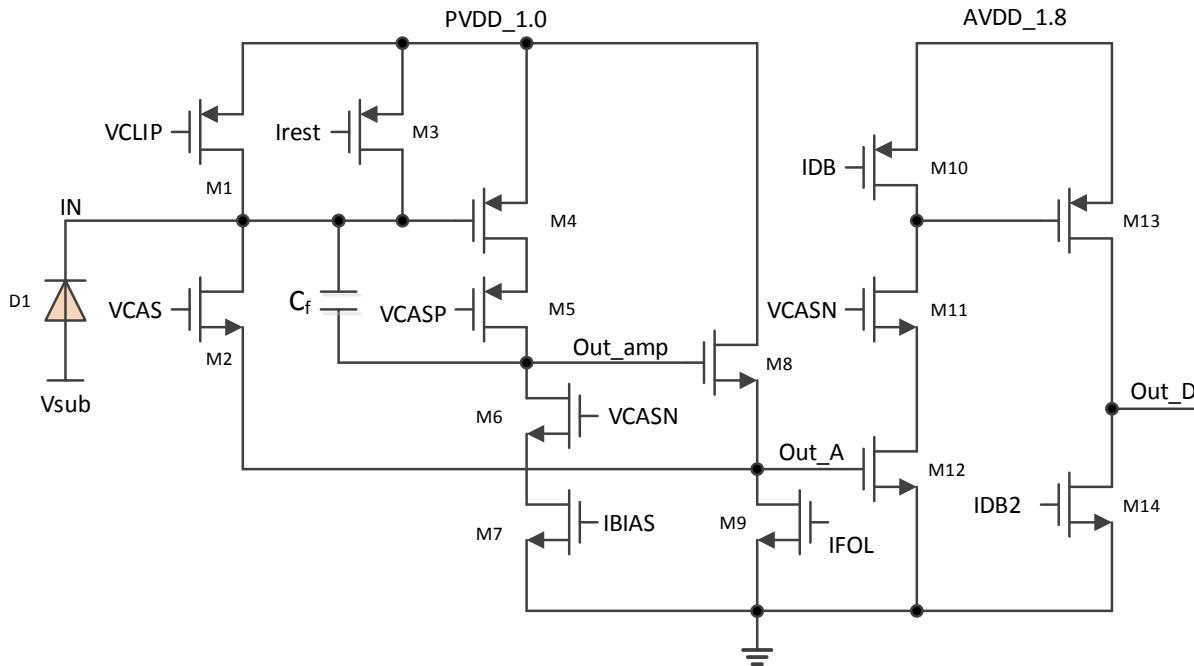
CSA based front-end circuit:

A direct cascode amplifier for the CSA

Simple structure with high gain → for a compact layout

A very low feedback capacitance  $C_f$  (0.2 fF) with low mismatch → for a high charge-to-voltage conversion gain, low noise and low mismatch between pixels

A single-end current comparator → for a compact layout



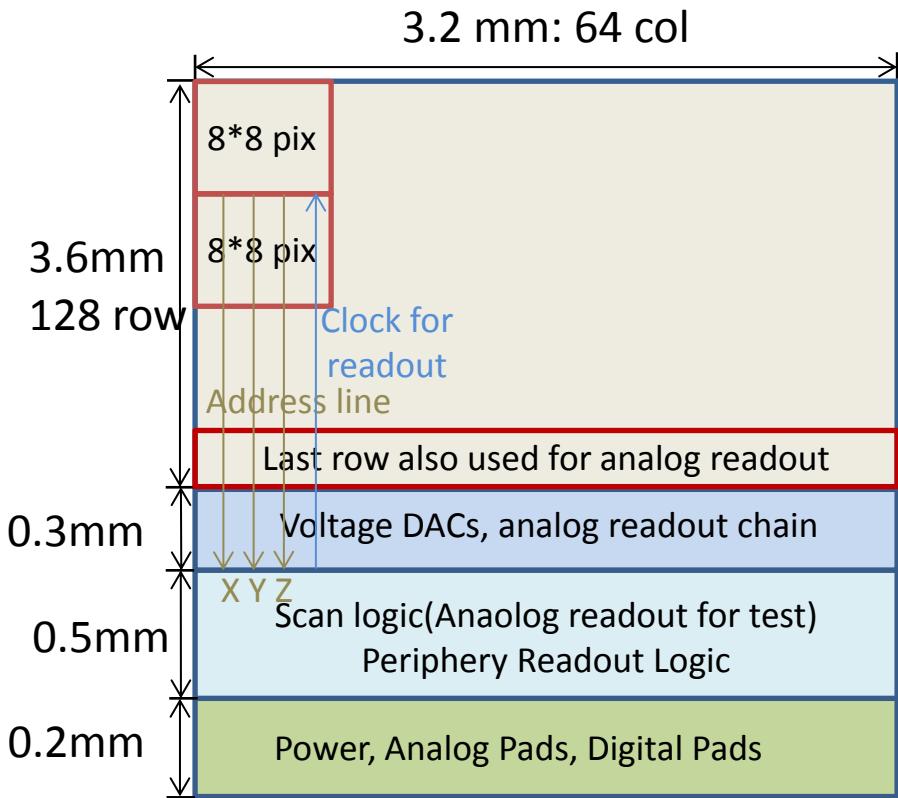
CSA based analog front-end circuit

Simulation results

- ENC: 24 e<sup>-</sup>
- Power cons.: 35 nW/pixel
- Threshold: 145 e<sup>-</sup>
- Peaking time < 550 ns @ Qin < 1.5 ke<sup>-</sup>
- Pulse duration < 8.3 μs @ Qin < 1.5 ke<sup>-</sup>

# MIC4整体设计

Ping Yang



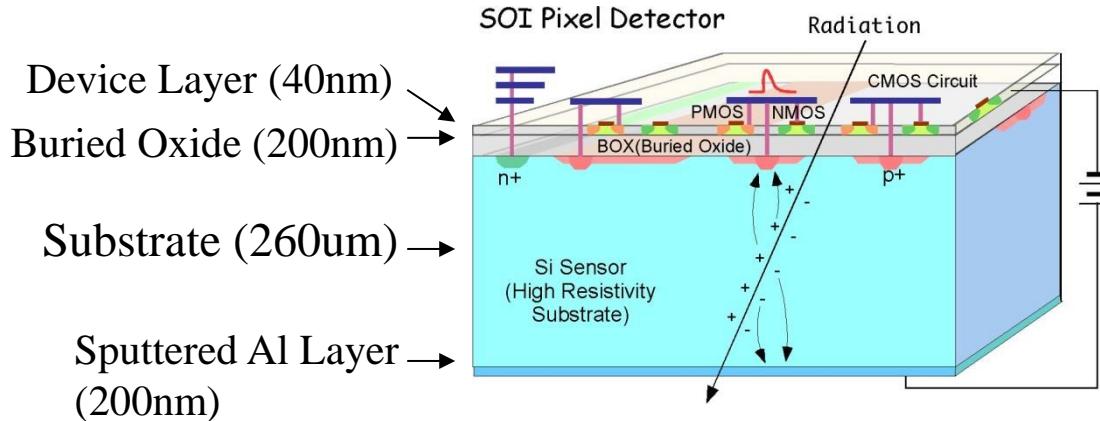
## MIC4 Chip:

- $3.2 \times 3.7 \text{ mm}^2$ ;
- $128 \times 64 \text{ pixels}$
- Integration time  $< 5 \mu\text{s}$
- Speed: 40 MHz/pixel
- Power:  $< 80 \text{ mV/cm}^2$ ;

## Chip periphery:

- Band Gap
- Voltage DAC
- Current DAC
- LVDS
- Custom designed PADs

# SOI pixel sensor相关的预研工作



- LAPIIS 0.2um process
  - Fully depleted CMOS
  - HR substrate
- INTPIX2P5耗尽特性研究, 2015
  - Infrared laser test
  - $^{241}\text{Am}$  source test
- Compact Pixel for Vertex (CPV芯片)
  - CPV1/2 (2015/2016)
  - Focus on Sensing diode + Front end

## Pixel Sensor的关键问题

- Sensing diode与front-end的设计优化
  - 空间分辨率
  - 模拟功耗
- Readout Architecture
  - 快速读出/时间标记
  - 数字功耗
  - 数据压缩与高速数据传输
- Radiation tolerance
  - 电离辐射
  - 非电离辐射
- Thinning
  - Backside processing

半导体辐射探测器研讨会, 北京, 2017.4.27-28

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# Laser Test on INPIX2P5

Yunpeng LU, Yi LIU

- INTPIX2P5 offers a good chance to look into the **depletion** of sensor (designed in 2011)
  - Pixel size  $19 \times 19 \text{ }\mu\text{m}^2$
  - **Analog readout (CDS)**
  - Central window of  $5 \times 9\text{ }\mu\text{m}^2$
- 1064nm focused to  $3.2\text{ }\mu\text{m}$ , simulating MIP
  - Pass through the central window of seed pixel

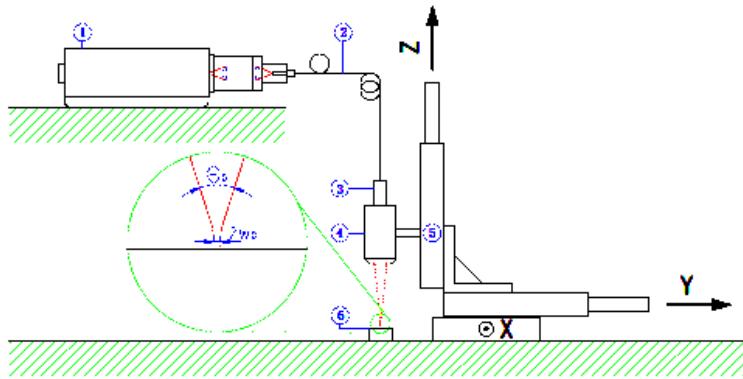
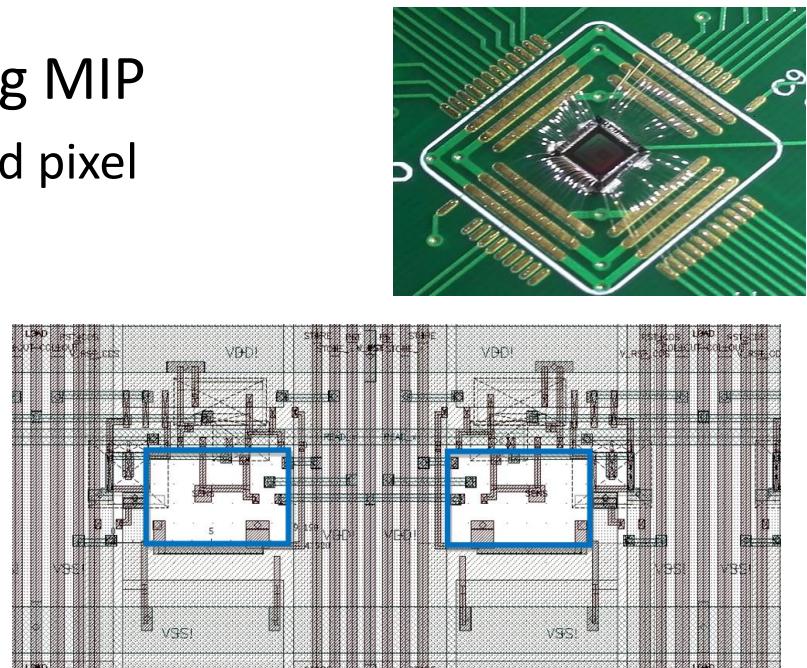
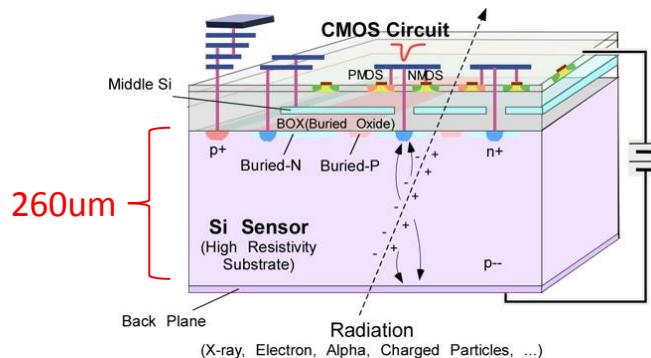


Fig. 2. ① Laser generator, ② optical fiber, ③ collimator, ④ lens, ⑤ 3D linear motion platform, ⑥ detector chip



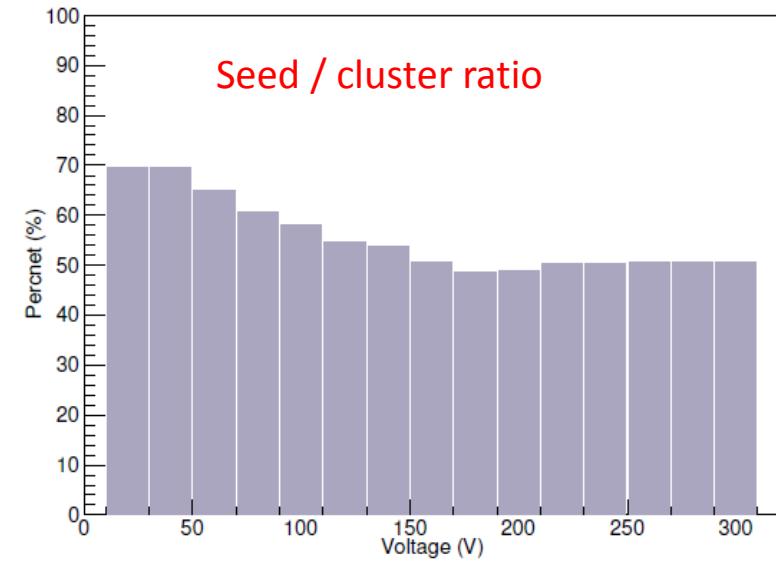
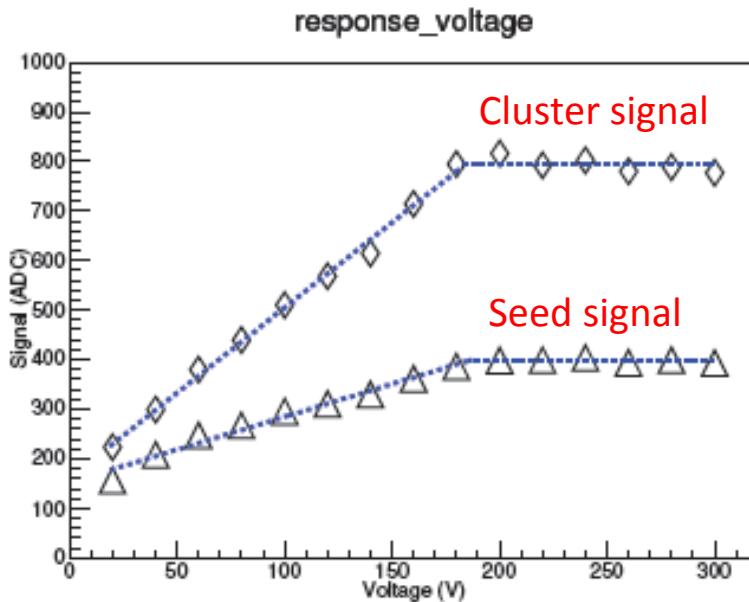
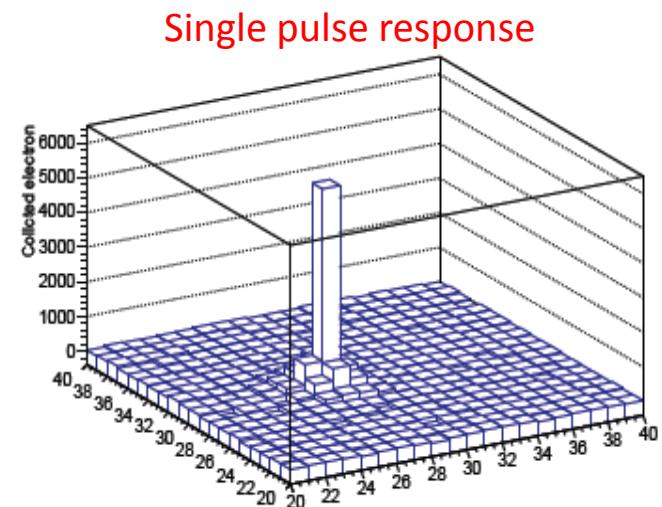
Layout of 2 pixels with only metal shown

# Laser test results

Yunpeng LU, Yi LIU

- 70% of charge collected by the seed pixel
  - $V_{bias} = 20V$ , expect to deplete 80um
- Signal increases with  $V_{bias}$ 
  - Fully depleted around 190V
  - Seed / cluster ratio decreases with  $V_{bias}$

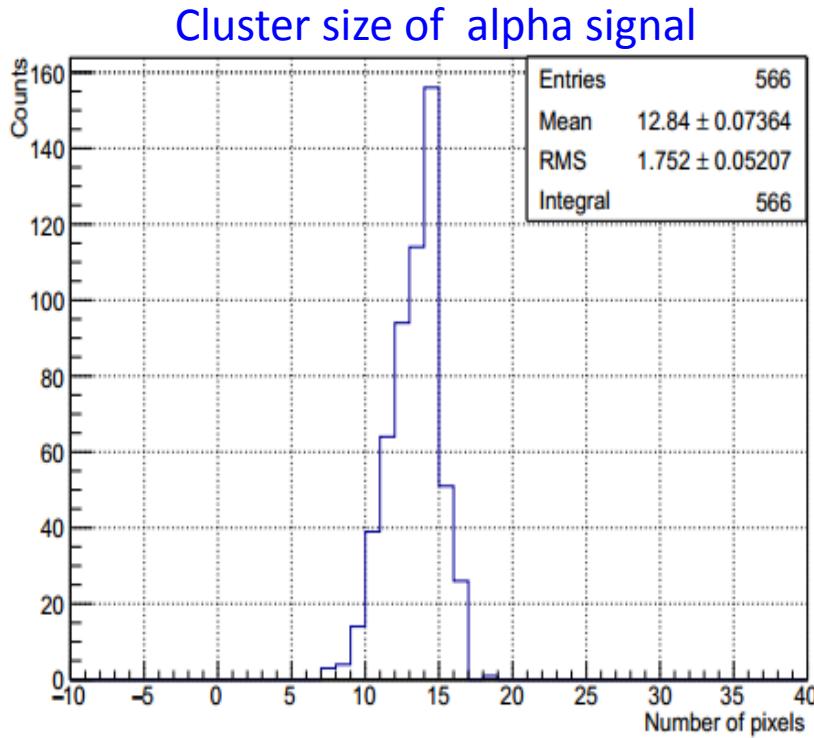
Y. LU, Chinese physics C, Vol. 40 (2016), 016202



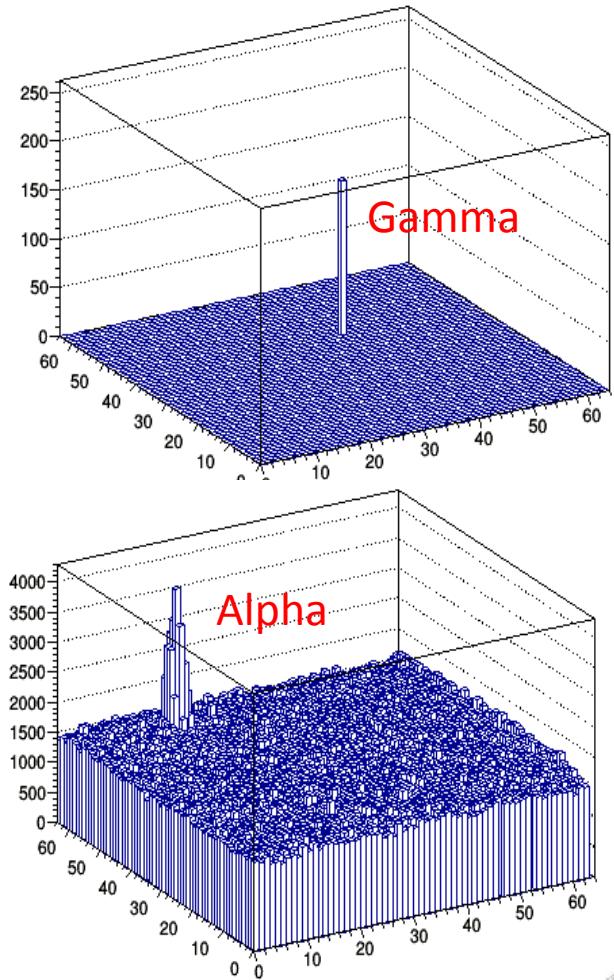
# $^{241}\text{Am}$ test results

Yunpeng LU  
Hongyang XING

- Full depletion confirmed by 5.4 MeV alpha
  - Backside illumination
  - $\sim 20 \mu\text{m}$  penetration depth

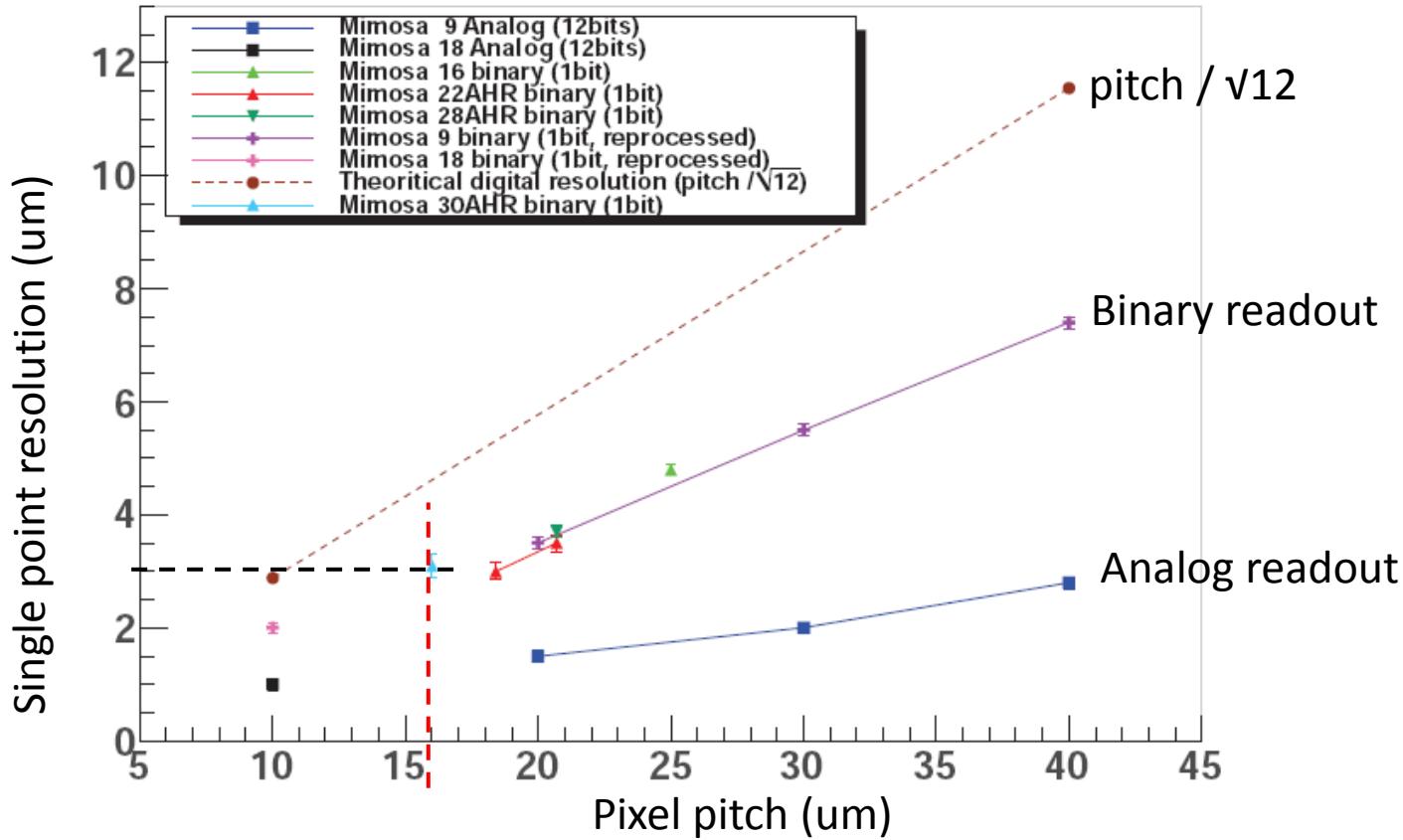


Typical signal distribution



# CPV for CEPC

- Compact Pixel for Vertex (CPV)
  - Small pixel size, 16um pitch
  - Digital pixel (in-pixel hit discrimination)



# A comparison of digital pixels

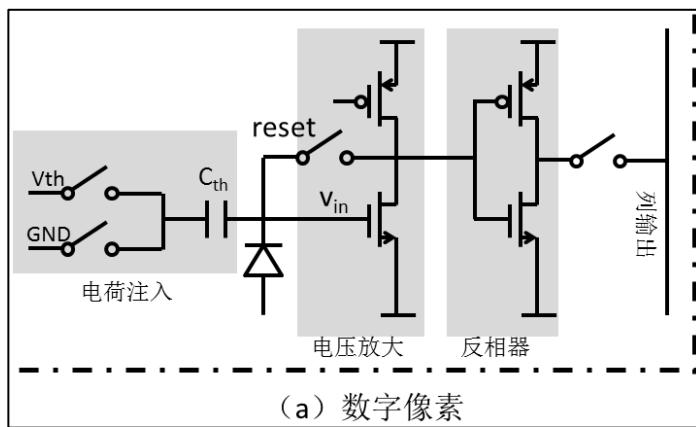
	ASTRAL	ALPIDE	CPV
Process technology	$0.18 \mu m$ CMOS		$0.2 \mu m$ SOI
Readout strategy	Rolling shutter	asynchronous	Rolling shutter
Readout time	$20 \mu s$	<2 $\mu s$	
Power	$85 \text{ mW/cm}^2$	$39 \text{ mW/cm}^2$	Analog power $< 10 \text{ mW/cm}^2$
Pixel size	$22 \times 33 \mu m^2$	$28 \times 28 \mu m^2$	$16 \times 16 \mu m^2$
Spatial resolution	$\approx 5 \mu m$		Expected $< 3 \mu m$
Total signal for MIP	$\approx 1200 e^-$ ( $20 \mu m$ epi-layer partly depleted)		$\approx 4000 e^-$ (back thinning to $50 \mu m$ , fully depleted)

- Unique opportunity to explore very compact pixel circuit
  - 3 times larger MIP signal
  - Possibly smaller cluster size

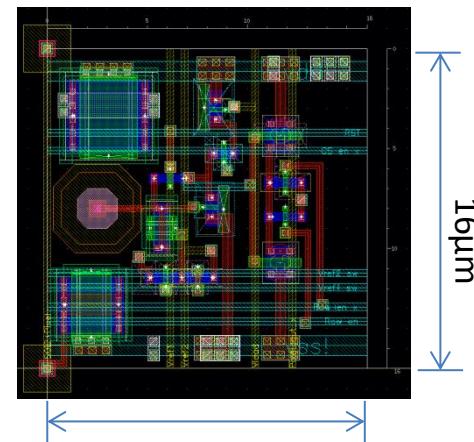
# Design of CPV1

Yunpeng LU

- First digital pixel of 16um pitch
- CS voltage amplifier, gain  $\sim 10$
- Inverter as **discriminator**
- Threshold charge injected to sensing node
- Pixel array: 64\*32 (digital) + 64\*32 (analog)
- Double-SOI process for shielding and radiation enhancement
- Submitted June, 2015

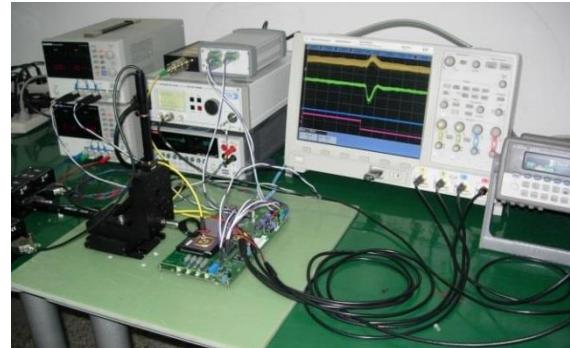


CPV1 digital pixel



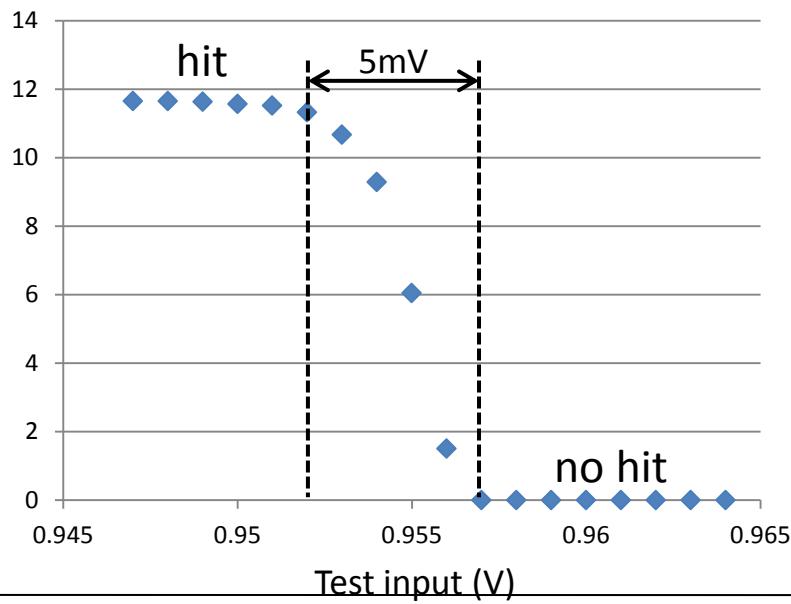
# Single pixel test

- Chip circuit function verified on single pixel
  - Voltage gain of amplifier  $\sim 10$
  - Threshold scan
  - Temporal noise  $\sim 50 e^- (< 20 e^- \text{ expected})$
- Bias voltage not applicable due to a design fault
  - Diode capacitance 3 times larger

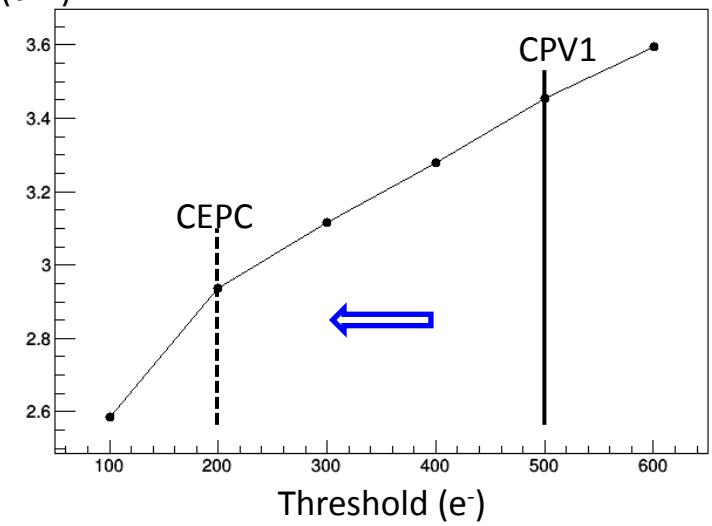


Yunpeng LU  
Zhigang WU

Hits registered



Resolution (um)  
Graph



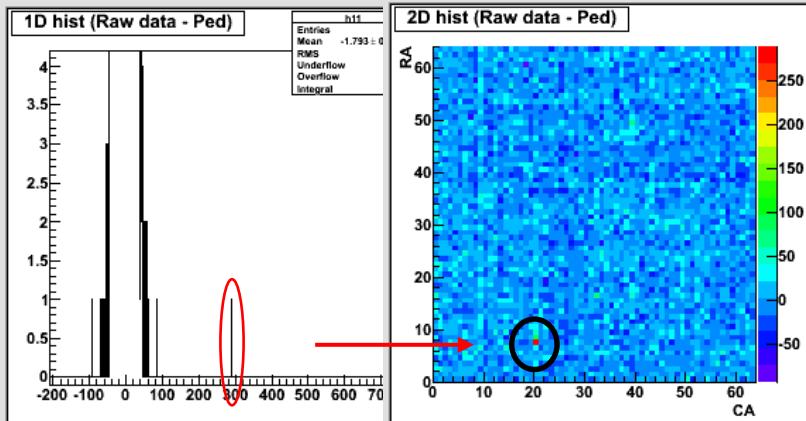
Resolution vs Threshold, Simulation by Z. WU

# $^{55}\text{Fe}$ radiative source test

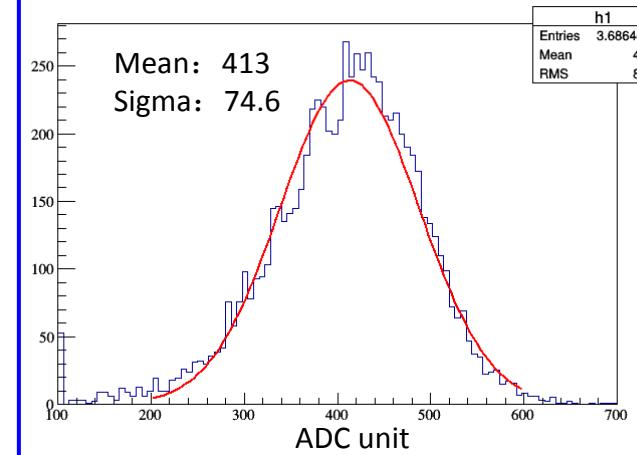
- Analog pixel array
  - 5.9keV X-ray photon ( $1640\text{e}^-$ );
  - Single photon event clearly visible;
  - Diode capacitance calibrated by using the 5.9 keV peak ( $3 \times 3$  cluster);
  - Average ENC =  $47\text{e}^-$ ;
- First proof of principle obtained.
  - Evaluation of digital pixel array is underway.

Yunpeng LU  
Zhigang WU

Analog readout of 5.9keV single X-ray photon



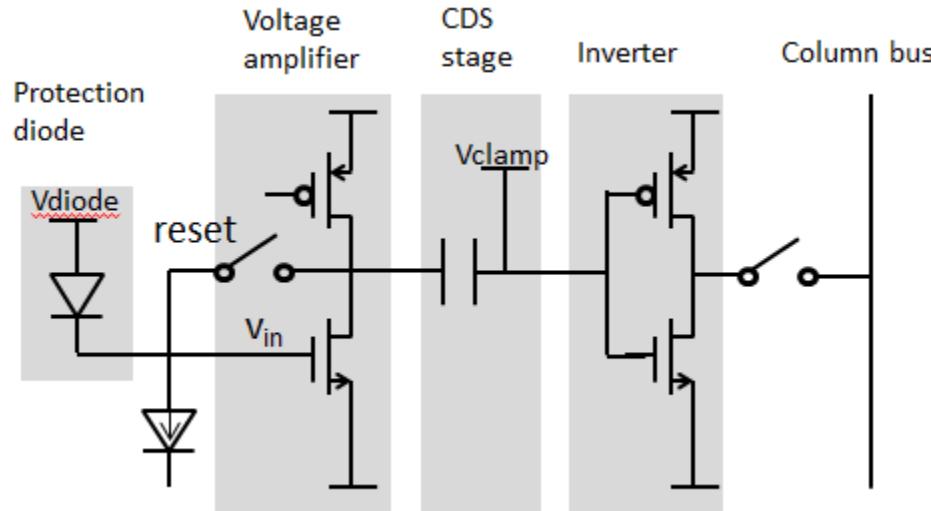
$^{55}\text{Fe}$  energy spectrum



# Design of CPV2

Yunpeng LU  
Yang ZHOU

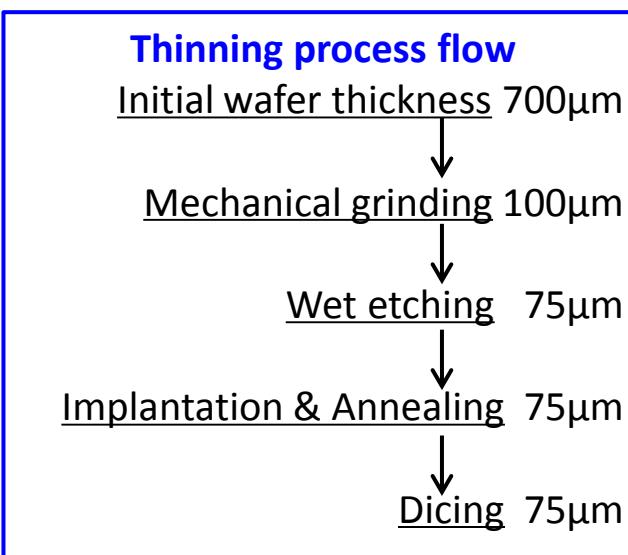
- Protection diode added
  - Enable full depletion on sensor
- In-pixel CDS stage inserted
  - improve RTC and FPN noise
  - replace the charge injection threshold
- Submitted June, 2016



# Thinning process for CPV2

- Wafer thinning -> Chip dicing
  - SOIPIX collaboration
  - Finished in March 2017
  - To be delivered to IHEP in May 2017

Yunpeng LU



# Summary

- Pixel sensor is the core component for vertex sub-detector.
  - Physics driven requirement defined.
  - Running constraints not settle yet.
- Sensor optimization, digital pixel circuit and fast readout are being pursued by active R&D efforts.
  - Fully depletion of SOI verified.
  - A variation of amplifier and discriminator explored.
  - Rolling shutter and data-driven readout compared.

# Acknowledgement

This work is supported by

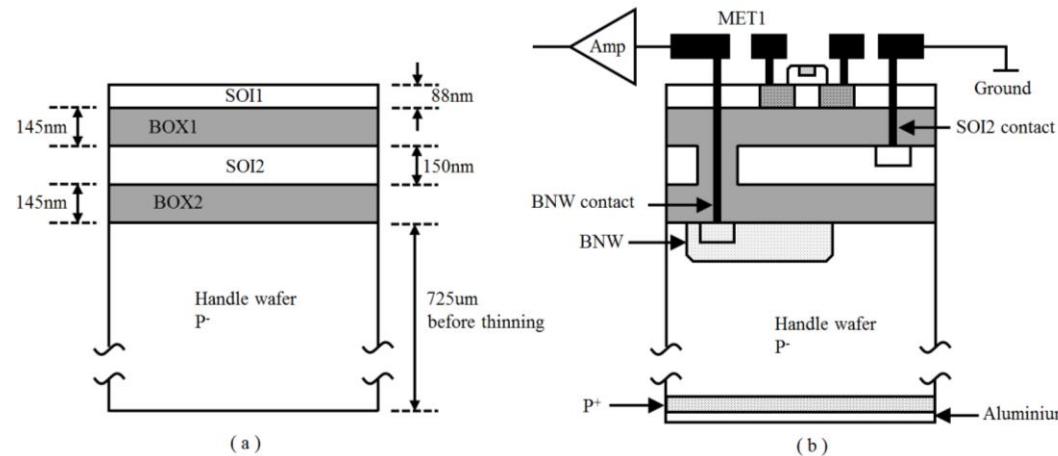
- 科技部重点研发计划，项目号2016YFA0400404
- 国家自然科学基金，项目号11575220, 11605217
- 中国科学院高能物理研究所创新基金，CEPC物理理论和探测器及实验关键技术预研
- 核探测与核电子学国家重点实验室
- 中国科学院粒子物理前沿卓越中心（CCEPP）

## Backup slides



# Double-SOI process

- Double-SOI wafer
  - Second SOI layer as shielding between Front-end and sensing diodes
  - Compensation voltage can be applied to mitigate TID effect



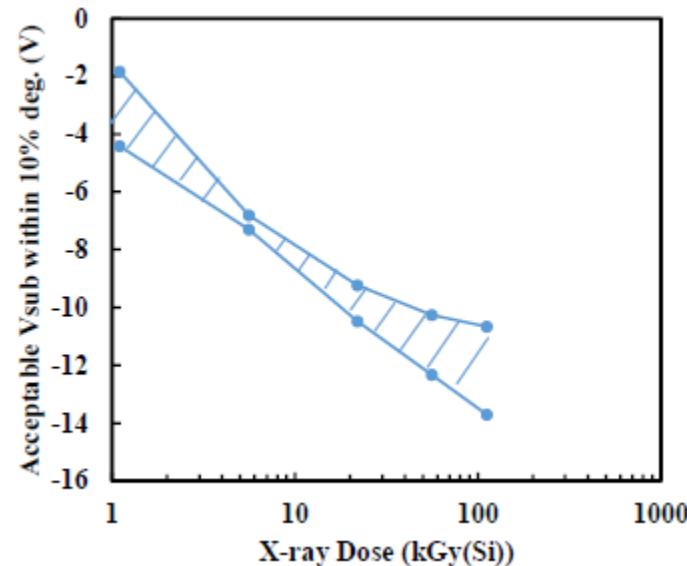
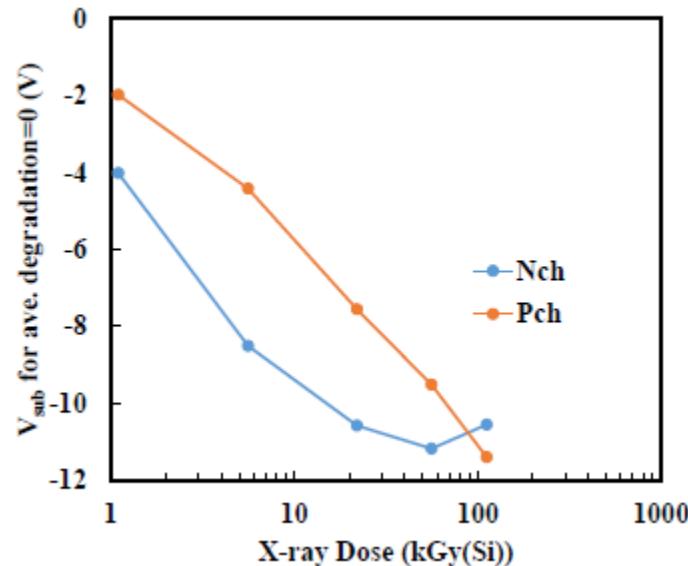
Double-SOI wafer before and after process

- Lapis FD-SOI pixel process
  - 0.2um CMOS, 1 Poly, 5 Metal layers
  - 8-inch wafer, 720 um thick
  - High resistive substrate: Cz (n)  $\sim$ 700  $\Omega\text{-cm}$ , FZ(n)  $>$  2k  $\Omega\text{-cm}$ , FZ(p)  $\sim$ 25k  $\Omega\text{-cm}$  etc.
  - Backside process: Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating

# Radiation hardness (transistor level)

Reference: Ikuo Kurachi, et al., <http://indico.ihep.ac.cn/event/6189/>

- Radiation damage mechanisms
  - SEU / TID / Non-ionized damage
- Measures to enhance TID tolerance
  - Optimization of transistors doping recipe (LDD)
  - Double SOI compensation
- Up to 100 kGy achieved by combining above two measures.
  - Drain current change less than 10%.

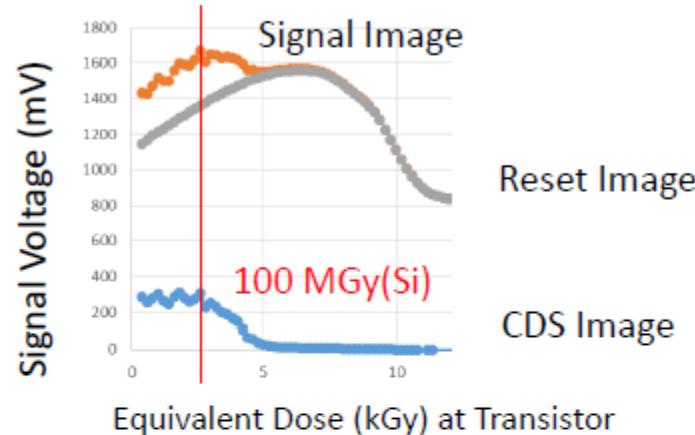
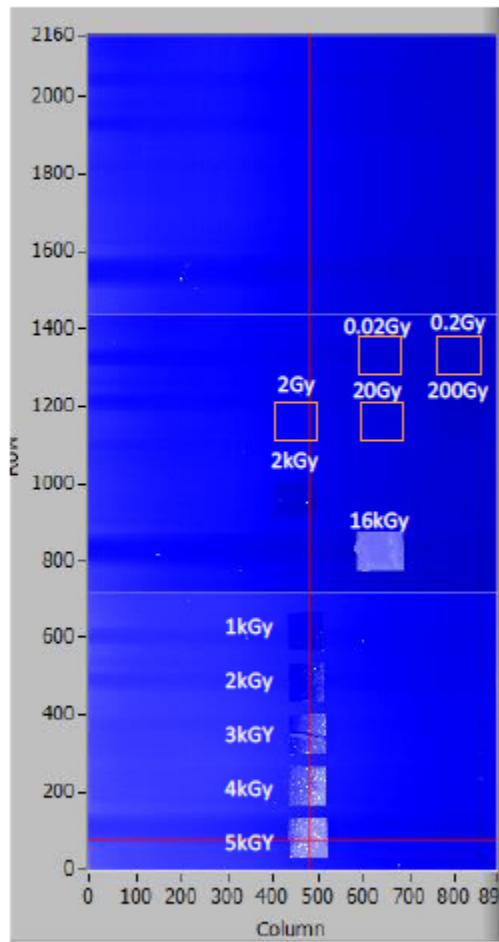




# X-ray Radiation Hardness: Sensor Level



BL29XU Beamline @ SPring-8



**Target Performance:** 1 Grad(Si) @ 7 keV input dose

**Results:** Operational up to 10 Grad(Si)

(equivalent to 250 krad(Si) @Transistor layer)

At 1 Grad(Si) (end of life), dynamic range is reduced by 2.5 % (20 mV)

Consistent with results obtained by a wafer-level high-throughput evaluation on the transistors<sup>1-3</sup>.

- 1) T. Kudo et.al., IEEE TNS (2014) Vol. 61(3), p. 1444.
- 2) I. Kurachi, et.al., IEEE Trans. Electr. Dev. (2015), Vol. 62(8), p. 2371
- 3) I. Kurachi, et.al., IEEE Trans. Electr. Dev. (2016), Vol. 63(6), p. 2293.