Design and Charaterization of a Low-Noise 64-channel Front-End ASIC with Leakage Compensation for CZT Detectors

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Outline

Part 1: Introduction to Lab

Location, Group, Lab at a glance

Part 2: Design Techniques of Low-Noise Readout ASIC for CZT detectors

Design requirements, proposed schematic, Charge sensitive amplifier, Shaper, Noise Optimization;

Part 3: Experimental Results and Discussion

D&R history, SENSROC tested results, performance evaluation;

Part 4: Conclusion

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Introduction to my Lab

- Location
  - Institute of microelectronics, located in the southeast of Xi'an City, China.

- Staff (6)
  - Professors (3) + Asst. Professor(3)
- Students (40+)
  - PhD student (7) + 20 Master student (20) + undergraduate student/year (20)

Lab at a glance


EDA Design Room (400 m^2)


Testing Room (90 m^2)


Microcircuit Fabrication (90 m^2)


Clean Room (90 m^2)

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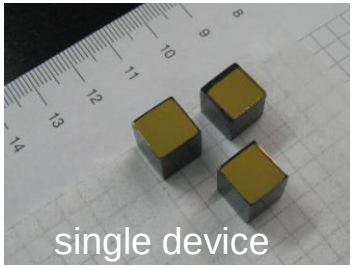
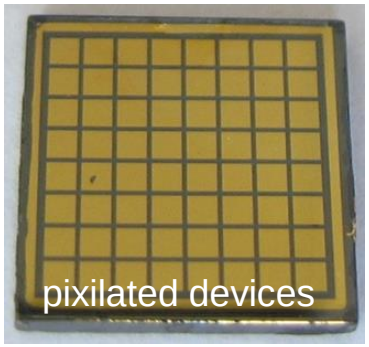
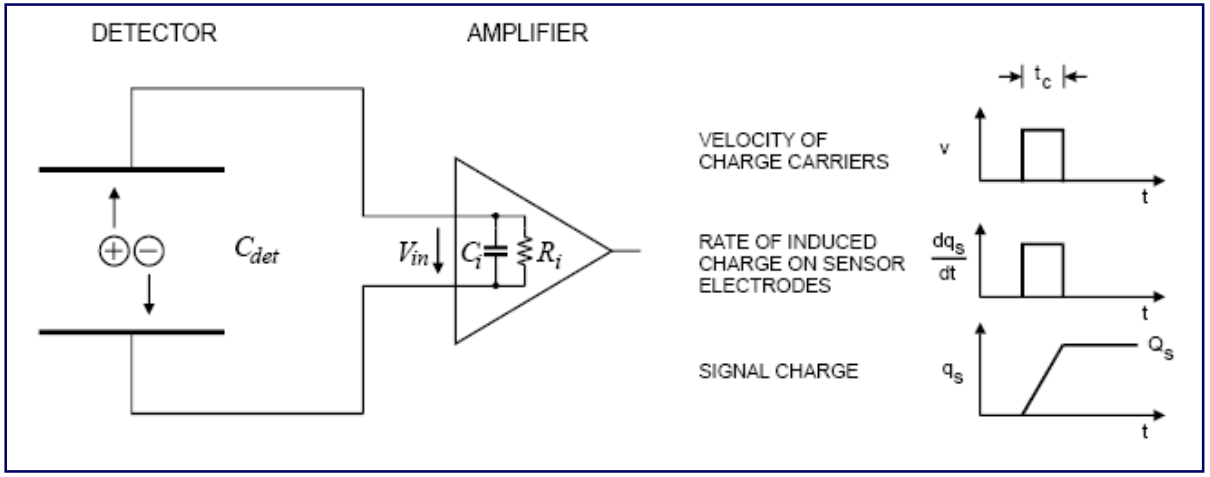
Front-End ASIC Design Requirements

CdZnTe Detector(碲锌镉探测器)

- Bias voltage → several hundred Volts（~500V）
- Leakage current →5 nA @ 100V for single device; ~100 pA @100 V for pixilated devices.
- Detector capacitance→ 5pF for single devices; ~1 pF /pixel for pixel devices.
- The average signal charge → $Q_s = \frac{E}{E_i} e$,where E_i= 4.65 eV



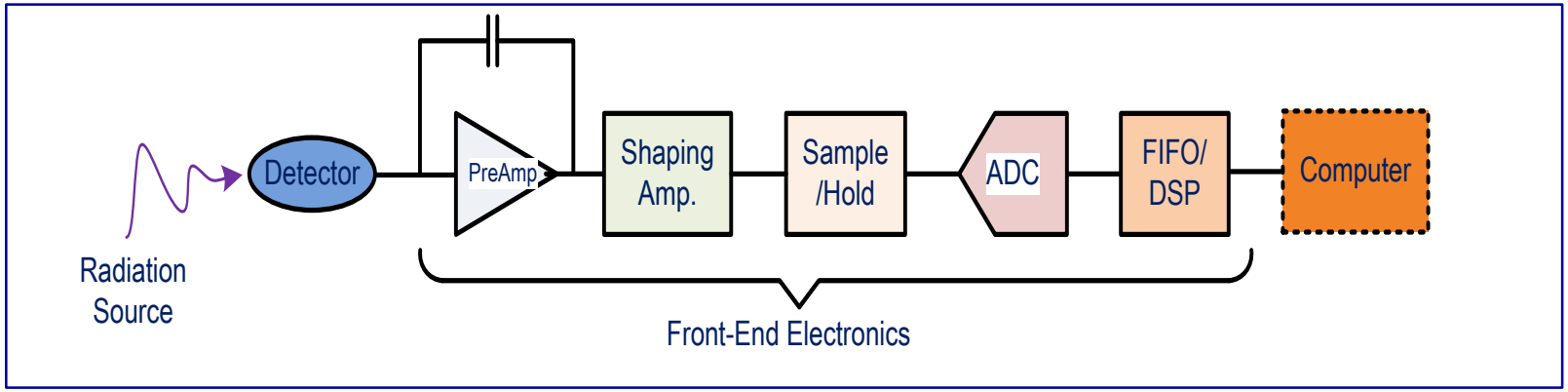


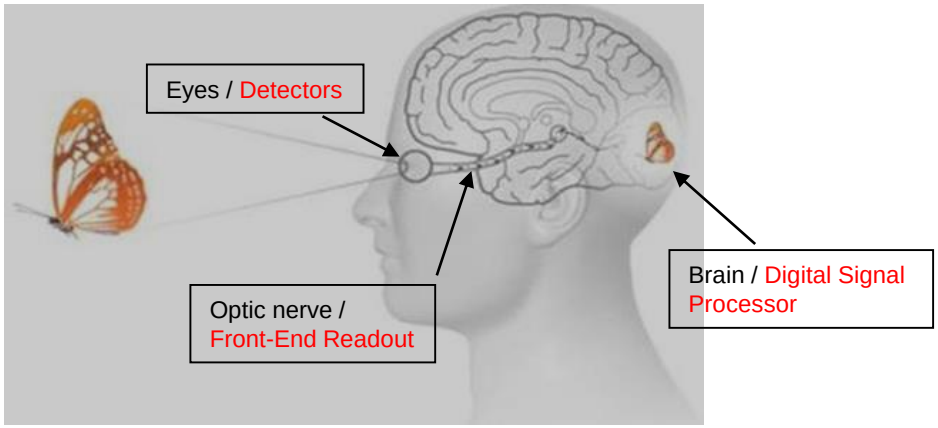


(School of Material, Northwestern Polytechnical University)

Front-End ASIC Design Requirements

Most analog front-ends follow a similar architecture





Functions

- Energy Measurement from signal amplitudes → particle tracking and imaging
- Time Measurement from triggers → Location targeting, coincidence

Front-End ASIC Design Requirements

Parameter	PMT	APD	SiPM	CZT,CdTe
Size	Bulky	Compat, thin	Compat, thin	Compat, thin
Gain	10^6~10^7	10^2~10^3	10^5~10^6	10^2~10^3
Noise	Low	moderate	Low	Low
Threshold Sensitivity	1 ph.e	10 ph.e	1 ph.e	--
Time resolution	~0.5 ns	~ 1ns	~0.5 ns	~ 7 ns
Energy resolution	~10 %	~13 %	~10 %	~4 %(0.2 ~ 20 keV)
Bias voltage	800 ~1500 V	100~2000V	25 ~50 V	800~ 1500 V
Cost	$	$$	$$$($)	$$$
MR Compatible	No	Yes	Yes	Yes

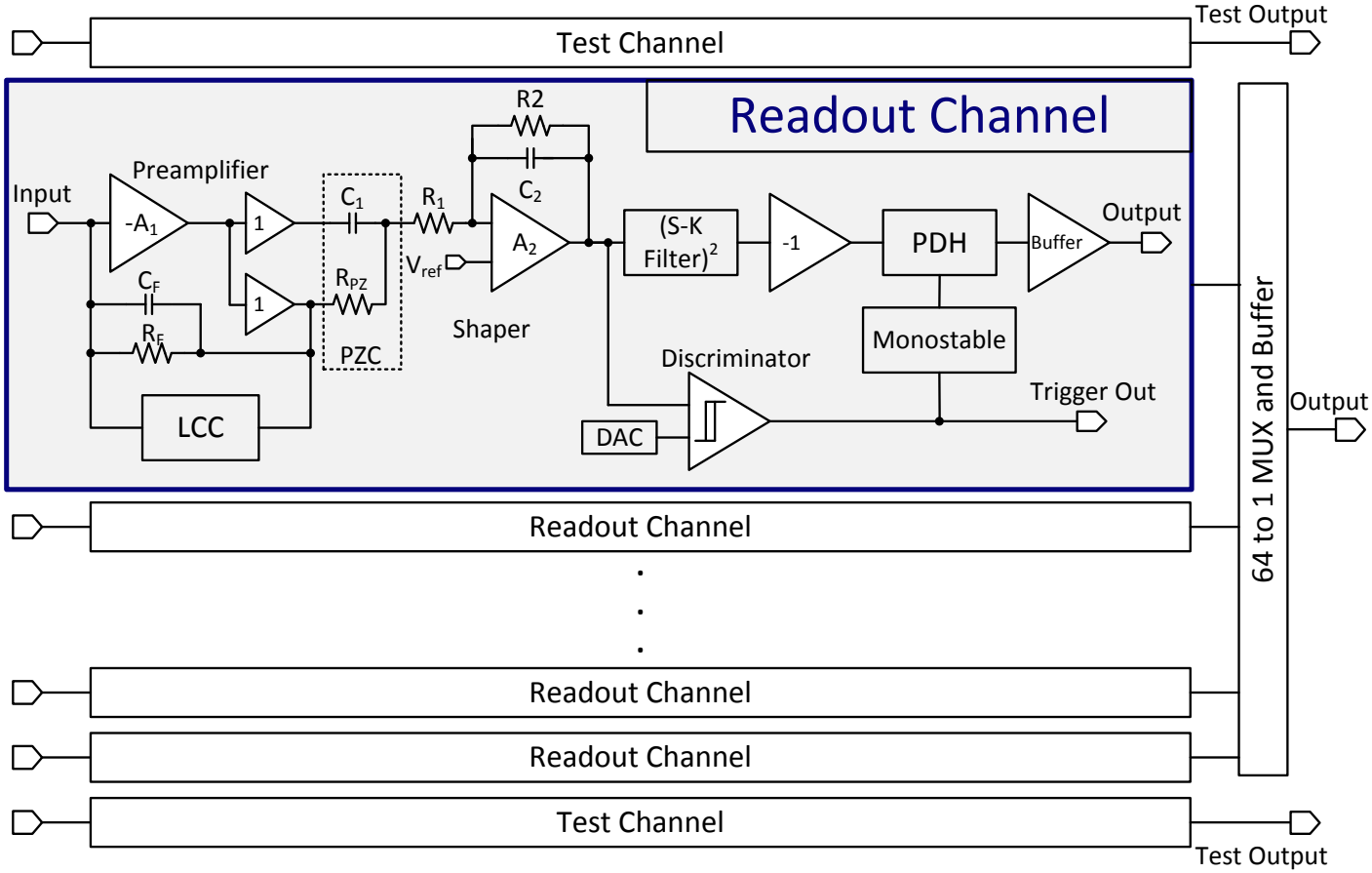
Overview of Detector Analog Front-Ends

State-of-the-art front-end ASICs for CZT detectors

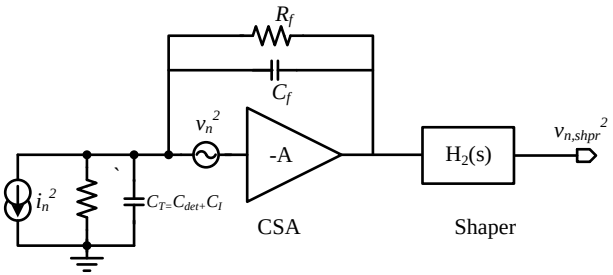
No.	Year	Designer	Country	Chip name/Classification	Process	Performance
1	2009	CEA Saclay DSM/ IRFU/ Service,	France	IDeF-X ECLAIRs	CMOS 0.35um	32 channel, gain =96mV/fC, ENC = 33e- + 7e-/pF
2	2004	NOVA R&D, Inc, University of California,	USA	RENA-1,2,3	CMOS 0.5um	ENC > 150e-
3	2005	Gamma Medica-Ideas ,	Norway	VA32TA6, VA64TA2	CMOS 0.35 μm N-well	ENC = 39.5e- + 10 e-/pF
4	2007	Brookhaven National Lab.,	USA	Readout ASIC	CMOS 0.25um	gain = 1V/fC, shaping time = 40ns ~320ns, ENC = 390 e- @1.8pF
5	2008	NASA,	USA	Low-noise readout array	IBM CMOS 0.18um	N/A
6	2009	Japan Aerospace Exploration Agency	Japan	Low-noise, 2D amplifier array	TSMC CMOS 0.35um	ENC = 88e- + 25e-/pF, Power = 150mW/pixel
7	2009	CEA Saclay,	France	IDeF-X ASIC family	AMS CMOS 0.35um	ENC = 33e- + 7e-/pF, shaping time = 6 us
8	2011	Japan Aerospace Exploration Agency	Japan	Low-Noise Front-End ASIC	TSMC CMOS 0.35um	ENC = 50±10 e- /pF
9	2014	IME, Northwestern Polytechnical Univ.	China	SENSROC/ Low-Noise ASIC	TSMC CMOS 0.35um	ENC = 66±14 e- /pF, 3mW/ch.

Proposed topology for CZT detectors

Multichannel Readout Scheme (RENA3, VA64TA2)



(NIM A，2016)



Proposed Low-Noise Design

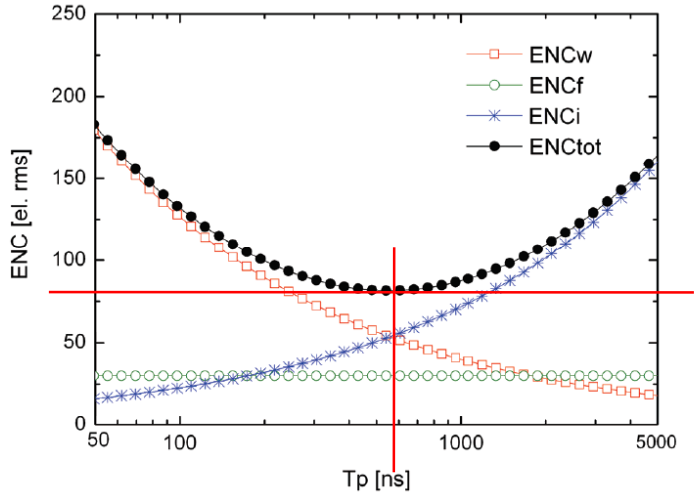
The ENC can be calculated as

$$ENC = e\sqrt{\frac{t_p}{8}\left(2qI_{\det} + \frac{4kT}{R_{bias}} + \frac{4kT}{R_f}\right) + (C_F + C_T)^2\left(\frac{4kT\gamma_n}{8t_p g_{m1}} + \frac{K_f}{2C_{ox}^2}\frac{1}{WL}\right)}$$

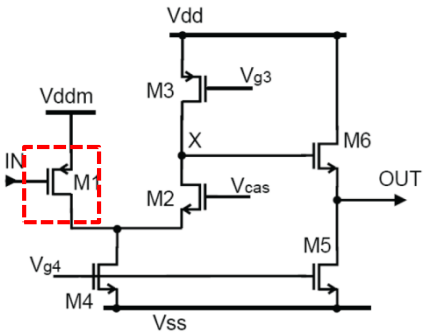
The ENC can be divided into three parts according to the current noise source, the voltage noise source and the 1/f noise source.

$$ENC^2 = ENC_i^2 + ENC_v^2 + ENC_f^2$$

$$\begin{cases} ENC_i^2 = 0.462t_p\left[qI_{\det} + 2kT\left(\frac{1}{R_{bias}} + \frac{1}{R_f}\right)\right] \\ ENC_v^2 = 3.696\frac{(C_F + C_T)^2}{t_p}\frac{kT\gamma_n}{g_{m1}} \\ ENC_f^2 = 3.696(C_F + C_T)^2\frac{K_f}{C_{ox}^2}\frac{1}{WL} \end{cases}$$



(P. Grybos, 2010)



Proposed Low-Noise Design

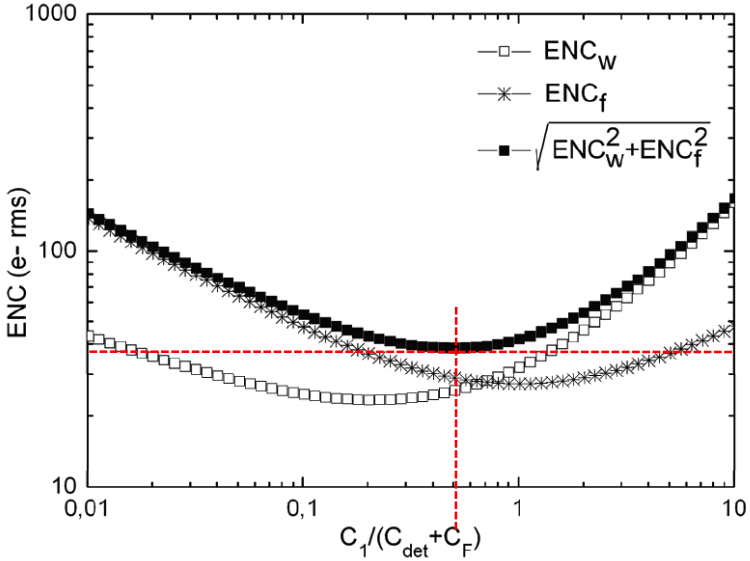
The minimum ENC_v is obtained if

$$C_I = \frac{C_{\det} + C_F}{3} \qquad W_{1,opt} = \frac{C_{\det} + C_F}{2C_{ox}L_{\min} + 6C_{ov}}$$

The minimum of ENC_f is obtained if

$$C_I = C_{\det} + C_F$$

- ✓ The optimum C_I is closer to $(C_{det} + C_F)/3$ for short peaking time.
- ✓ When the peaking time is longer, $(C_{det} + C_F)$ is more appropriate.

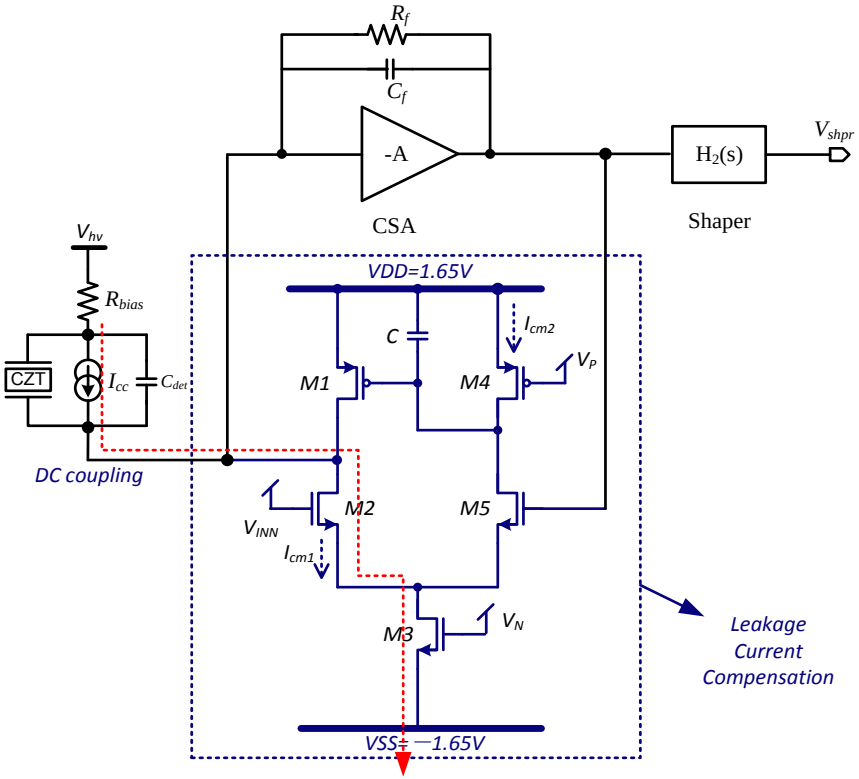


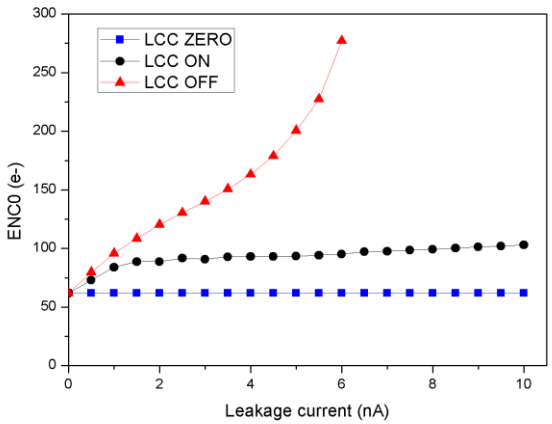
(P. Grybos, 2010)

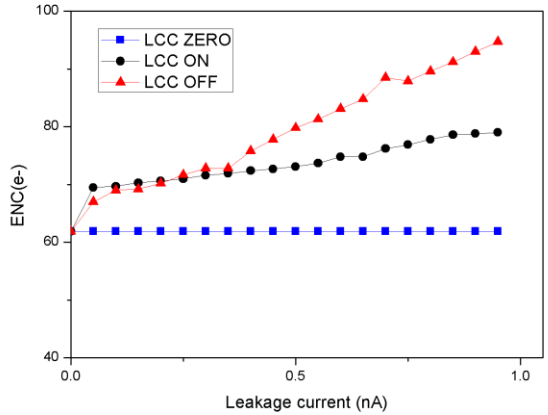
Proposed Leakage Compensation

Leakage compensation range 0-10nA

- ENC < 100 e- pF for CZT
  (Cell 5 nA, pixilated 100 pA)





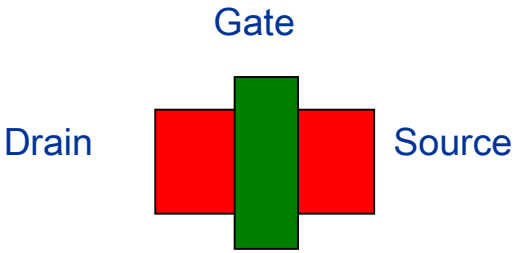


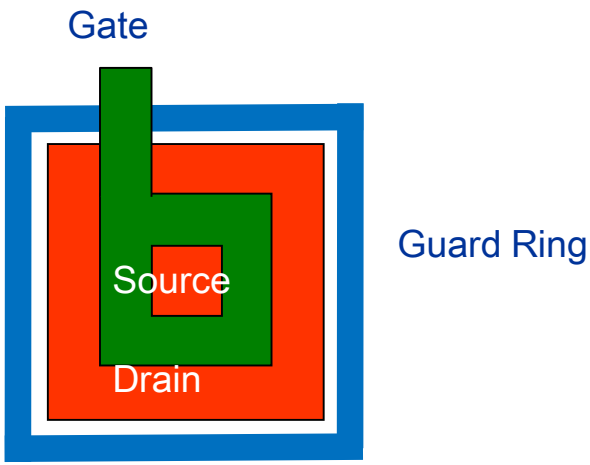
Proposed Radiation-Hardened-by-Design

RadHard Analog Circuit Design

- Enclosed gate layout
- Guard ring
- Capacitive hardened
- Increase channel length
- Increase driving capability

$$\frac{W}{L} = \frac{8\alpha}{\ln \frac{d'}{d' - 2\alpha L}} + \frac{4K(1-\alpha)}{\sqrt{\alpha^2 + 2\alpha + 5\ln\frac{1}{\alpha}}} + \frac{3(d-d')}{2L}$$

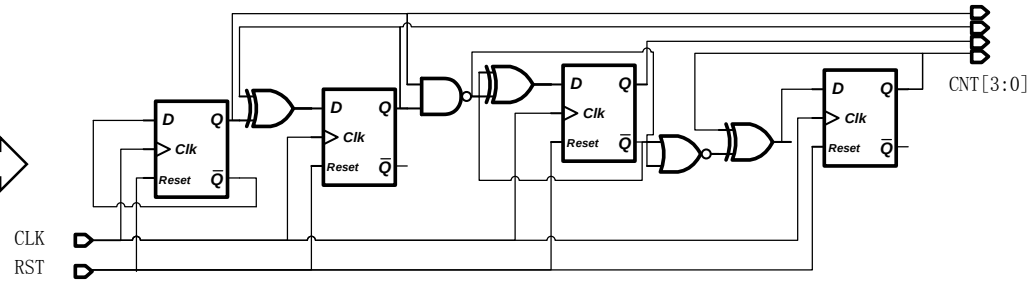


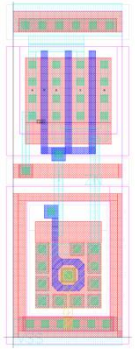


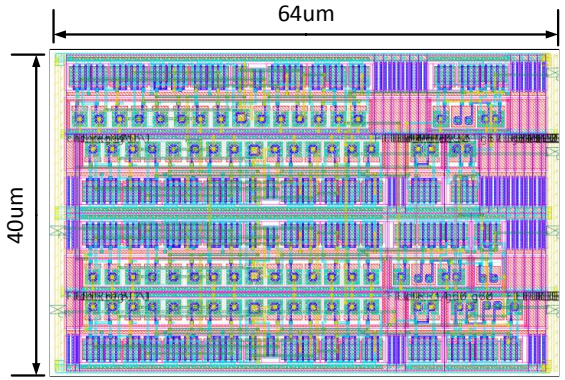
Proposed Radiation-Hardened-by-Design

RadHard Digital IC Design
Example: 4-bit Counter

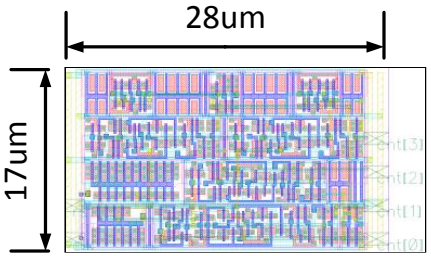
```
module counter(clk,rst,cnt);

input clk,rst;
output [3:0] cnt;

always @ (posedge clk or negedge rst)
begin
        if (!rst)
                cnt <= 4'b0;
        else
                cnt <= cnt + 4'b1;
end
```







RadHard



Non-RadHard

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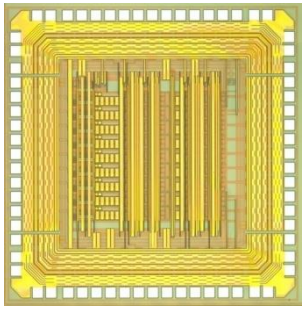
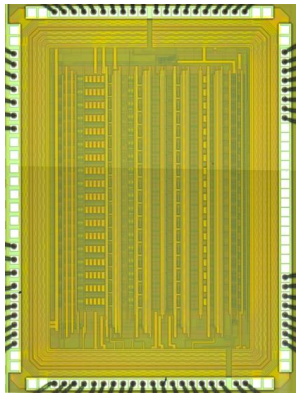
Rearch & Development History

RadHard Mixed Signal IC Design Flow

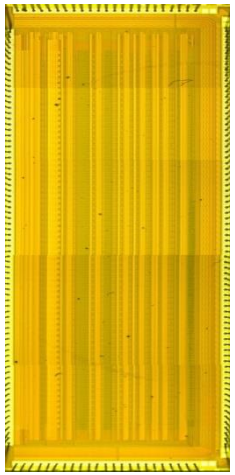
- ✓ Four CMOS Technologes：TSMC 0.18um/0.35um、SMIC 0.18um/CSMC 0.35um
- ✓ 8 prototypes、2 engineering samples, 20^{+}versions of readout IP
- ✓ SENSROC series ASICs



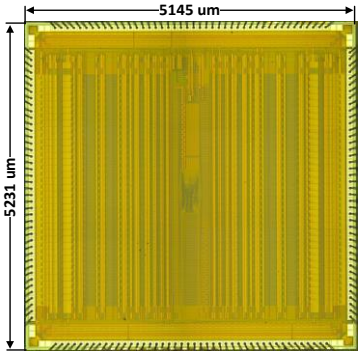
SENSROC2：CSA-shaper ASIC（2012）



SENSROC5：16-channel ASIC（2014）



SENSROC8：64-channel ASIC （2015）



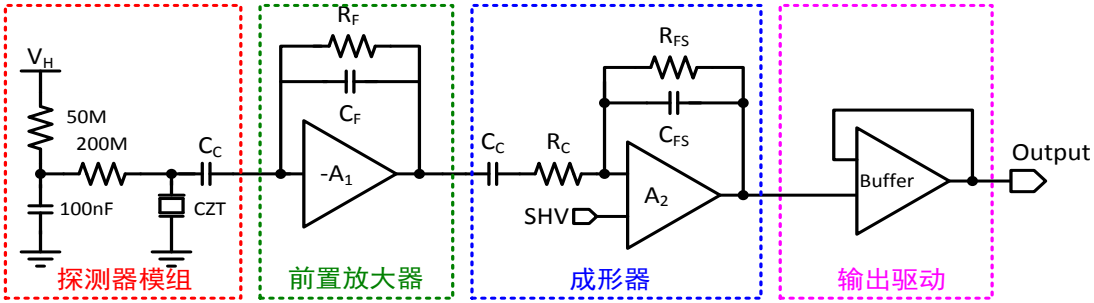
SENSROC10：64-channel ASIC （2016）

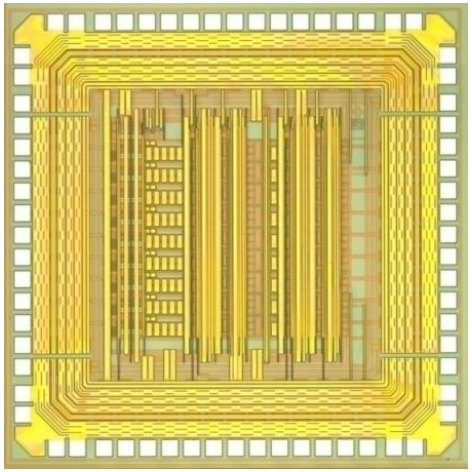
功能增强，集成度增加，性能优化

Rearch & Development History

SENSROC2：CSA-Shaper ASIC (2012)

Phase I:
1) Verify the process;
2) Verify the topology
3) Verify the design and test flow





Microphoto of SENSROC2

Parameter	SENSROC2
Process(μm)	CMOS 0.35um 3.3V
Die size	2.0 mm × 2.0mm
Power Supply (V)	±1.65 V
Input range(e-)	2k~60k
ENC (rms)	58.5 e-+8.4e-/pF (after 200krad(Si) TID)
Radiation Hardness	TID: 200k rad (Si)
Application	CZT/Si-PIN Detector

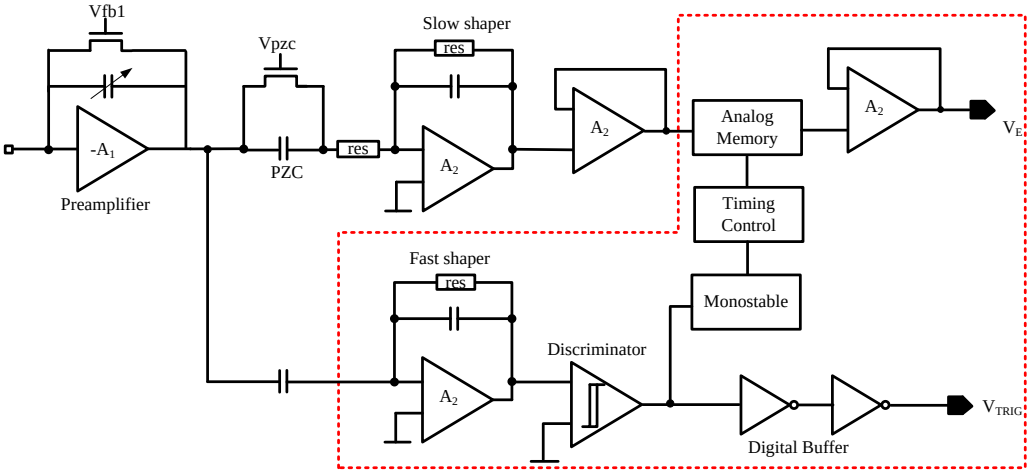
Rearch & Development History

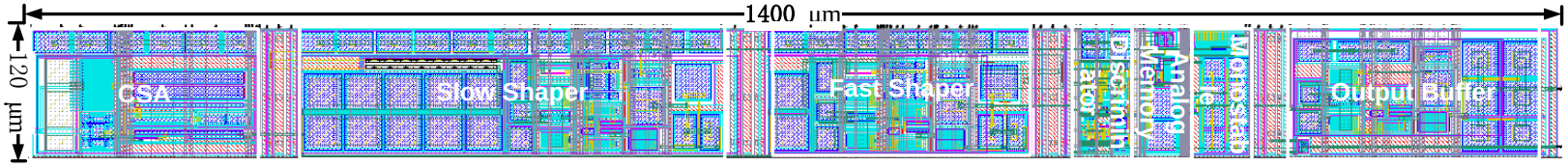
SENSROC5: 16-channel Front-End ASIC(2013)

» Topology：Preamp.+ Shaper（slow, fast）+ Analog Memory + Discriminator（be compatible with VA64TA2，RENA3）

Phase II:

1) Verify peak-detect-and-hold circuit;
2) Verify multichannel integration;
3) Verify timing controlling

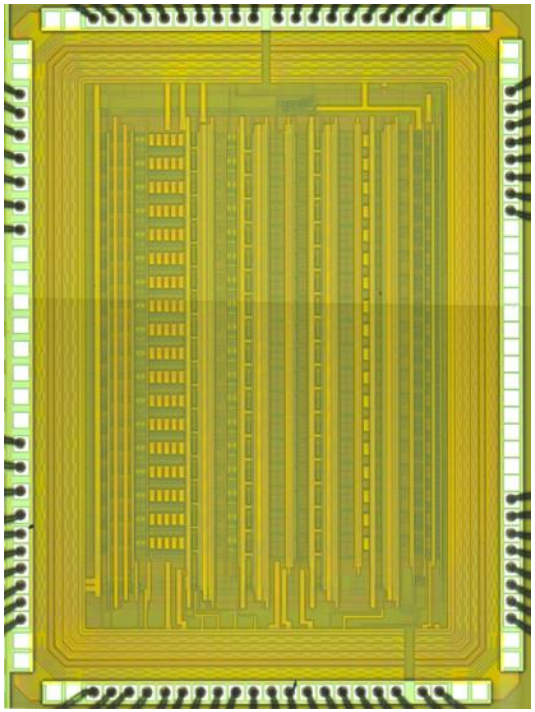




(W. Gao et al, IEEE TNS, 2014)

Rearch & Development History

Tested results of SENSROC5



Microphoto of SENSROC5

Performance overview of SENSROC5

Parameters	SENSROC5
Process(μm)	CMOS 0.35
Power Supply (V)	0/3.3V
Topology	CSA(PMOS) + CR-RC Shaper + PDH+TRIG
Channel No.	16
Input range(e-)	2k~247k
ENC (rms)	50 e-+14e-/pF (tested)
Radiation Hardness	N/A
Applications	X-ray and γ-ray imaging

(W. Gao et al, MEJ, 2015)

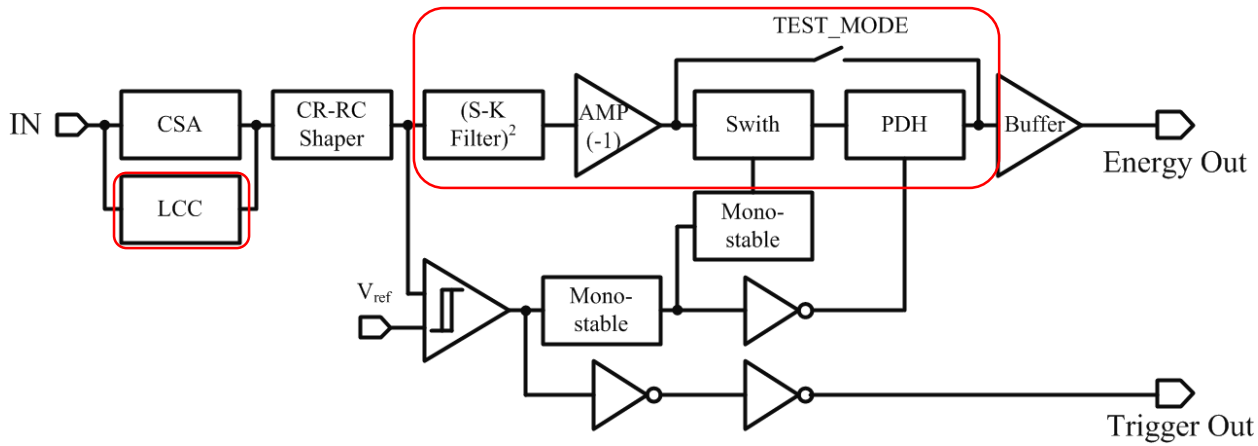
Performance Improvement

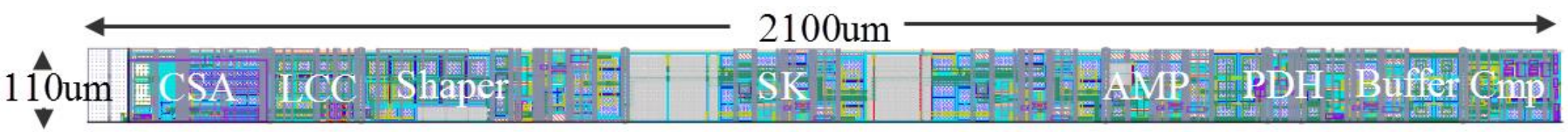
SENSROC8: 64-channel Front-End ASIC(2013)

- Topology：Preamp.+ Shaper（slow, fast）+ Analog Memory + Discriminator（be compatible with VA64TA2，RENA3）

Phase III:

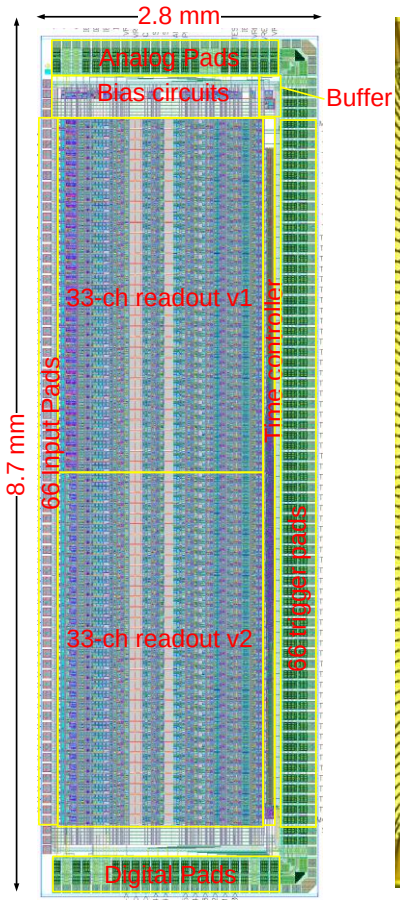
1) Verify DC coupling
2) Verify high-order pulse shaping;
3) Verify 64-channel integration
4) Verify testing schemes



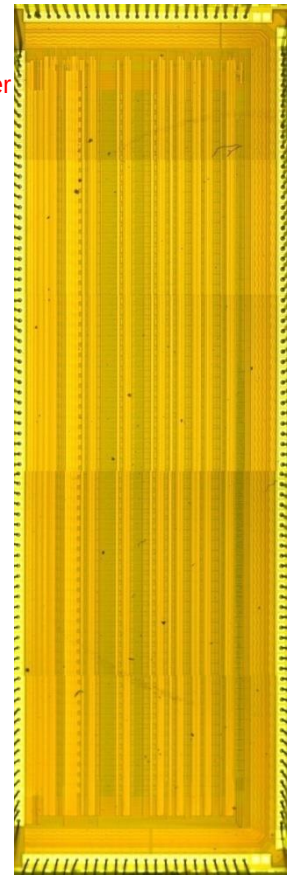


Performance improvement and increase blocks

Performance Overview of SENSROC8



layout



microphoto

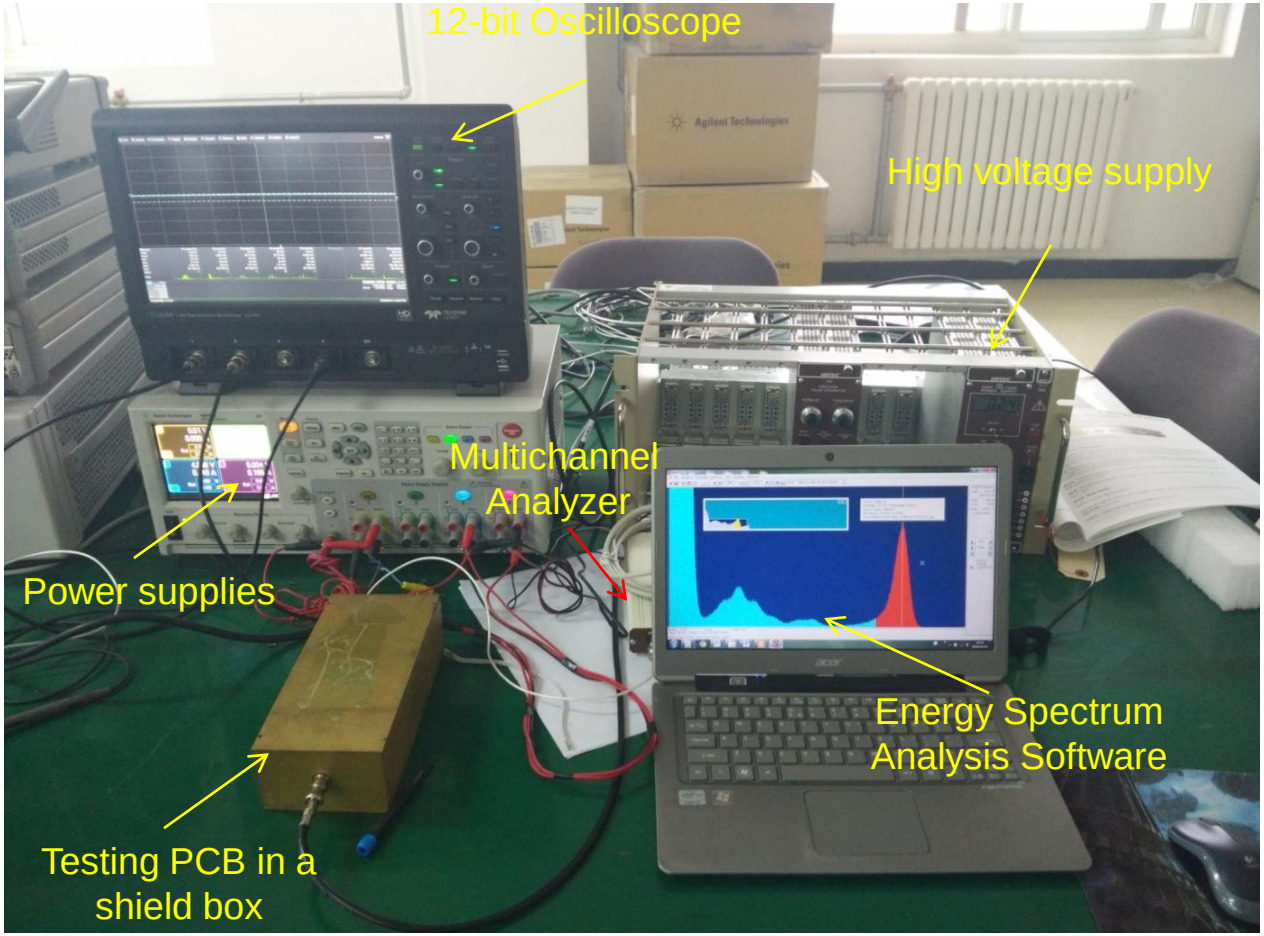
Performance overview of SENSROC8

Parameters	SENSROC8
Process(μm)	CMOS 0.35
Power Supply (V)	0/3.3V
Topology	CSA(PMOS) +CR-RC Shaper + $(SK)^2$ filter + PDH+TRIG+DRV
Channel No.	64
Input range(e-)	2k~247k
ENC (rms)	66 e-+14e-/pF (tested)
Radiation Hardness	To be tested
Applications	X-ray and γ-ray imaging

(B. Gan, W. Gao et al, IEEE NSS/MIC, 2015)

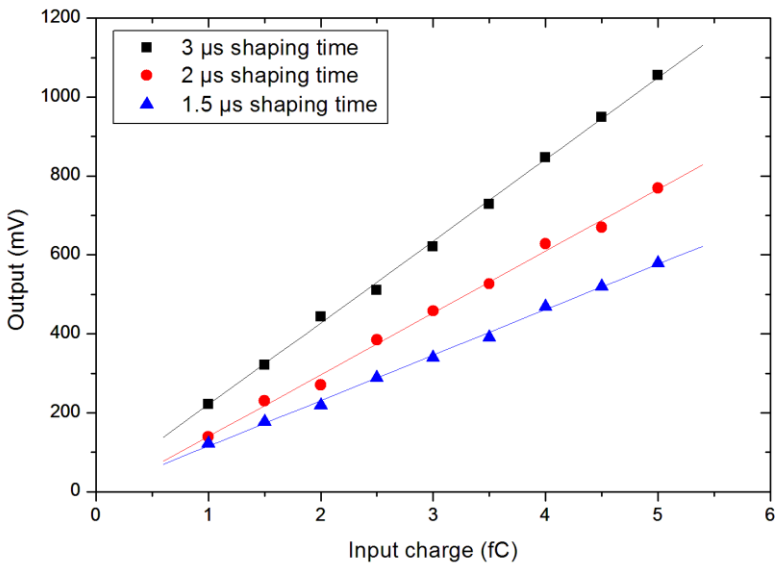
Experimental Results and Discussions

Testing Setup

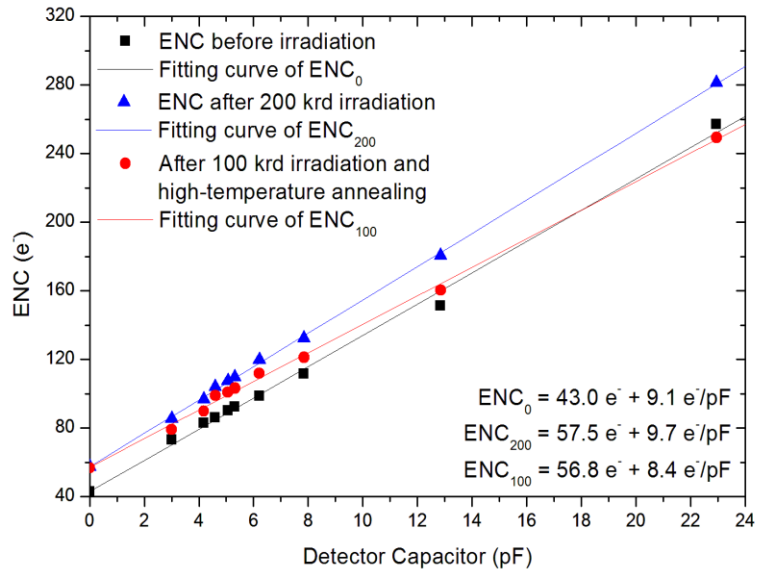


Experimental Results and Discussions

Output vs. Input charges



ENC vs. detector capacitance



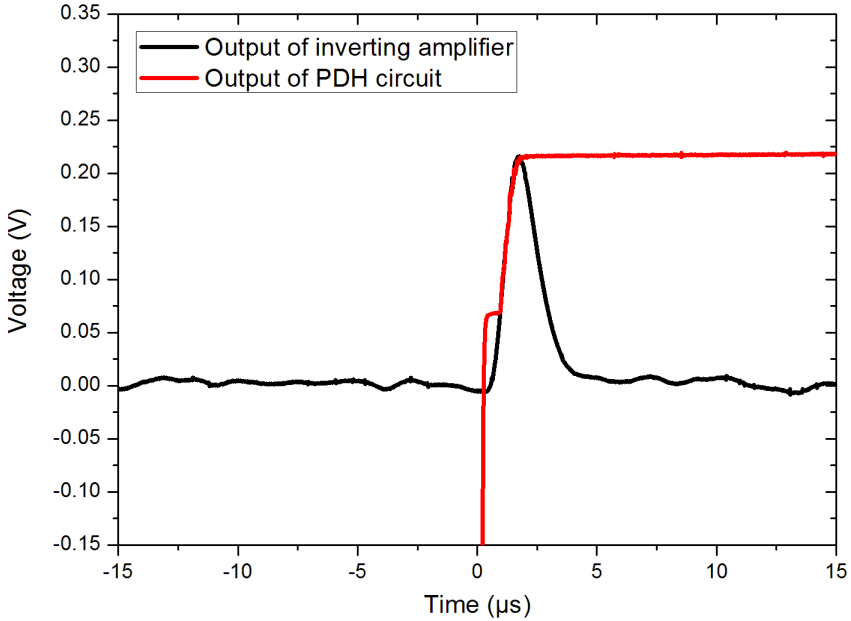
(西核所测试报告, 2012)

CSA+ CR-RC Shaper

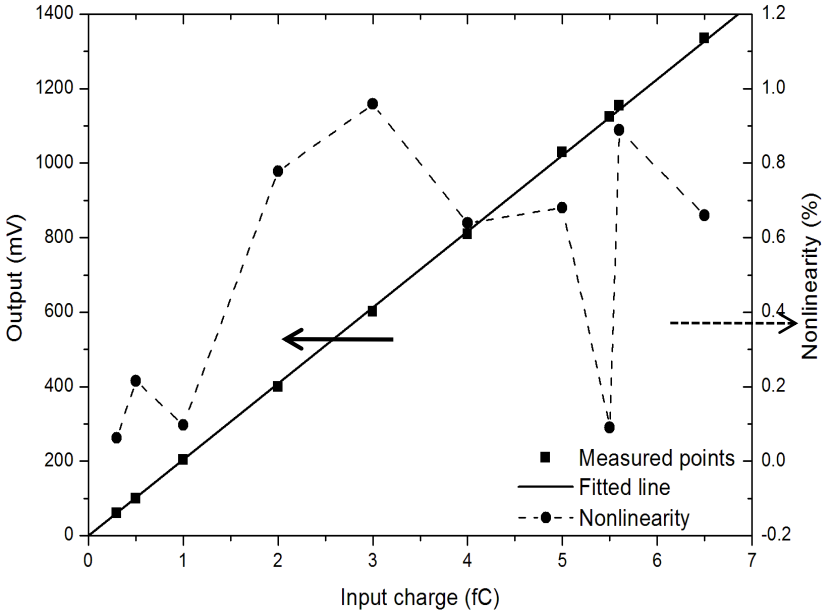
- Gain→115 mV/fC @ 1.5 μs, 154 mV/fC @ 2 μs, 210 mV/fC @ 3 μs
- ENC → 56.8 e- + 8.4 e-/pF, when TID > 200 krad(Si)

Performance improvement and increase blocks

Test results of PDH



Output Vs. input chages

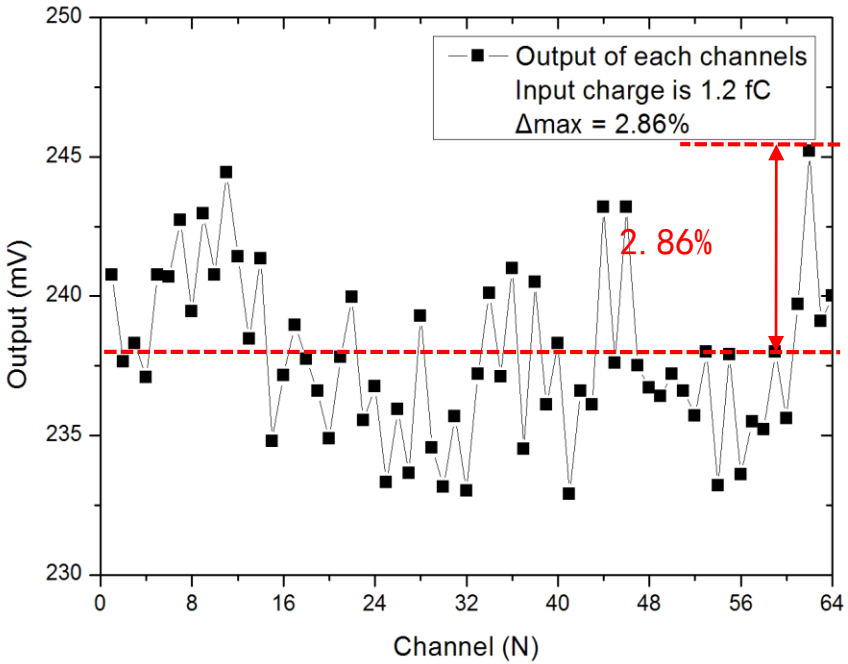


CSA+CR-RC Shaper+SK^2+PDH

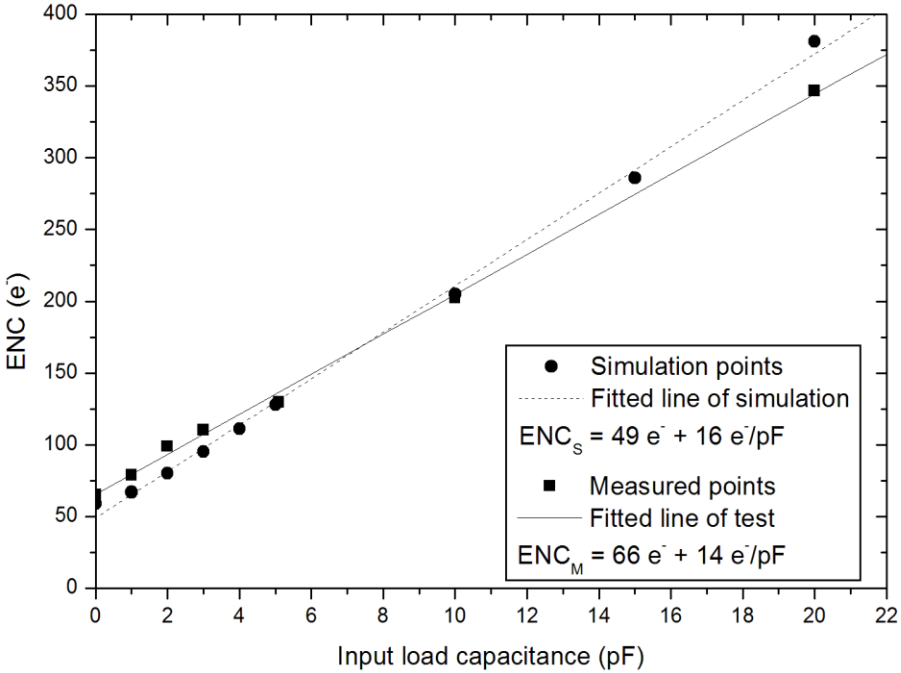
- Shaping time is from 1 μs~ 3 μs; Gain→65mV ~ 200 mV/fC;
- Nonlinearity → < 1%.

Performance improvement and increase blocks

Consistency between channels

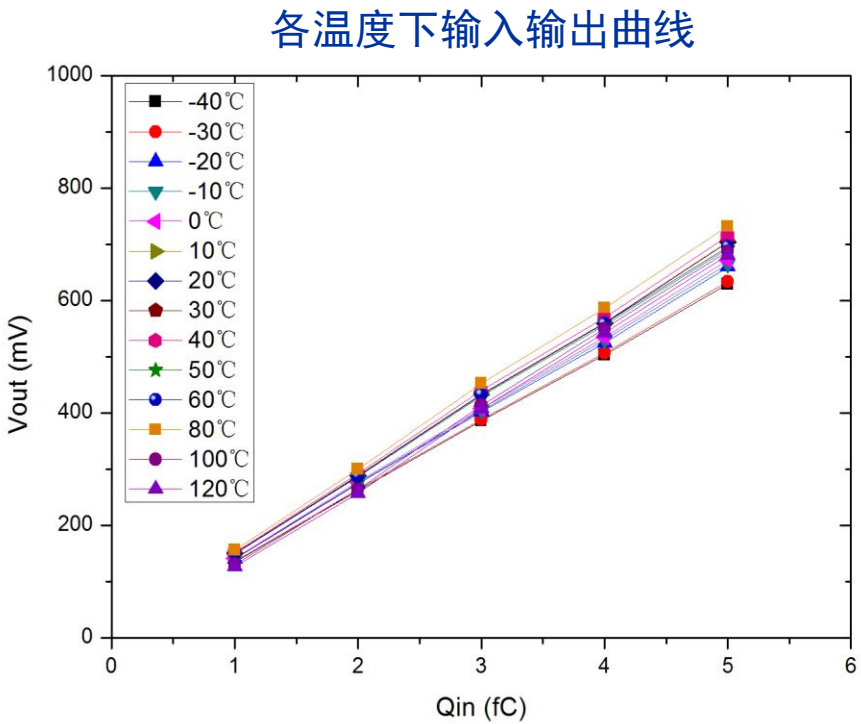


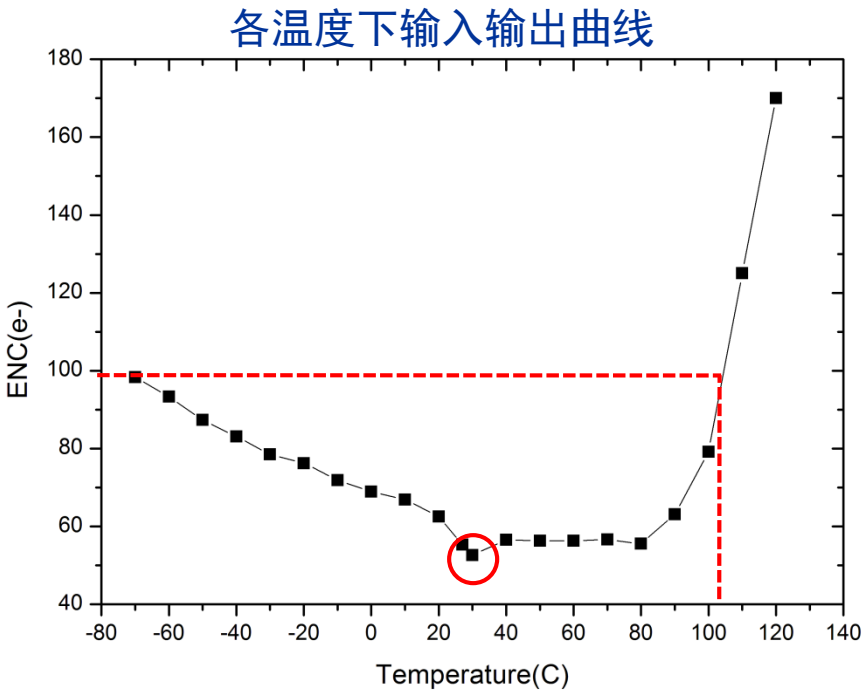
ENC simulation and tested results



- Consistency → less than 2.86%;
- ENC→ 66e- + 14 e-/pF;

Performance improvement and increase blocks

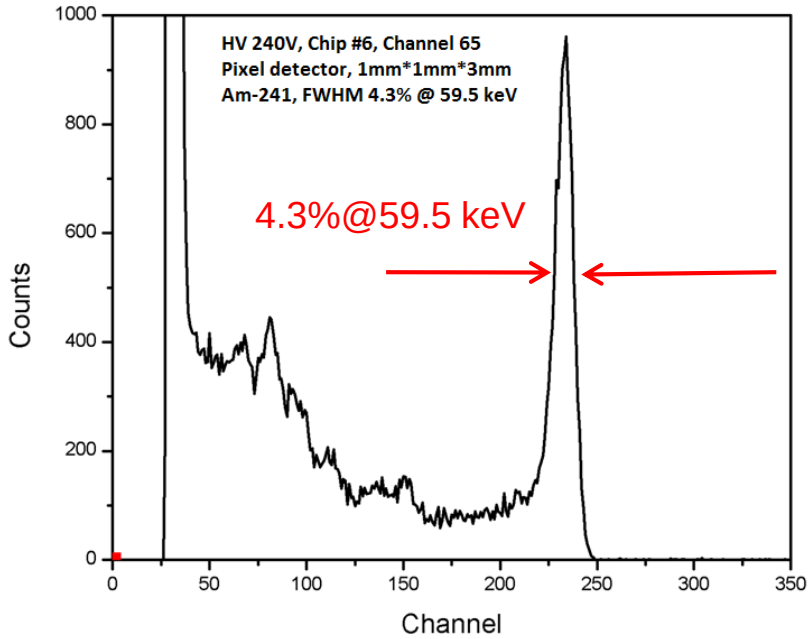


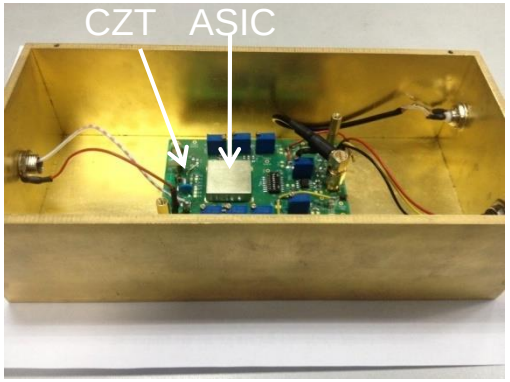


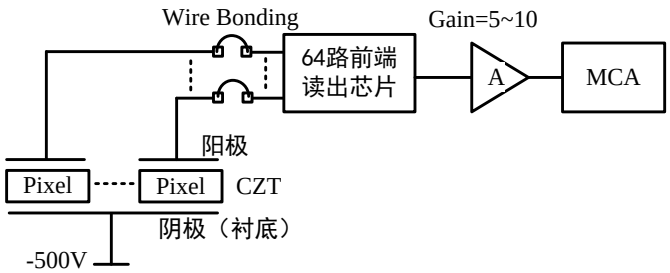
- From -40℃ to 120℃，the deviation of output voltage is between ±10%;
- From 0℃ to 102℃， ENC < 100 e- @ 5 pF;

Performance improvement and increase blocks

Energy spectrum resolution of SENSROC8







1） IMDETEK CZT Detector（8×8 pixels 240V），DC Coupling;
2）irradiation by AM-241, Energy spectrum resolution (FWHM) is 4.3%@59.5 keV。

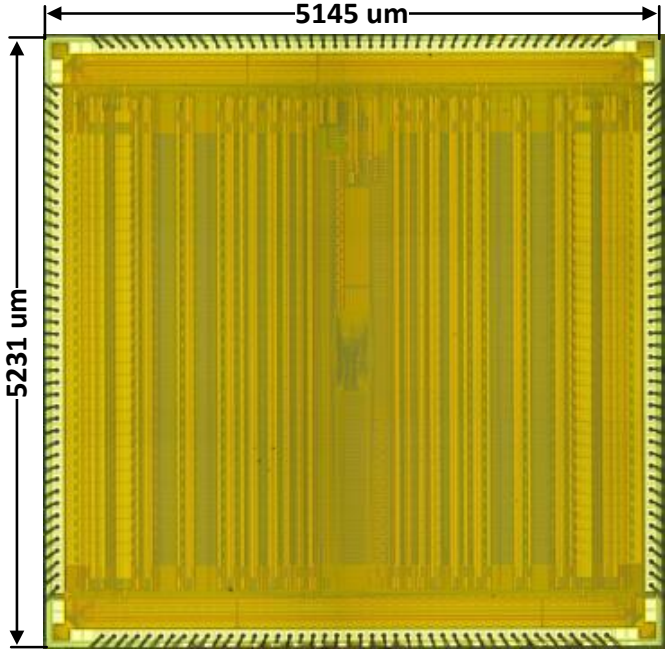
Performance Evaluation

Comparison of SENSROC8 versus State-of-the-art Front-End ASICs

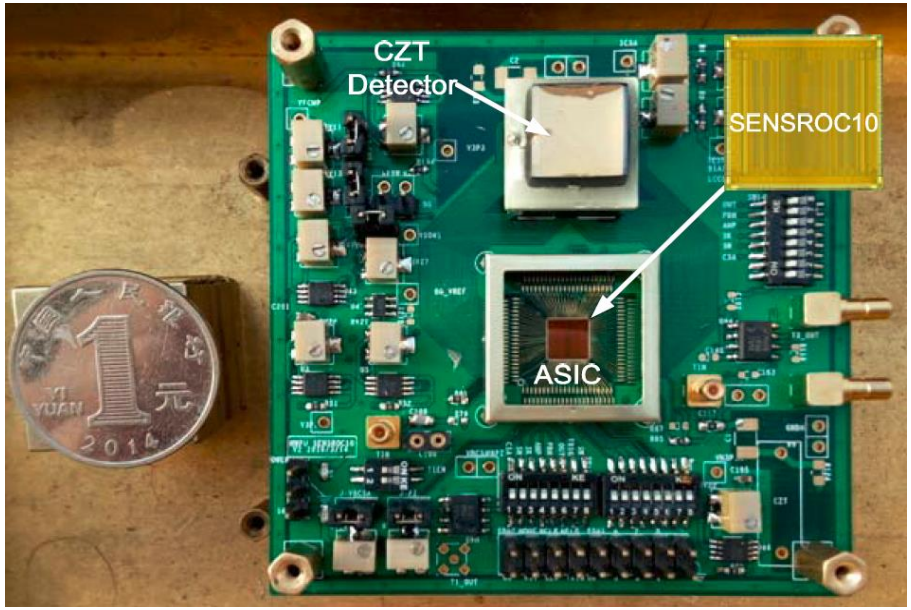
Parameters	IDeF-X (France)	RENA 2,3 (USA)	VA64TA2 (Norway)	SENSROC (China)
Process	CMOS 0.35μm	CMOS 0.35μm	CMOS 0.35μm	CMOS 0.35μm
Channel numbers	32	36	64	64
Die size (mm^2)	2.8×6.4	6.90×6.38	7.15×6.02	8.7 ×2.8
Power Diss.	3mW / Ch.	6 mW / Ch.	N/A	9 mW/Ch.
Dynamic Range	0~8 fC	9 fC ~54 fC	+/-15 fC	0.32 fC ~28.8 fC (11.2keV ~ 1MeV)
Non-linearity	<3%	< 10 %	<7.5 %	< 1%
Gain	200 mV/fC	N/A	32 μA/fC	65 mV/fC
ENC	33e+7 e/pF	<150 e @ 2pF	39e+10 e/pF	66 e + 14 e/pF
Crosstalk	<3%	N/A	<2 %	< 1%
Applications	X-ray spectroscopy in space applications	Si strip and CdZnTe detectors, X-ray imaging	X-ray and Gamma ray imaging	CdZnTe detector for X- and gamma ray imaging

64-channel ASIC for CZT-based Biomedical Imaging

Optimization of SENSROC8 → SENSROC9、10 (layout→ input pads at two sides)



Microphoto of SENSROC10

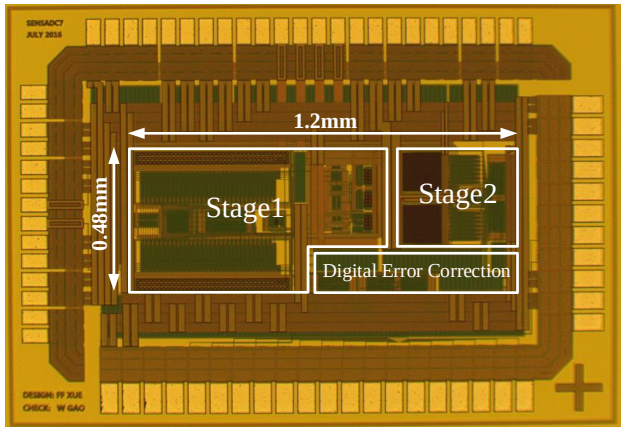


SENSROC9 Test Board

Applications on the way…

12bit ADC for High-Energy Physics and Biomedical Imaging

RadHard Pipeline-SAR ADC (2012-2016)



Parameter	Tested Results
Technology	CMOS 0.18 μm
Resolution	12 bit
Sampling Rate	10MS/s
Supply Voltage	Analog 1.8 V/Digital 1.8 V
ENOB	10.8bits
DNL	+1.06/ −0.57LSB
INL	+1.38/ −1.54 LSB
Power	10 mW
FoM	0.56 pJ/conv

Proposed Techniques

- ✓ A novellow-power MDAC;
- ✓ Improved capacitance array;
- ✓ Radiation-Hardened-by-Design Methodology;

(F.Xue, W. Gao et al, Jint, 2016)

Outline

Part 1: Introduction to Lab

Location, Group, Lab at a glance

Part 2: Design Techniques of Low-Noise Readout ASIC for CZT detectors

Design requirements, proposed schematic, Charge sensitive amplifier, Shaper, Noise Optimization;

Part 3: Experimental Results and Discussion

D&R history, SENSROC tested results, performance evaluation;

Part 4: Conclusion

Conclusion

Content in this presentation

1. Overview of analog front-ends for radiation detection.
   - ✓ Detector signal, topology, why ASIC, State-of-the-art front-end ASICs, applications ;
2. Design requirements and key techniques
   - ✓ CZT detectors, ASIC requirements, development history, low-noise design, RHBD
3. Experimental results and discussions
   - ✓ SENSROC2,5,8 topology, tested results, performance evaluation

Future work

1. Testing with a package (BGA, CQFP…) and applications;
2. Development of 128-channel (or more) front-end ASICs if needed.

Thanks for Your Attention.

(Questions?)