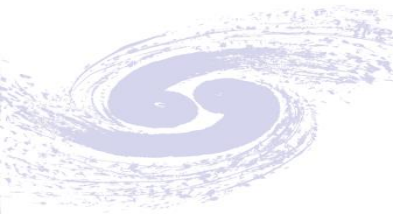




用于硅漂移探测器的高频采样电子学研究

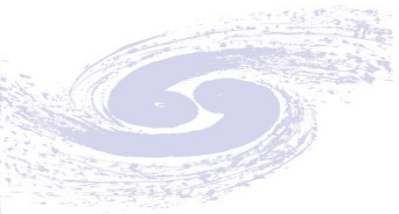
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主要内容

- 背景介绍
- 系统方案设计
- 研究进展
- 总结



背景介绍

- 同步辐射能谱测量是同步辐射实验重要的需求
- 提高电子学系统的采样频率可以提高计数率，从而获得更多的信息量

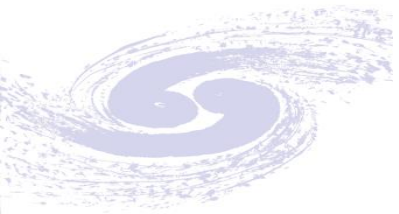


■ 硅漂移探测器

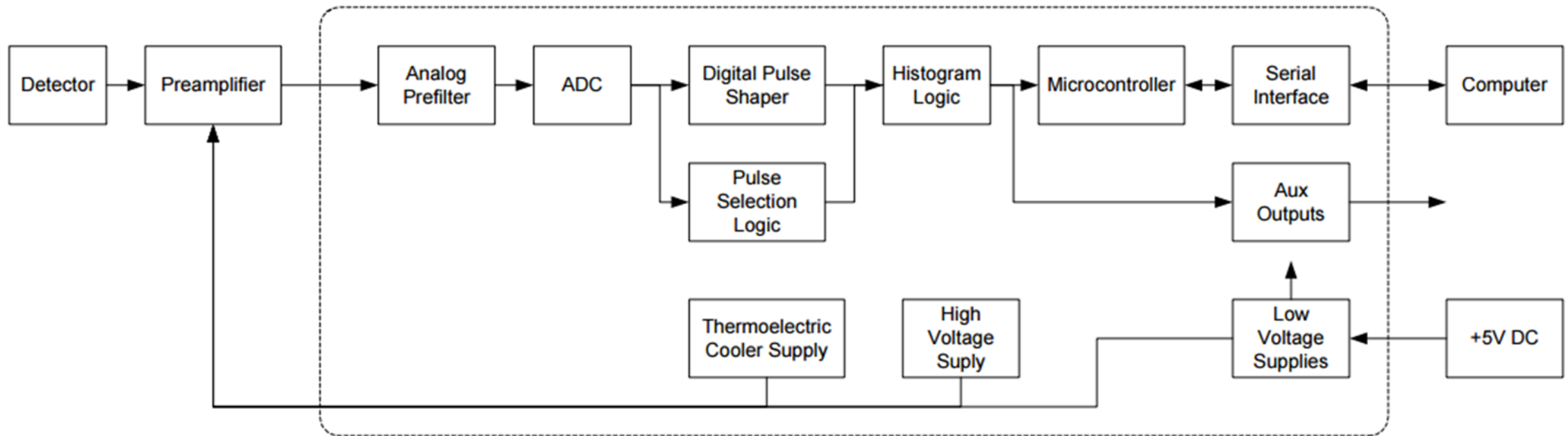


优点：

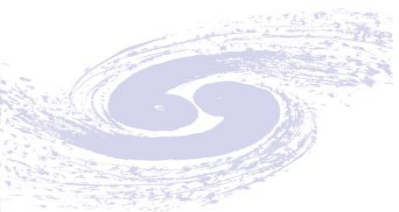
- 高能量分辨率
- 高量子效率
- 高计数率
- 高信噪比
- 高线性度
- 广泛应用于X 射线荧光光谱、空间X 射线探测等领域



系统方案设计

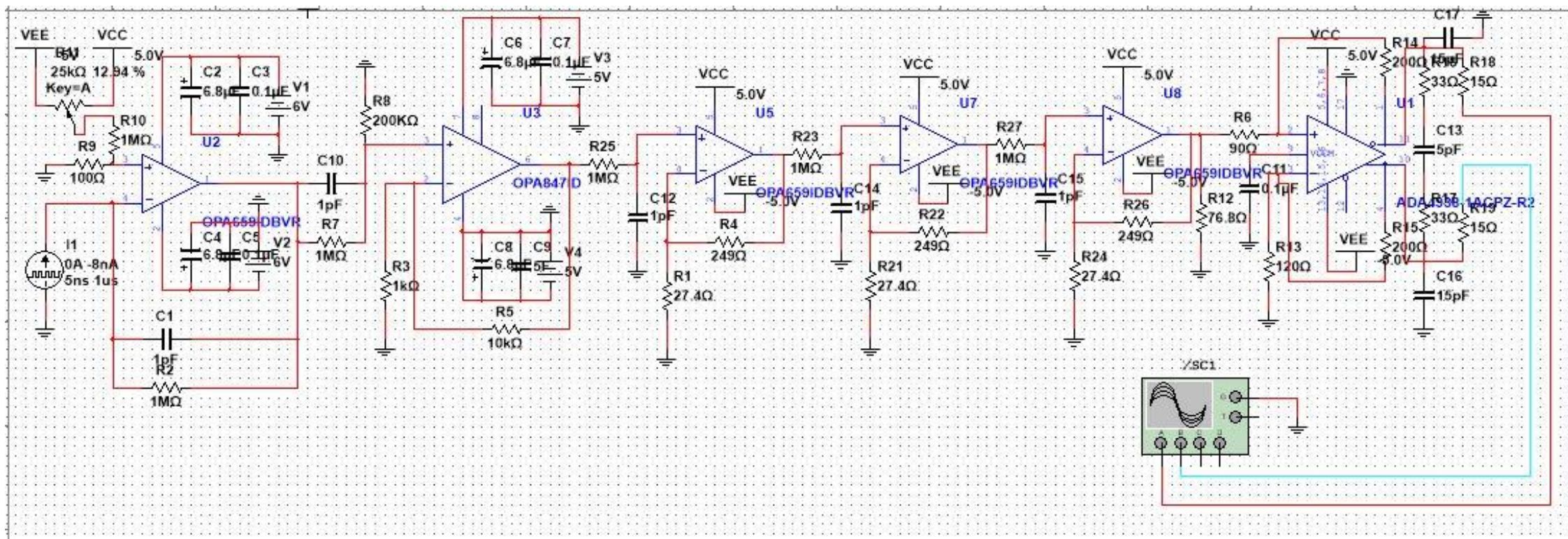


数字滤波

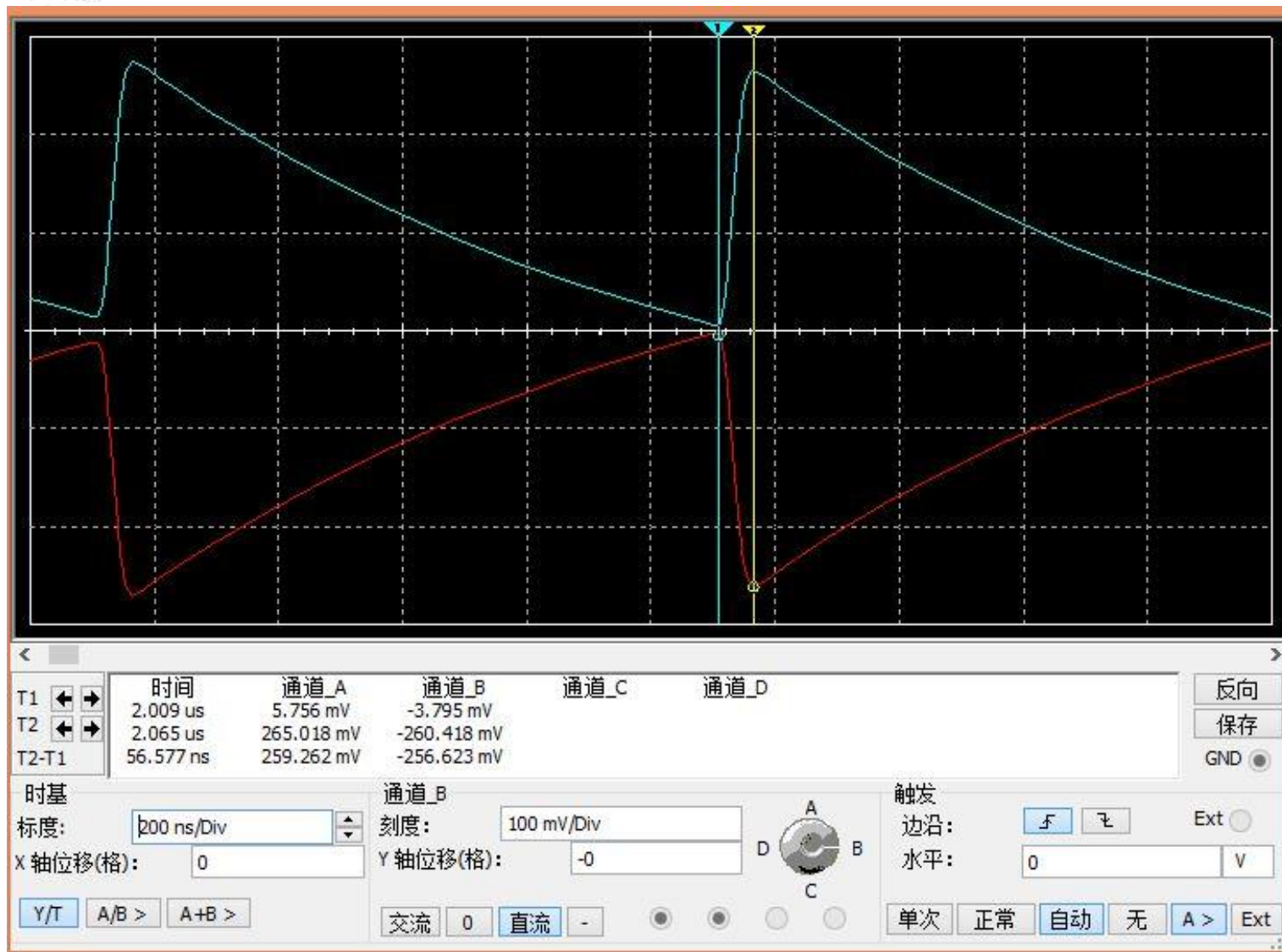


前端电子学部分

原理图仿真

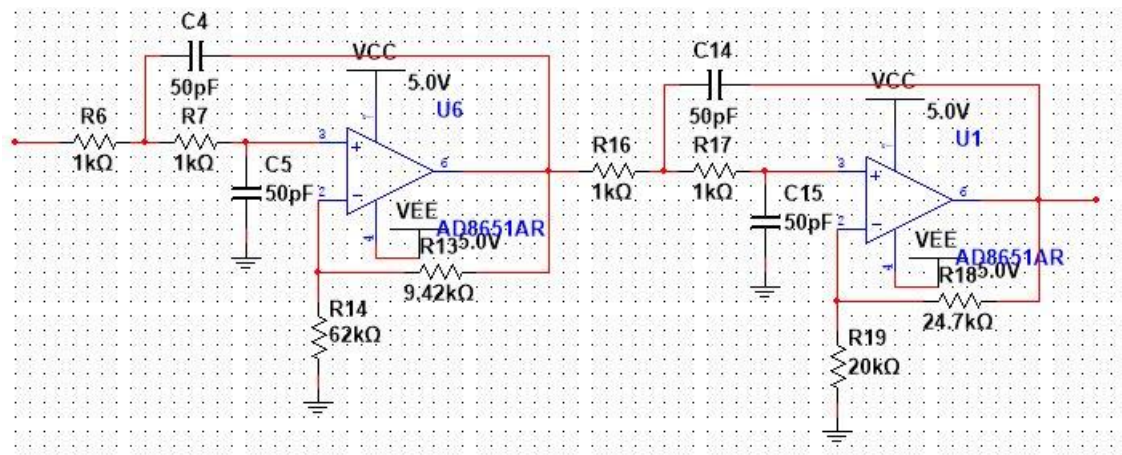


■ 仿真结果

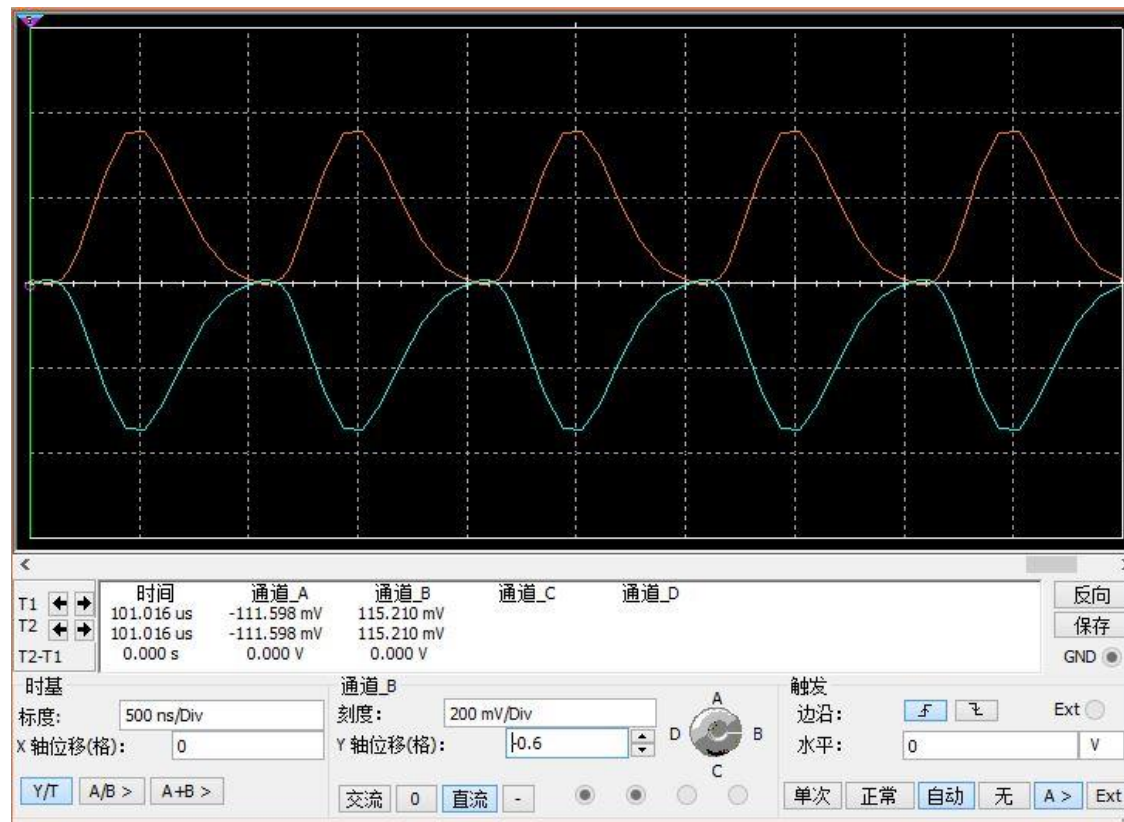


- 前沿约70ns
- 输入能量在5~20keV之间时输出峰值在200mV~800V之间 (图为6.5keV情况)

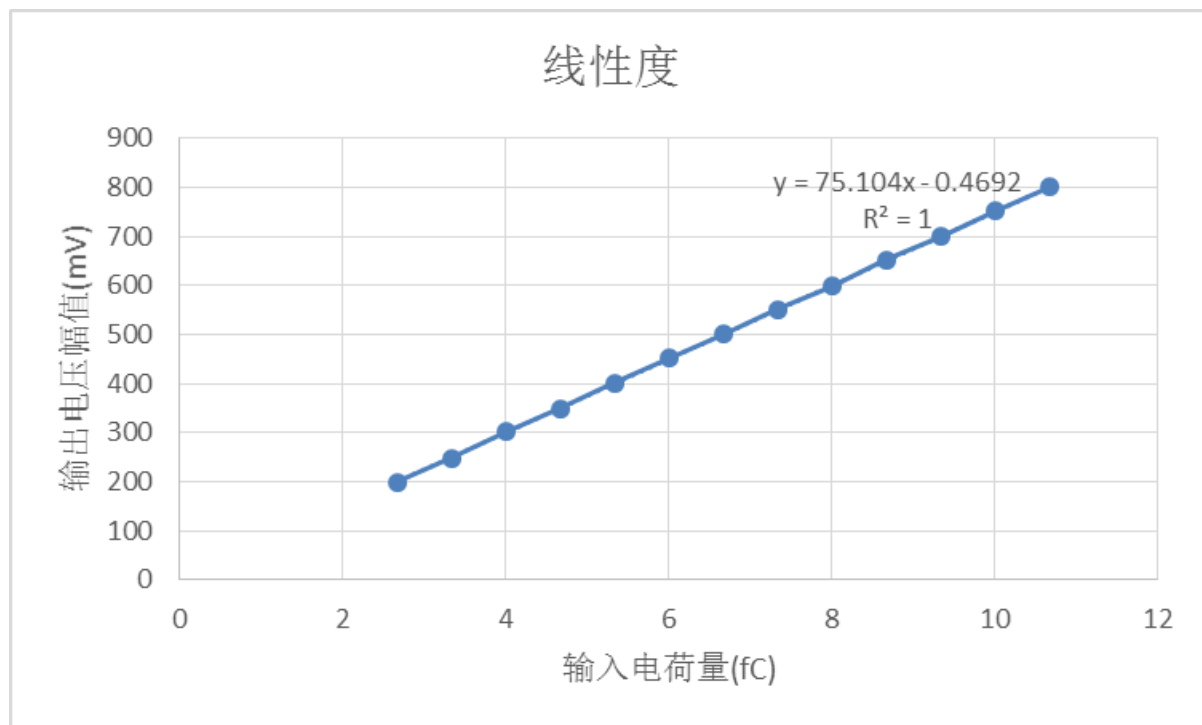
■ 高斯成形



- 输出信号经过Sallen-key 二阶低通滤波器进行高斯成形



线性度测量

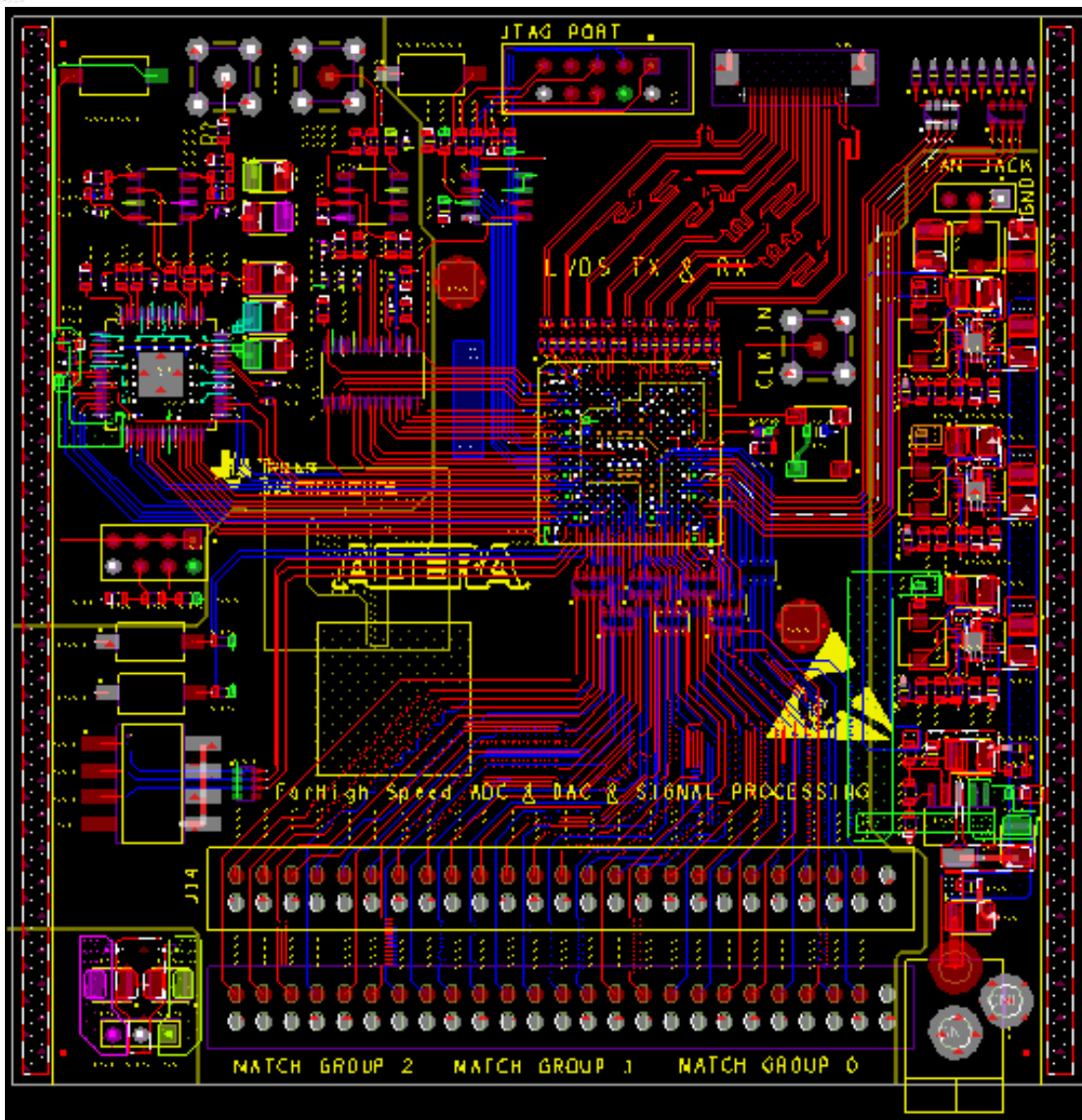


积分非线性

$$\varepsilon_i = \pm \frac{|V_{oMi} - (aQ_i + b)|_{\max}}{aQ_M + b} \times 100\%$$

求得积分非线性为0.2247%

数据采集电子学部分



- ADS5500
- Altera公司Cyclone IV系列的EP4CE10F1717N



■ 閾值甄別

```
always@(posedge clk or negedge rst)
```

```
begin
```

```
  if(!rst)
```

```
    ADdata_Out <= 10'd0;
```

```
  else if((ADdata_In >= Threshold)
    && !adc_or)
```

```
    ADdata_Out <= ADdata_In;
```

```
  else
```

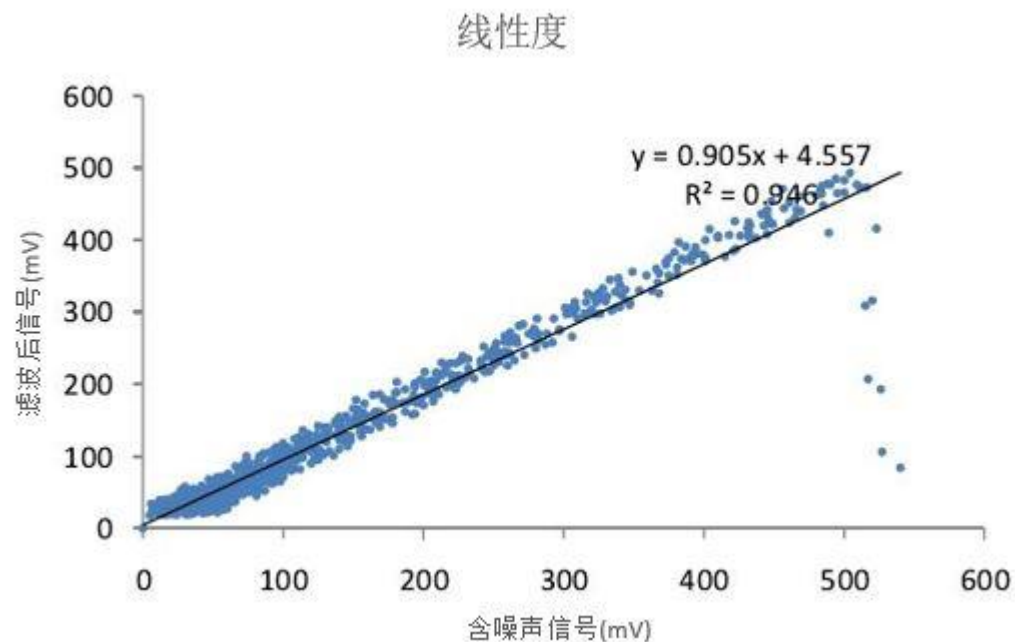
```
    ADdata_Out <= 10'd0;
```

```
End
```

■ Threshold值可调节

■ 用于处理噪声基底

FIR滤波器



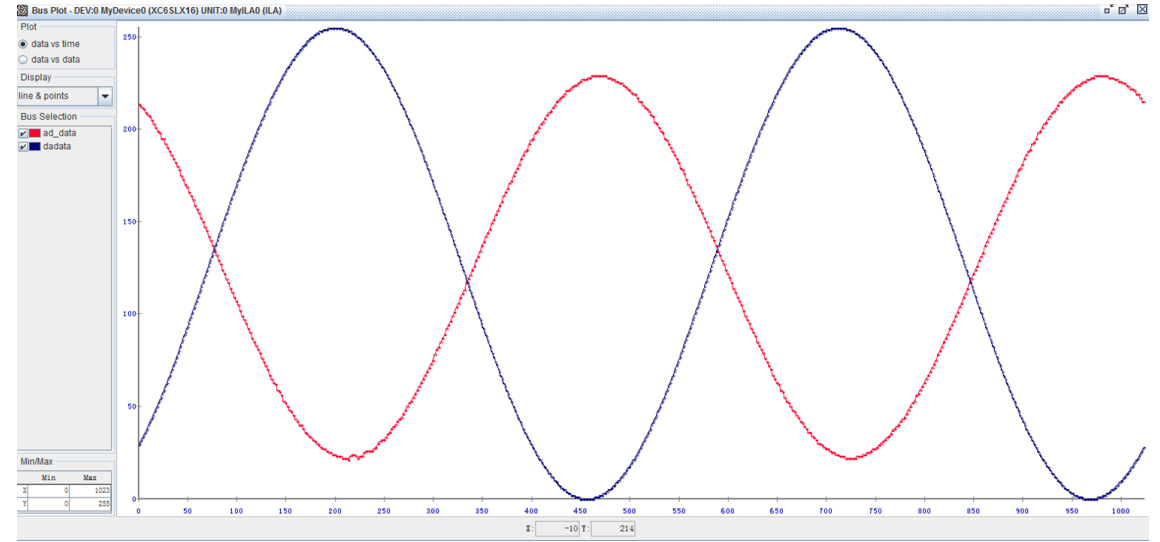
- 通过调用已有的IP核，实现滤波功能
- 经过滤波后输出信号与输入信号间的线性度有明显的下降，可以实现滤除高频噪声的功能

AD采样

利用chipscope查看输入与输出信号

The screenshot shows the Xilinx ISE IDE interface. The 'Hierarchy' window on the left displays the project structure, including the 'adtest' module and its sub-components like 'u1 - ad (ad.v)', 'u2 - volt_cal (volt_cal.v)', and 'u3 - uart (uart.v)'. The main editor window shows the Verilog code for the 'adtest' module, which is configured with a 100ms clock and two 13-bit ADCs. The code includes input and output declarations, clock assignments, and signal wiring for two channels.

```
20 ///////////////////////////////////////////////////////////////////
21 `timescale 1ns / 1ps
22 module adtest(
23     input clk100m,
24     input reset_n,
25
26     input rx,
27     output tx,
28
29     input [13:0] ad1_in,
30     output ad1_clk,
31
32     input [13:0] ad2_in,
33     output ad2_clk
34
35 );
36
37 parameter SCOPE_DIV =100;
38
39 assign ad1_clk=clk100m;
40 assign ad2_clk=clk100m;
41
42 wire [13:0] ad_ch1;
43 wire [13:0] ad_ch2;
44 wire [7:0] ch1_sig;
45 wire [7:0] ch2_sig;
```



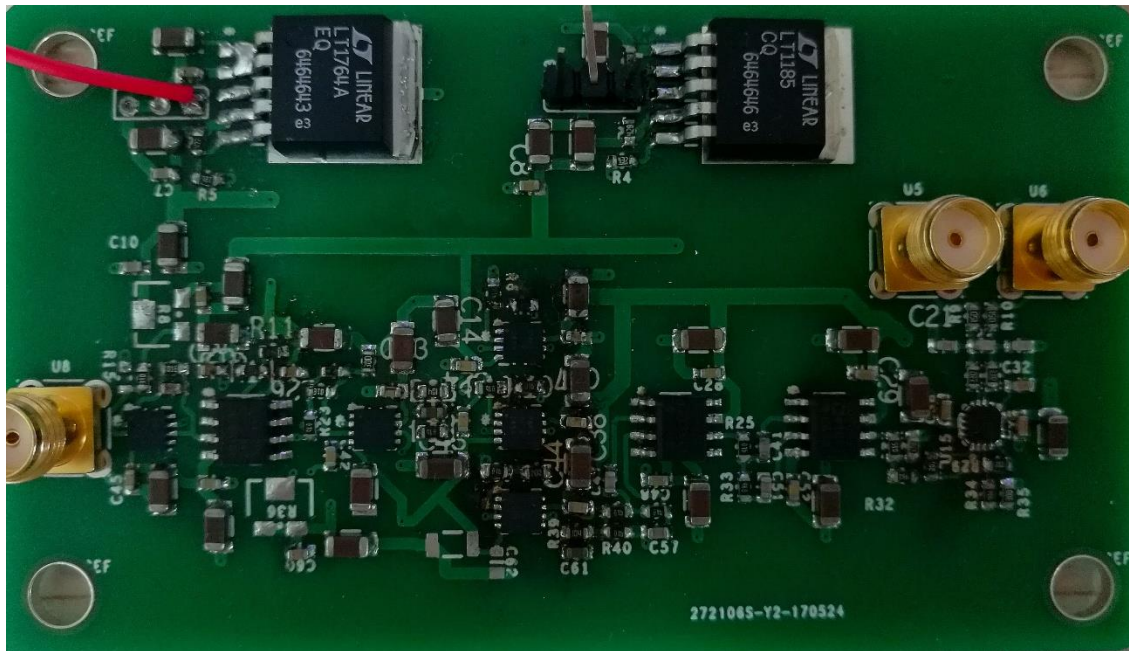
数据通过RS232串口输出

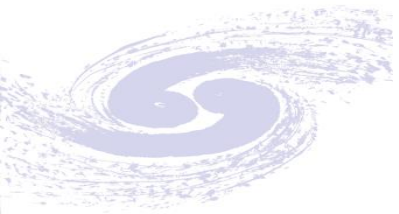
The serial port configuration window shows the following settings: COM3, 9600 baud rate, NONE parity, 8 data bits, and 1 stop bit. The '关闭串口' (Close Serial Port) button is highlighted. The '清空接收区' (Clear Receive Area) and '接收区' (Receive Area) buttons are also visible. The '自动清空' (Auto Clear) checkbox is checked, and the '十六进制显示' (Hexadecimal Display) checkbox is unchecked. The '保存显示数据' (Save Display Data) button is highlighted, and the '更改' (Change) button is also visible. The path 'C:\COMDATA' is shown at the bottom.

AD1	AD2
-3.742V	-0.095V
+4.111V	-0.095V
-3.776V	-0.100V
+4.013V	-0.097V
-3.525V	-0.097V
+3.613V	-0.097V
-3.022V	-0.102V
+2.998V	-0.102V
-2.285V	-0.097V
+2.163V	-0.097V
-1.367V	-0.097V
+1.184V	-0.090V

研究进展

- 方波信号输入，经电容转换成电荷输入
- 三级放大60dB（1000倍）





总结与展望

- 目前系统已经完成了前放部分的设计和制作，正在进行初步的调试和优化，数据采集电子学部分也正在设计实现中。



谢谢