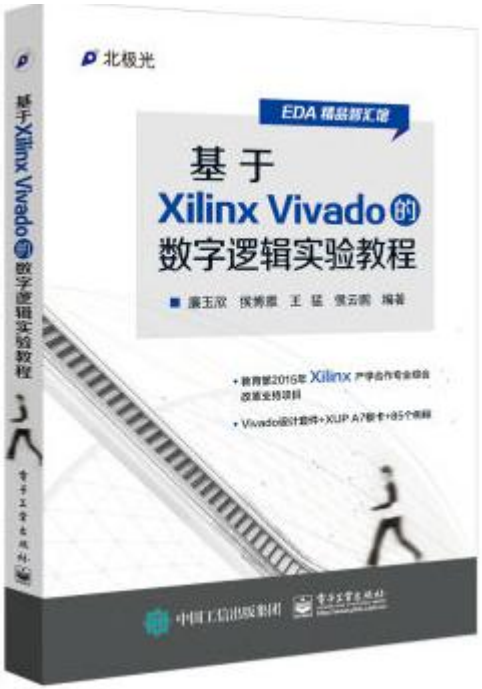
status summary

2017 4.5 -- 4.7

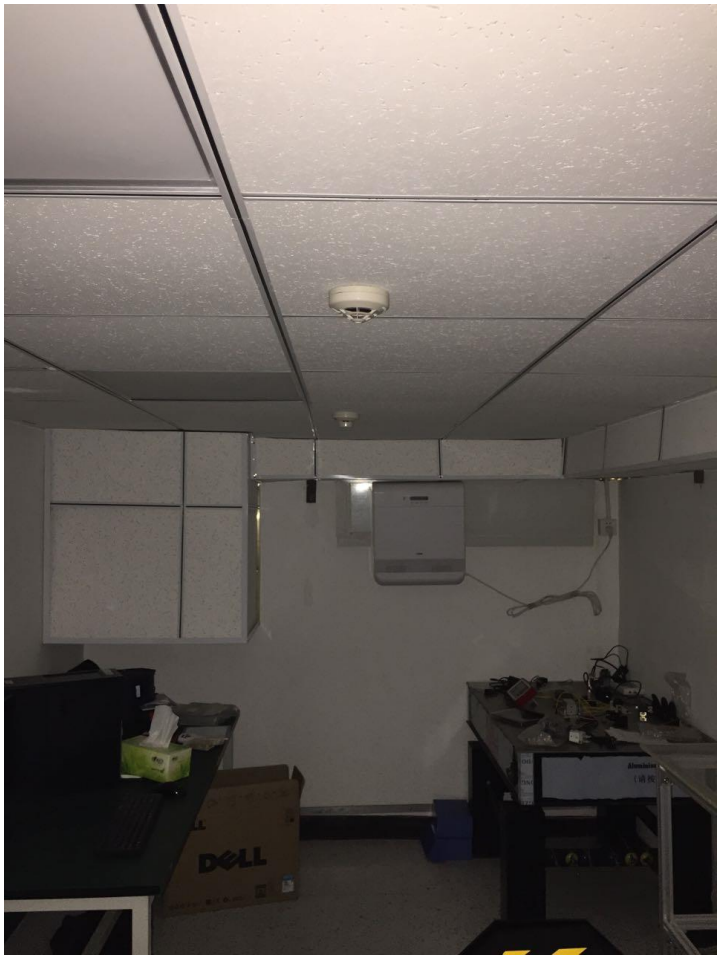
Liu kai

Review

- read an introductory book about vivado and verilog.[**done**]
- **learned:**
  - how to use vivado
  - basic verilog
- **first verilog program tested**:OK
    - a logic gate with two inputs
    - following pages show the details.
- **Plan:**
  - run Ju Xudong's code ASP.



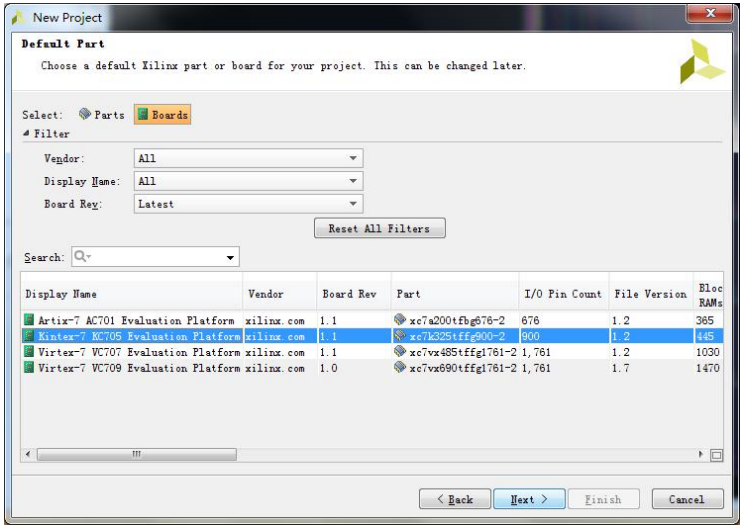
clean room

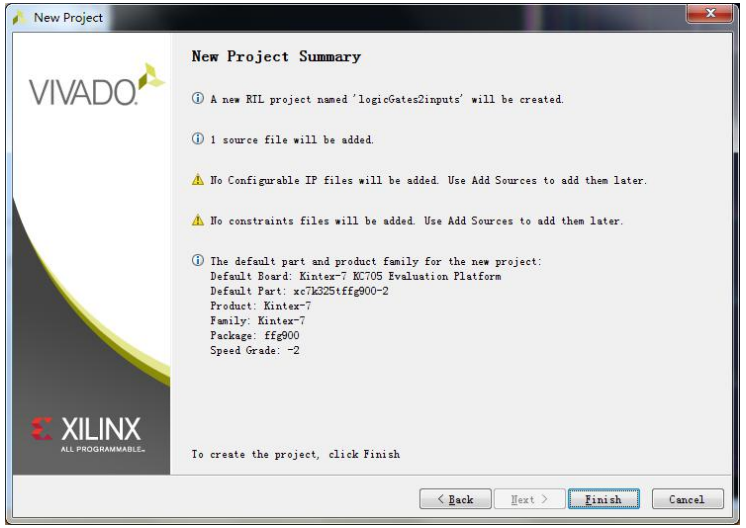


notes on learning vivado and verilog

logic gate with two inputs

create new project





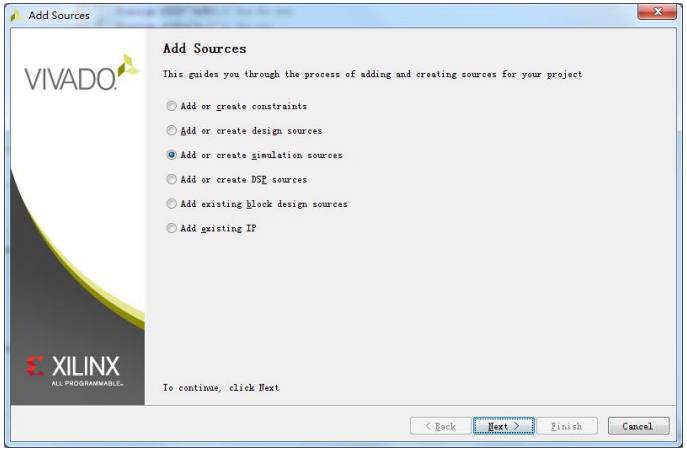
verilog source file

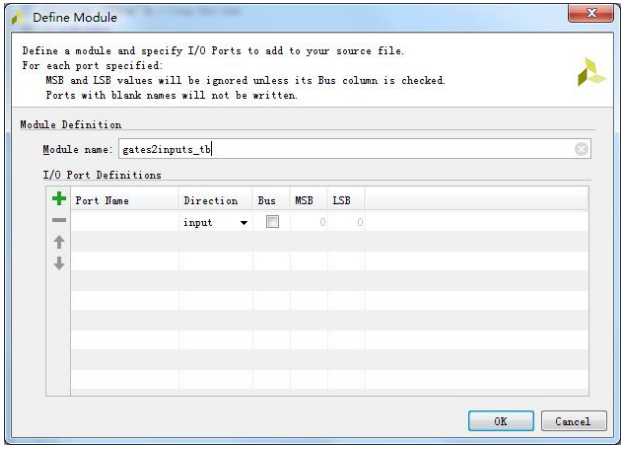
gates2inputs.v | gates2inputs_tb.v | Untitled 7

G:/fpga/learning/logicGates2inputs/logicGates2inputs.srcs/sources_1/new/gates2inputs.v

```
1   module gates2inputs(
2   input a,
3   input b,
4   output [5:0]y
5   );
6     assign y[0]=a&b;// and gate
7     assign y[1]=~(a&b);// yu fei men
8     assign y[2]=a|b; //or
9     assign y[3]=~(a|b);// huo fei men
10    assign y[4]=a^b;// yi huo men
11    assign y[5]=a~^b;//tong huo men
12  endmodule
```

仿真文件



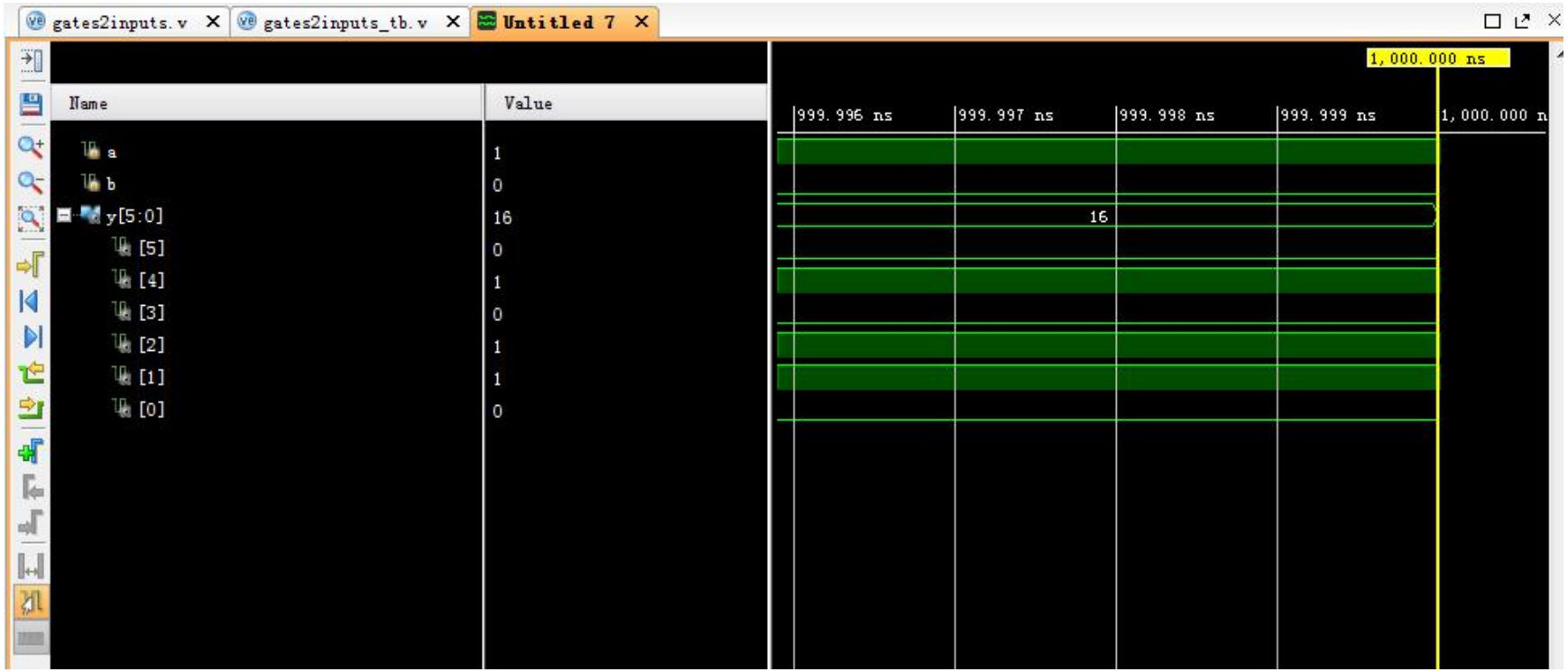


gates2inputs.v | gates2inputs_tb.v | Untitled 7

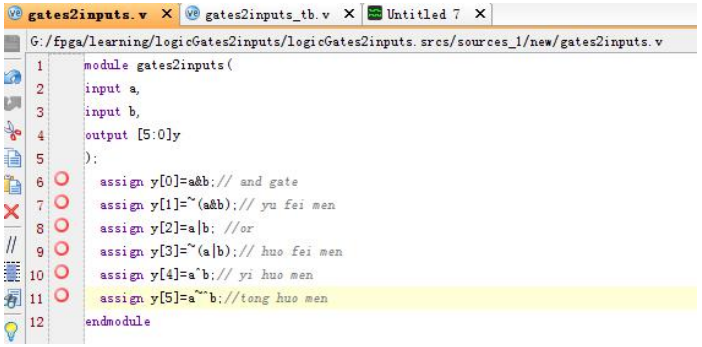
G:/fpga/learning/logicGates2inputs/logicGates2inputs.srcs/sim_1/new/gates2inputs_tb.v

```
1   module gates2inputs_test;
2   reg a,b;
3   wire [5:0]y;
4   gates2inputs Gtest(a,b,y );
5   initial
6   begin
7   //a=0;b=0;#100;//sleep 100 time units
8   //a=0;b=1;#100;
9   a=1;b=0;#100;
10  //a=1;b=1;#100;
11  end
12  endmodule
```

仿真结果


gates2inputs.v
gates2inputs_tb.v
Untitled 7
Name
Value
a
1
b
0
y[5:0]
16
[5]
0
[4]
1
[3]
0
[2]
1
[1]
1
[0]
0
1,000.000 ns
999.996 ns
999.997 ns
999.998 ns
999.999 ns
1,000.000 n
16

波形图怎么看？


gates2inputs.v
gates2inputs_tb.v
Untitled 7
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