UT – A Silicon Strip Detector For The LHCb Phase I Upgrade

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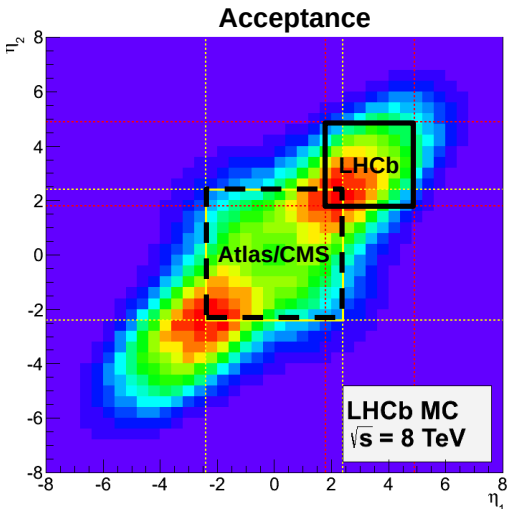
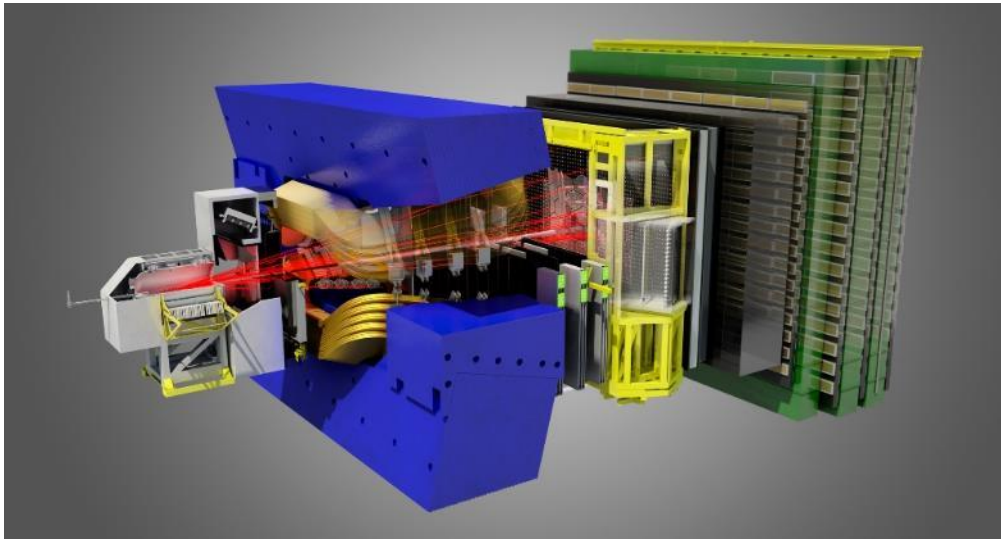
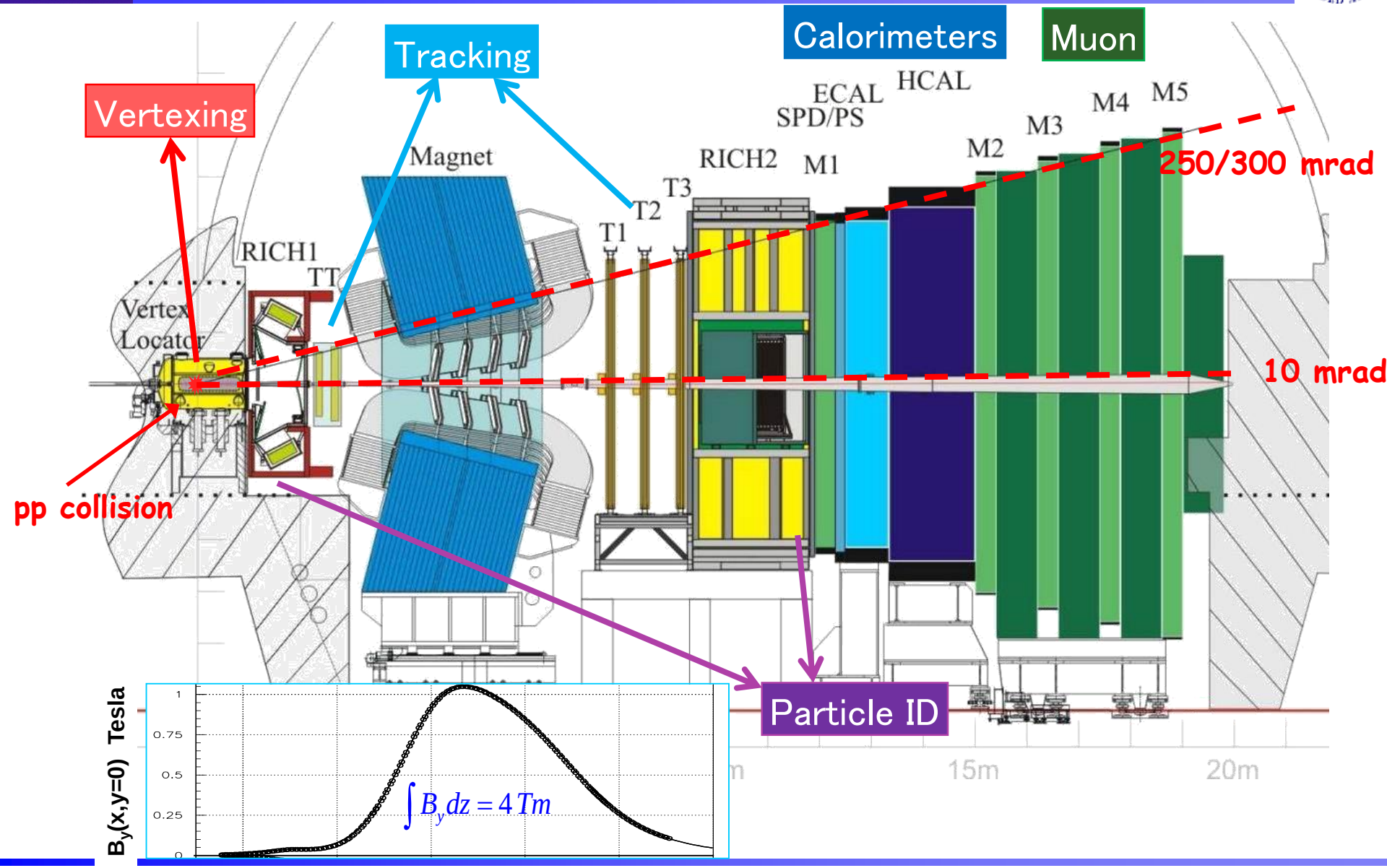
LHCb-A Forward Spectrometer

- LHCb experiment was designed to study CP-violation & search for new physics phenomena in b & c sectors
- The detector covers the forward region: $2<\eta<5$. Boost in Z $\Rightarrow$ good decay length measurement. Production of $b\bar{b}$ are correlated $\Rightarrow$ flavor tagging.
- It provides precision measurements:
  - Spatial resolution ~ 4 μm @ vertex detector.
  - $\Delta p/p = 0.4\%$ at 5 GeV/c, 0.6% at 100 GeV/c.
  - Impact parameter resolution ~20 μm for high-pT tracks.
  - Decay time resolution $45\ fs$ (e.g. $B_s \rightarrow J/\psi\ \varphi$).
  - Excellent particle identification.



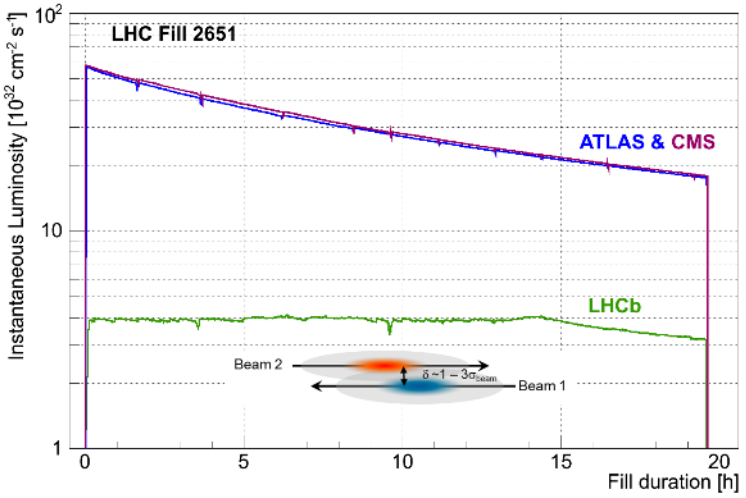


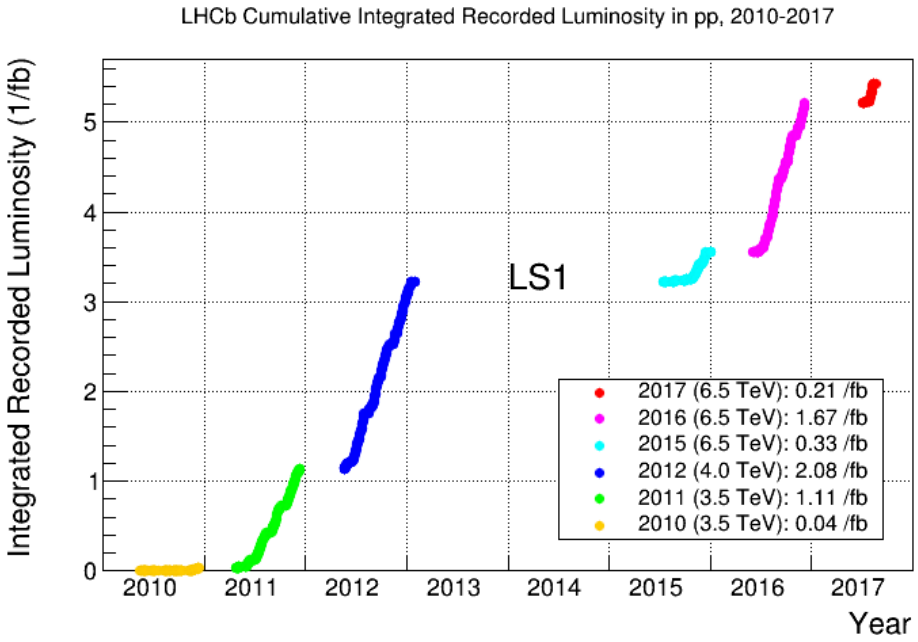
The Current LHCb Detectors



LHCb Operation

- Initial optimal $\mathcal{L}\sim 2\times10^{32}\text{cm}^{-2}\text{s}^{-1}$, ~1 visible interactions per crossing due to LHCb trigger and readout scheme.
- The trigger is re-optimized. LHCb runs @ $\mathcal{L}\sim 4\times10^{32}\,\text{cm}^{-2}\text{s}^{-1}$, ~1.7 visible int./Xing.
- Operates at flat luminosity within each fill.

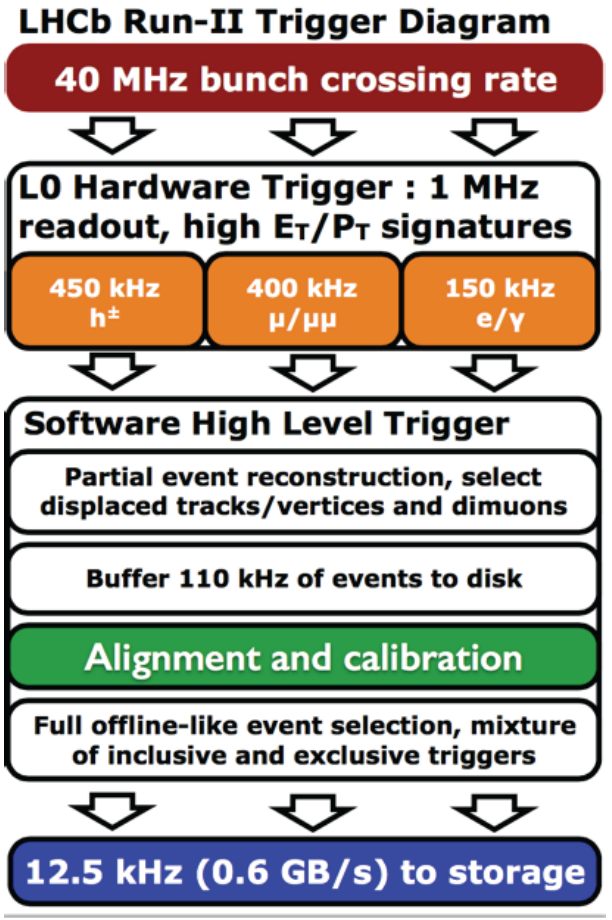




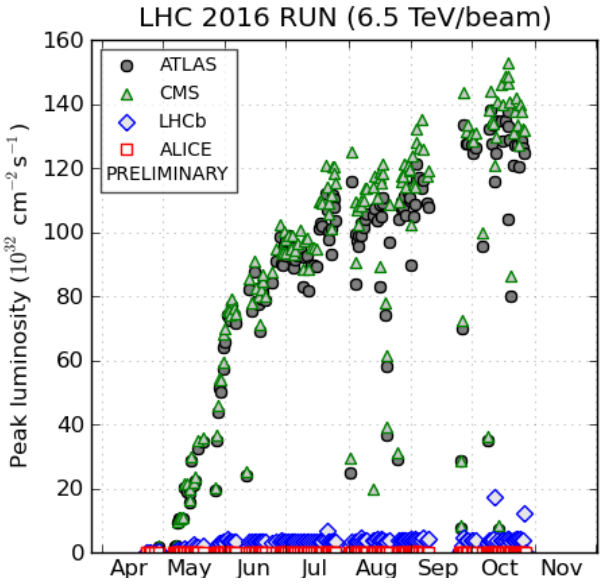
- Already collected ~ 5.5 fb^{-1} data in run 1 and 2.
- Project to collect total >~ 8 fb^{-1} by the end of run 2 (~end of 2018).

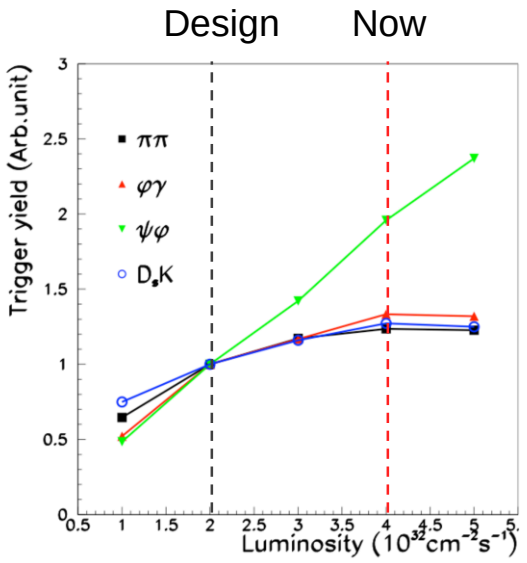
LHCb Trigger

- Three-level trigger of increasing complexity.
- L0 hardware trigger is based on calorimeter & muon systems. It selects events with high P_T muon or high E_T hadron.
- L0 reduces rate from 40 MHz to 1 MHz, with a latency of 4 μs, mandated by the fact that the whole detector can be read out at 1 MHz.
- Two-stage software High Level Triggers (HLT), partial reconstruction in the 1st level, and full reconstruction in the 2nd level.
- The software application runs on a large computing cluster (~40K jobs).
- The event rate is reduced to ~12 kHz.
- The 2nd level HLT was done offline in Run 1. And the 1st level output rate was 5 kHz.



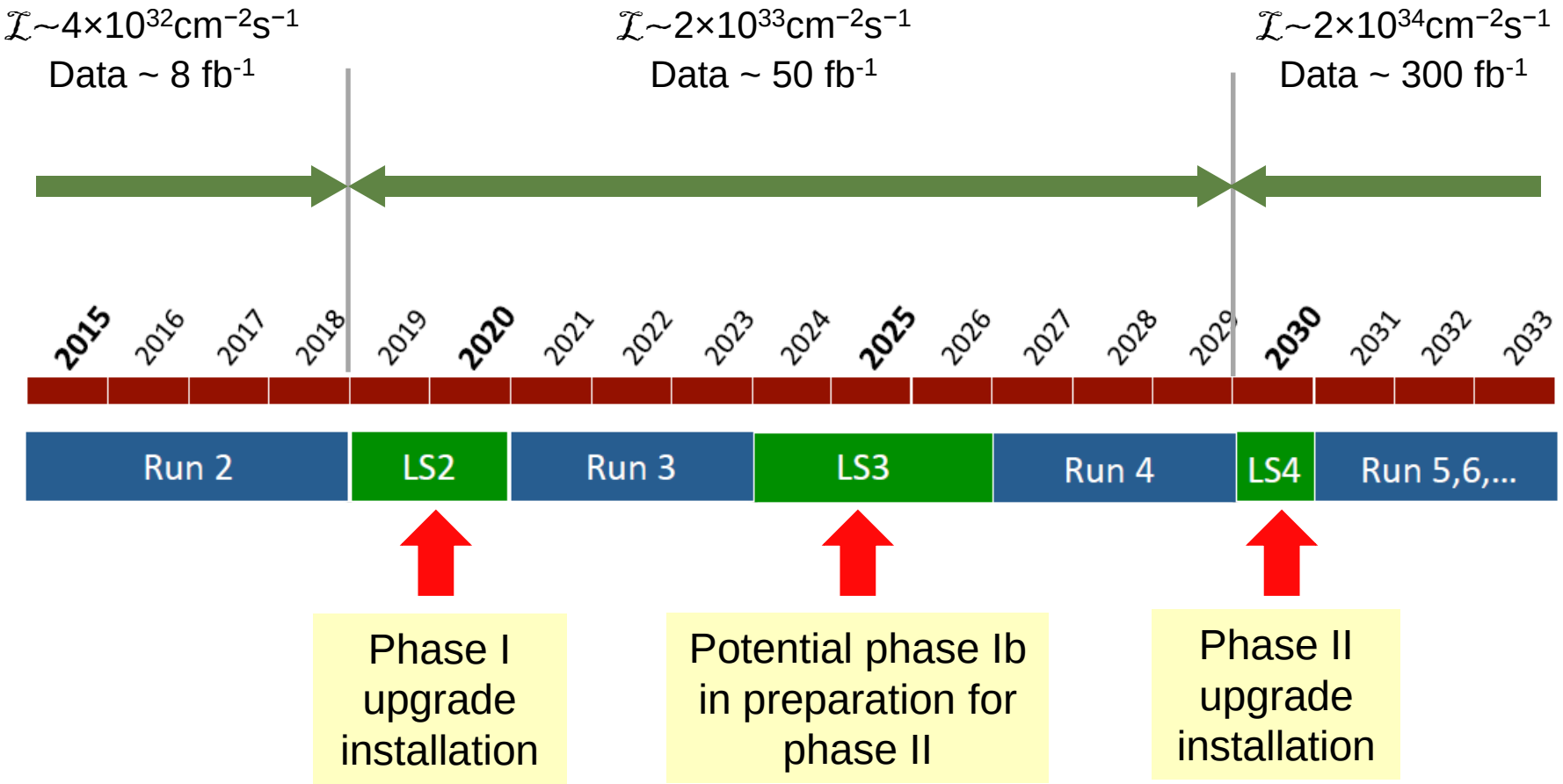
Limitation of The Current Detector





- LHC could deliver LHCb with higher luminosity (ATLAS/CMS @ x40 luminosity).
- The 1 MHz readout bandwidth and the hardware trigger are severe bottle necks. Physics yields for hadronic channels saturate with increasing $\mathcal{L}$
- Detector was designed for 5 years at half the current $\mathcal{L}$. Higher luminosity would mean more radiation damage and performance degradation.
- CPU time for event reconstruction increases exponentially due to increasing track and primary vertex multiplicity and combinatory.

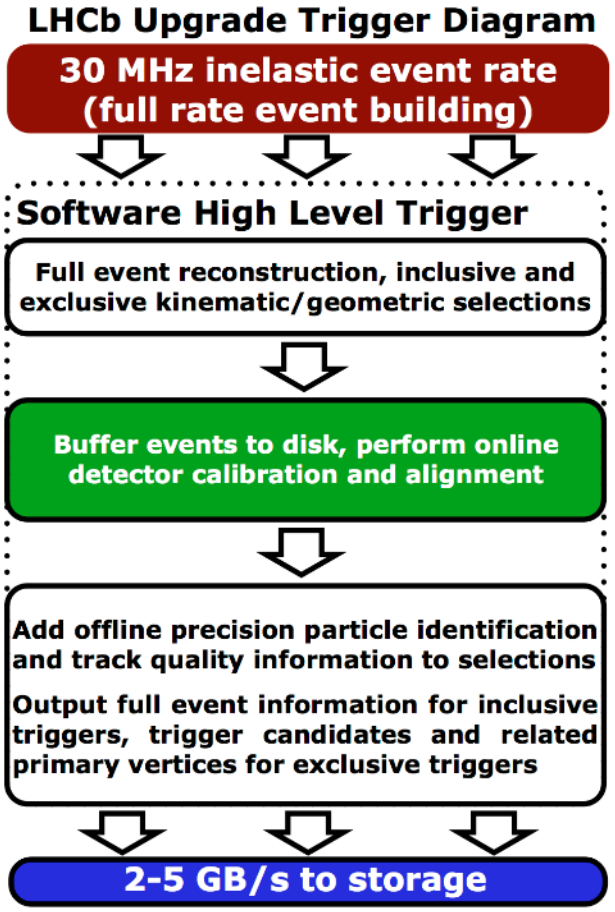
LHCb Upgrade Plans



LHCb Phase I Upgrade

Phase I Upgrade Strategy

- Run @ $2x10^{33}$ $cm^{-2}s^{-1}$ for 5 years, ~50 fb^{-1}.
- Remove L0 hardware trigger, read out all detectors at each bunching crossing.
- Flexible software trigger is performed entirely on a CPU farm. Information from all sub-detectors are available to enhance the trigger decision and maximize the signal efficiency at high rate.
- All detectors be read out @ 40 MHz
  - Replace FE electronics of most detectors.
  - A new read out network to cope with multi-TB/s data stream.
- Detectors work at a higher luminosity
  - High granularity for increased multiplicities.
  - Radiation resilience.

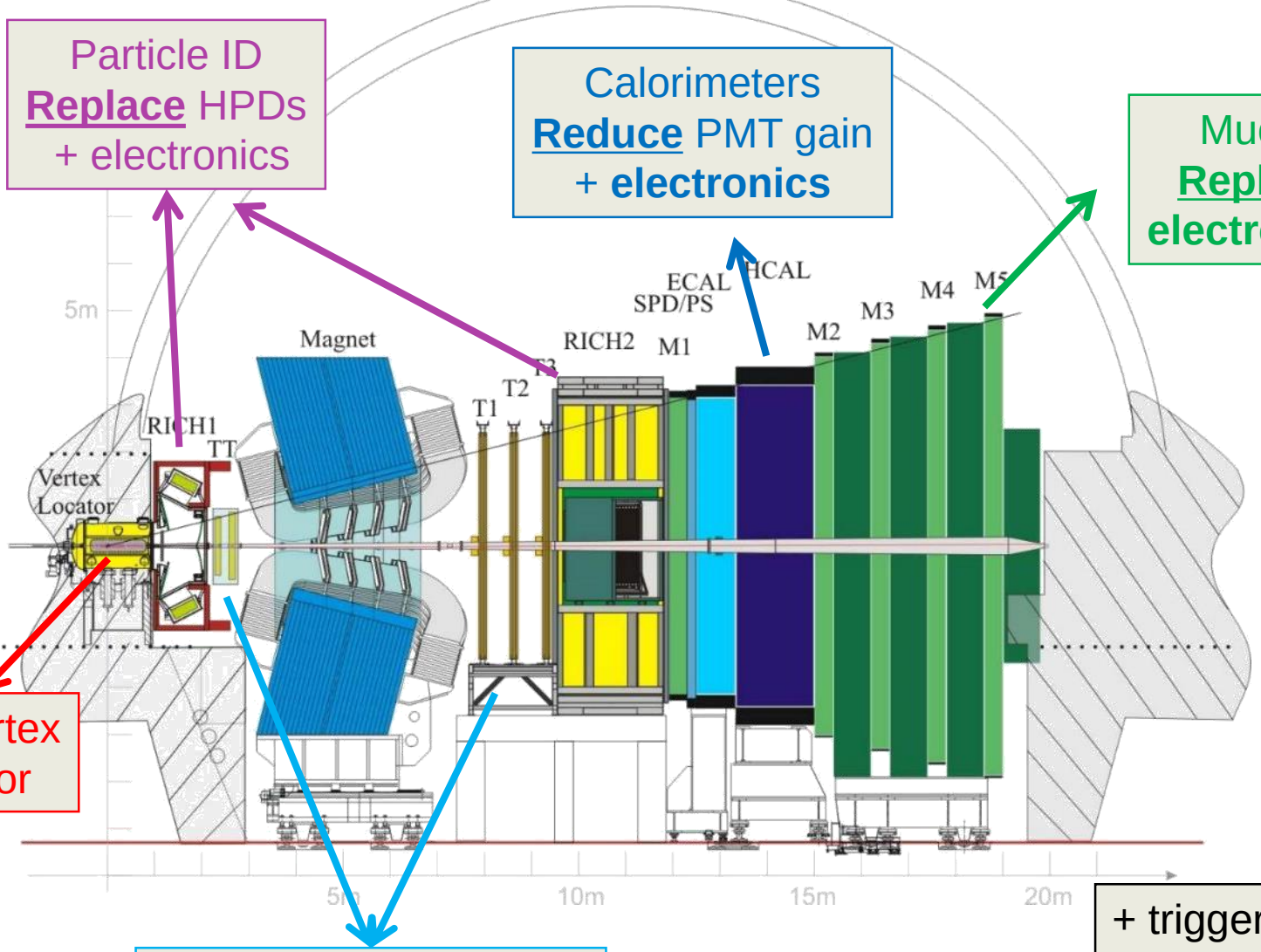


The Phase-I Upgraded Detectors

Particle ID
Replace HPDs
+ electronics

Calorimeters
Reduce PMT gain
+ **electronics**

Muon
Replace
electronics



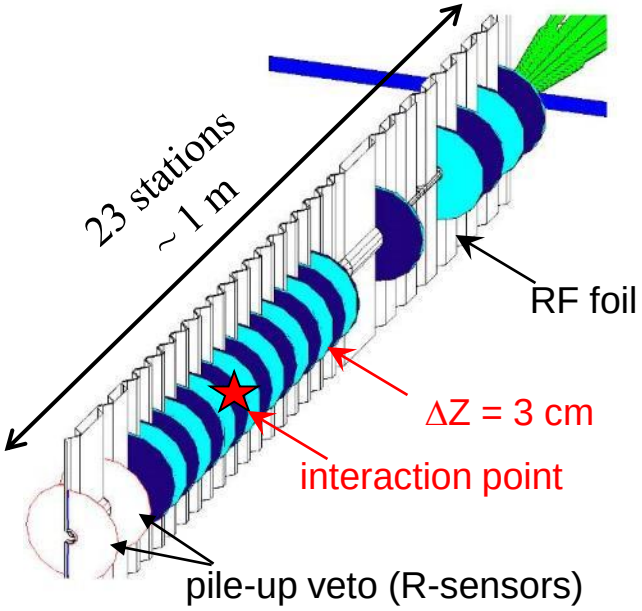
New Vertex
Detector

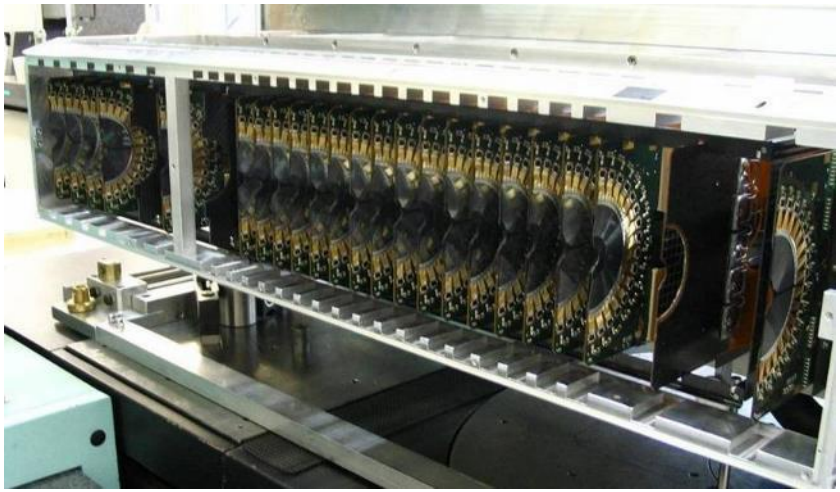
New Tracking stations

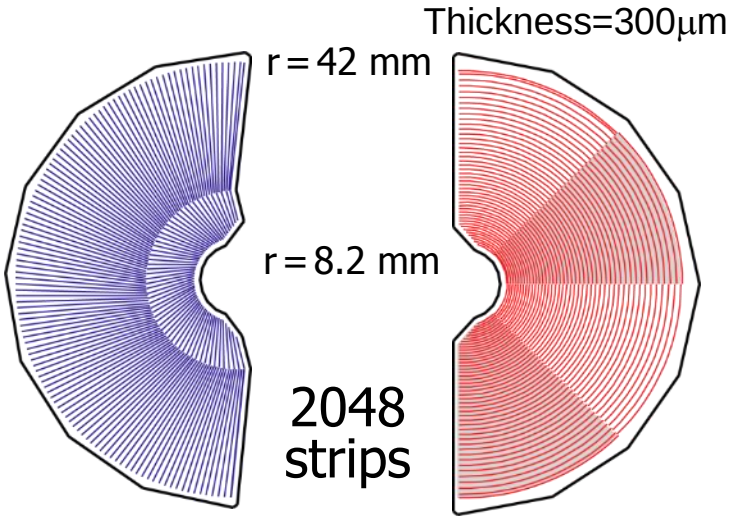
+ trigger-less
readout system

Current Vertex Locator

- Silicon micro-strip, n+ in n-bulk rad-hard sensors, max fluence ~7×10^{14} n_{eq}cm^{-2} for full lifetime.
- R-Φ geometry, 40–100μm pitch.
- Serialized (x32) differential analog output from Beetle ASICs outside of the sensors.
- Optimized for
  - Tracks originating from beam-beam interactions.
  - Fast online 2D (R-z) tracking.
  - Fast offline 3D tracking in two steps (R-z then ϕ).



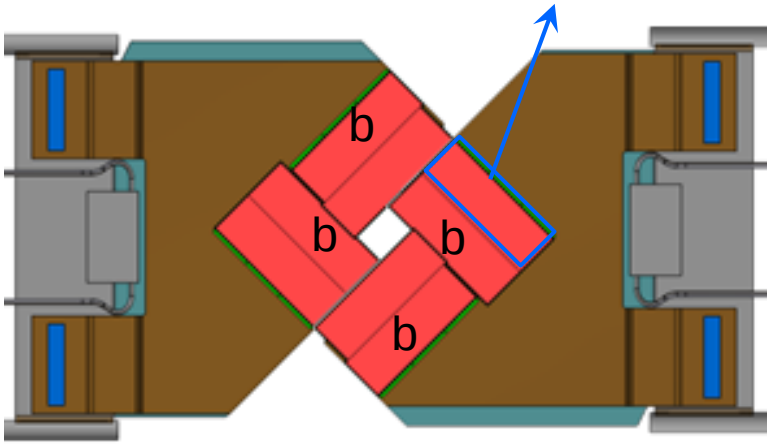


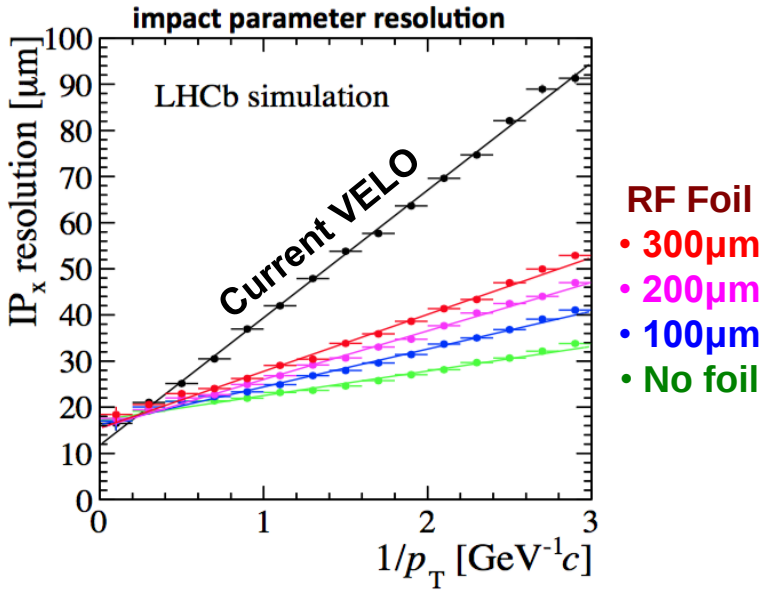


VELO Pixel Detector

- Similar geometry as the current one: 26x2 modules, 25 mm gap.
- Si pixel sensors, pixel size 55×55μm^2.
  - n+ in n-bulk type.
  - Sensor size ~43×15 mm^2
  - Reduced thickness 300 ⇒ 200 μm.
  - Closer to beam 8.2 ⇒ 5.1 mm.
  - More rad-hard, Φ_{max} ~8×10^{15} n_{eq}cm^{-2}
- Thinner RF foil, 300 ⇒ 250 μm
- Read out by 3 VeloPix ASICs per sensor, which are bump bonded to the sensor.
- VeloPix is custom designed, 256 x 256 pixel matrix, binary readout at 40 MHz, and can handle 800 Mbits/s data rates.

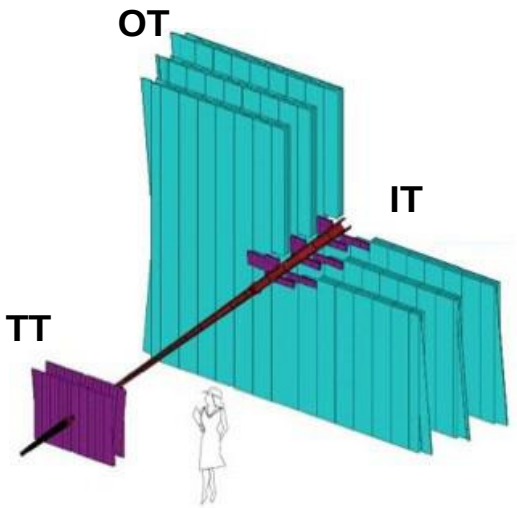
Each sensor ~43x15mm^2

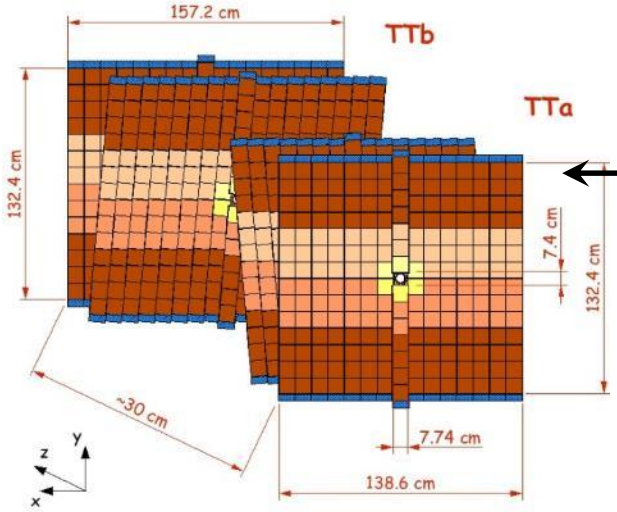


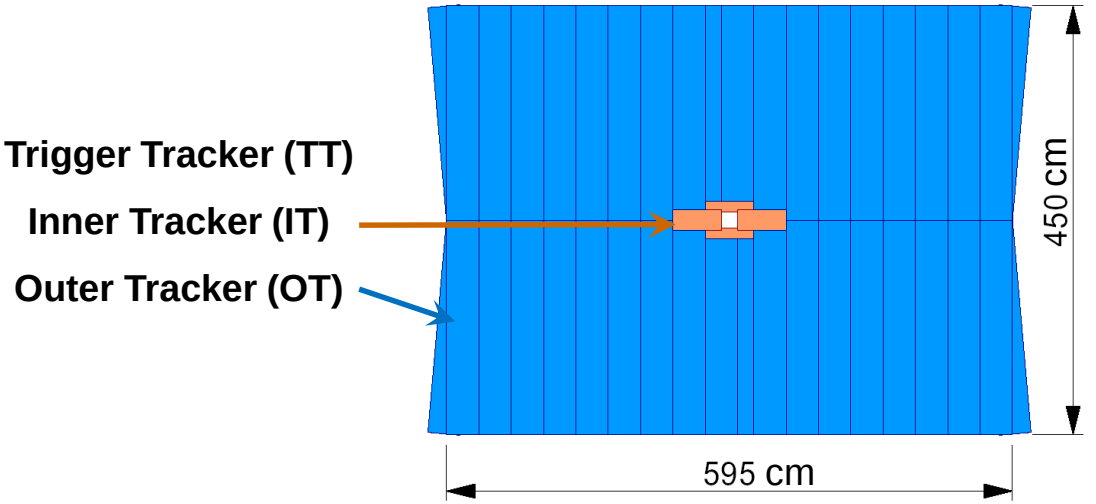


The Current Tracking Stations

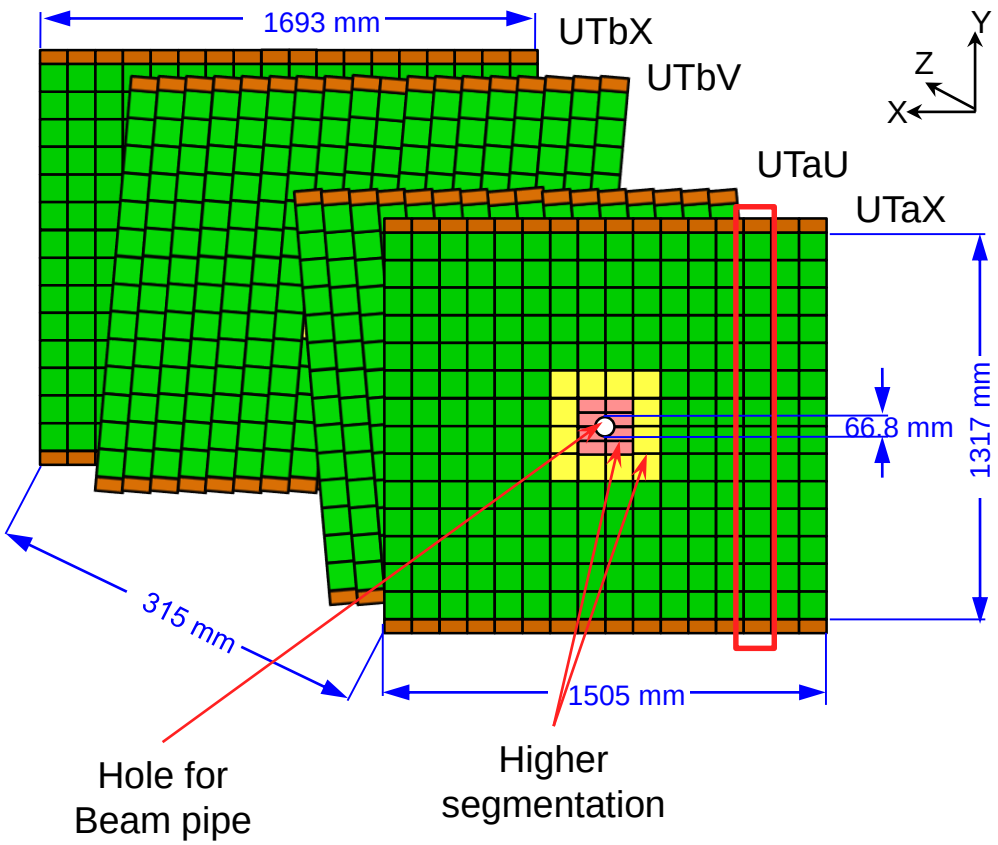
- The tracking stations consist of 4 planes TT before the magnet, 3x4 planes of IT & OT after the magnet.
- Four planes (x,u,v,x) of each group are at (0°,+5°,-5°,0°), provide stereo measurements, precision horizontally.
- TT & IT are p-type silicon strip detectors, read out by Beetle ASICs outside active area.
  - TT: 183 μm pitch, 500 μm thick, up to 37.6 cm long
  - IT: 200 μm pitch, 320/410 μm thick, 11/22 cm long.
- OT is made of Kapton/Al straw drift tubes d=5 mm, with $Ar+CO_2+O_2$ gas, providing ~0.2 mm resolution.







The UT Detector System

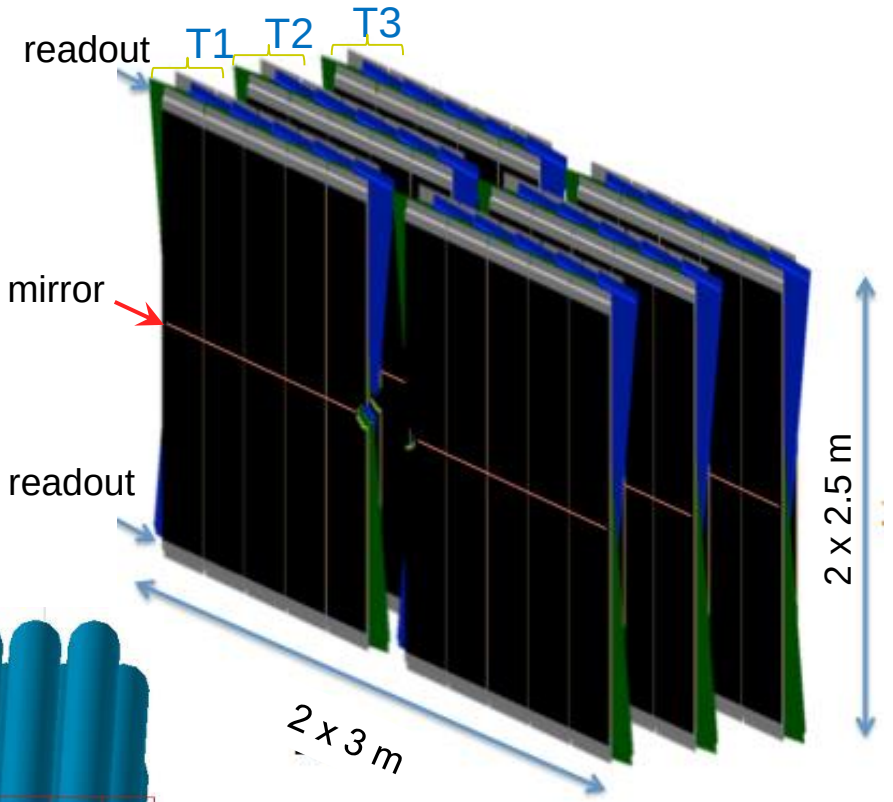


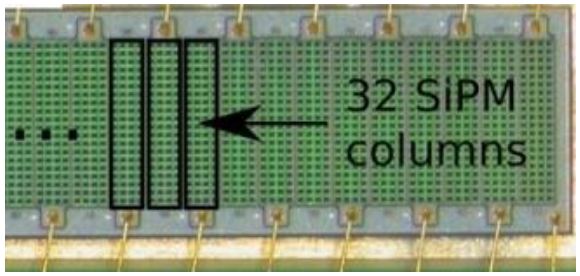
- UT is to replace TT. It has a similar geometric configuration.
- Much improved coverage: circular hole surrounds beam pipe; sensor overlaps in X & Y directions.
- Reduce material at small angle.
- Higher segmentation, especially in the central regions, < 2% strip occupancy.
- Sensor is more radiation resilience, Φ_{max} ~5×10^{14} n_{eq}cm^{-2}.
- Read out at 40 MHz by custom SALT ASICs in the sensor proximity.
- Digital event packed in ASIC, sent out at the end of detector via optical fibers.

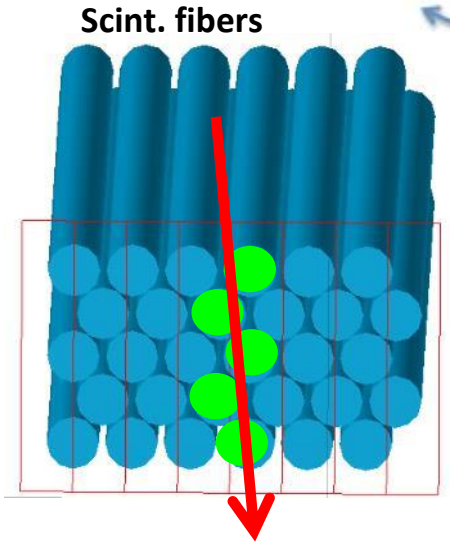
(More details will be discussed)

Scintillation Fiber Detector

- IT+OT trackers will be replaced by a 12-plane scintillation fiber detector.
- Each plane is made of 6 layers staggered Ø250 μm fiber mats.
- Total ~ 10,000 Km long fibers.
- Read out with arrays of SiPMs (–40°C) + custom made PACIFIC ASIC. One SiPM channel extends over the full height of the mat.
- Spatial resolution ~80 mm.
- Single hit efficiency ~99%.



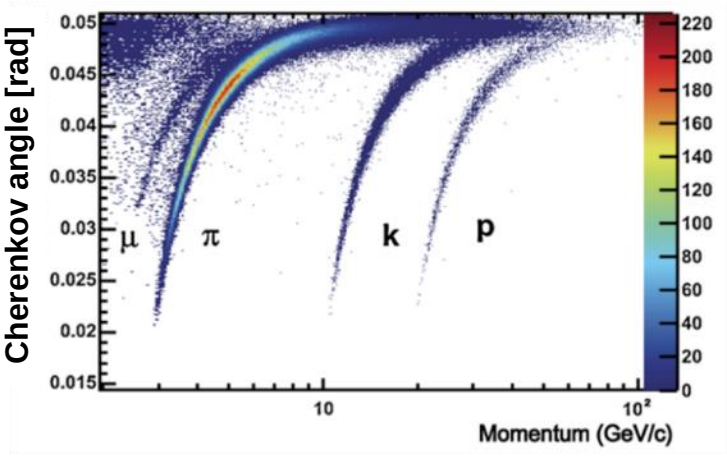




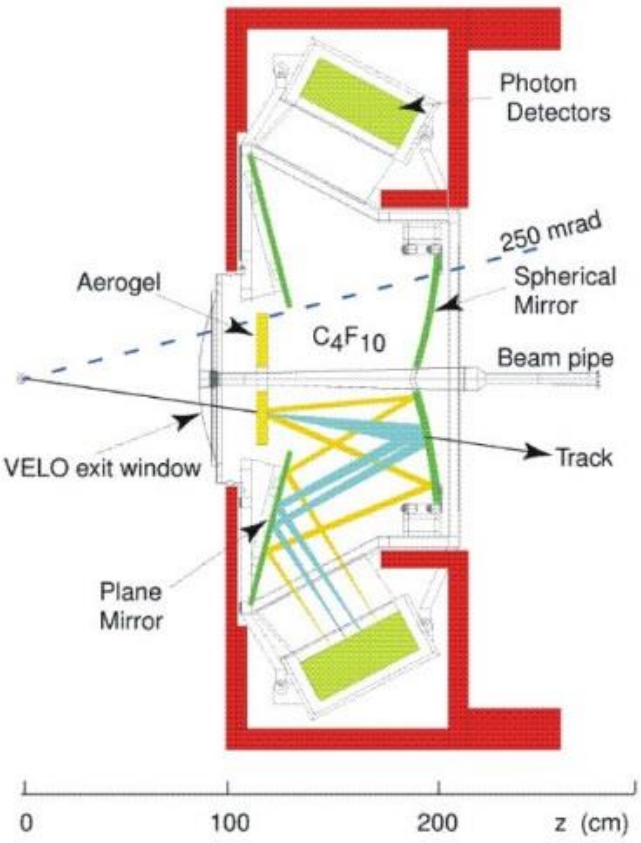
Ring Imaging Cherenkov Detectors

- Two RICH detectors: RICH1 (aerogel+C_4F_{10}) for 2<P<60 GeV & RICH2 (CF_4) for 15<P<100 GeV tracks.
- Cherenkov radiation photons are focused on HPD plane.
- HPDs have embedded FE electronics, 1 MHz readout.
- Provide excellent PID, e.g. 5% $\pi \Rightarrow$ K of 95% efficiency..

- Remove aerogel radiator to compensate for increased occupancy. RICH1 focal plane & optics are modified to increase the size of Cherenkov rings.
- Replace HPD with Multi-Anode PMT (80% active area), and new front end electronics at 40 MHz.



RICH1

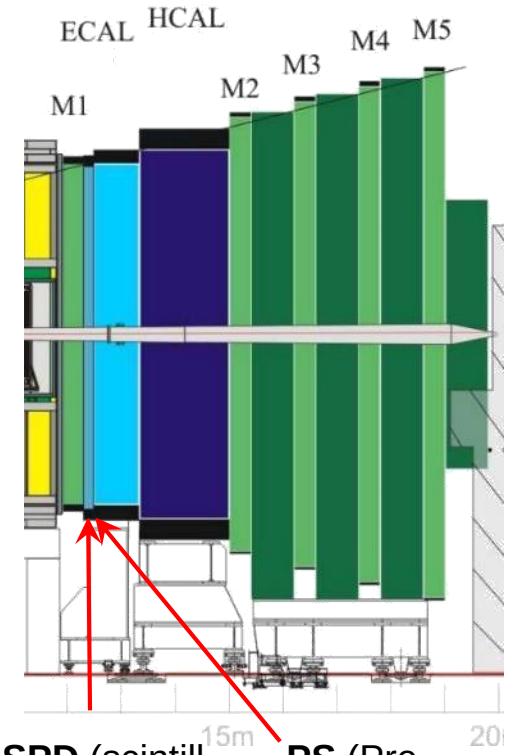


Calorimeters & Muon

SPD+PS+ECAL:25 X0

HCAL: 5.6 λ_i

Calorimeters + Muon: 20 λ_i



SPD (scintill. pad detector)

PS (Pre-shower)

Calorimeters:

- Select high E_T e/γ/h for L0 trigger.
- e/γ/hadron ID, energy & position.
- SPD & PS are separated by 15 mm ($2.5X_0$) lead. They use scint. pads, read out by MAPMT, coupled by wave length shifting (WLS) fibers.
- ECAL uses Pb + scintillator, and HCAL uses Fe + scintillating tiles, read out by PMT.
- Fine segmentation at the center.

Muons:

- Total 5 stations M1-M5.
- Triple-GEM (gas electron multiplier) detector @ the center of M1 for high hit rates.
- The rest are MWPCs, of higher granularity close to beam.
- Alone gives $\delta p/p \sim 20\%$ for L0 trigger.
- Muon ID cut off ~ 6 GeV.

CALO upgrade:

- Remove SPD & PS
- Replace the inner ECAL modules after ~20 fb^{-1}
- Reduce PMT gain by factor of 5, to reduce aging due to higher luminosity.
- New FE electronics for 40 MHz readout.

MUON upgrade

- Remove M1
- Add shield in front of M2 at the center to reduce the rate.
- New readout electronics

Phase II Upgrade

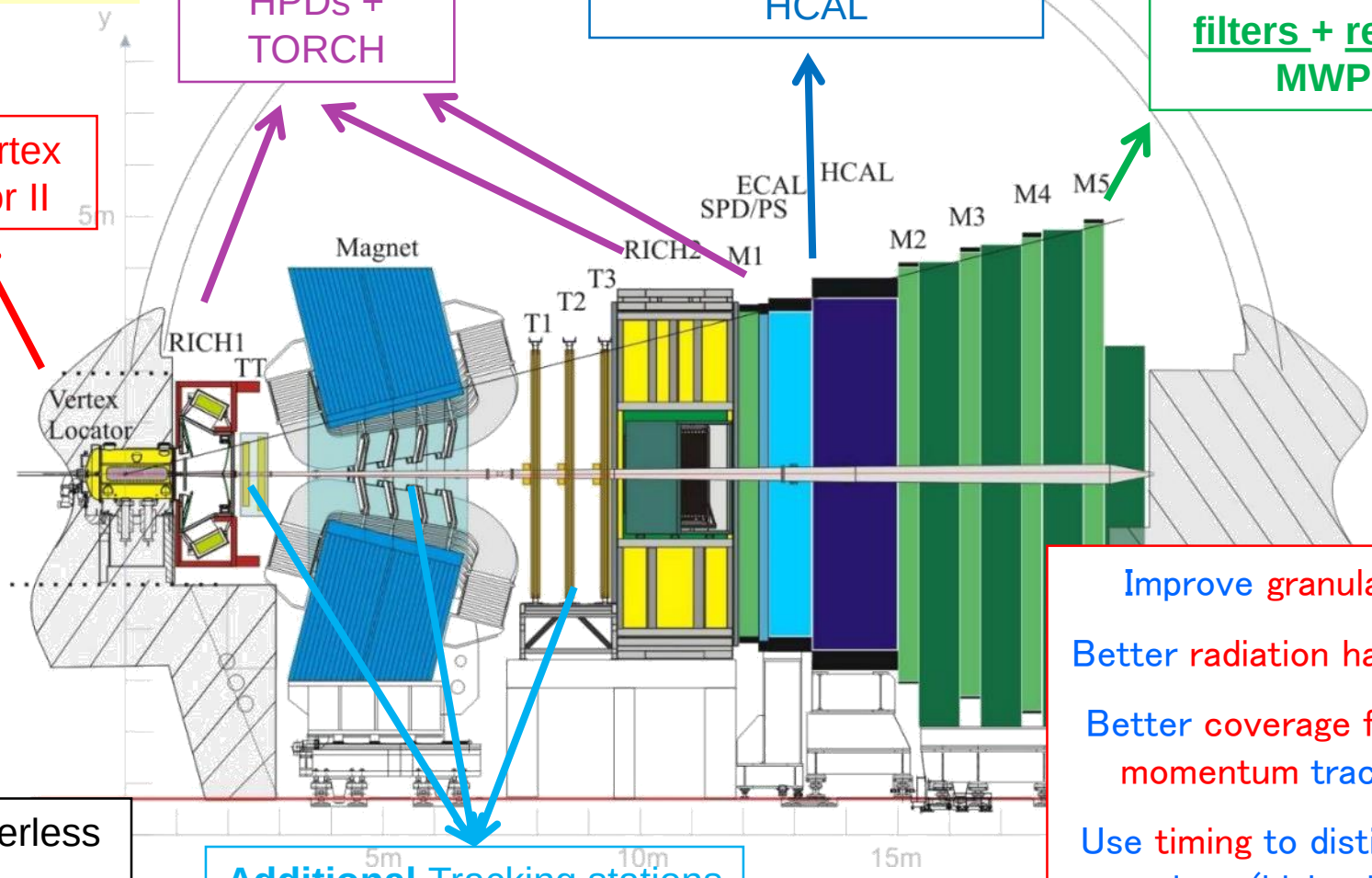
$\mathcal{L} \sim 2\times10^{34}\text{cm}^{-2}\text{s}^{-1}$
Data ~ 300 fb^{-1}

Particle ID
Replace
HPDs +
TORCH

New ECAL, **remove**
HCAL

More MUON
filters + replace
MWPC

New Vertex
Detector II



Improve granularity

Better radiation hardness

Better coverage for low momentum tracking

Use timing to distinguish vertices (high-pileup)

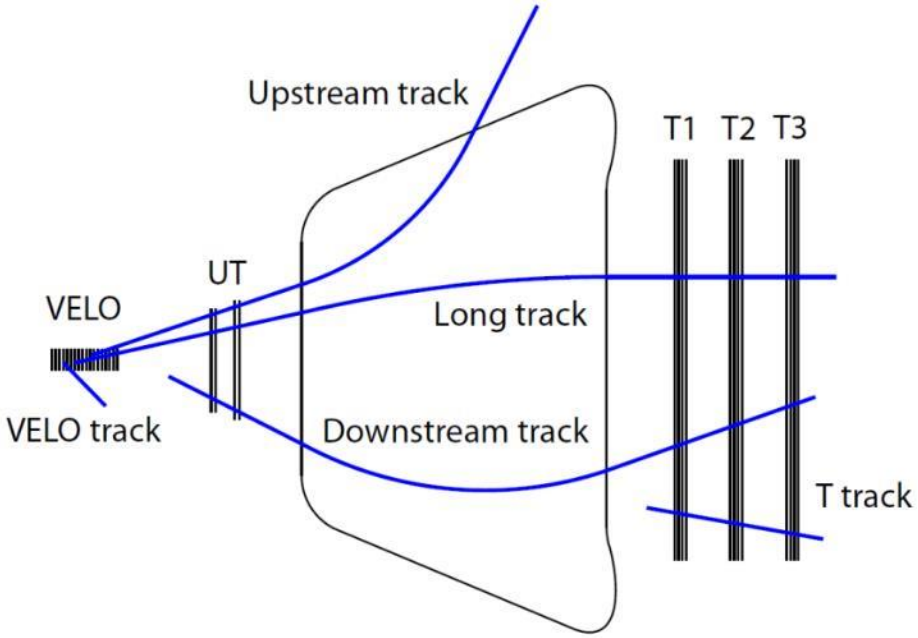
Keep triggerless readout

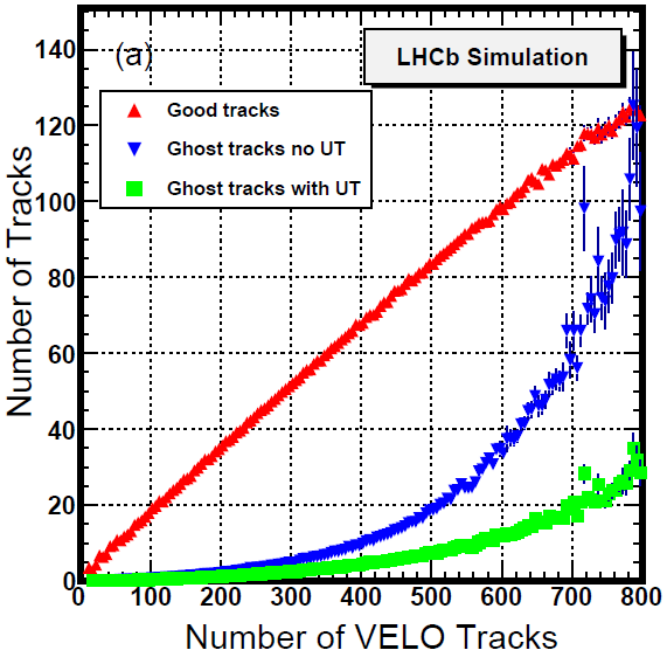
Additional Tracking stations

UT R&D Project

UT In The LHCb Tracking System

- Provide fast estimates of momentum in the software trigger.
- Reduce ghost rate in the long tracks.
- Increase reconstruction efficiency of long lived particles: e.g. $K_s^0 \rightarrow \pi^+\pi^-,\ \Lambda \rightarrow p\pi^-$.





The UT General Data Flow

Distribute master CLK & TFC, send out & collect slow control data.

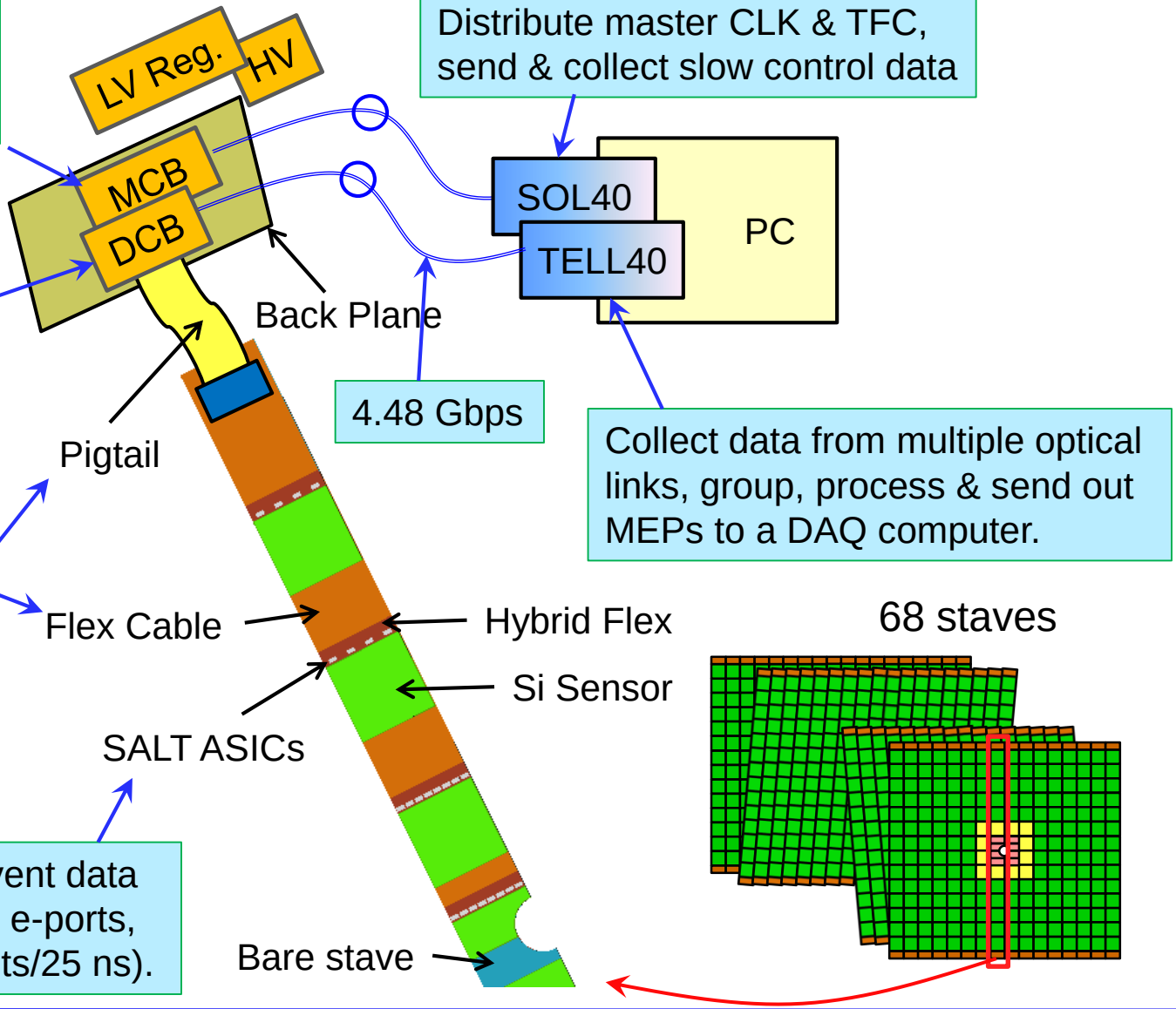
Partition a GBT 112-bit frame into sub-frames, 1 sub-frame / ASIC.

Carry 320 Mbps SLVS e-link signals & 100 kbps I^2C signals.

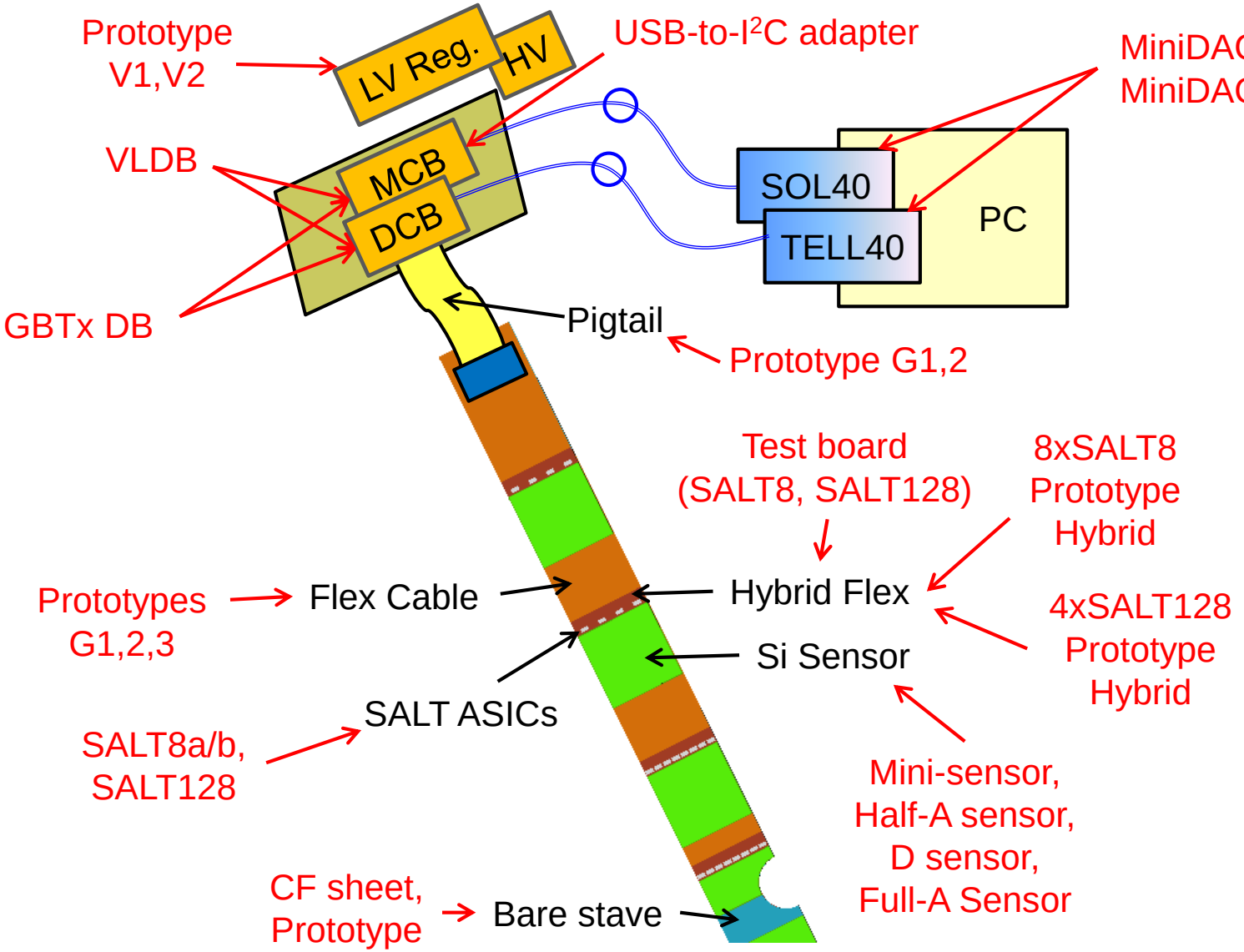
Digitize signal, pack event data & send out via multiple e-ports, 320 Mbps / e-port (8 bits/25 ns).

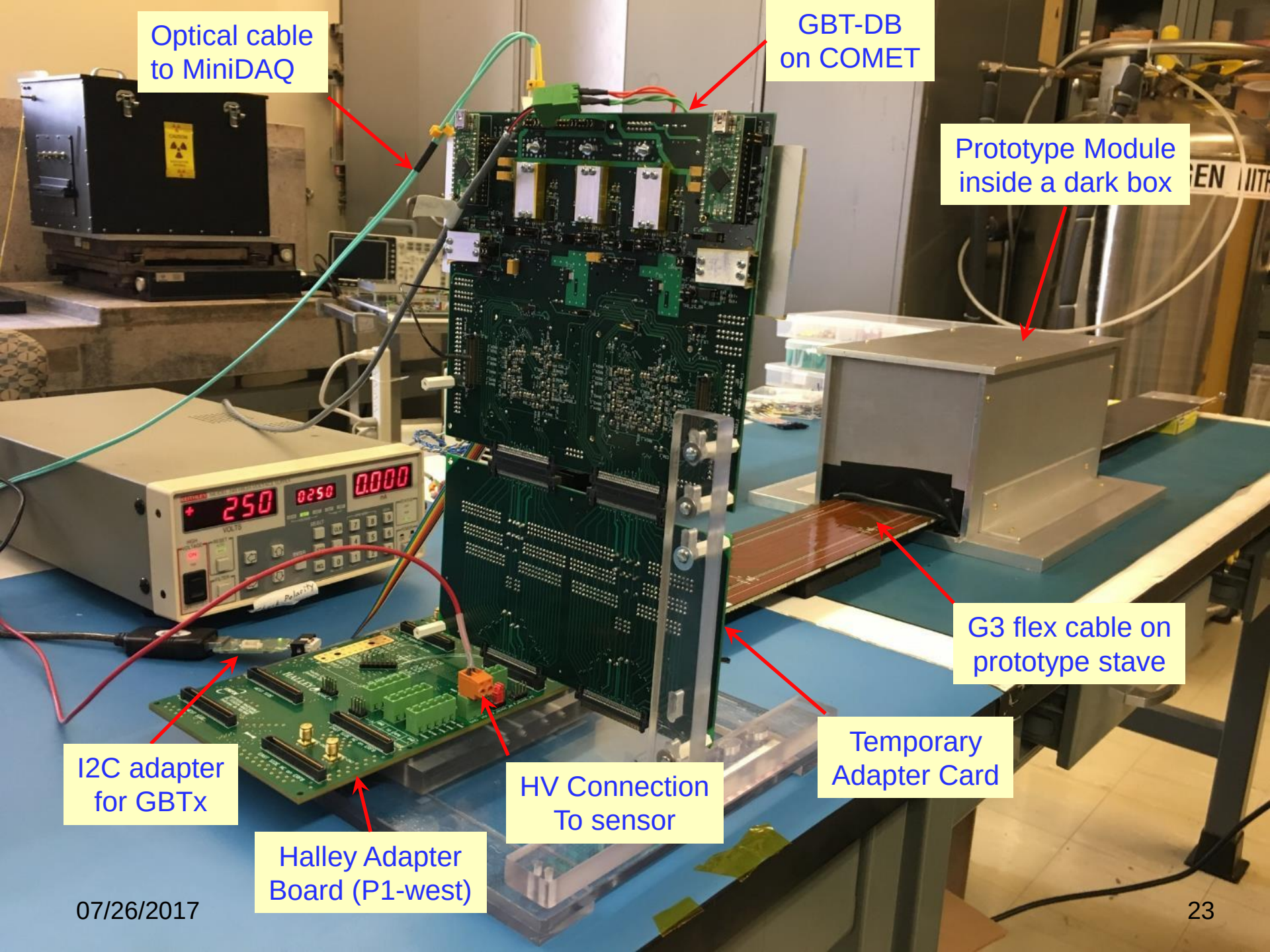
Distribute master CLK & TFC, send & collect slow control data

Collect data from multiple optical links, group, process & send out MEPs to a DAQ computer.



The UT Slice System

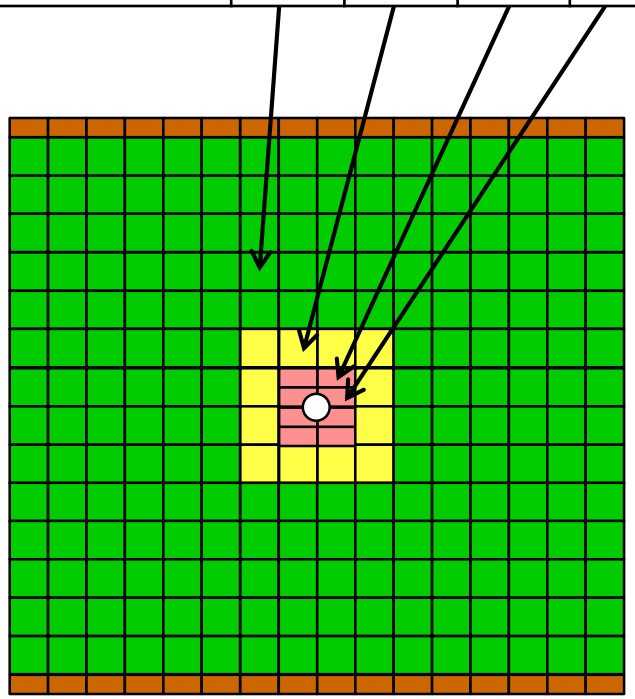



Optical cable to MiniDAQ
GBT-DB on COMET
Prototype Module inside a dark box
G3 flex cable on prototype stave
Temporary Adapter Card
HV Connection To sensor
I2C adapter for GBTx
Halley Adapter Board (P1-west)

Silicon Sensor

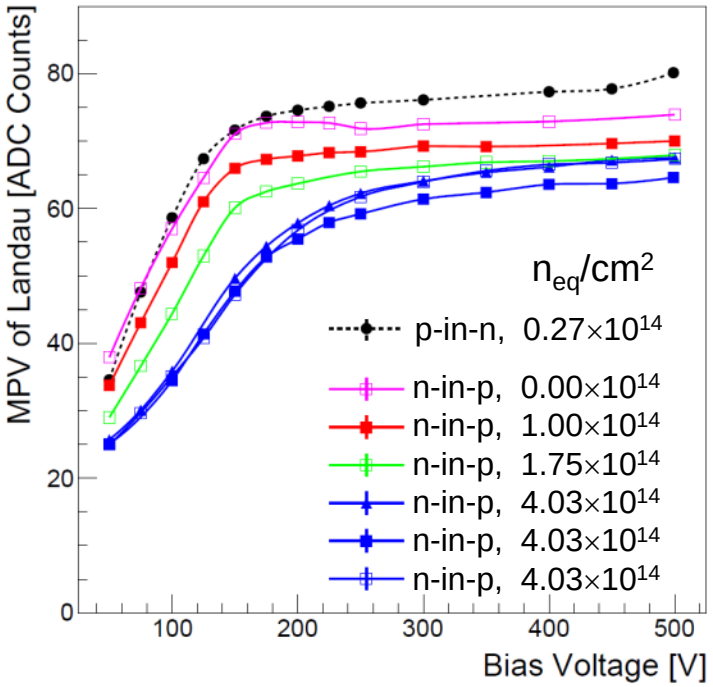
Silicon Sensors

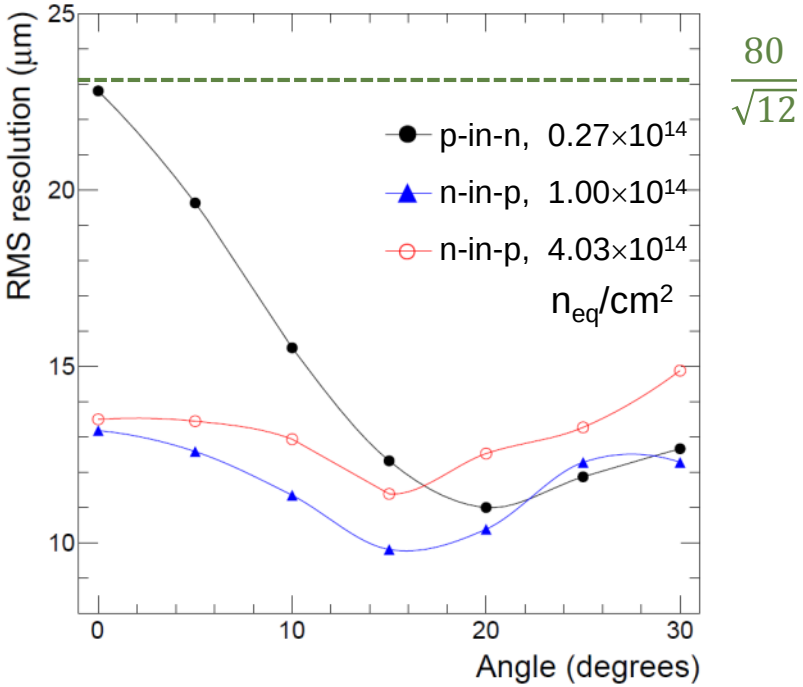
Sensor	A	B	C	D
Pitch (μm)	187	94	94	94
Length (mm)	98	98	49	49
Strips/sensor	512	1024	1024	1024
Number	888	48	16	16



- Silicon strip sensors, finer granularity in the central region, <2% strip occupancy.
- Four different types of sensor: 97.5×99.5 mm^2 (A & B), half length (C & D).
- Strip pitch187, 94 μm, Guard rings 800 μm. Wafer resistivity 3-5 KΩ•cm. Per strip capacitance ~2-12 pF.
- The inner most sensor receives ~5×10^{14} $n_{eq}cm^{-2}$ radiation fluence for 50 fb^{-1}. The inner-most of A type receives ~ 1/20.
- Most sensors (92%) are A-types, p^+-in-n technology (aka n-type), 320 μm thick. B/C/D/ sensors are n^+-in-p type, and thinned to 250 μm. A-sensors of the central staves may be p-type to avoid different signs of HV on the same stave.
- Sensors are biased from front-side HV contact, up to 500 V. The full depletion voltage is ~200 V.

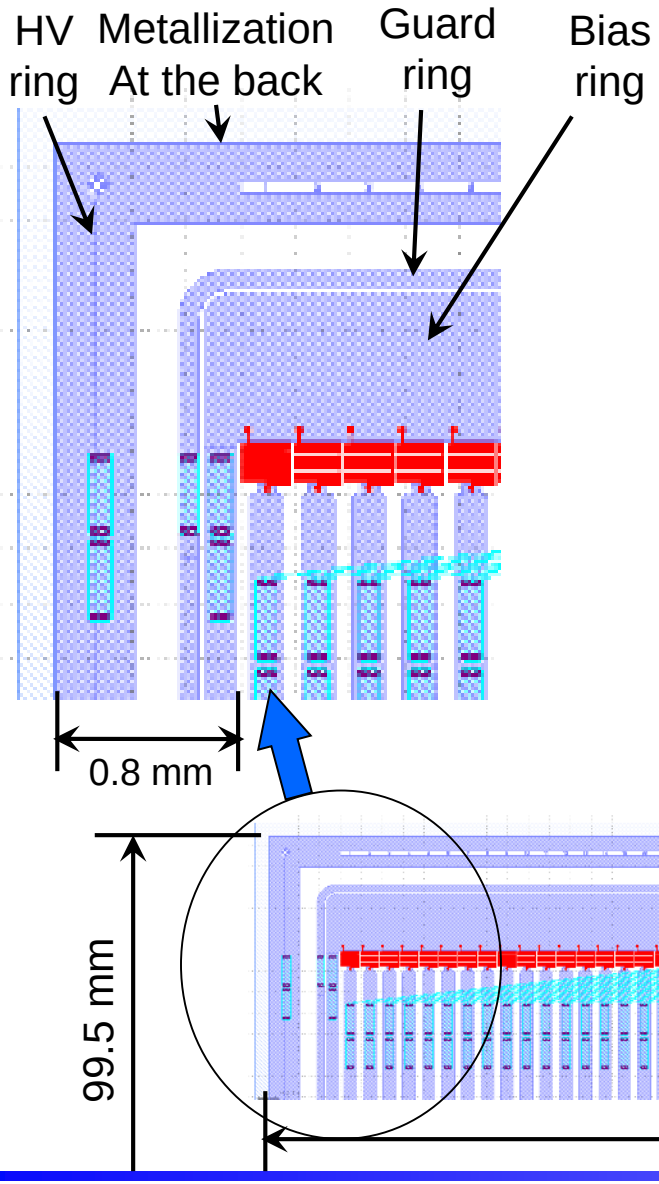
Sensor Performance In Test Beam





- For the n^+-in-p sensors, there is a gradual loss in total charge collected with increased radiation dose.
- All sensors reach plateaued @ 300-400V, S/N rate >~ 15. They should be efficient after 50 fb^{-1} running (5×10^{14} n_{eq}/cm^2).
- More charge sharing at normal incidence for irradiated n^+-in-p sensors.

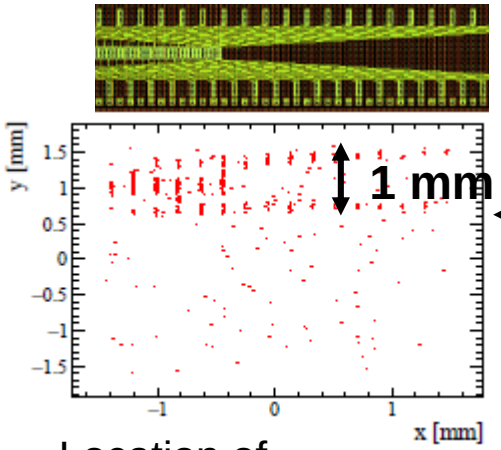
Sensor Layout



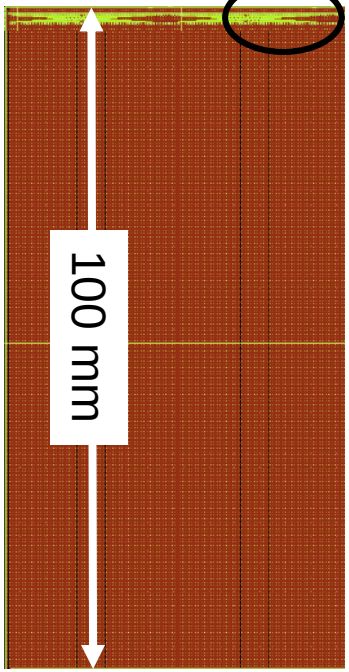
- Strip pitch of type A sensor is 187 μm, larger than the pitch of input pads on the SALT chip (80 μm).
- Embedded pitch adapters is implemented to match the two. There are also 4 ground pads per 128 strips.
- Strip pitch of types B/C/D (94 μm) is close enough. However, we still need to conclude whether the ground pads are necessary, before deciding on pitch adapter.

Inefficiency In The PA Region

- Very local to the Fan-In PA region, between adjacent strips where double-metal crosses.
- This region is mostly covered by the sensor overlap (in Y)
- For n-type sensors, the inefficiency disappears after irradiation.

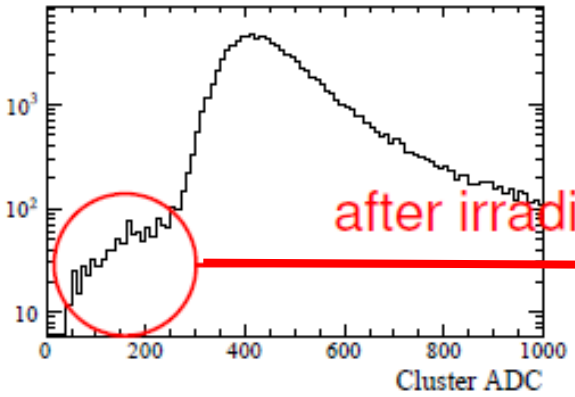


Location of missed hits

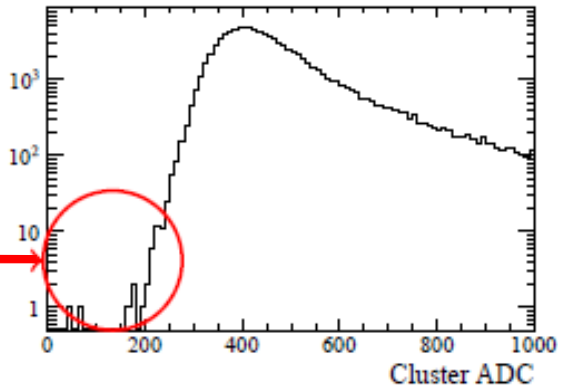


½ width A-type

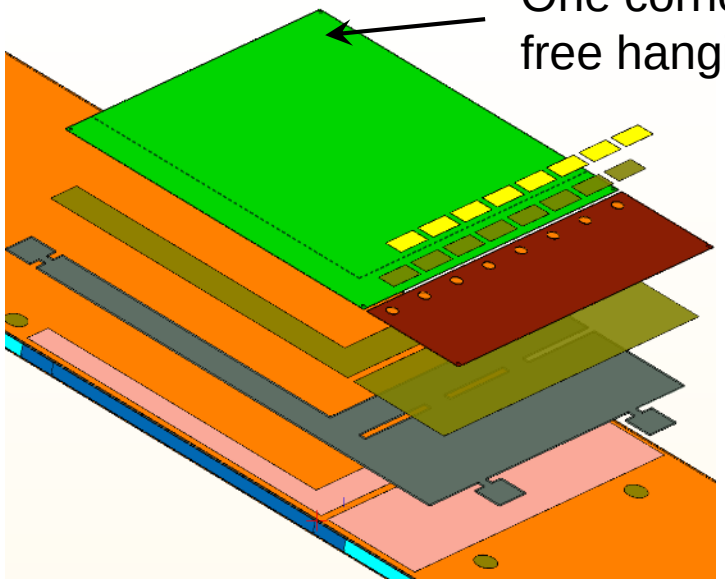
Before irradiation

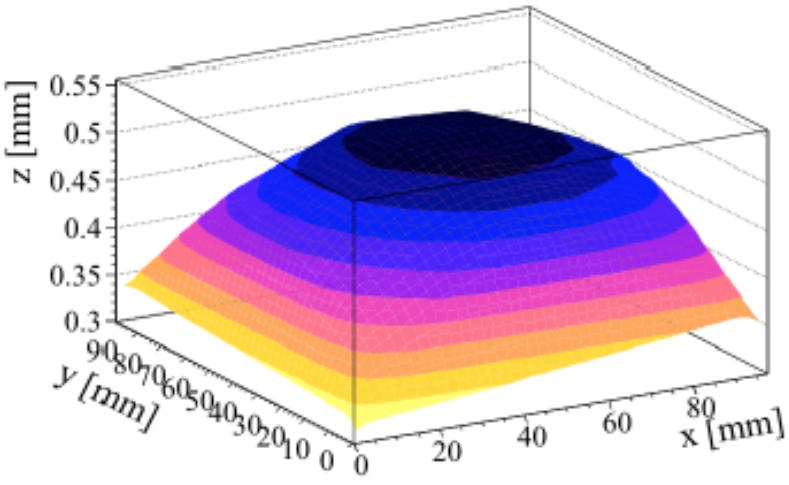


After irradiation



Sensor Bow

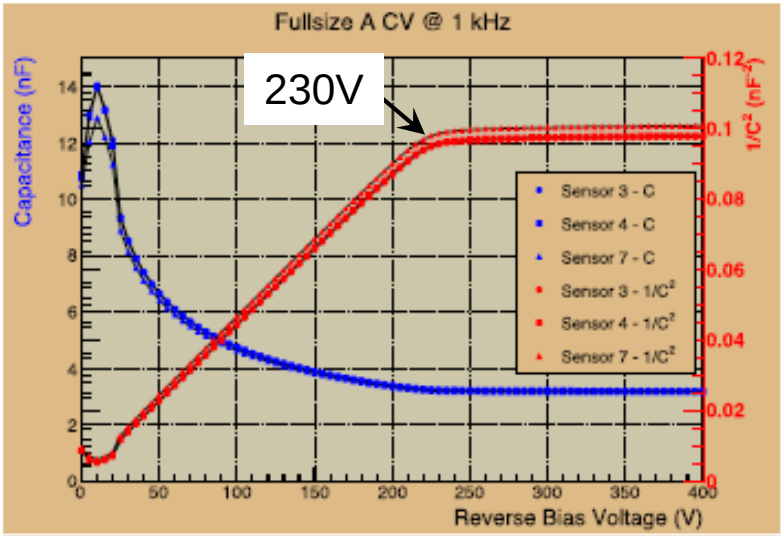




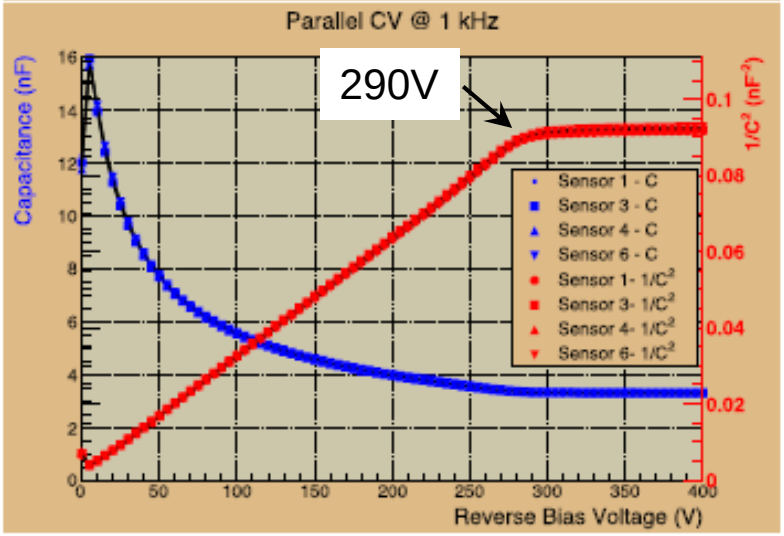
- On UT module the sensor is glued at two edges. One corner is free hanging. This is to avoid over-constrain.
- We require that that sensor bow to be < 250 μm.
- It is measured on 7 out of 10 full size A sensors with a SmartScope. They have consistent bow up in the center ~100 – 200 μm.
- Nevertheless, the corner will be protected, maybe with silicon.

CV Curve & Depletion Voltage

- The sensors are characterized on a probe station.
- CV response @ 1 kHz is a common way to determine the depletion voltage.
- Full size prototype A sensors have consistent depletion voltages: ~230V for n-type sensor, ~290V for p-type sensor.



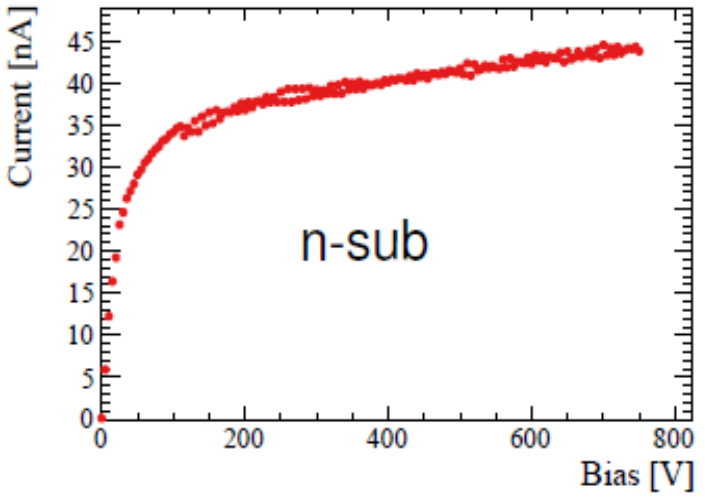
n-substrate

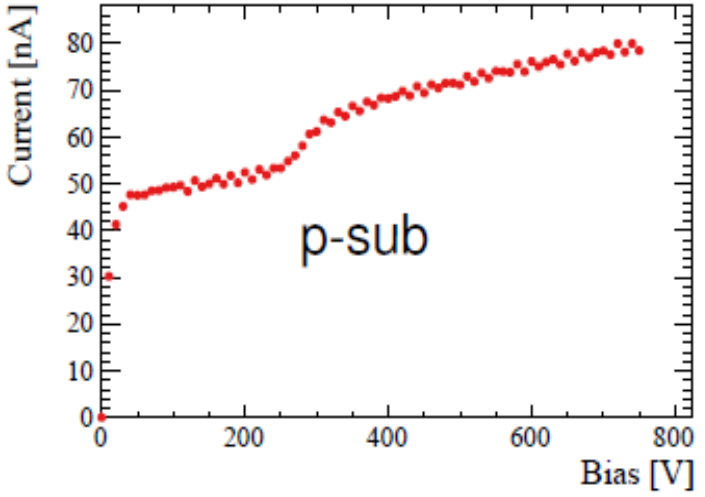


p-substrate

IV Curve & Breakdown

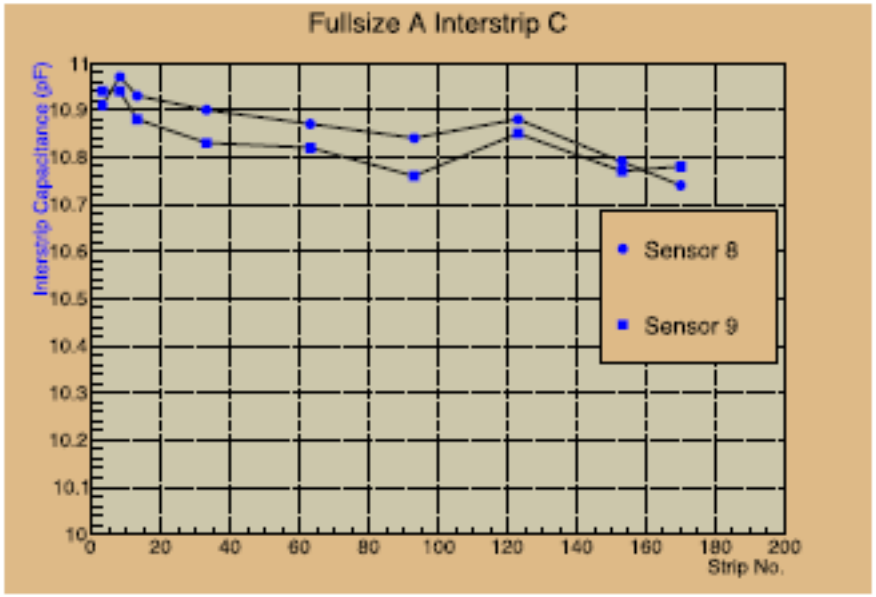
- n-substrate current ≈ 40 nA at depletion at room temperature
- p-substrate ≈ 70 nA
- Linear increase after; no sign of “soft breakdown”
- Three minis from one wafer breakdown at low voltage, one other at ≈ 700 V





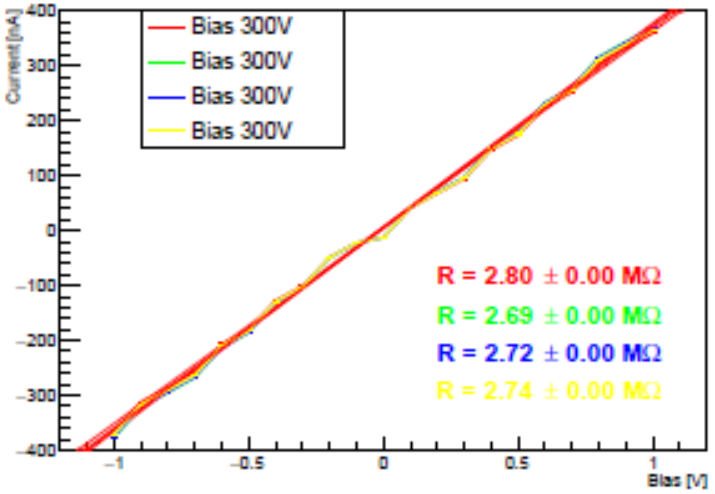
Inter-Strip Capacitance

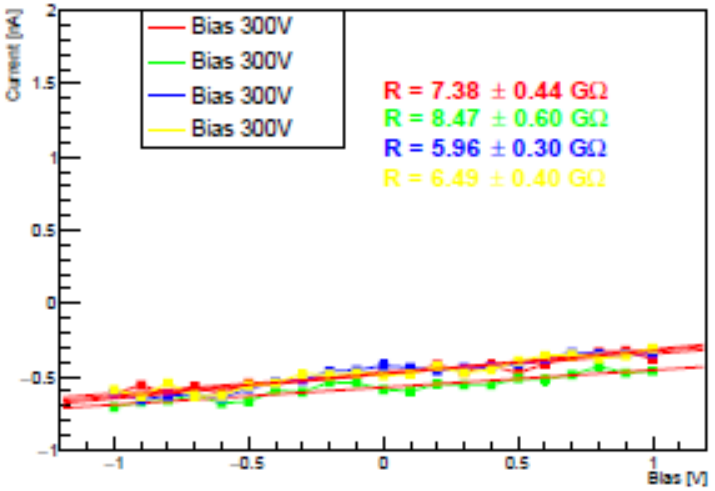
- Measured between AC contacts when sensor biased
- Corresponds to capacitance seen by electronics
- Similar result for p-substrate



Bias Resistance & Inter-strip Resistance

- Simultaneously measure bias resistance and interstrip resistance
- Difficult to precisely measure $R > 1\,\mathrm{G}\Omega$
- Meets specifications



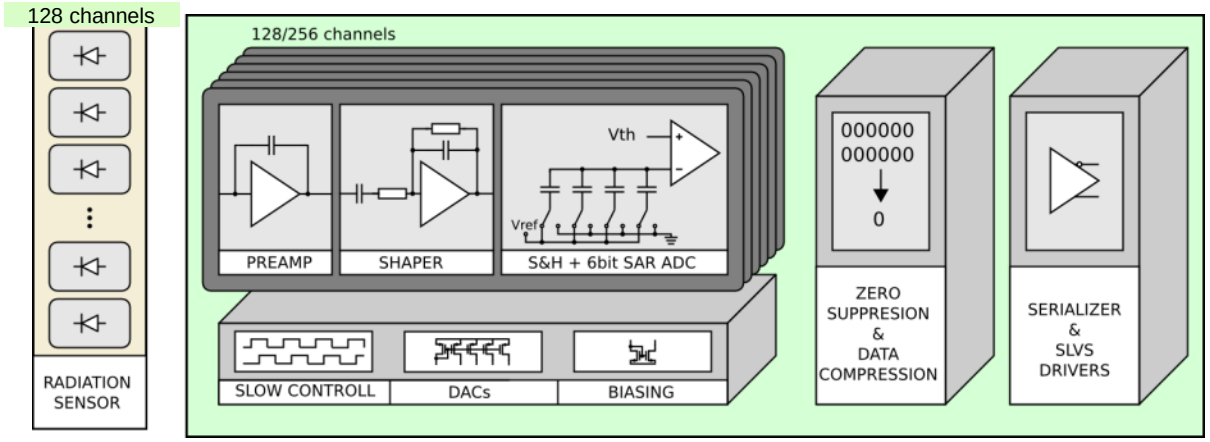


Sensor Status

- The majority of UT modules uses n-substrate A sensors. Thus the R&D program puts this n-type sensor at relatively higher priority, so that the time consuming module & stave construction can start soon.
- The latest n-type sensors are satisfactory. So the production will start soon. The delivery is expected to start at the end of 2017.
- There is at least another test beam for the p-type sensors before we can finalize the design.
- All the sensors will have visual inspection, IV, CV characterization. On selected samples, we will measure sensor bow, inter-strip capacitance, bias resistance & inter-strip resistance.

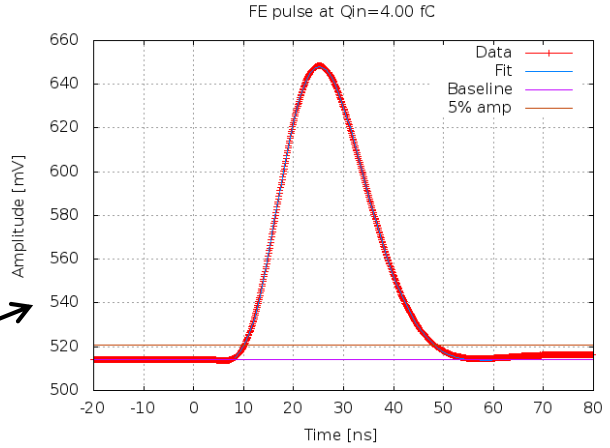
SALT ASIC

Front End ASIC - SALT



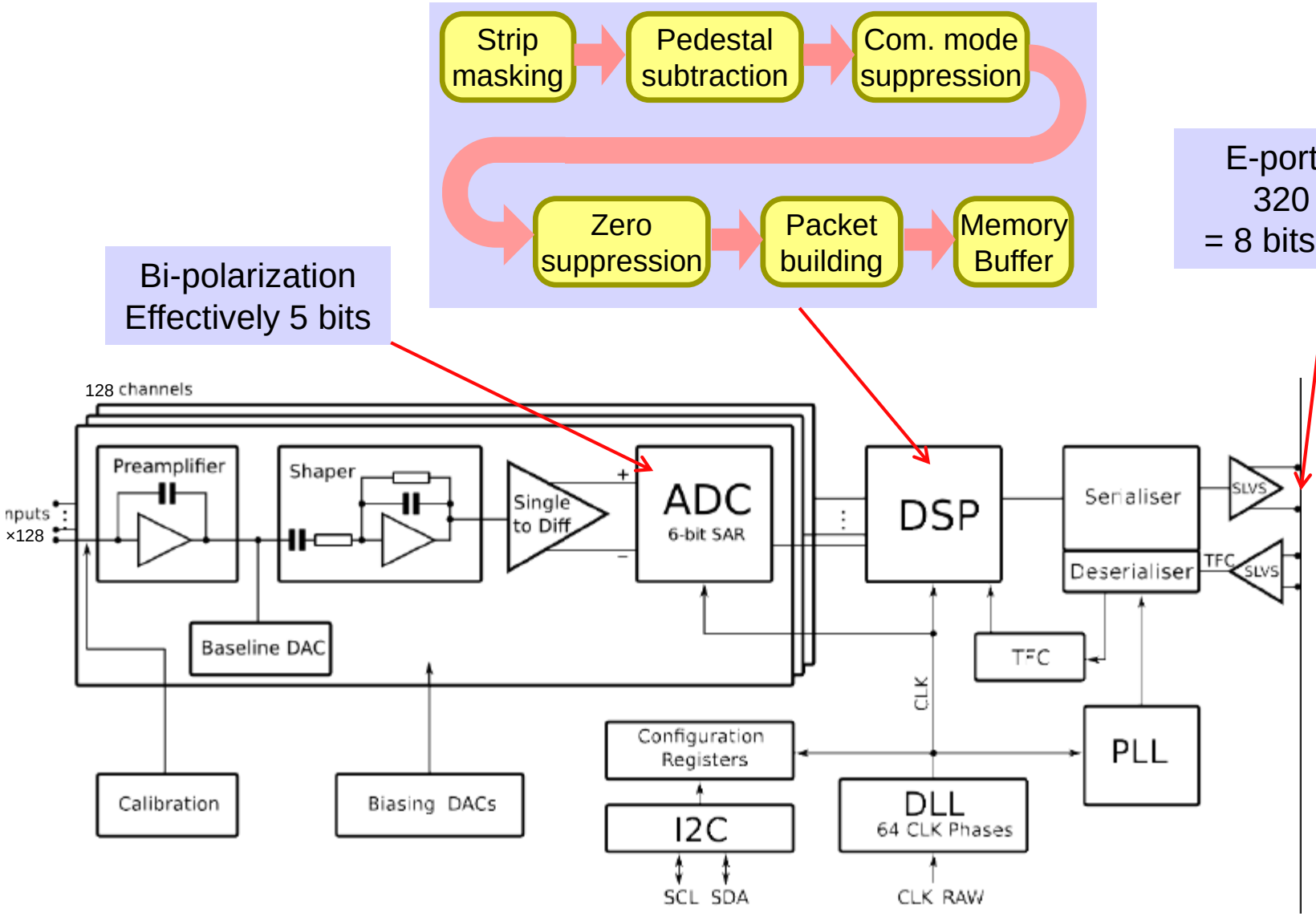
SALT – custom design for UT.

Preamp-shaper prototype



- CMOS 130 nm technology (IBM, TSMC).
- 128 channels, per channel preamplifier & 6-bit ADC.
- Sensor capacitance 2-12 pF, AC coupled.
- Dynamic range ~ 30 ke, both input signal polarities.
- Noise: ENC ~ 1000 e @ 10 pF + 50 e / pF.
- Pulse shape: T_{peak} < 25 ns, short tail ~5% @ 25ns+T_{peak}.
- DSP functions: pedestal, common mode subtraction, zero-suppression.
- Serialization & data transmission via 320 Mbps e-ports.
- Power consumption < 6 mW / channel.

SALT ASIC

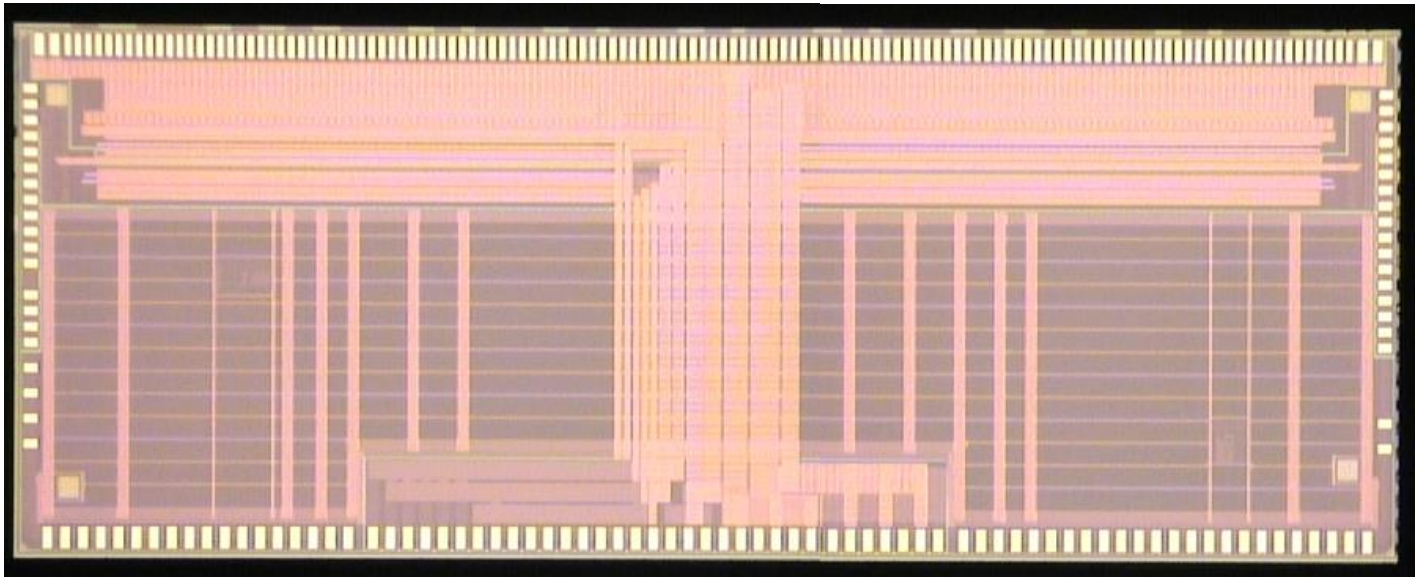

Strip masking
Pedestal subtraction
Com. mode suppression
Zero suppression
Packet building
Memory Buffer
Bi-polarization
Effectively 5 bits
E-port speed:
320 Mbps
= 8 bits×40 MHz
128 channels
nputs
×128
Preamplifier
Shaper
Single to Diff
ADC
6-bit SAR
DSP
Serialiser
SLVS
Deserialiser
TFC
SLVS
Baseline DAC
TFC
CLK
Configuration Registers
PLL
Calibration
Biasing DACs
I2C
DLL
64 CLK Phases
SCL SDA
CLK RAW

SALT ASIC Prototypes

Pads for sensor inputs & gnd

V3: 10900 × 4095 μm^2

Pads for debugging



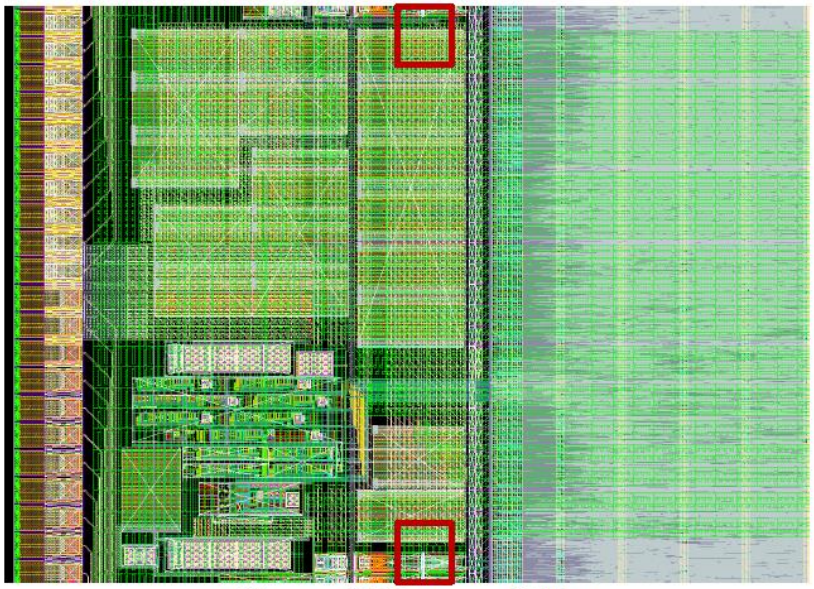
Pads for debugging

Pads for LV, GND, digital data etc

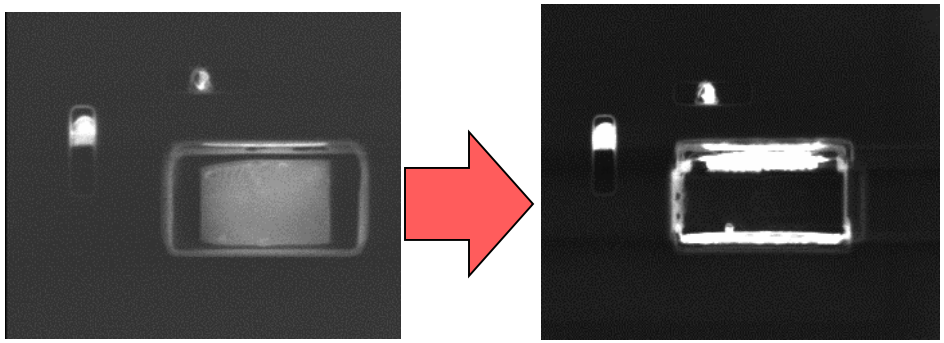
- Three prototype versions had been produced.
- The first 2 have only 8 channels and limited functions.
- The 3rd version has 128 channels. All major functions had been implemented.

SALT128 FIB Editing

- In the study of the power consumption, it was found that there is significant current leak in the analog domain (>200 mA extra).
- The source was eventually identified, and FIB editing was done on 5+8 ASICs. Several other issues disappeared after editing.
- Results shown here are from FIB edited ASICs.
- The leak was not caught in the checks before submission. This is quite alerting. Cautions will be taken to make sure that this will not happen again.

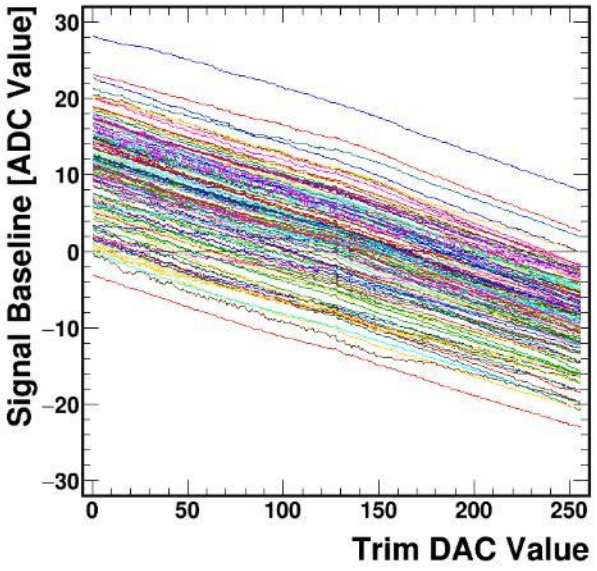


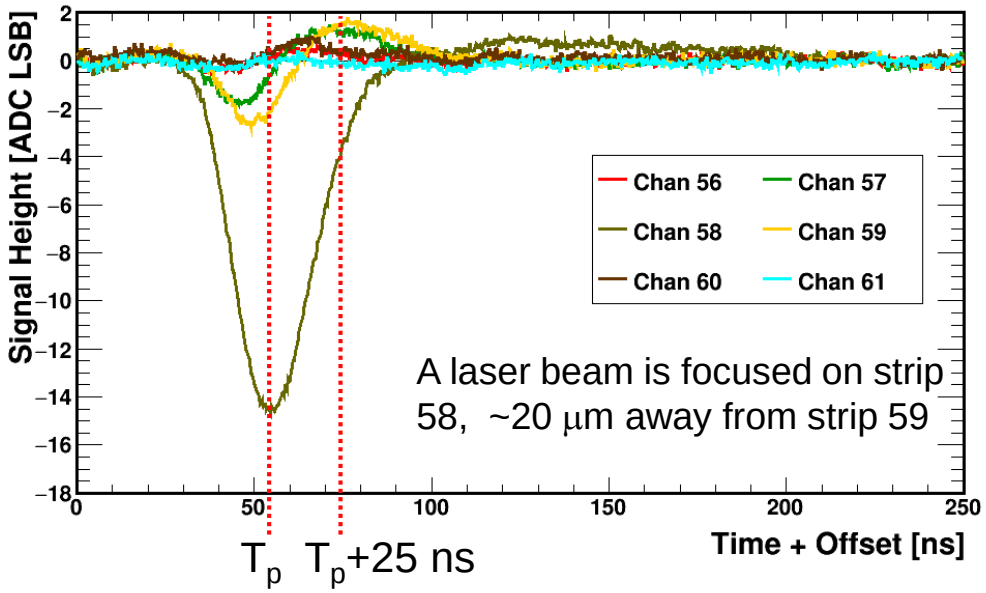
Two MET7 (copper) paths must be cut



Provided by AEG

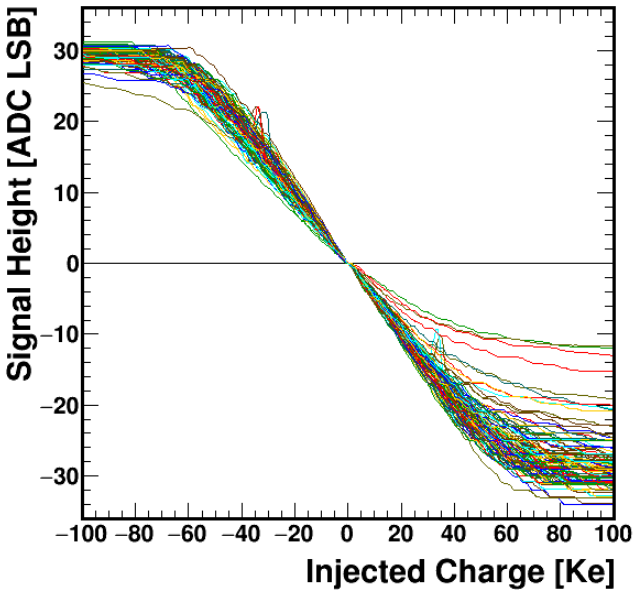
Performance of Ver1 SALT128

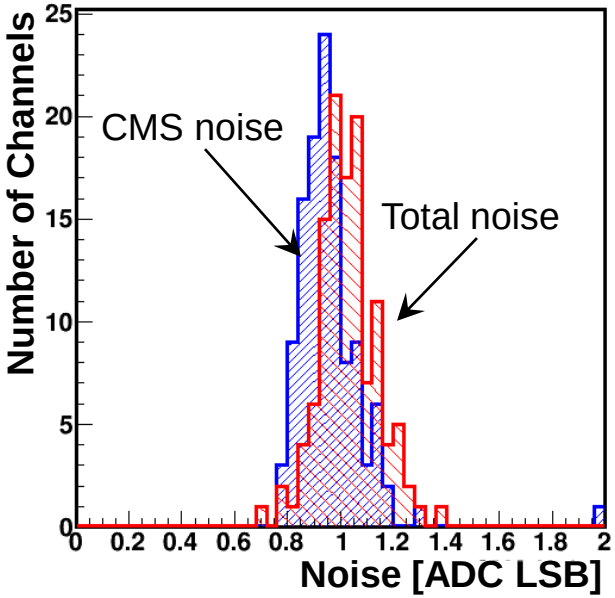




- Version 1 SALT128 works generally as designed.
- The trimDAC can be used to align the baseline of all channels. Uniformity of baseline needs to be improved, or the trimDAC range needs to be enlarged.
- In a test with a laser beam the pulse shapes are reasonable in the channel that receives signal and its adjacent channels.
- Signal height at T_p+25 ns (spill over effect) is too high. Adjusting electronics bias reduces this height. Uniformity is again an issue.

Gain Curve & Noise Performance





- Gain curves are obtained with internal test pulse generation. The main trend is as expected. But the polarity asymmetry and uniformity are not ideal.
- The total noise is ~1.02 LSB. In side ASIC common mode (CM) noise can be removed, which accounts for ~0.50 LSB in this test. The CM suppressed noise ~0.90 LSB, i.e. ~2000 ENC, which is significantly more than design goal (~1000 ENC).

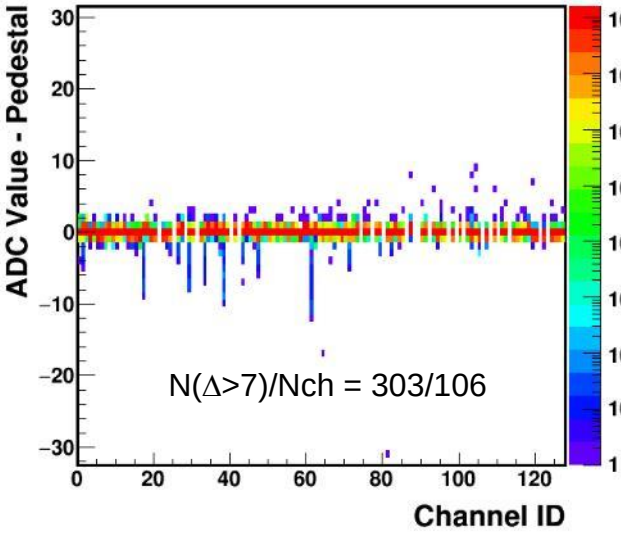
SALT Radiation Test

- SALT ASIC uses SAR (successive approximation) ADC, which is more vulnerable to radiation.
- At an earlier stage, a small chip (by IBM) that contains 8 ADC channels were tested. The SEU rate was found to be very small.

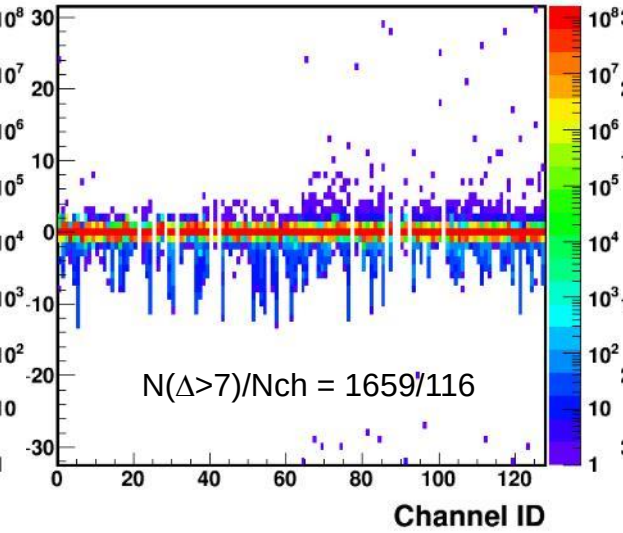
- With SALT128 more functions were tested in a proton beam.
- A few interesting features in the analog (mixed mode) domain were found, which lead to re-optimization, even redesign of certain parts.
- In the digital domain SEUs were observed in different parts, including configuration registers, TFC pipeline. TMR was implemented in most part. In the next SALT design the whole digital domain in triplicated.
- We did not observe current increase of TID or SEL effects. SEU in PLL was observed, but at very low rate.

ADC SEUs

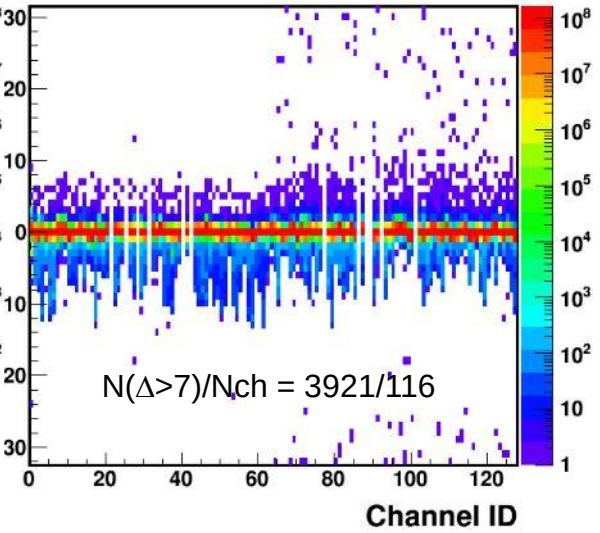
Run145749 $\mathcal{L}$ ~2.1u



Run150520 $\mathcal{L}$ ~12.5 u



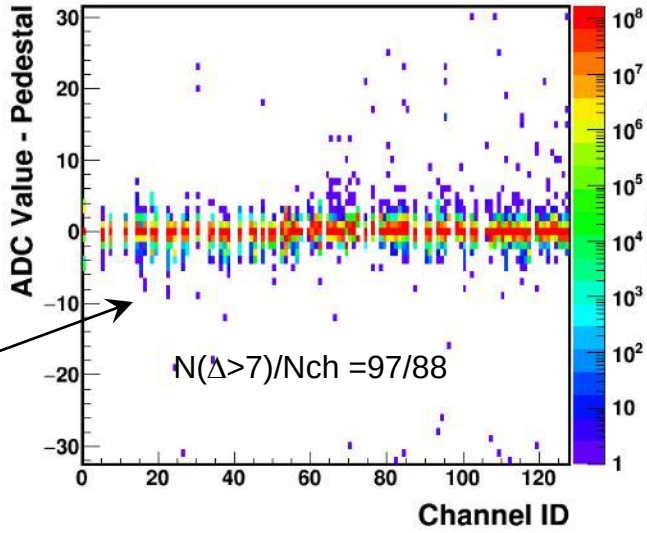
Run154615 $\mathcal{L}$ ~45.8 u



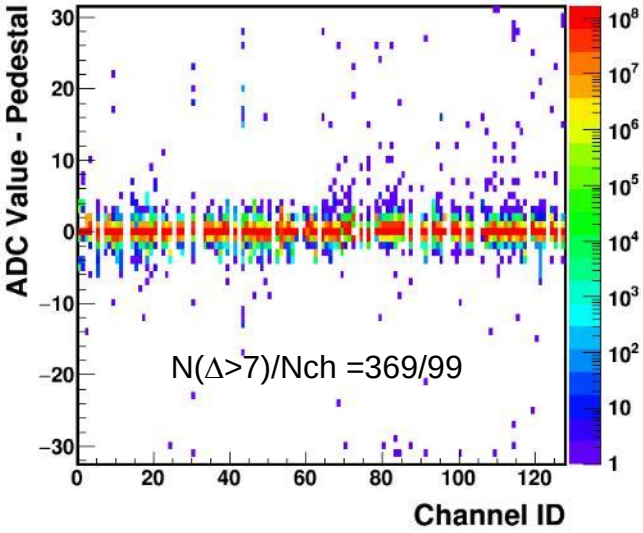
After ~10 Mrad

Much less after 10 Mrad

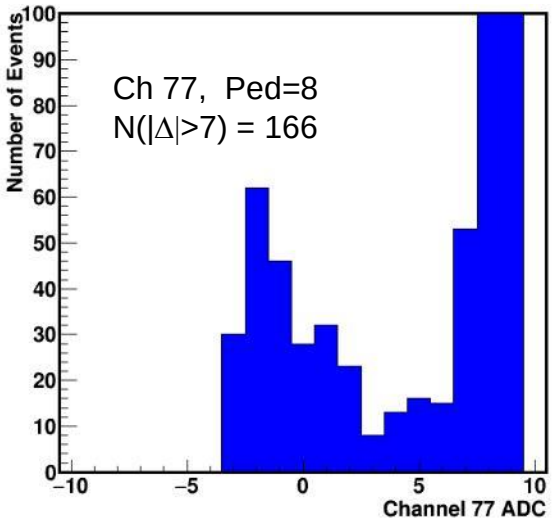
Run191254 $\mathcal{L}$ ~55.4 u

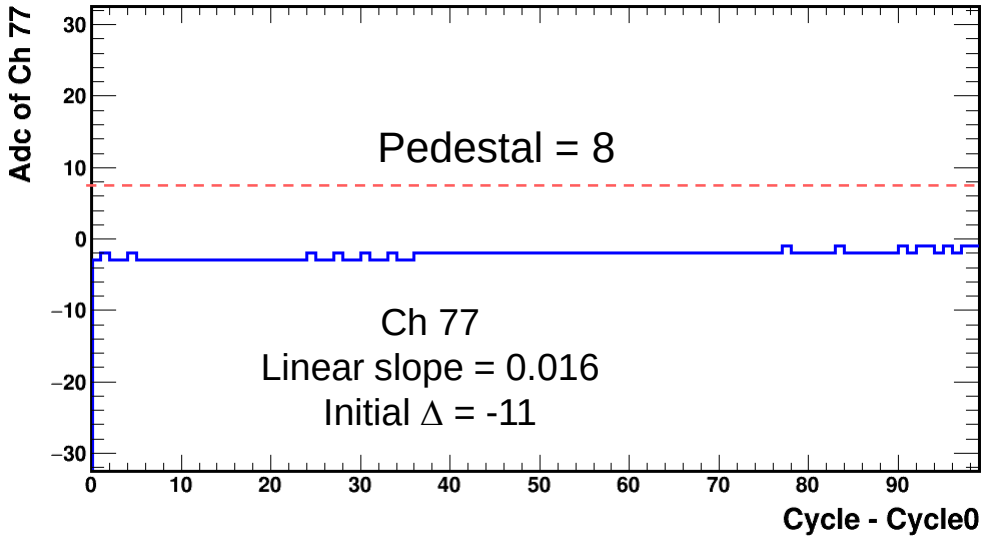


Run191927 $\mathcal{L}$ ~55.0 u



Consecutive ADC SEUs





T = cycle x 1.6 μs.
Only 1st 100 events are shown

- In many cases, the ADC value was offset by a significant value.
- Then in the consecutive events the value continues to be high and gradually returns to base.
- The time constant is on the order of 1 ms.
- In post-irradiation study it is found that the Krummenacher feed-back in the preamplifier may produce such phenomenon.

Status of SALT

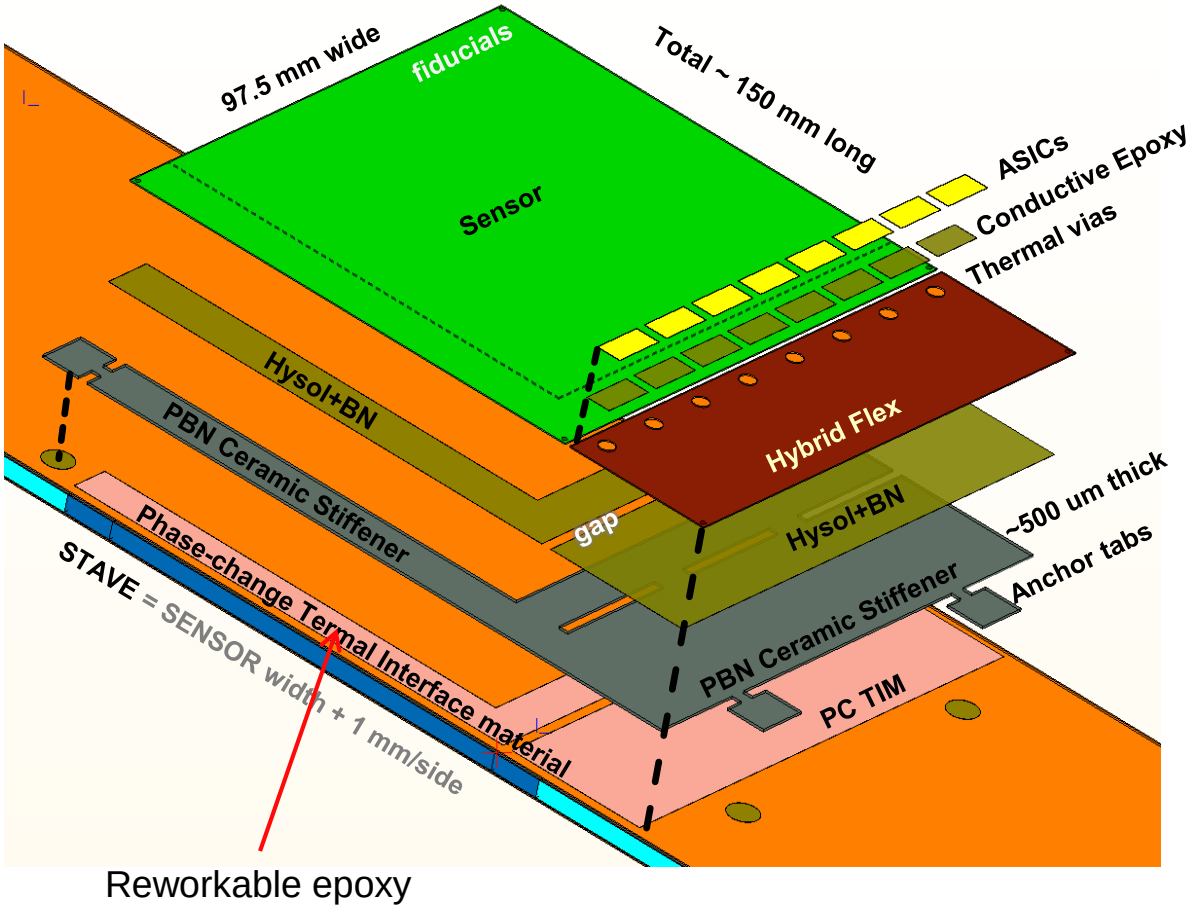
- A new revision of the SALT design is in the process of submission.
- All the issues that we found on bench test, laser test and radiation test had been addressed.
- New ASICs should be available around the end of September.
- If all issues are solved and no new issues surface, then this one is considered the pilot run. The ASICs will be used immediately for module production.
- ASICs from the real production will be first tested on wafers before dicing; After the selected good ones are mounted on the supporting hybrid flex circuitries, burn-in tests will be performed.

Modules & Staves

UT Module (Exploded View)

Sensor: –5°C, ΔT=5°C

Bias: up to 500 V

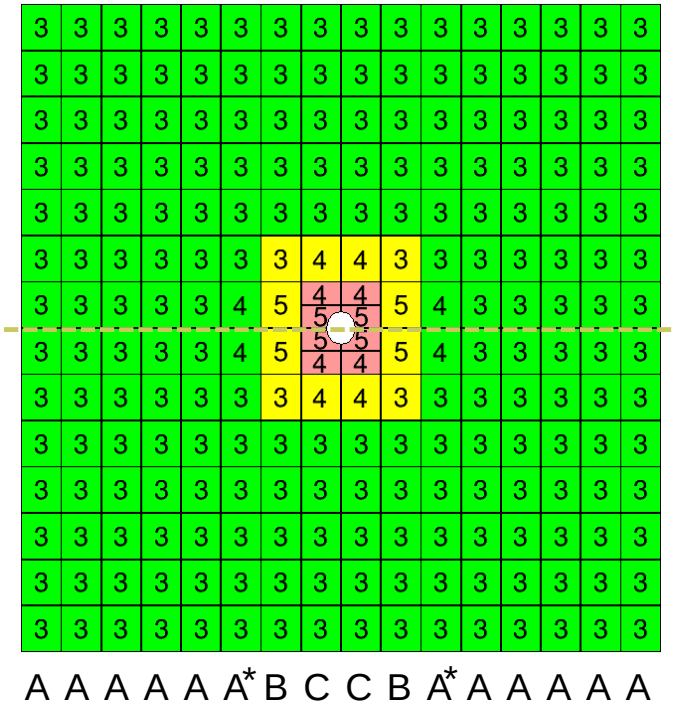


- Provide connection between ASICs & flex cable.
- Protect wire bonds during testing and handling.
- Maximize heat transfer from ASICs to stave, minimize heat transfer to sensor.
- Isolate sensor bias from stave facings (ground).
- Stiffener CTE matches to Si. Not to over-constrain sensor, allows for bow.

Active E-ports Per ASIC

ASICs / sensor
Green: 4, Yellow: 8, Red: 8

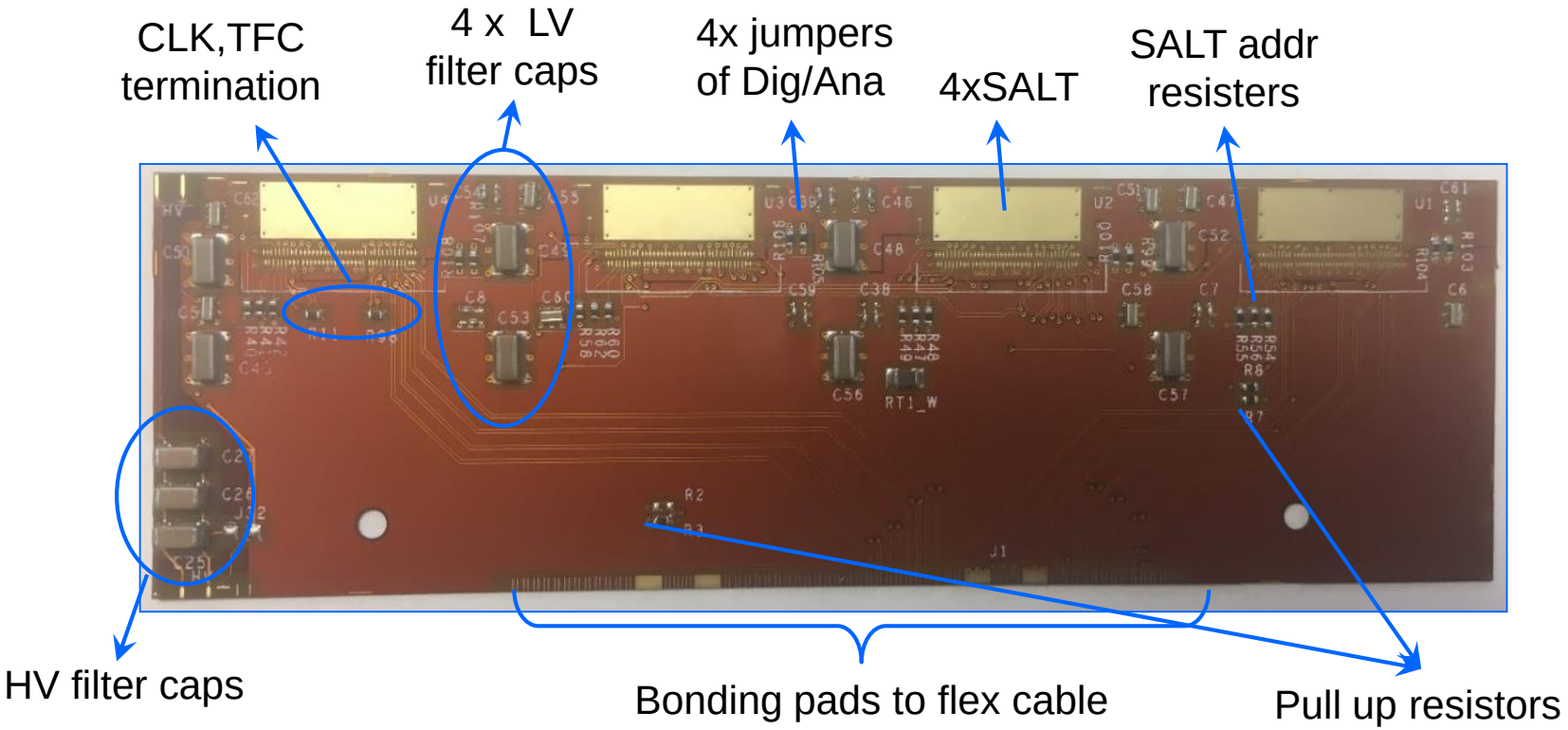
Value indicates # of e-ports/ASIC



Works up to $\mathcal{L}=2.8\times10^{33}$ cm^{-2}s^{-1}

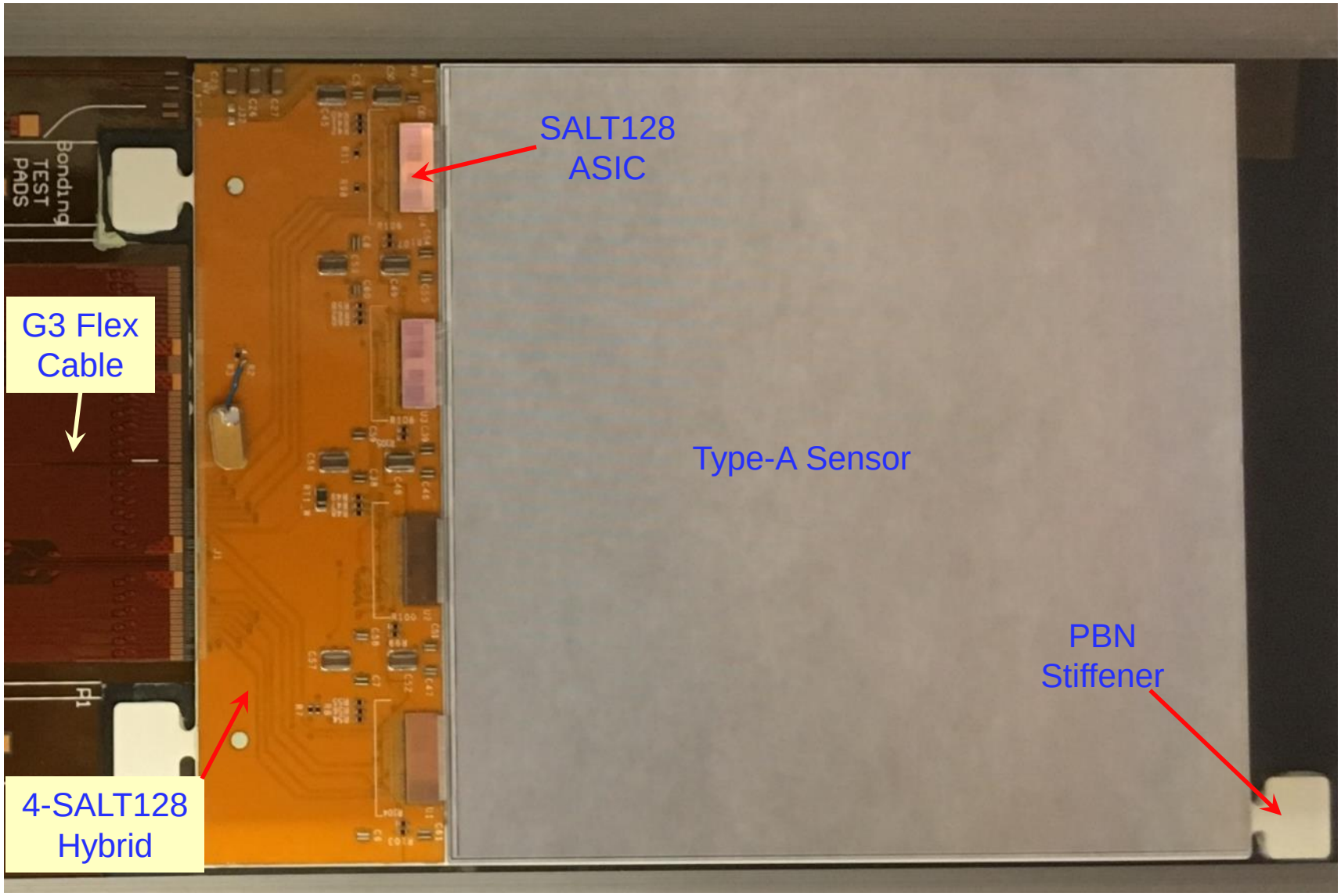
- The hit density is much higher at the center close to beam.
- Sensors have finer granularity at the center. The 20 sensors/plane at the center need 8 ASICs / sensor, whereas the majority need 4 ASICs / sensor.
- Even so the ASICs at the center has more hit data to be shipped out. They need 4 or 5 e-ports / ASIC @ 320 Mbps rate. The majority needs only 3 / ASIC.
- SALT has 6 data e-ports in design. The number of active e-ports is configured via ECS.
- More e-ports are connected on module & stave. The end-of-stave electronics will connect only the useful ones.

Prototype 4-ASIC Hybrid Flex

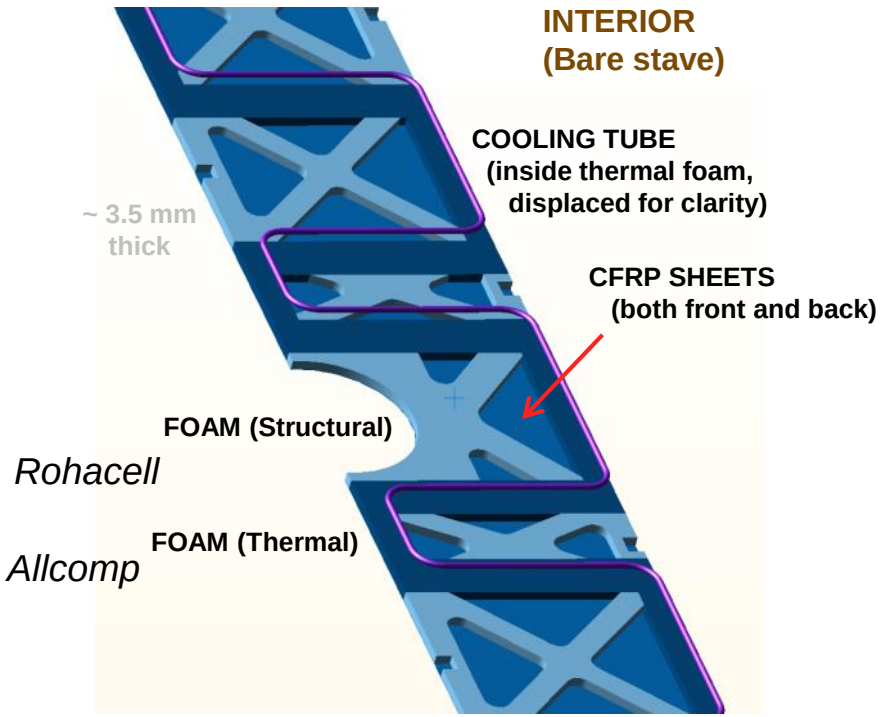


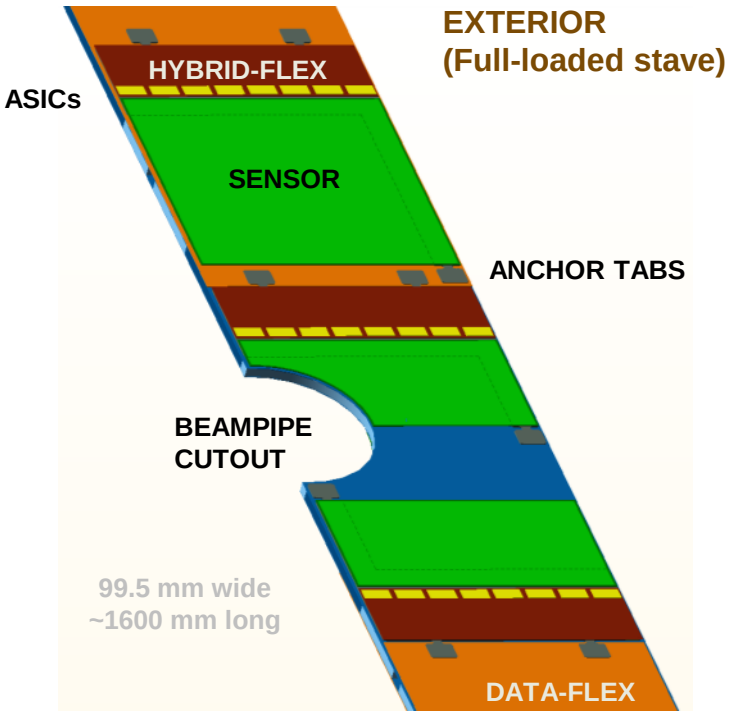
- Hybrid flex has 4 layers: signal/gnd/Vcc/signal, 466 μm thick.
- Works fine in the slice system. Need to validate the filtering caps with the new SALT ASICs. Production readiness review on January 2018.
- Optimize production panel layout, for cost saving and testability.
- Hybrid flex for 8 ASICs has no space between ASICs. Width is increased by 2 mm to 99.5 mm for HV connection.

Prototype Type-A Module



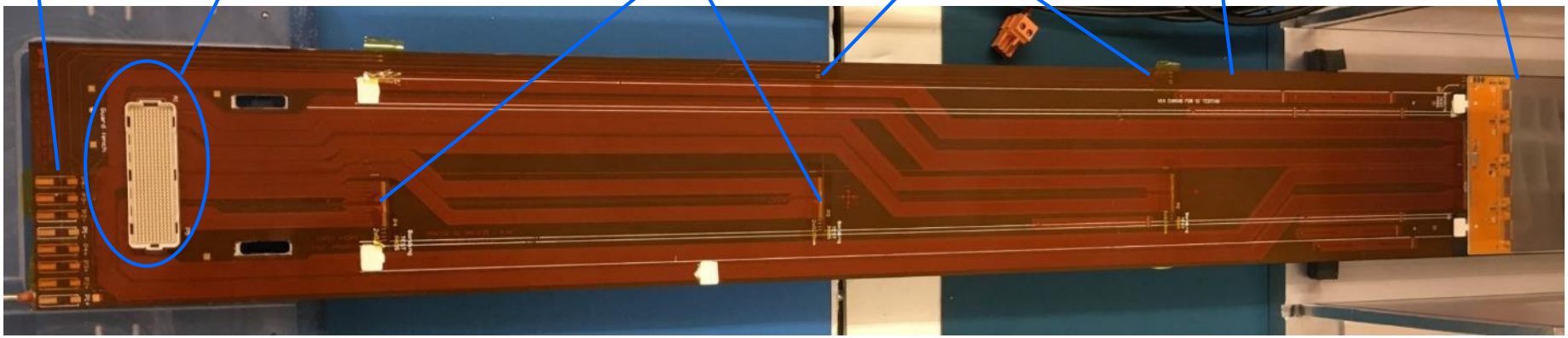
UT Stave Structure





- 2 CFRP (Carbon fiber reinforce polymer) face sheets attached to foam core, forming a sandwich structure, all epoxy construction.
- Ti cooling tube is embedded in the thermal foam: 2.275 mm OD, 135 μm wall.
- Cooling tube in “snake” shape to make run under all ASICs.

Generation 3 Flex Cable

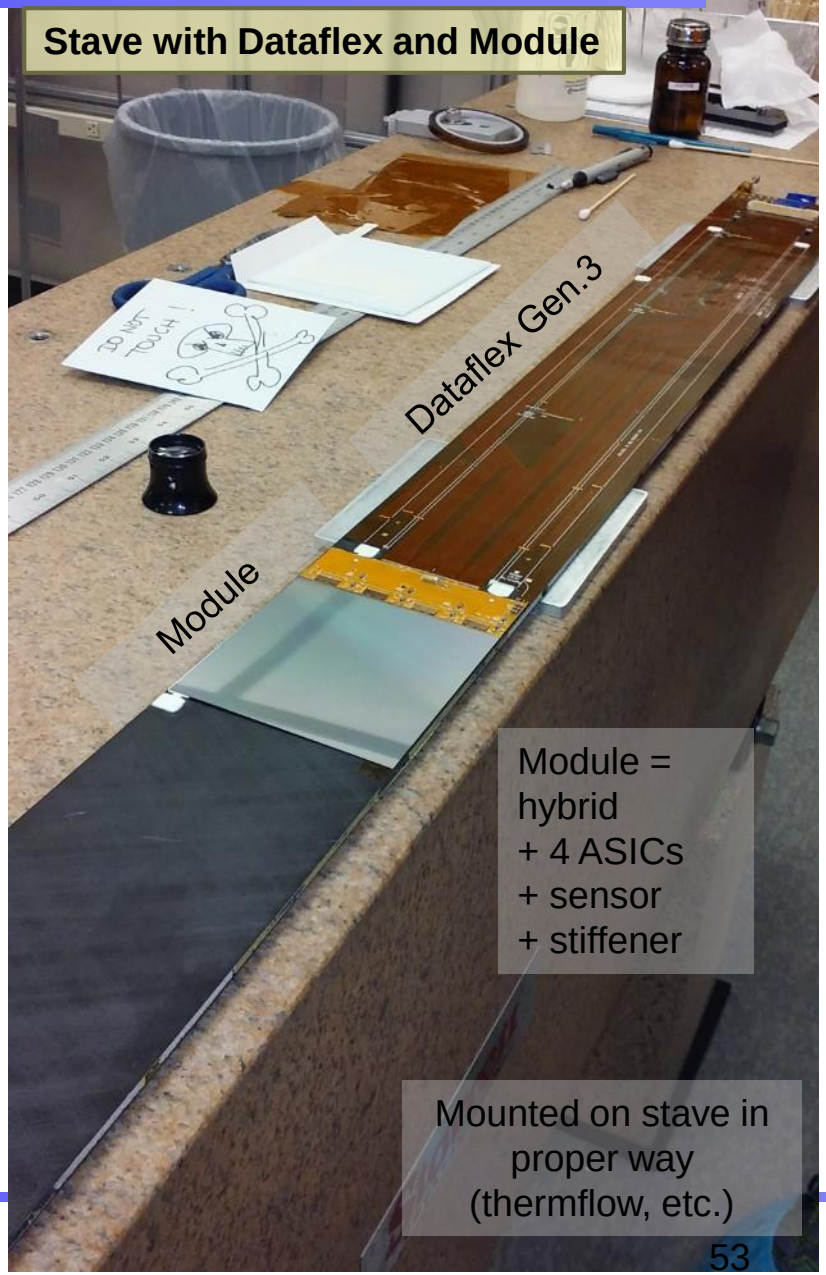


- Three layers: signal (22.5 μm), LV (34 μm), signal (22.5 μm), HV traces on each layer. Total thickness 425 μm
- Main concerns: overall material, LV/gnd drop, signal line impedance, production yield.
- Gen3 prototype had been thoroughly tested alone and in the slice test system.
- Production readiness review at the end of August this year.

Module Construction & Mounting

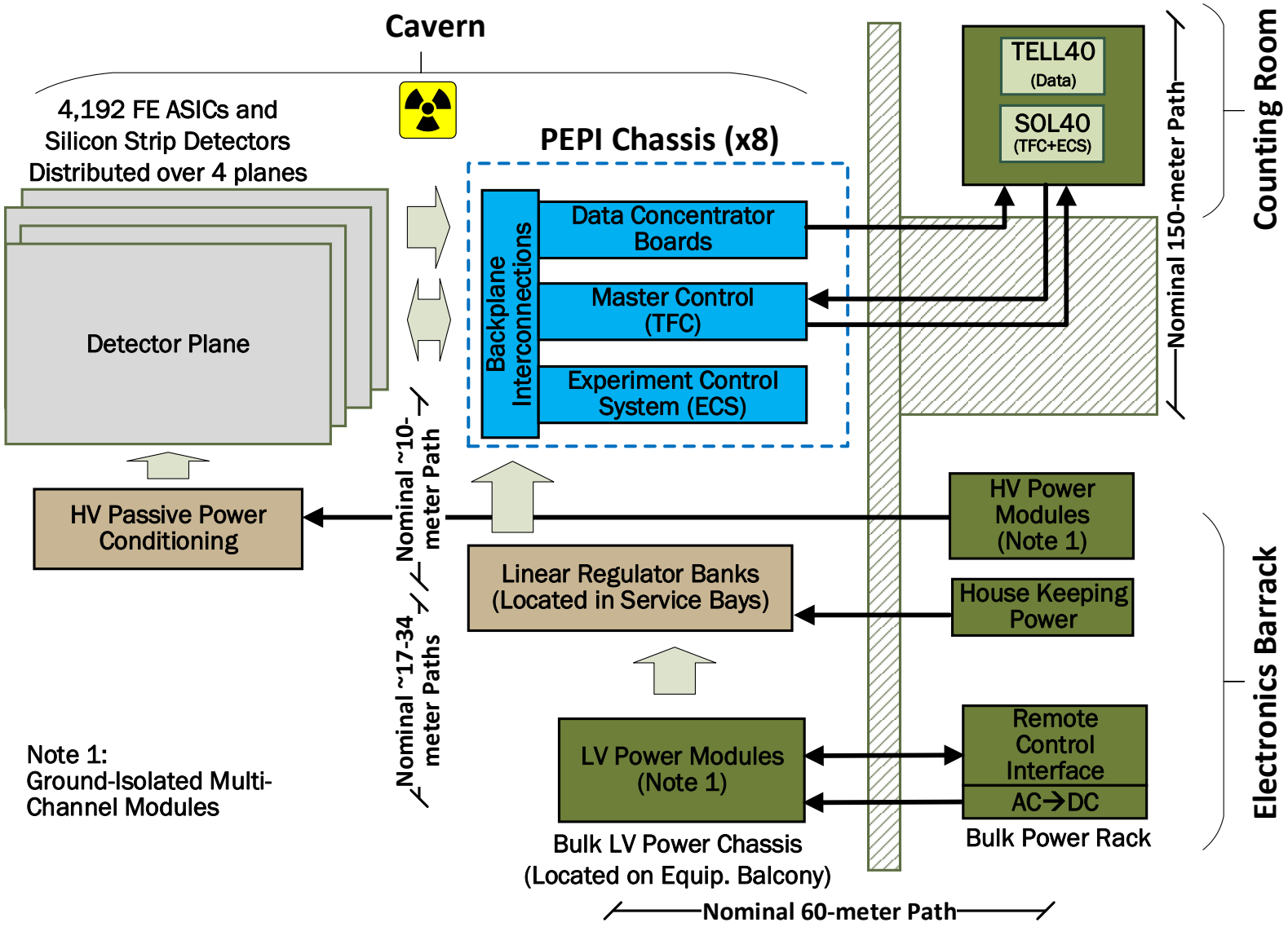
4-ASIC module and dataflex mounted on stave (*by hand*) for SALT128 Slice Test

…also have removed a module successfully



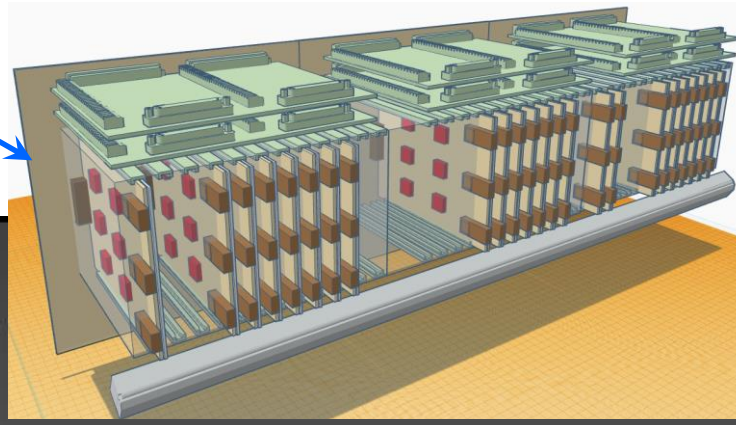
Peripheral Electronics & Other Supports

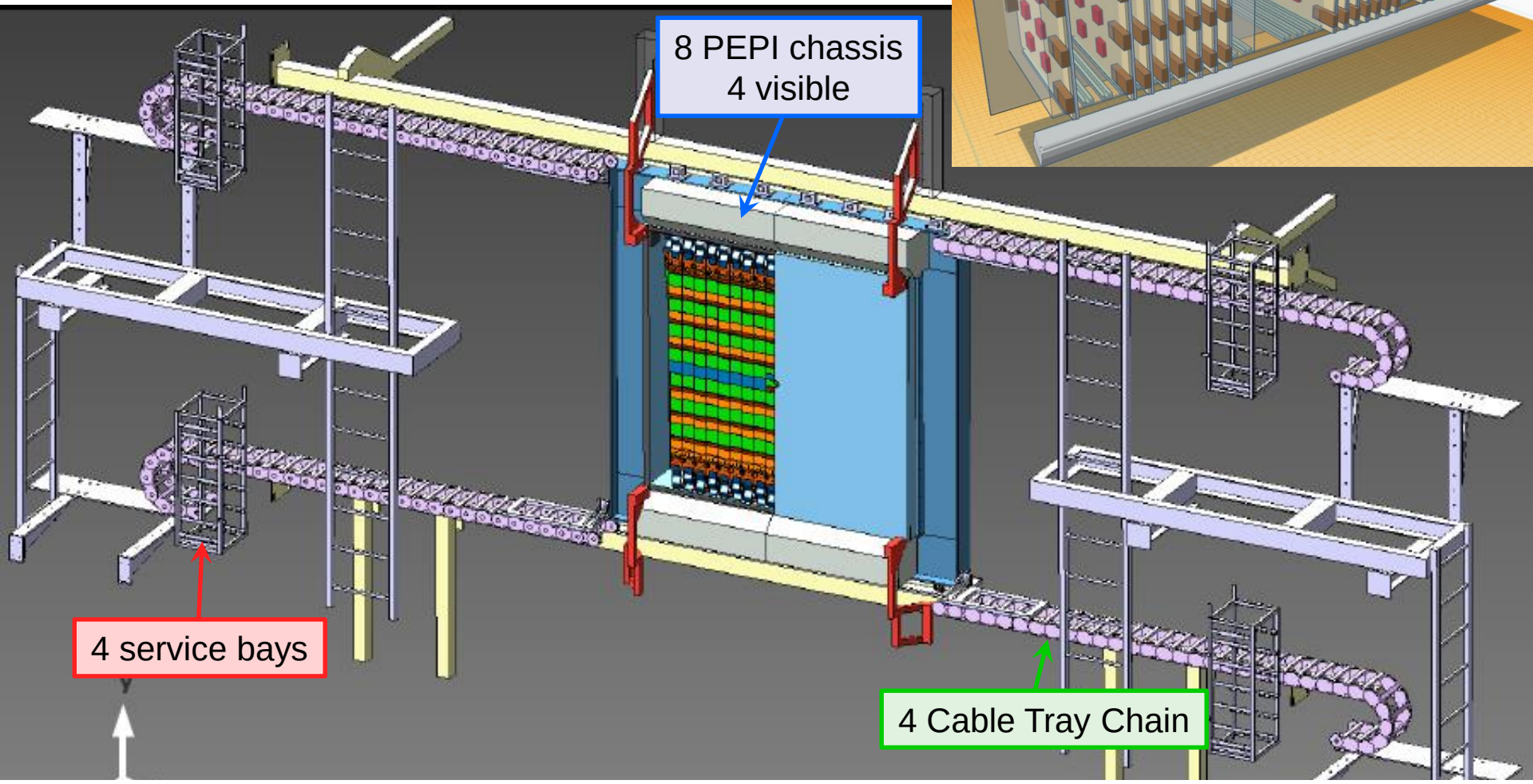
Locations of Major Components



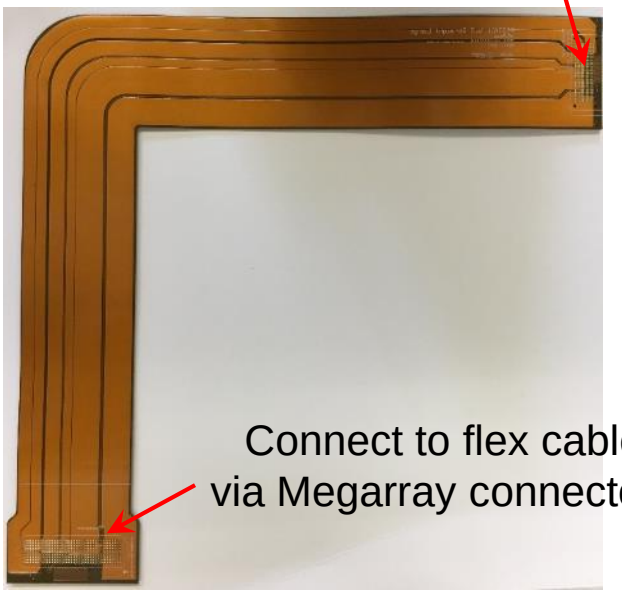
UT Detector Area

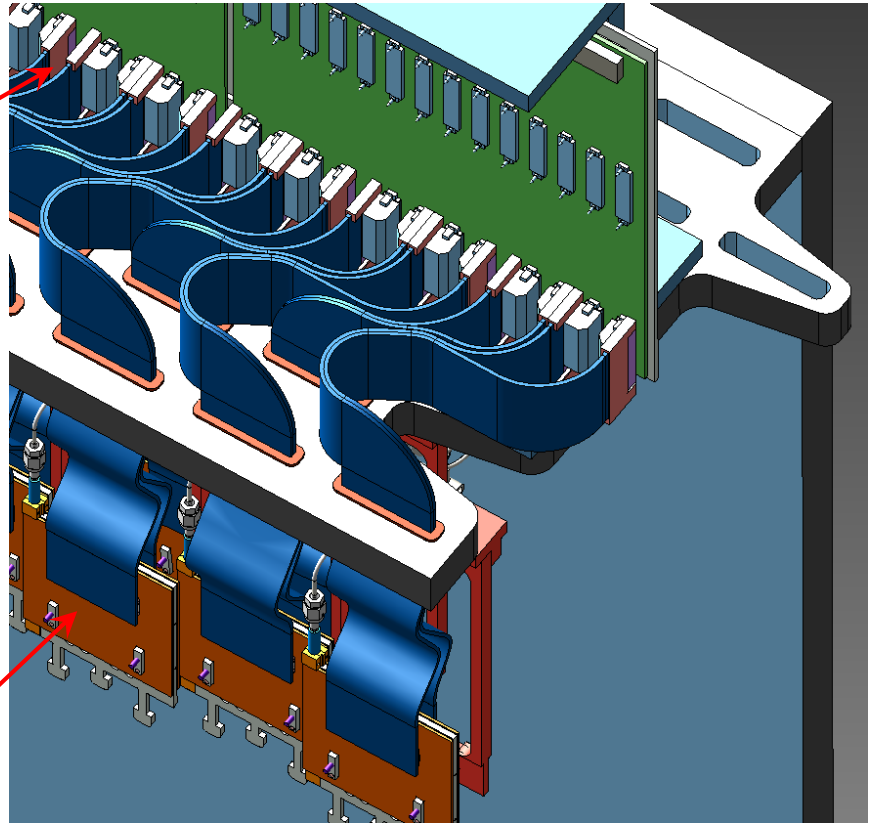
3 back planes inside a PEPI chassis,
Hold up to 3x12 electronics boards





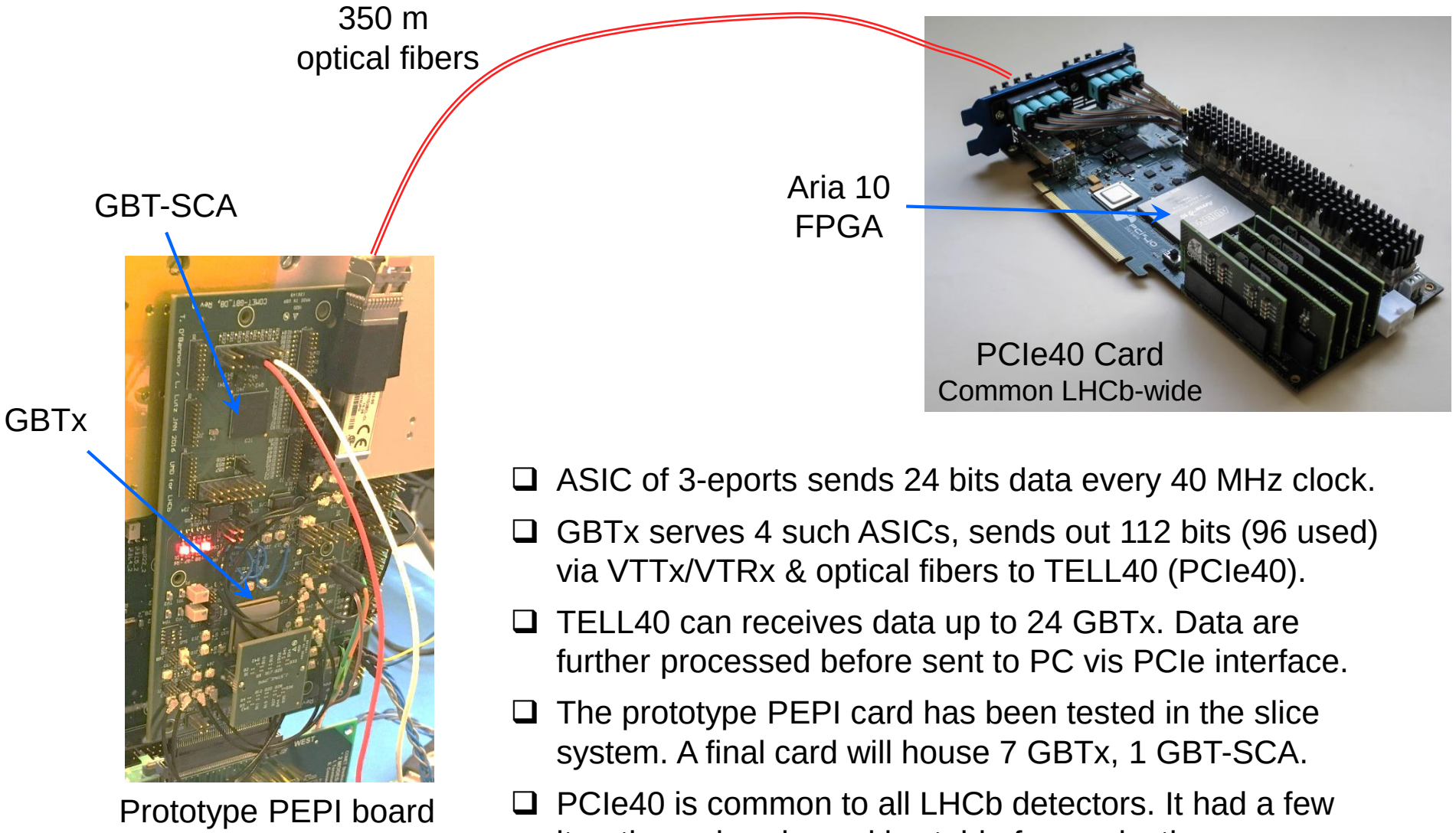
Pigtail Cable





- Pigtail cable connect flex cable on stave to back plane in PEPI chassis.
- It needs to be fed through the UT box, and bent to match due to X/U/V/X stereo issue.
- The 2nd iteration has been produced and will be validated in the slice test.

Event Data Transportation



- ASIC of 3-eports sends 24 bits data every 40 MHz clock.
- GBTx serves 4 such ASICs, sends out 112 bits (96 used) via VTTx/VTRx & optical fibers to TELL40 (PCIe40).
- TELL40 can receives data up to 24 GBTx. Data are further processed before sent to PC vis PCIe interface.
- The prototype PEPI card has been tested in the slice system. A final card will house 7 GBTx, 1 GBT-SCA.
- PCIe40 is common to all LHCb detectors. It had a few iterations already, and is stable for production.

Status of UT

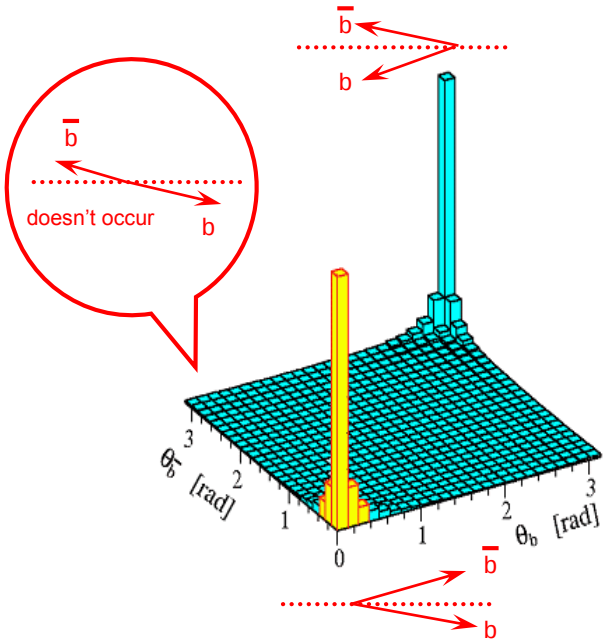
- The LHCb UT project has a budget of ~ 6.5 M CHF. The collaboration is also relatively small.
- It starts a few years later than other detector upgrade programs. Thus it has a very tight schedule.
- The R&D program is very challenging, e.g. the SALT design. I hope that the current new design will meet the requirements.
- Most other parts are very close to, or had already started transition from the R&D phase to the production phase.
- The plan is to install the 1st half in 2019 and the 2nd half in year 2020.

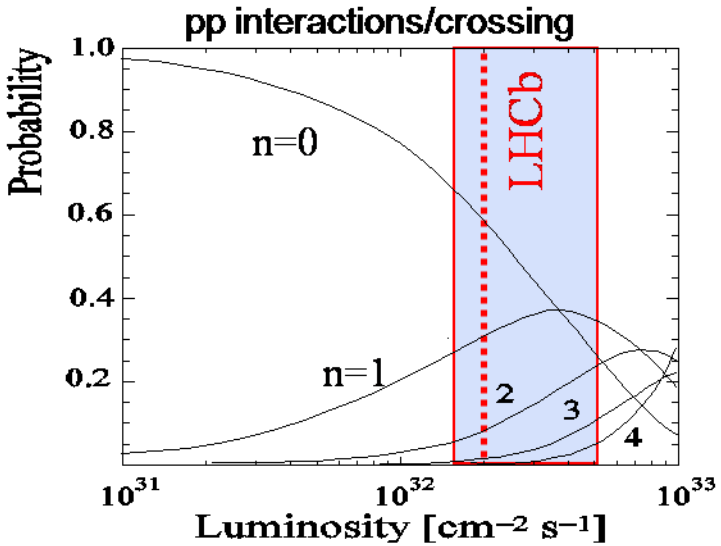
Backup Slides

The LHCb Environment

A dedicated b-physics experiment

- Designed to maximize B-acceptance within cost and space constraints.
- Forward spectrometer ($1.9 < |\eta| < 4.9$), where b are maximally boosted, benefits proper time measurement.
- One arm is OK since $b\bar{b}$ directions are correlated.
- Production σ_{bb}~500 μb, Min. bias: σ_{inel} ~ 80 mb.



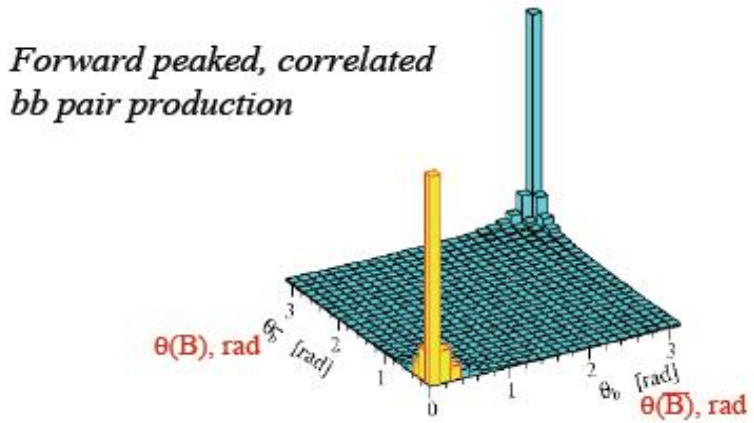


- Choose to run at $\langle L \rangle \sim 2 \times 10^{32}$ cm^{-2}s^{-1} (2 fb^{-1}/year), ~10^{12} bb pairs produced per year.
- Maximize probability of single interaction per crossing.
- Clean environment (average interactions per crossing $\langle n \rangle \sim 0.5$), easier to reconstruct.
- Less radiation damage (the closest tip ~7 mm away from beam).

LHCb Environment

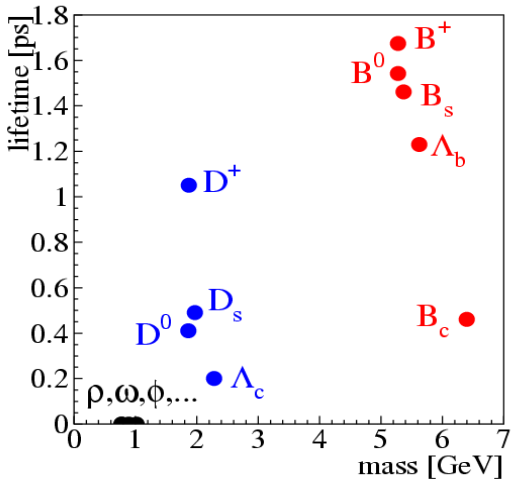
LHC environment

- pp collisions at E_{CM} = 14 TeV
- t_{bunch} = 25 ns ↔ bunch crossing rate = 40 MHz
- <L> = 2×10^{32} cm^{-2} s^{-1} @ LHCb interaction region
  - ➥ 10-50 times lower than for ATLAS/CMS



Cross sections

Physical quantity	Value	Event rate	Yield / year
s total	~ 100 mb		
s visible	~ 60 mb	~ 12 MHz	
s (c-cbar)	~ 3.5 mb	~ 700 kHz	~ 7×10^{12} pairs
s (b-bbar)	~ 0.5 mb	~ 100 kHz	~ 10^{12} pairs



Expected B-signal rates

- **branching ratios ~ 10^{-9} – 10^{-4}**

➔ **10 – 10^6 events / year ?**

B-hadrons are heavy and long-lived !

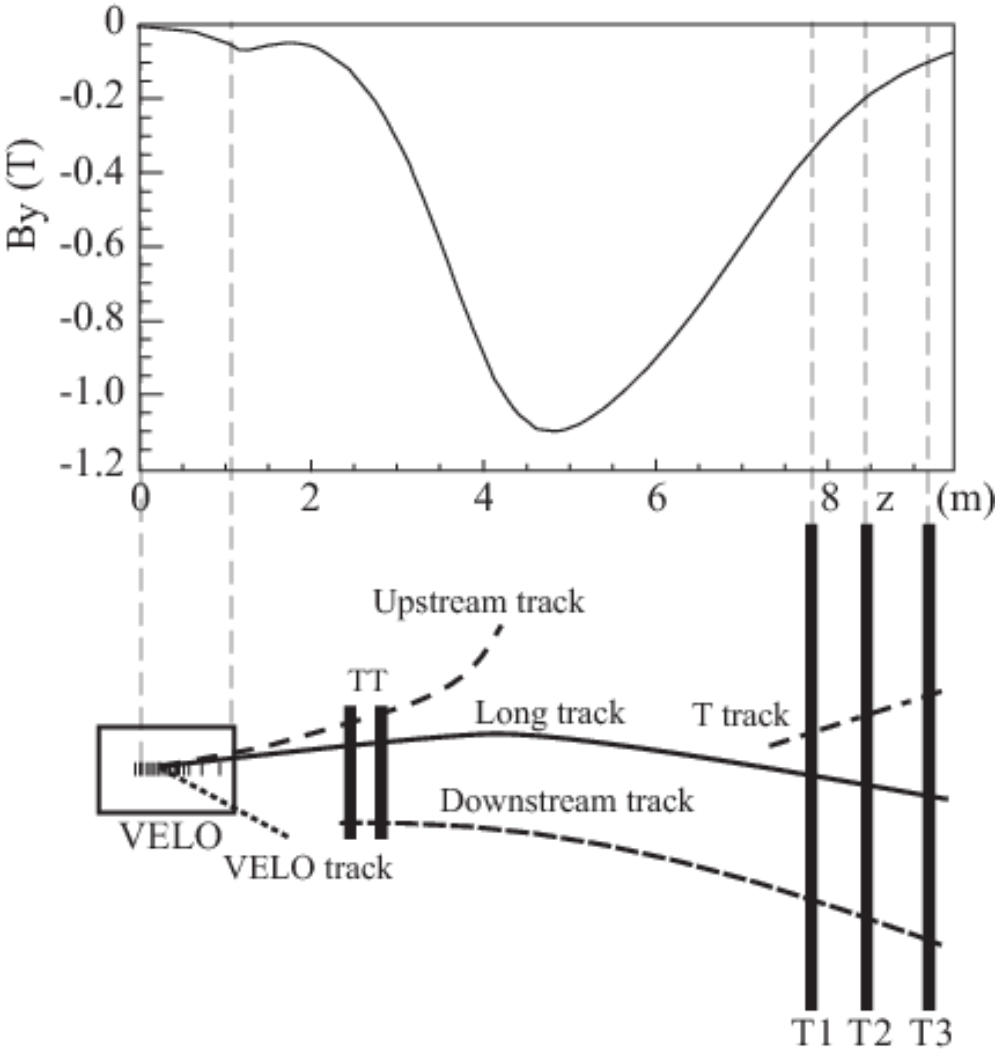
LHCb physics prospects for a Phase-I upgrade

Expect to collect a total of ~8 fb^{-1} of data up to 2018 and 50 fb^{-1} of data after 2018
→ moving towards theory precision measurements!

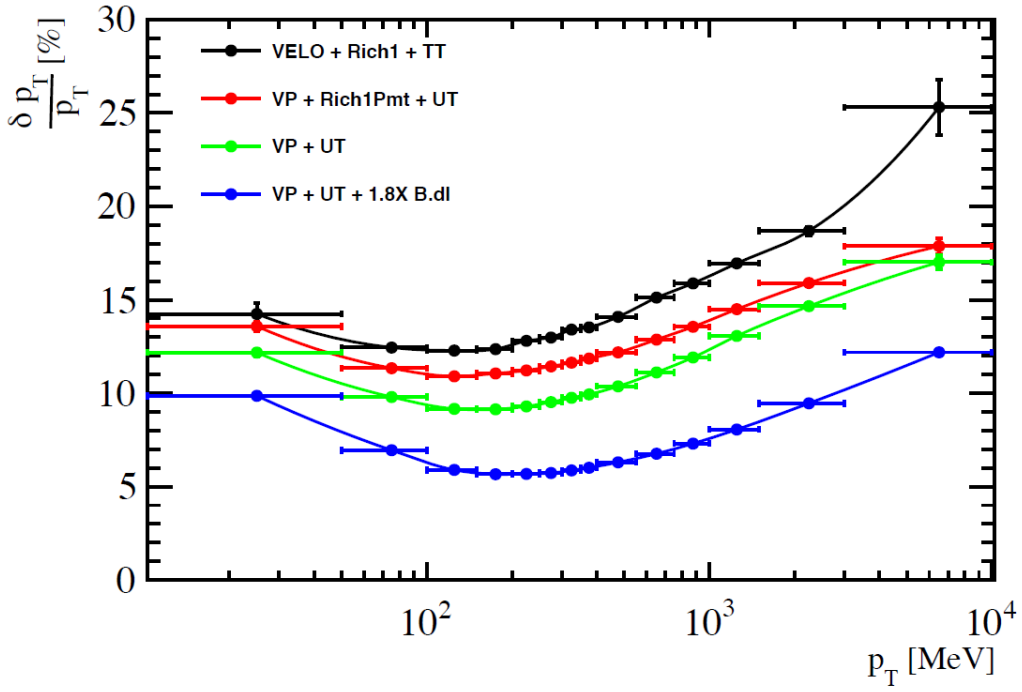
Type	Observable	Current precision*	LHCb 2018 *	Upgrade (50 fb^{-1})	Theory uncertainty
B_s^0 mixing	$2\beta_s$ $(B_s^0 \to J/\psi\,\phi)$	0.10 [9]	0.025	0.008	~ 0.003
	$2\beta_s$ $(B_s^0 \to J/\psi\, f_0(980))$	0.17 [10]	0.045	0.014	~ 0.01
	$A_{\rm fs}(B_s^0)$	6.4×10^{-3} [18]	0.6×10^{-3}	0.2×10^{-3}	0.03×10^{-3}
Gluonic penguin	$2\beta_s^{\rm eff}(B_s^0 \to \phi\phi)$	–	0.17	0.03	0.02
	$2\beta_s^{\rm eff}(B_s^0 \to K^{*0}\bar{K}^{*0})$	–	0.13	0.02	< 0.02
	$2\beta^{\rm eff}(B^0 \to \phi K_S^0)$	0.17 [18]	0.30	0.05	0.02
Right-handed currents	$2\beta_s^{\rm eff}(B_s^0 \to \phi\gamma)$	–	0.09	0.02	< 0.01
	$\tau^{\rm eff}(B_s^0 \to \phi\gamma)/\tau_{B_s^0}$	–	5 %	1 %	0.2 %
Electroweak penguin	$S_3(B^0 \to K^{*0}\mu^+\mu^-; 1 < q^2 < 6\,{\rm GeV}^2/c^4)$	0.08 [14]	0.025	0.008	0.02
	$s_0\, A_{\rm FB}(B^0 \to K^{*0}\mu^+\mu^-)$	25 % [14]	6 %	2 %	7 %
	$A_{\rm I}(K\mu^+\mu^-; 1 < q^2 < 6\,{\rm GeV}^2/c^4)$	0.25 [15]	0.08	0.025	~ 0.02
	$\mathcal{B}(B^+ \to \pi^+\mu^+\mu^-)/\mathcal{B}(B^+ \to K^+\mu^+\mu^-)$	25 % [16]	8 %	2.5 %	~ 10 %
Higgs penguin	$\mathcal{B}(B_s^0 \to \mu^+\mu^-)$	1.5×10^{-9} [2]	0.5×10^{-9}	0.15×10^{-9}	0.3×10^{-9}
	$\mathcal{B}(B^0 \to \mu^+\mu^-)/\mathcal{B}(B_s^0 \to \mu^+\mu^-)$	–	~ 100 %	~ 35 %	~ 5 %
Unitarity triangle angles	γ $(B \to D^{(*)}K^{(*)})$	~ 10–12° [19, 20]	4°	0.9°	negligible
	γ $(B_s^0 \to D_s K)$	–	11°	2.0°	negligible
	β $(B^0 \to J/\psi\, K_S^0)$	0.8° [18]	0.6°	0.2°	negligible
Charm CP violation	A_Γ	2.3×10^{-3} [18]	0.40×10^{-3}	0.07×10^{-3}	–
	ΔA_{CP}	2.1×10^{-3} [5]	0.65×10^{-3}	0.12×10^{-3}	–

* Outdated estimations, already doing better (γ at ~7° already…)

LHCb Tracker & Megnetic Field



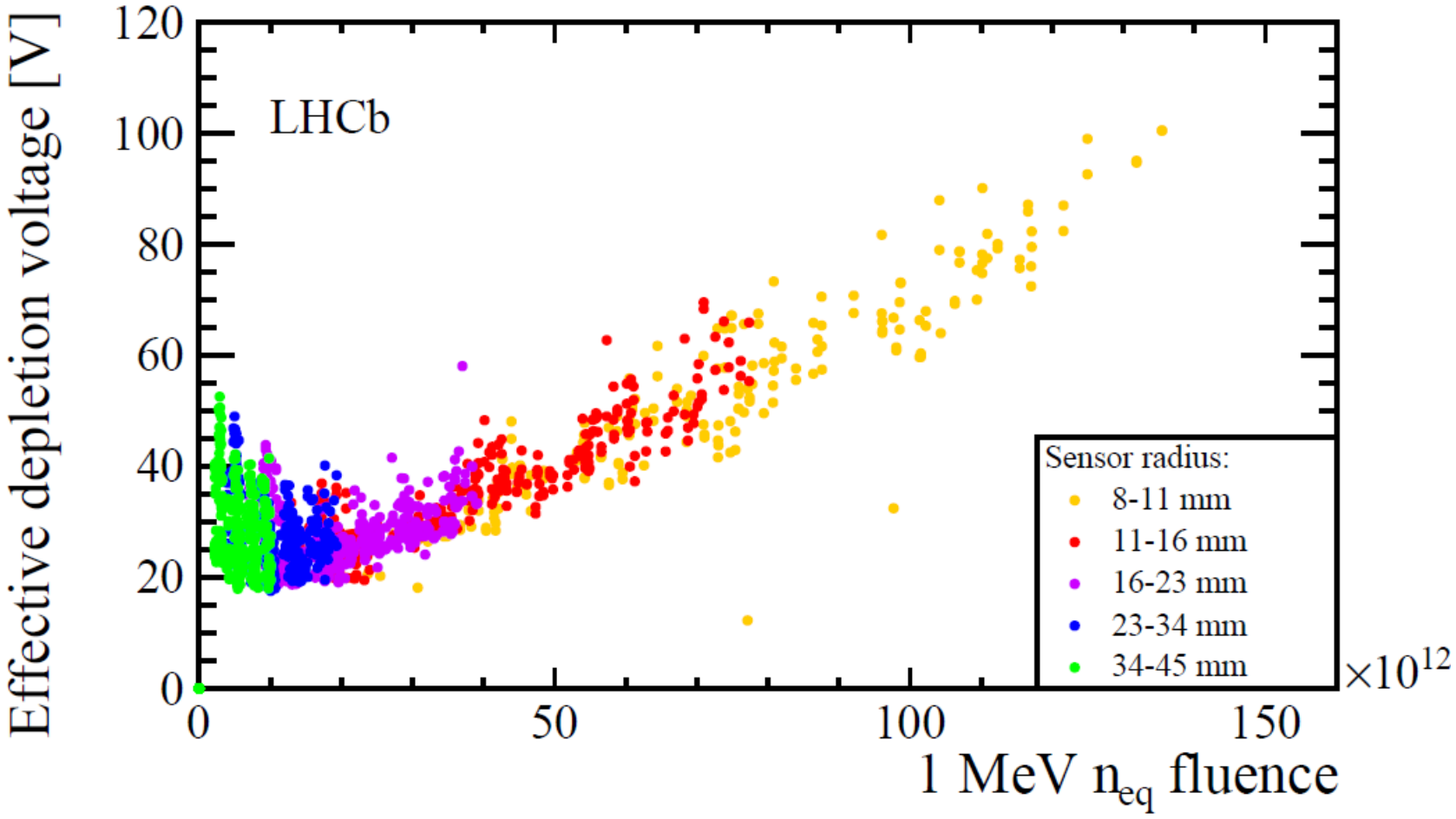
VP + UT In Trigger



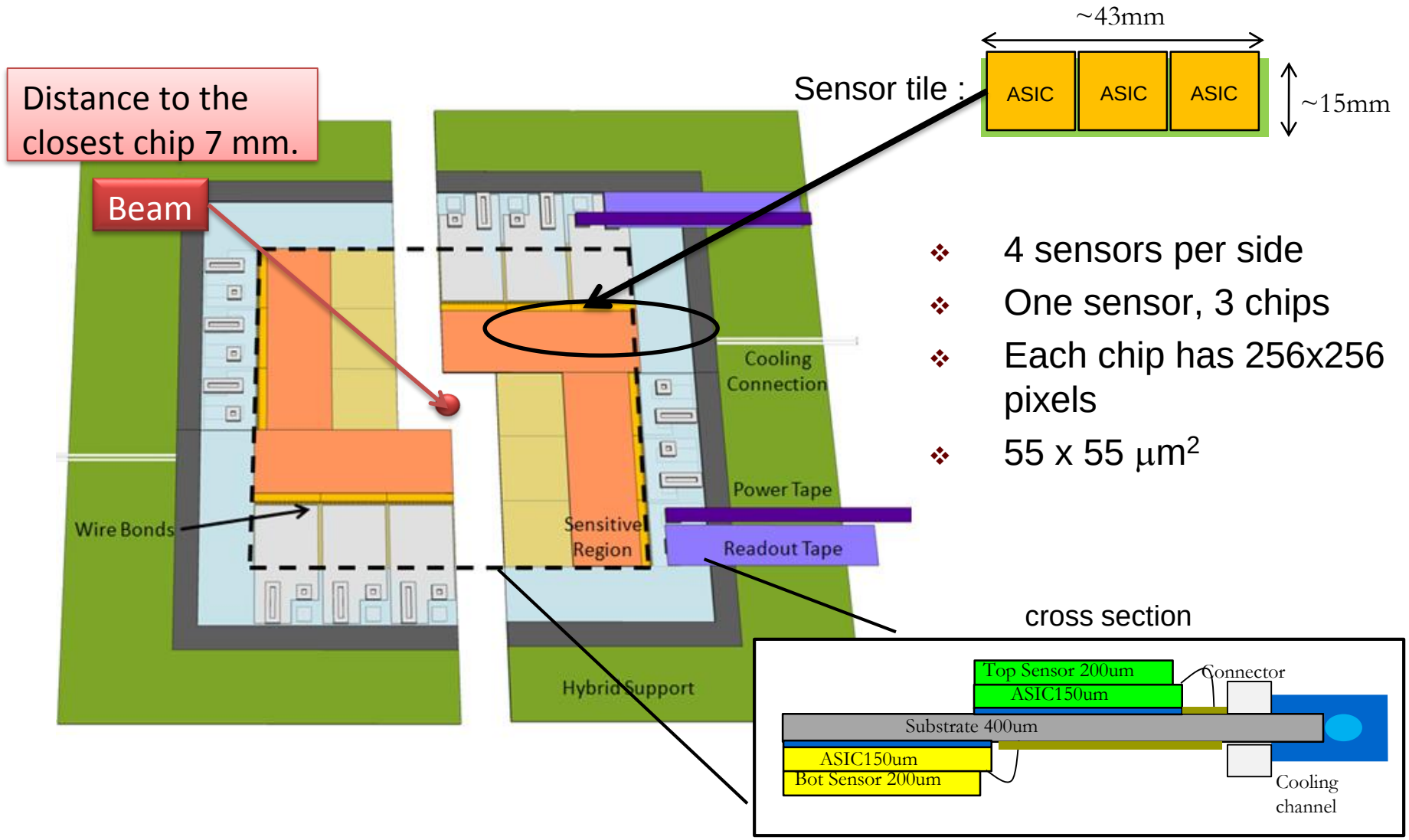
	ϵ(%)	GR(%)	t(ms)
No p-estimate	96.3	52.1	25.7
$\delta p/p = 0.0$	96.7	2.9	3.0
$\delta p/p = 0.1$	96.7	3.4	5.2
$\delta p/p = 0.2$	96.7	4.9	8.2
$\delta p/p = 0.3$	96.7	7.2	16.6

better p_T resolution
+
drastic reduction in ghost rate
+
large gain in reconstruction time!

Deletion Voltage vs Radiation Fluence



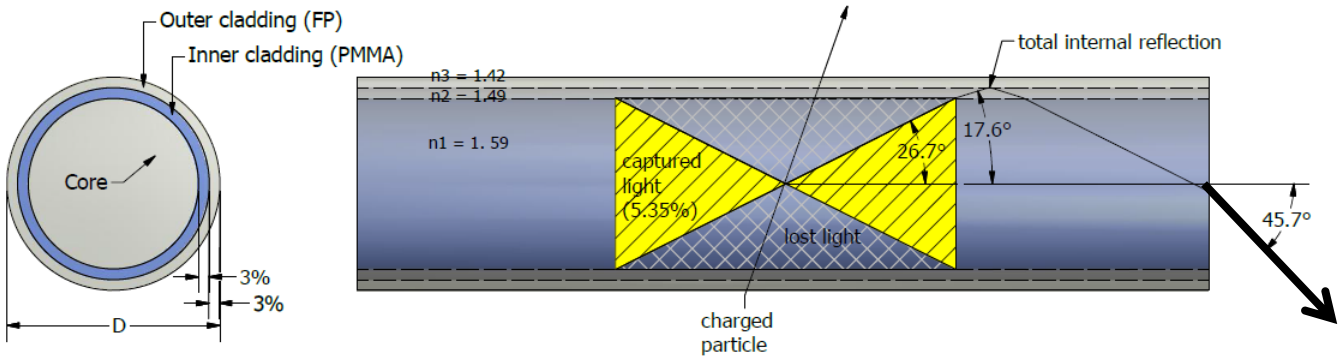
VELO Pixel Module



- 4 sensors per side
- One sensor, 3 chips
- Each chip has 256x256 pixels
- 55 x 55 μm^2

SciFi Tracker: Scintillation Fiber

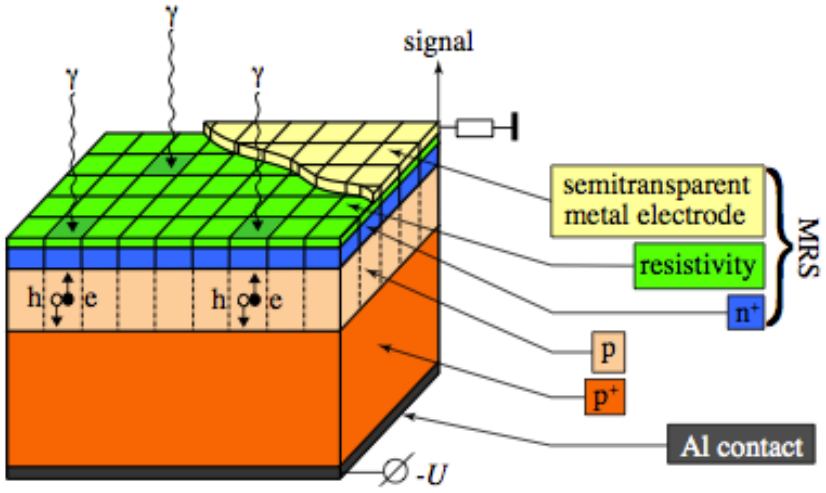
Kuraray SCSF-78MJ fibres: Ø (250 ± 15) µm, 6 fibre layers per mat, each layer with 512 fibres with length 2.5m → 10,000 km fibres

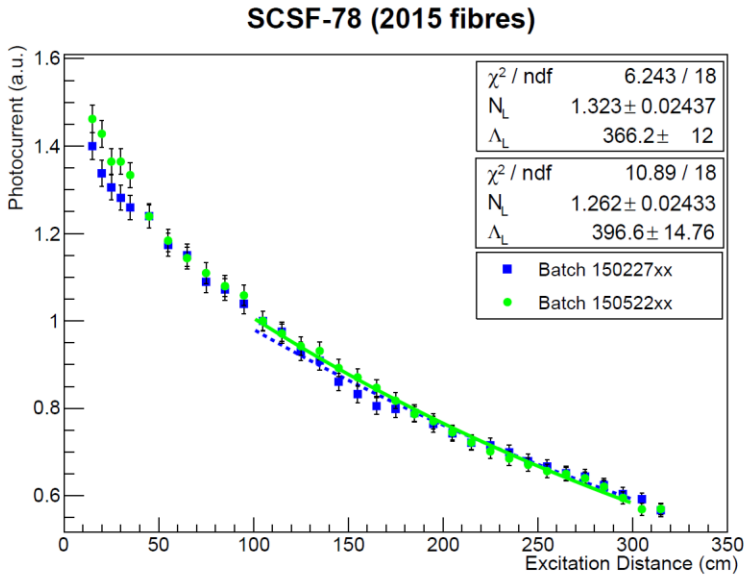


Peaks @ λ~ 450 nm

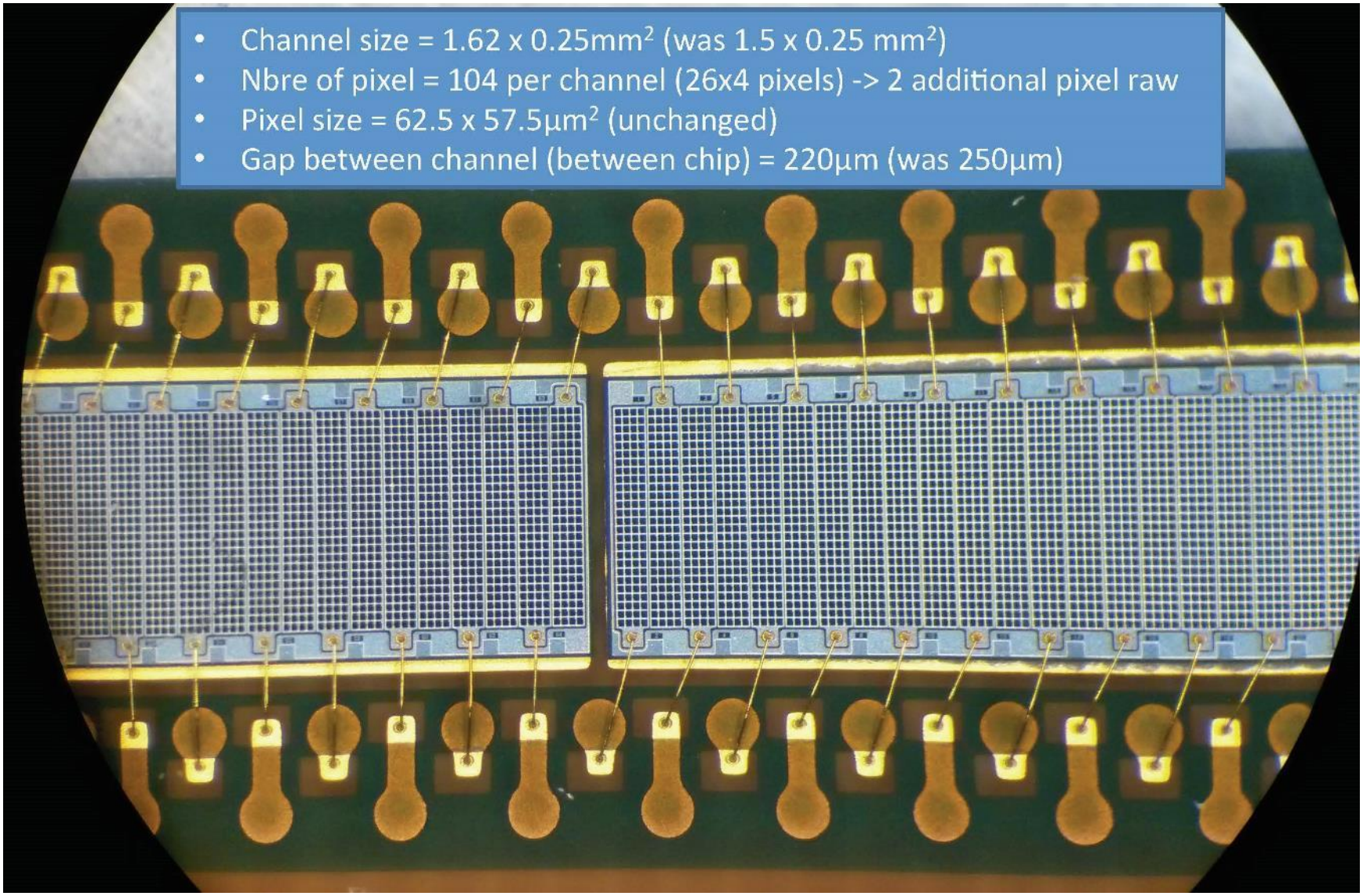
Only a few photons after 2.5m

300 photons per MIP produced (only 5% captured)

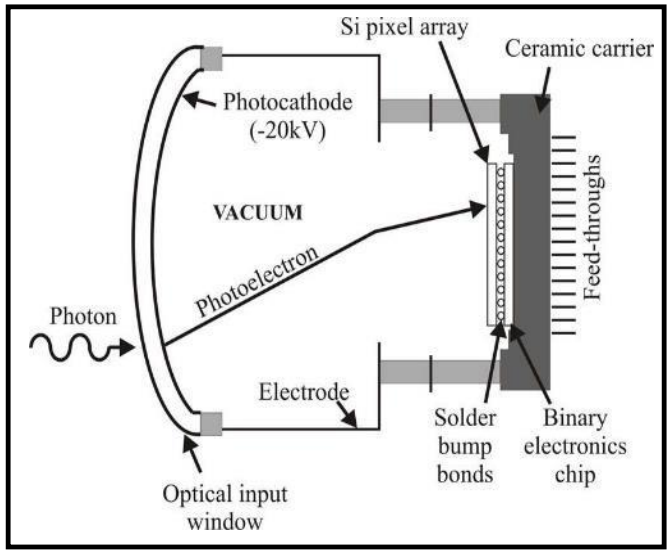




SiPM Array


• Channel size = 1.62 x 0.25mm² (was 1.5 x 0.25 mm²)
• Nbre of pixel = 104 per channel (26x4 pixels) -> 2 additional pixel raw
• Pixel size = 62.5 x 57.5µm² (unchanged)
• Gap between channel (between chip) = 220µm (was 250µm)

HPD & MAPMT

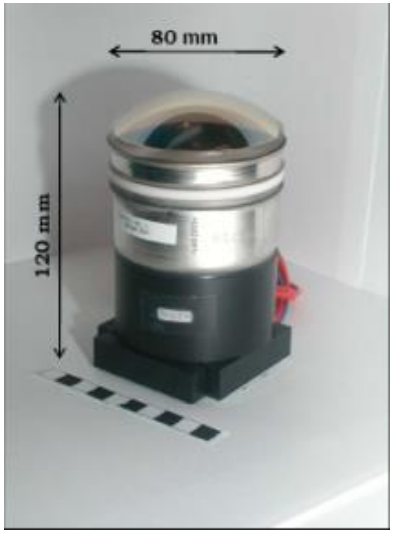


384+2688 MAPMTs for upgrade

size 23x23 mm^2, 80% coverage.

8x8 pixels, readout by CLARA.

Resolution in RICH1: 0.78 mrad

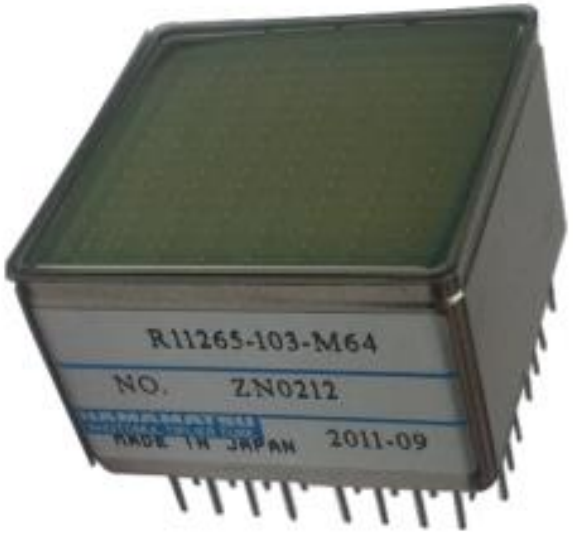


196+288 HPDs in RICH1 & 2

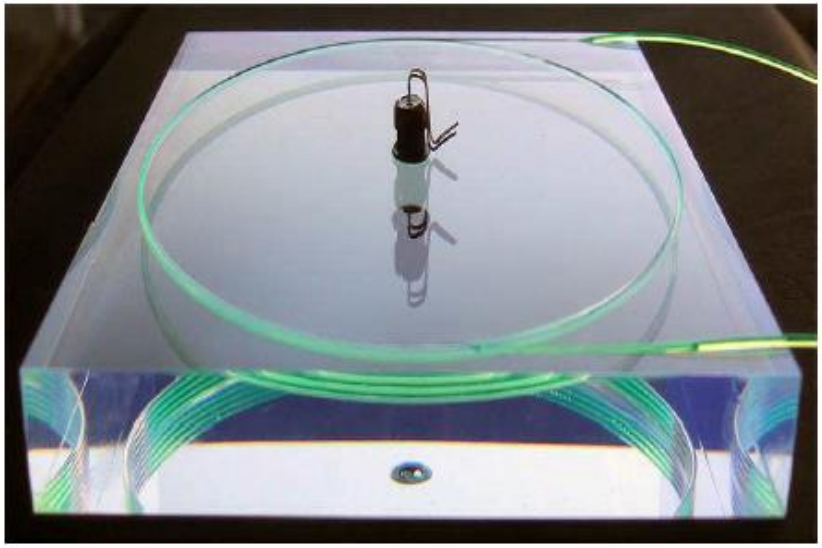
Φ=80 mm, 64% coverage

32x32 pixels of 500 μm^2 each

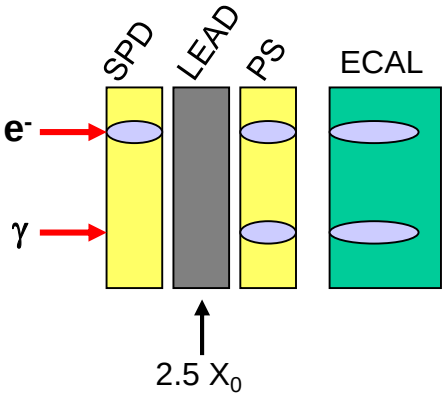
Resolution in RICH1: 1.6 mrad

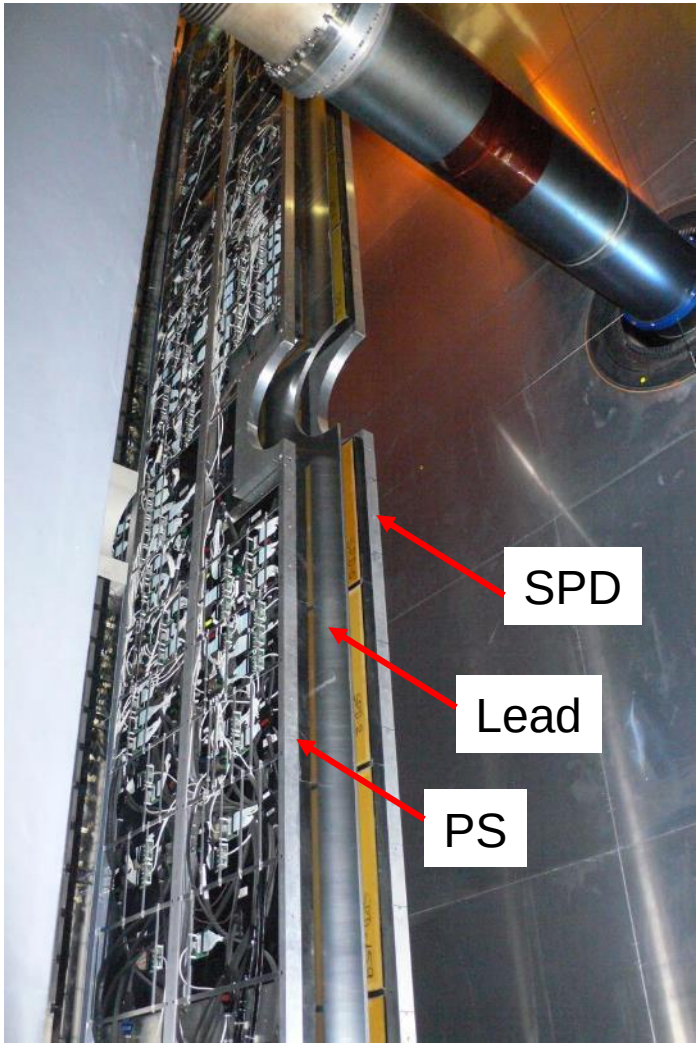


Scintillating Pad Detector & PreShower

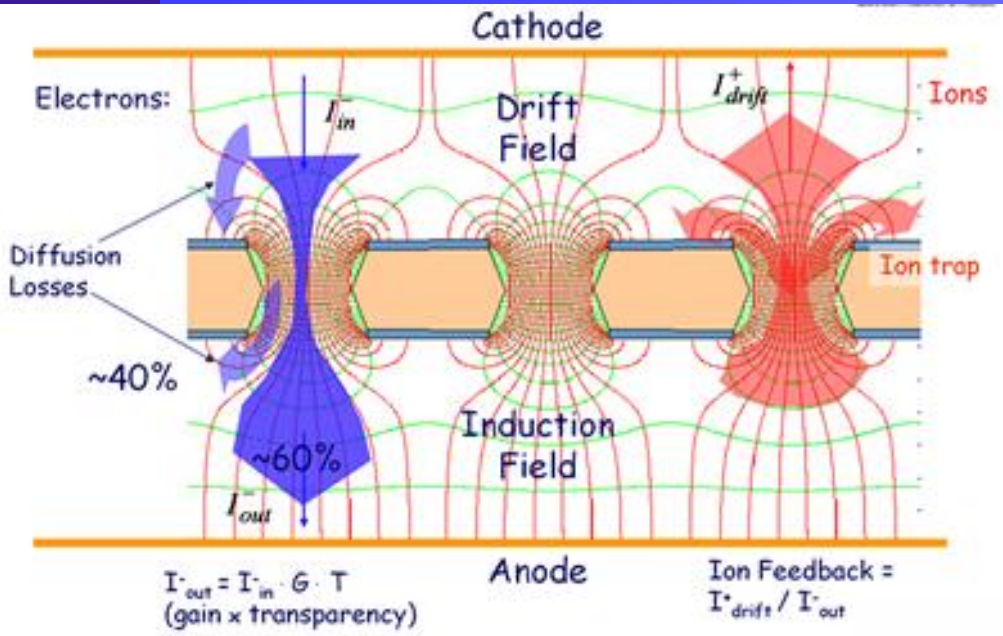


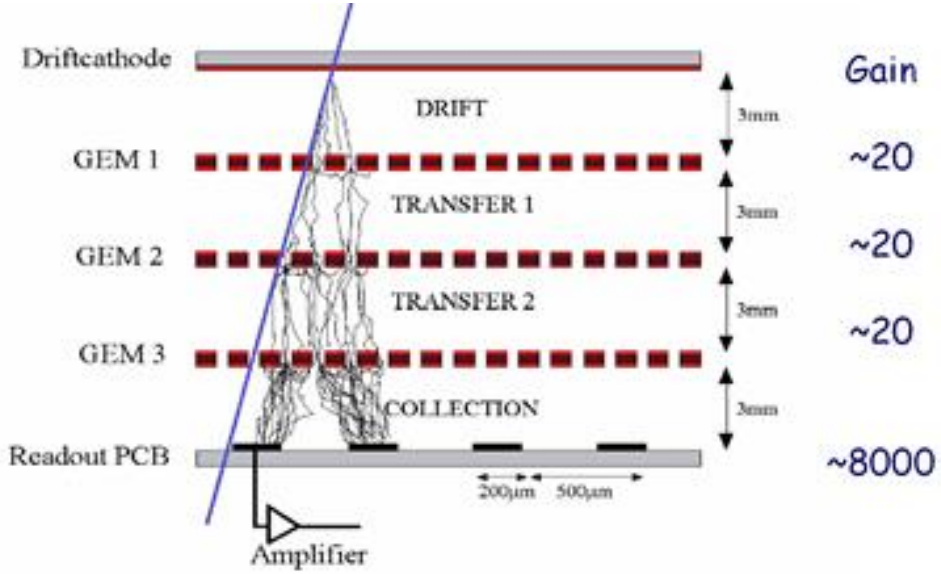
4 loops of wave length shift fiber





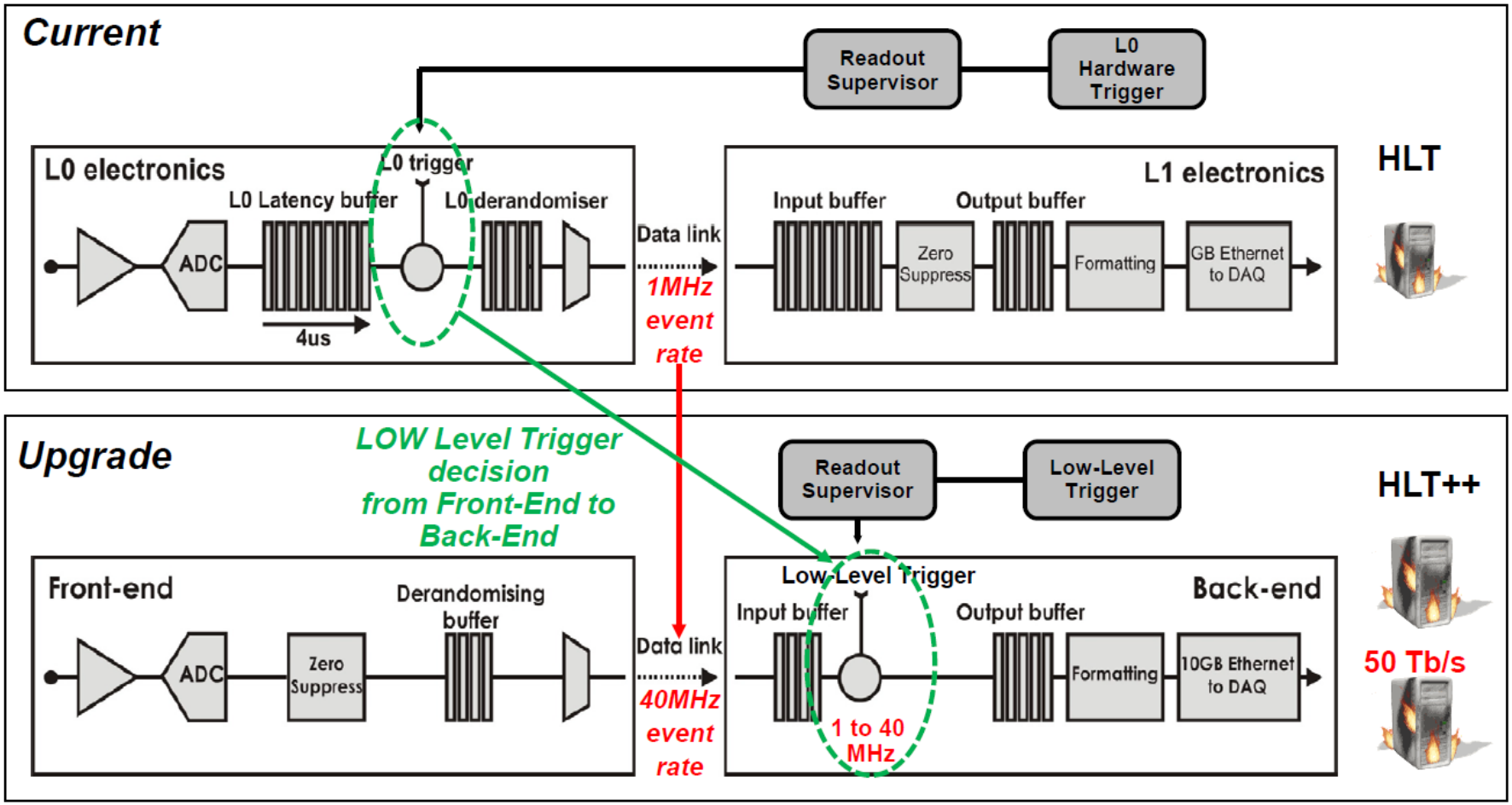
Gas Electron Multiplier (GEM)



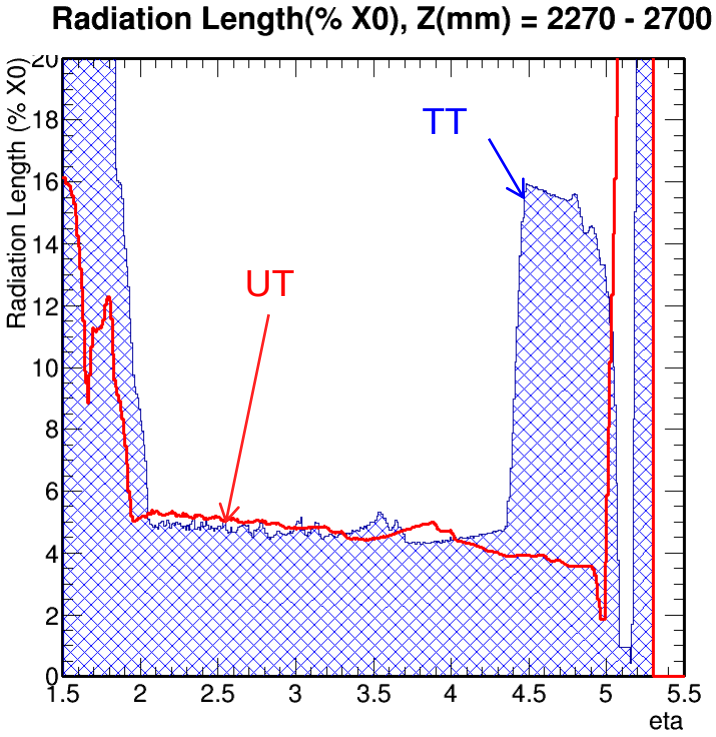


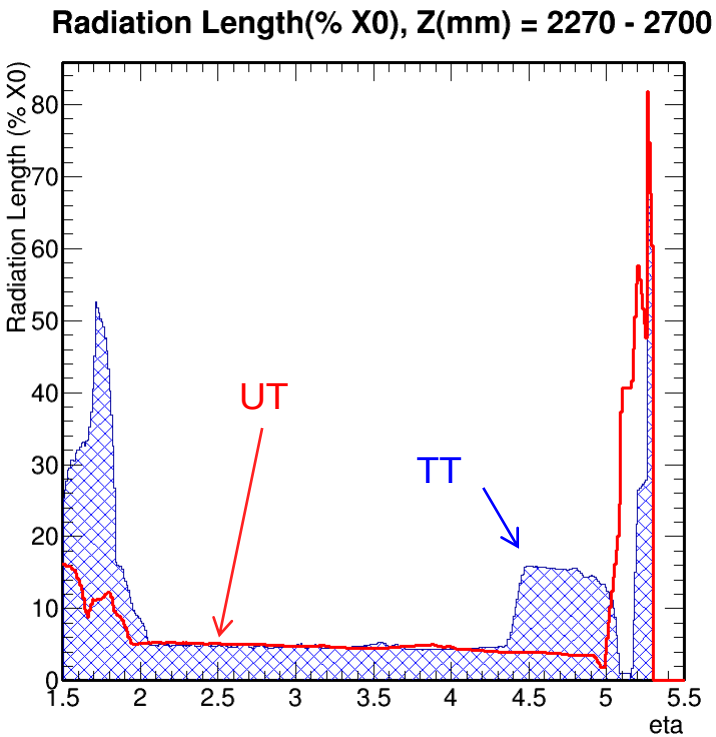
Reference: https://web.infn.it/GEMINI/

LHCb Readout Scheme



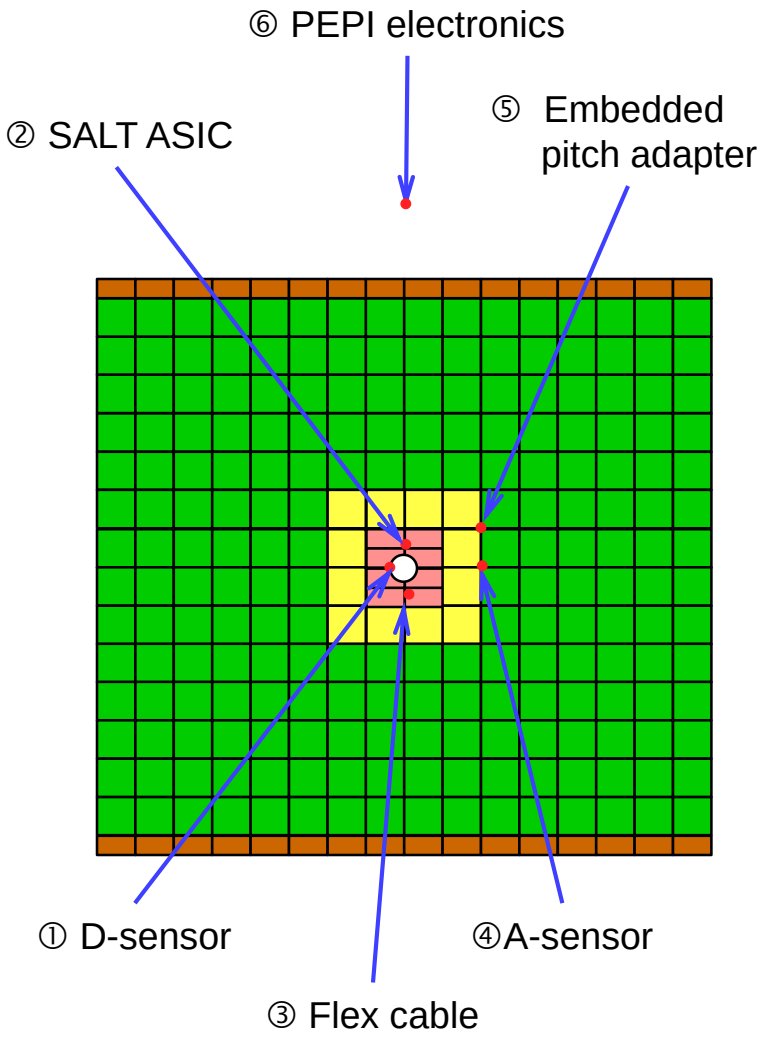
Radiation Length Plots





- Radiation length between Z=2270-2700 mm, including 0.14% X_0 of air, 0.34% of UT box.
- The total radiation length between $2<\eta<4.9$ in the new UT release (2) is 4.6% X_0. RL per UT plane is 1.02% X_0.
- Beam jacket is from the current best design. The overall $\int RL \cdot d\eta = 7.02\%\ X_0$ in this design, slightly smaller than 7.49% X_0 in the TT design. More importantly, it occupies much smaller angle ($\eta>5$), instead of ($4.4 < \eta < 5$) where tracks are used in physics study.

Radiation Levels @ Interesting Locations



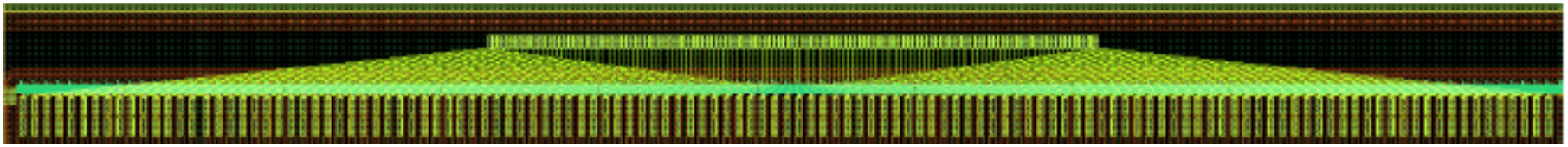
Radiation effects may depend on total ionization dose (MRad), or displacement damage (1-MeV n_{eqv}/cm^2).

	X,Y (mm)	TID (Rad)		Fluence (cm^{-2} 1MeV n_{eqv})	
		Simul.	Test	Simul.	Test
1	34.2, 0	12 M	40 M	1.4×10^{14}	5×10^{14}
2	16.7, 50	7.3 M	20 M	0.78×10^{14}	2×10^{14}
3	0, 80	4.0 M	10 M	0.35×10^{14}	1×10^{14}
4	187, 0	1.1 M	2.2 M	1.1×10^{13}	2.2×10^{13}
5	187, 94	0.90 M	1.8 M	0.9×10^{13}	1.8×10^{13}
6	0, 1100	36 K	70 K	1.1×10^{12}	2×10^{12}
7*	~ 4000, 0	n.a.	20 K ?		

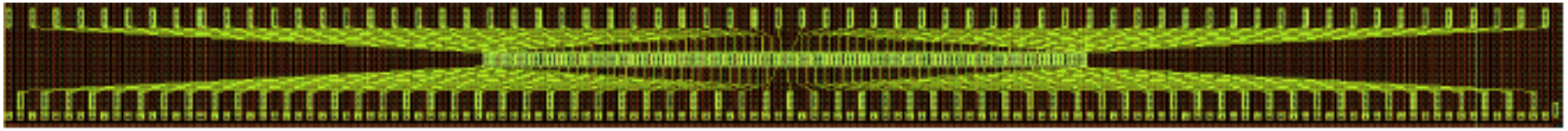
for service boxes, not simulated.

Different Pitch Adapters

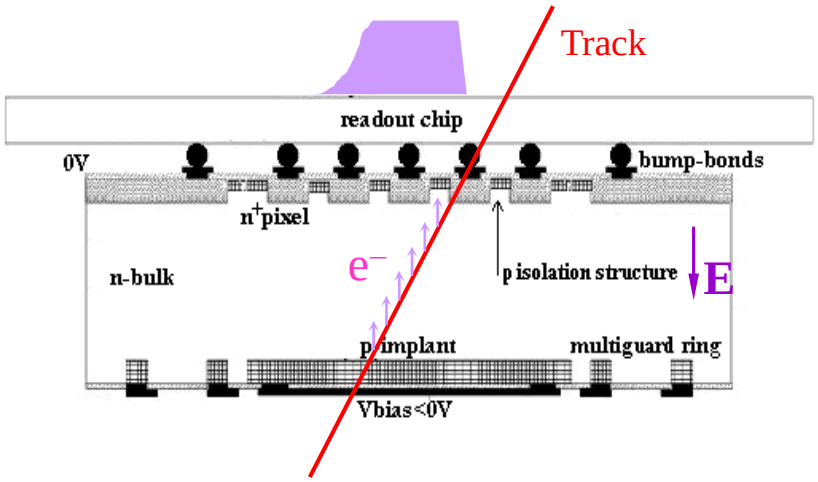
Fan up



Fan in

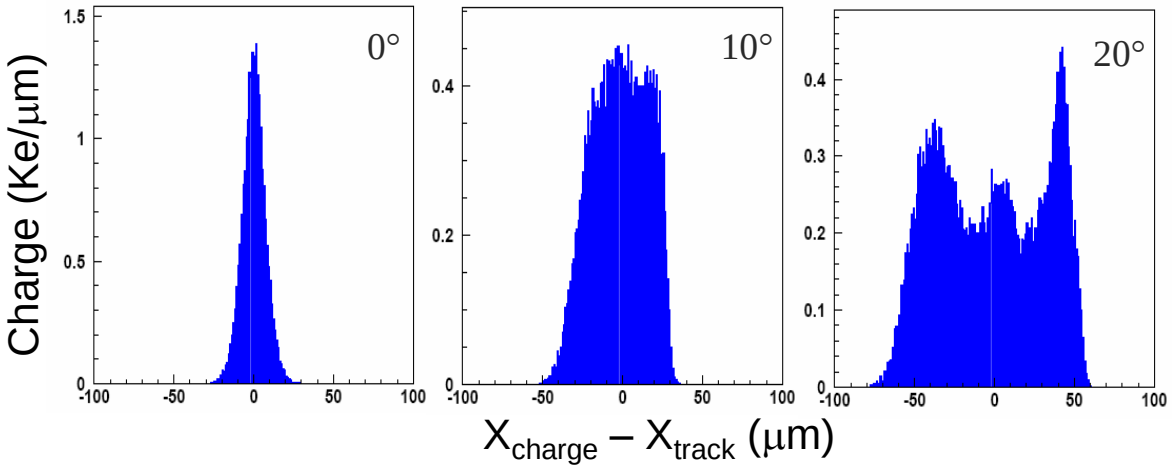


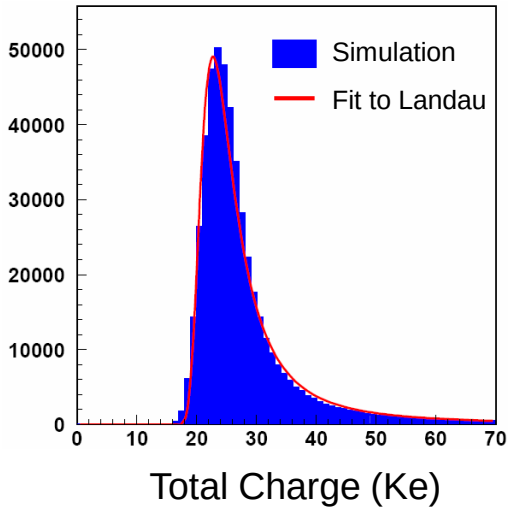
Signal In Silicon Detector



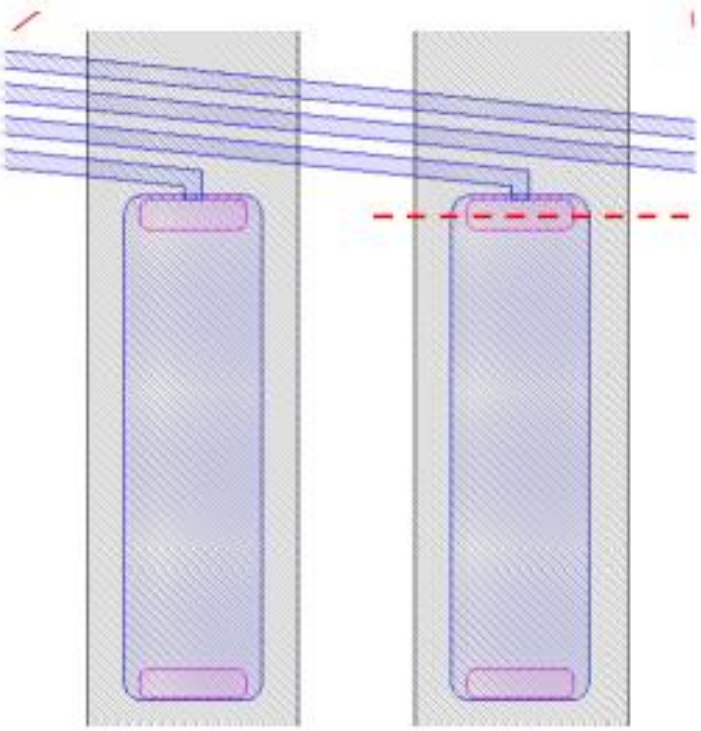
- Energy is deposited by charged track along its path, produces electron/hole pairs (via excitation, ionization, δ-rays).
- Electron cloud drifts (~few ns) towards readout strips along E field (corresponding to doping and bias voltage applied).
- Diffusion results in cloud spread (~ few μm).
- Realistic front end electronics: noise, crosstalk, gain uncertainty, threshold, and threshold dispersion, digitization accuracy, etc.
- Irradiation effects are to be included.

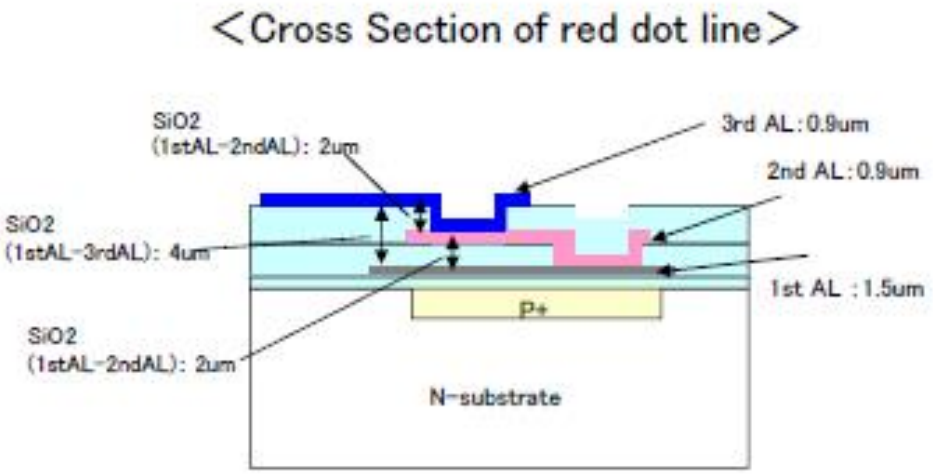
d = 300 μm, V_{depl} = 70 V, V_{appl} = 100 V





Triple Metallization Layer

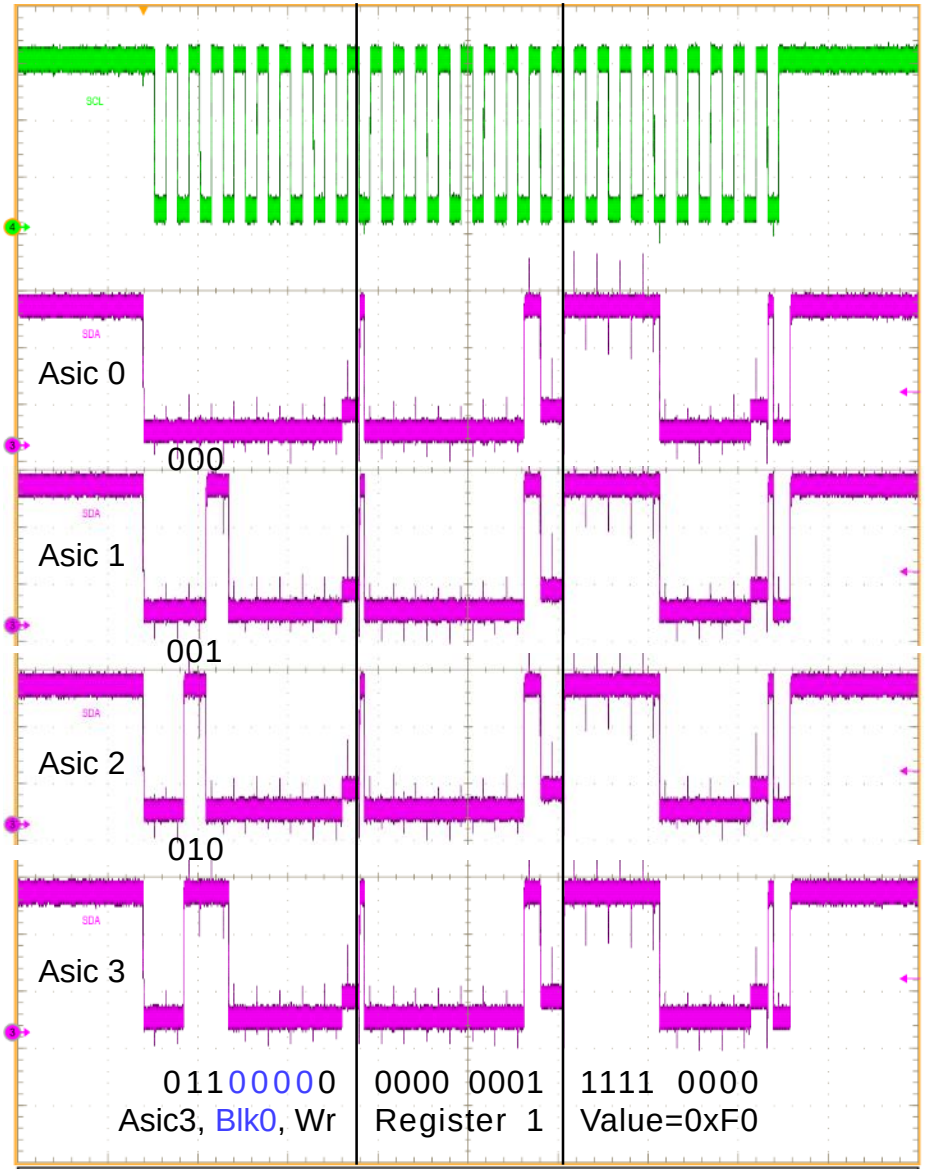




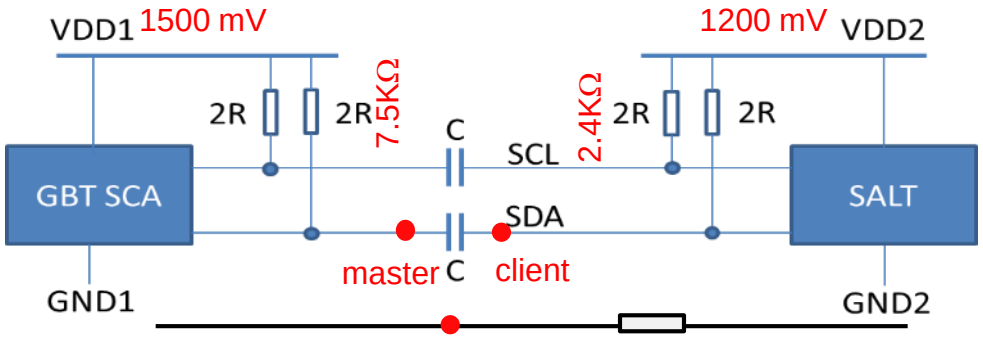
※ 2nd AL works as a relay point for connecting the 1st AL and 3rd AL.

Multiple ASIC I2C Communication

- One I²C master (GBT-SCA), and 4 clients (SALT128) in the system.
- The GBT-SCA can configure and read back register values from all 4 ASICs without any problem.

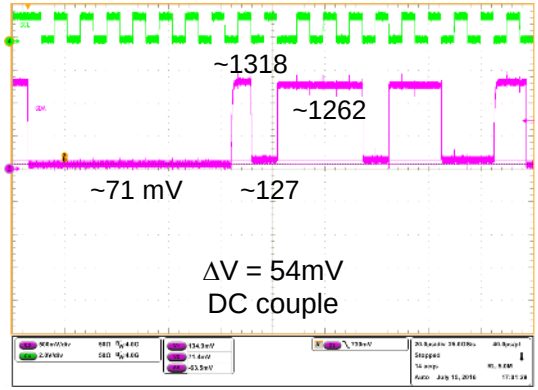


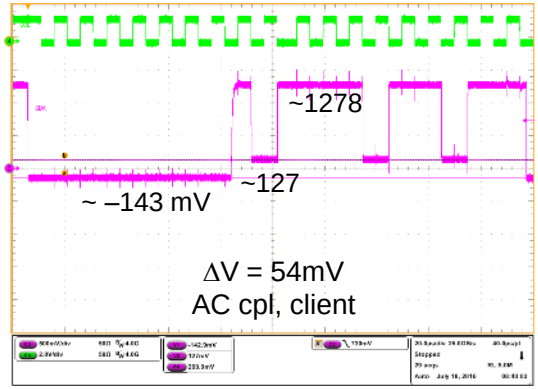
I2C Test With AC Coupling

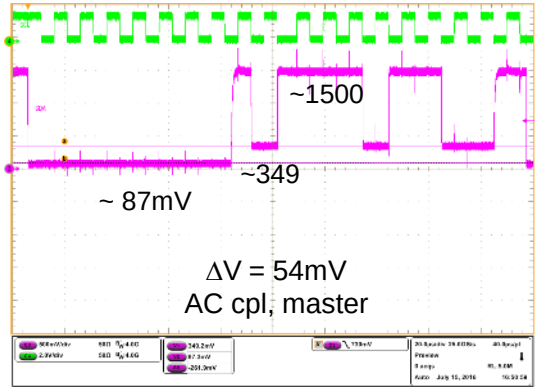


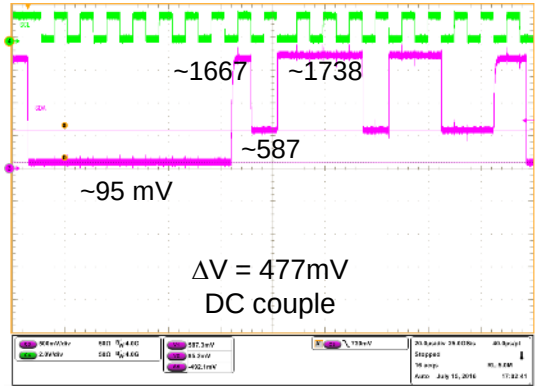
ΔV=GND2-GND1

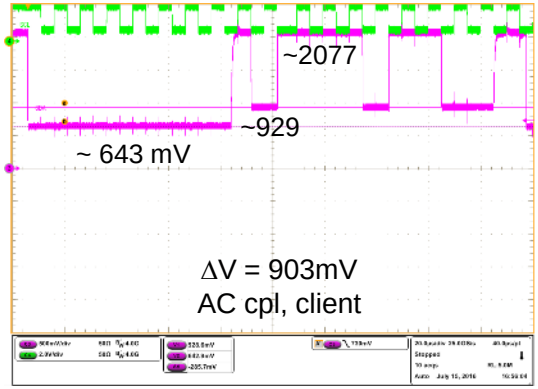
Read value 0xED

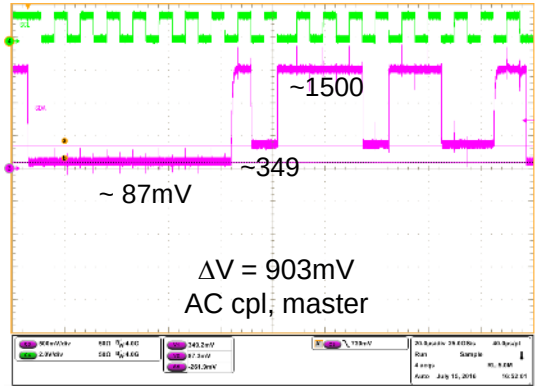








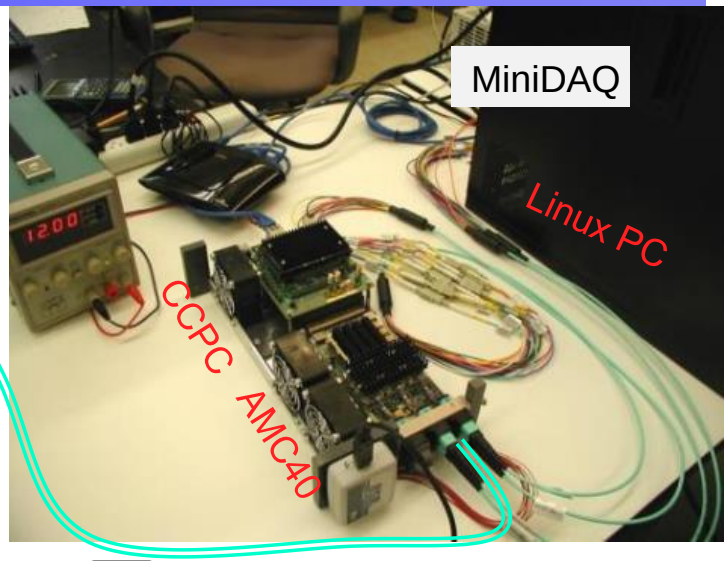




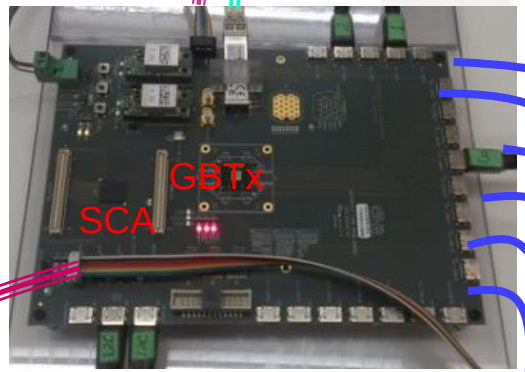
SALT128 Bench Test Setup

GBT frame data
(TFC/ECS & event)
4.48 Gbps

I²C signal to
config GBTx

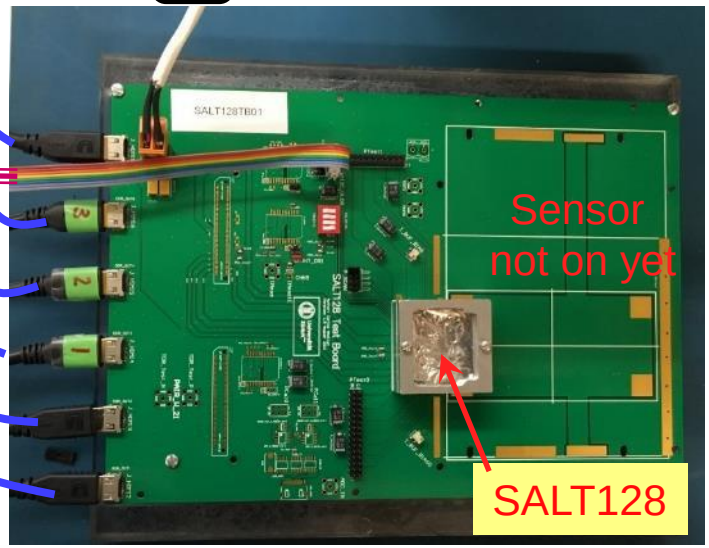


VLDB



LV

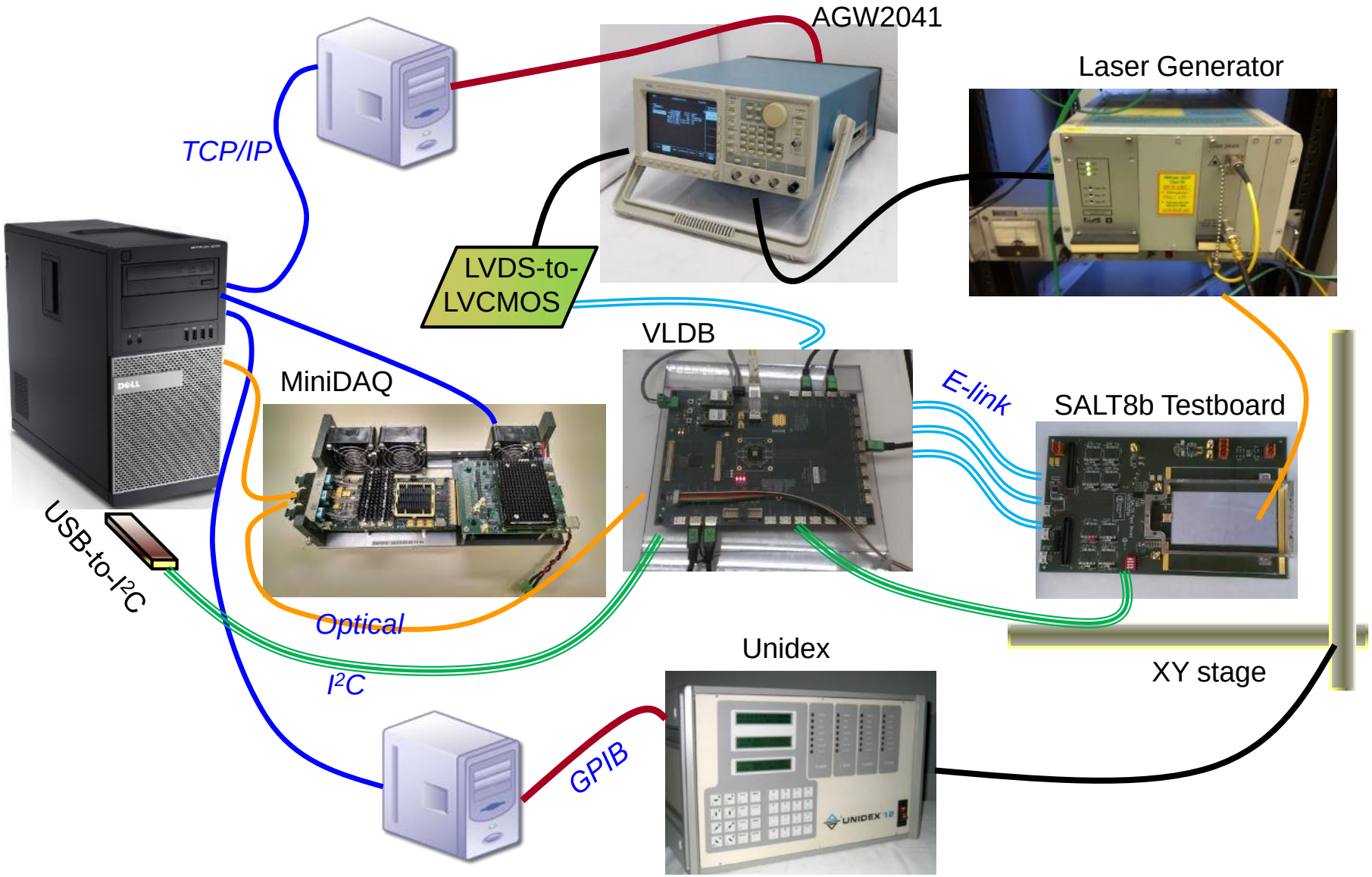
I²C signal to
config SALT8
100 kbps



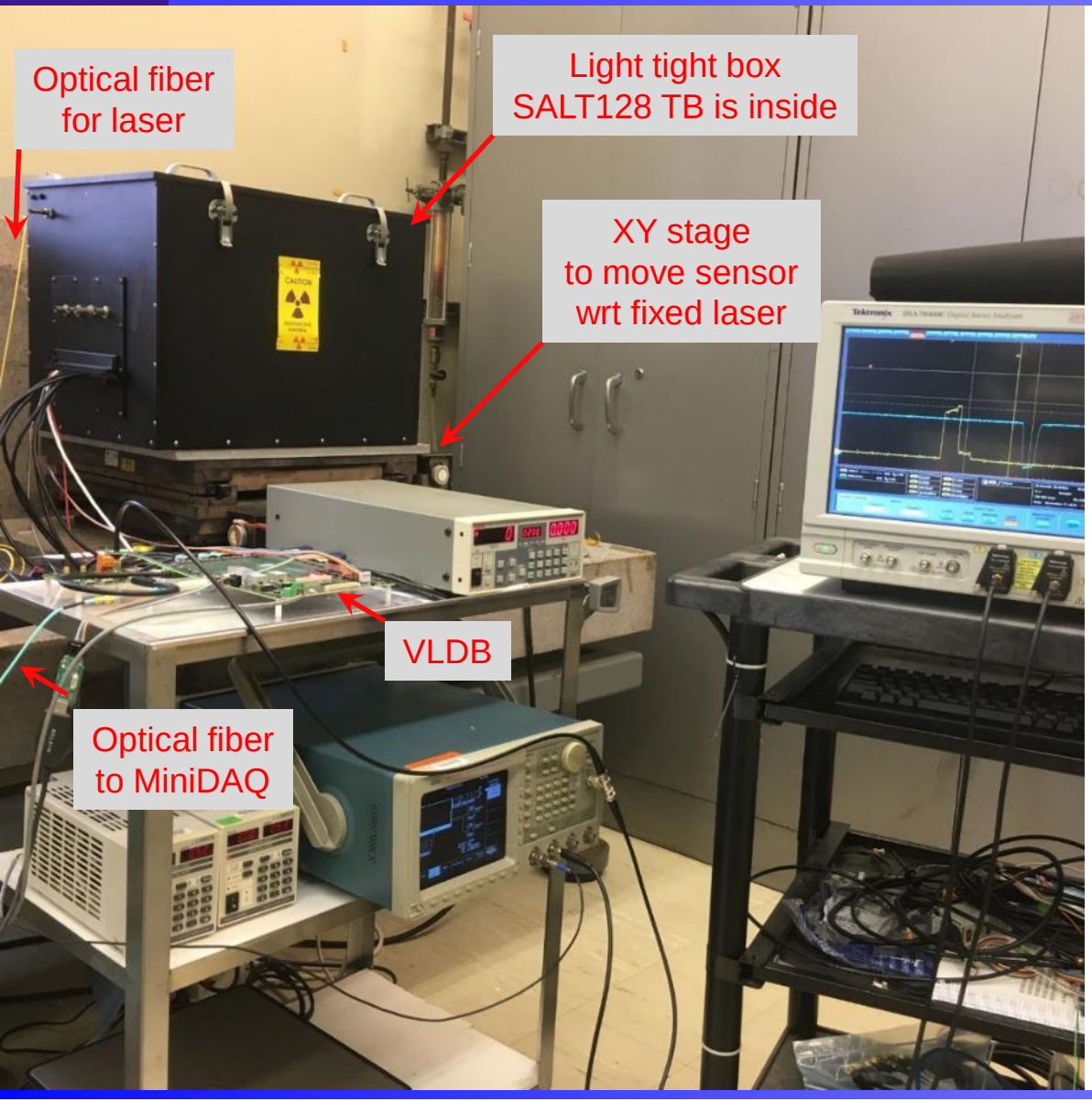
6x E-link data
320 Mbps

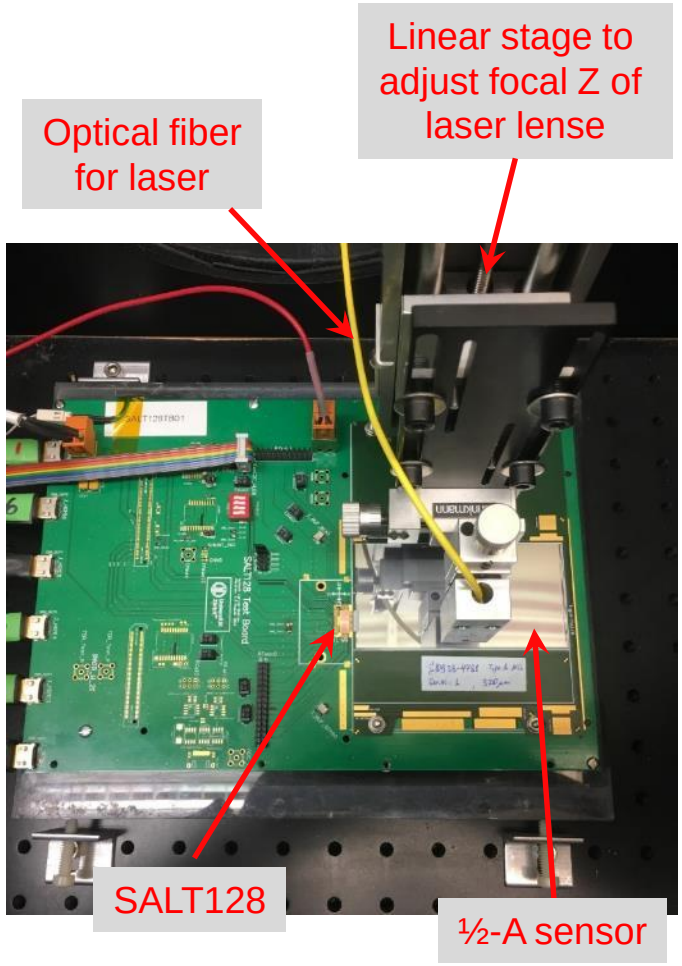
Designed by
Carlos Abellan

Devices & Information Flow

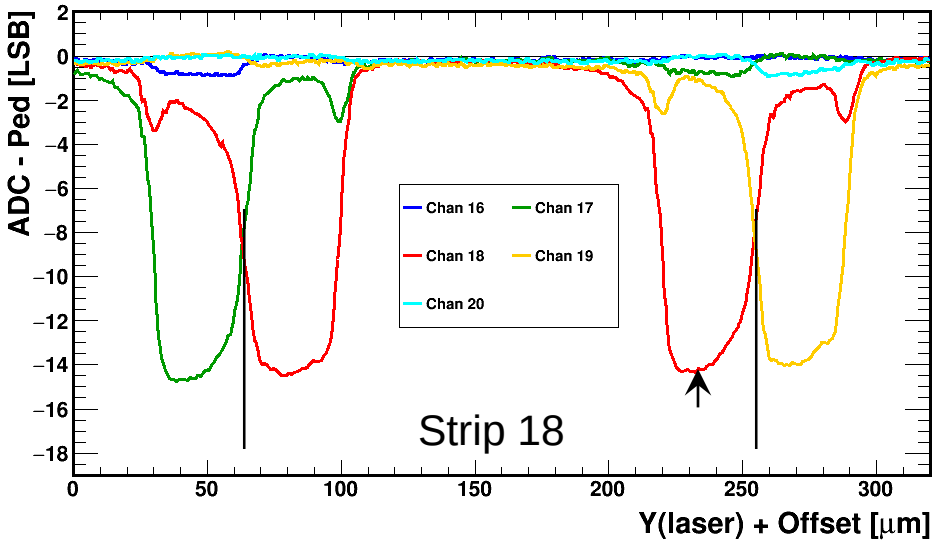


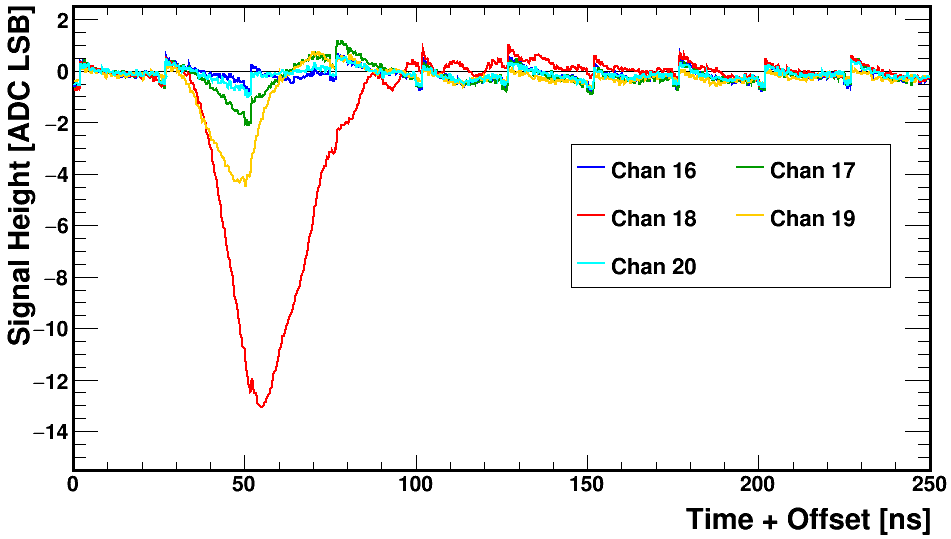
Laser Test Setup





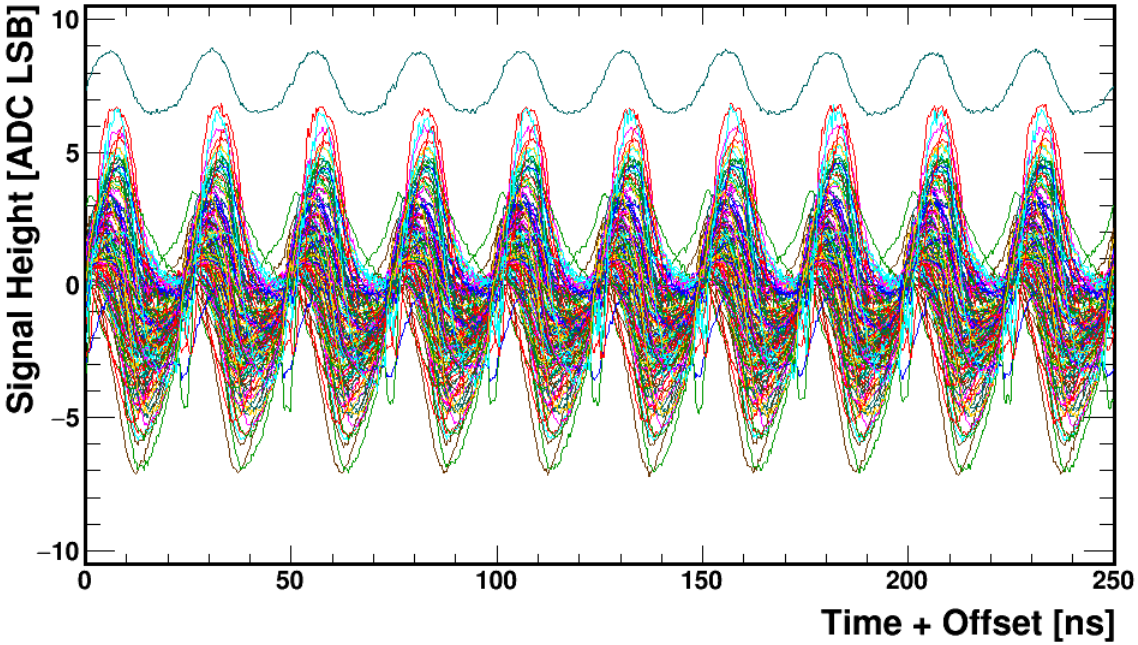
C8+Sensor Y Scan In Laser (Ch 18)



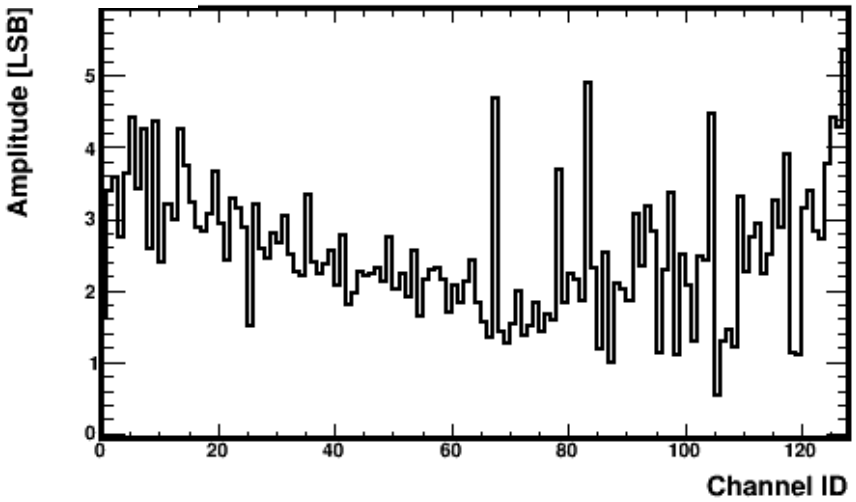


- Channel 18 is a good one. It is used to set up & adjust the laser system.
- The laser beam is focused on ch 18, ~ 20 μm from the border with ch 19 to generate pulse shapes.
- Bandgap parameters were adjusted for C1s. They are still valid and give Vcm ~ 600 mV.
- Analog bias parameters were tuned for C1s with laser source. They will be retuned later as FIB edited ASIC may be different.

C10s Baseline Oscillation

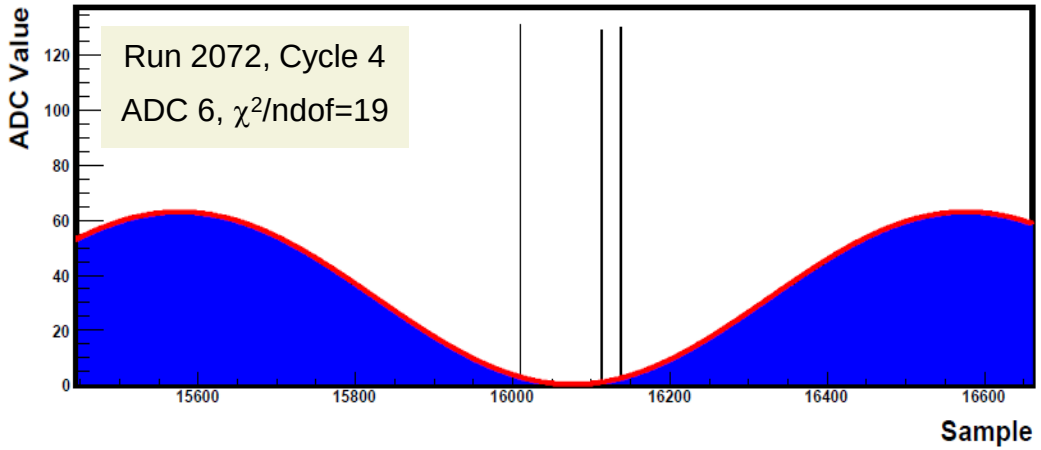


C10 + sensor

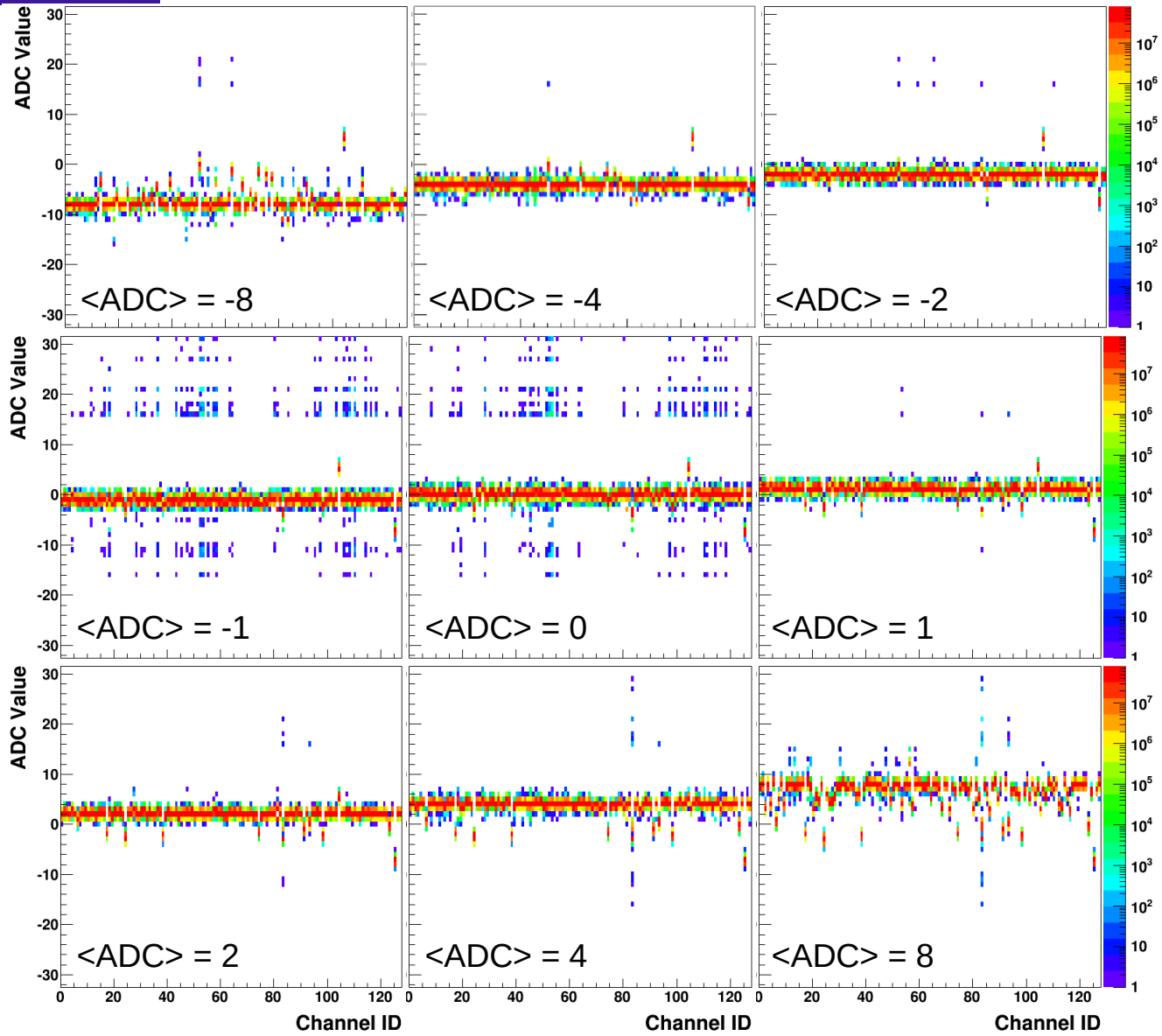


Radiation Test Of SAR ADC

- SALT chip uses 6-bit SAR (*successive-approximation-register)* ADC, which is more susceptible to SEUs.
- A prototype 8-channel ADC (from IBM) was tested in 226 & 60 MeV proton beams at MGH in June 2014.
- Beam intensity: radiation level from ~ LHCb running to ×1000 to boost statistics.
- A 40 KHz sine wave signal was injected & digitized at 40 Msps. A SEU sample can be identified by comparing measurement against expectation from fit.
- A few SEU candidates were observed from 2×10^8 samples. $\Rightarrow$ Whole UT system has ~7×10^{-6} SEU channels per bunch crossing in LHCb nominal running.

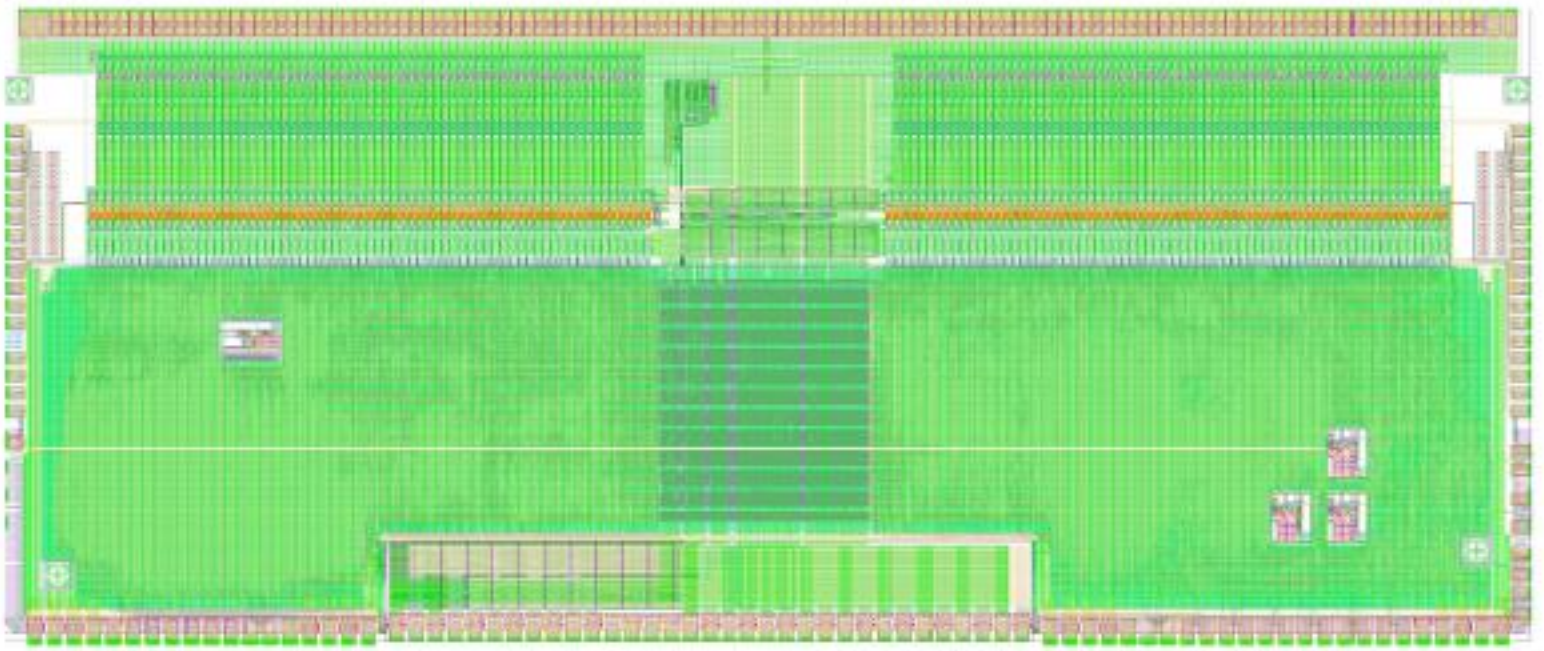


ADC Error vs Value: C10 Post-Irradiation



- 80 M evts/chan/plot.
- After 2 Mrad irradiation in a proton beam.
- TrimDACs are tuned to have same <ADC> for all channels.
- It seems that there are more problems when ADC values ~ –1 to 0.

Layout of New SALT ASIC

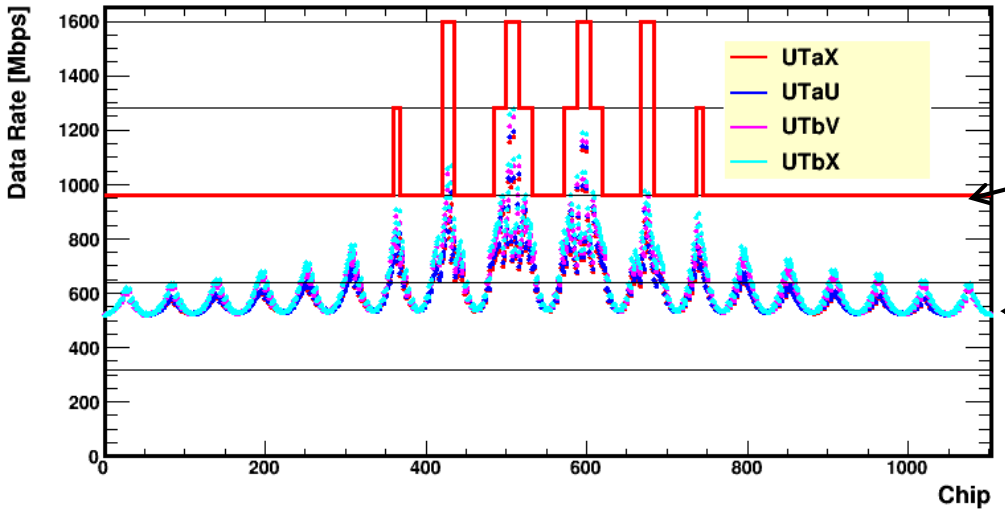


Update of UT Event Packets

Header (12 bits)				Data	Comment
BXID	Parity	Flag	Length		
4-bit	1-bit	1-bit	6-bit	12n-bit	
0000_b	1_b	1_b	$11\ 0000_b$	Not present	Idle packet (append if not enough data)
bxid	*		$01\ 0001_b$		BXVeto
			$01\ 0010_b$		HeaderOnly
			$01\ 0011_b$		BusyEvent (nHits>63)
			$01\ 0100_b$		BufferFull
			$01\ 0101_b$		BufferFullNZS
			$00\ 0110_b$	data	NZS packet, true length is fixed in firmware
	*	0_b	nHits	data	Normal event (nHits≤63)
12-bit bxid				pattern	Synch packet

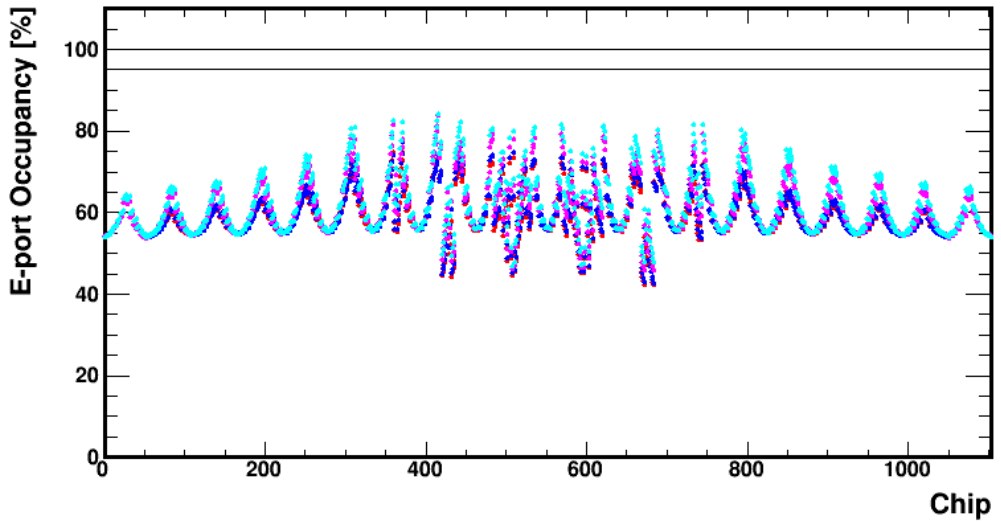
- Memory buffer will not be cleared upon a Synch command. A Synch packet is not required to occupy a full GBT sub-frame. It appends at the end of the buffer just like other types of packet.
- The Synch pattern has a fixed length (12 bits), and configurable, default=0xFFF. Consecutive Synch commands will be sent with a few HeaderOnly's ahead.
- Multiple idle packets instead just 1 are added when there is not enough data. The number of idle packets are factor of ×6, ×8, ×10 for 3, 4 or 5 e-ports/ASIC configurations respectively. The number is configurable, default = 6.

Data Rate And Active E-ports



Capability of active e-ports

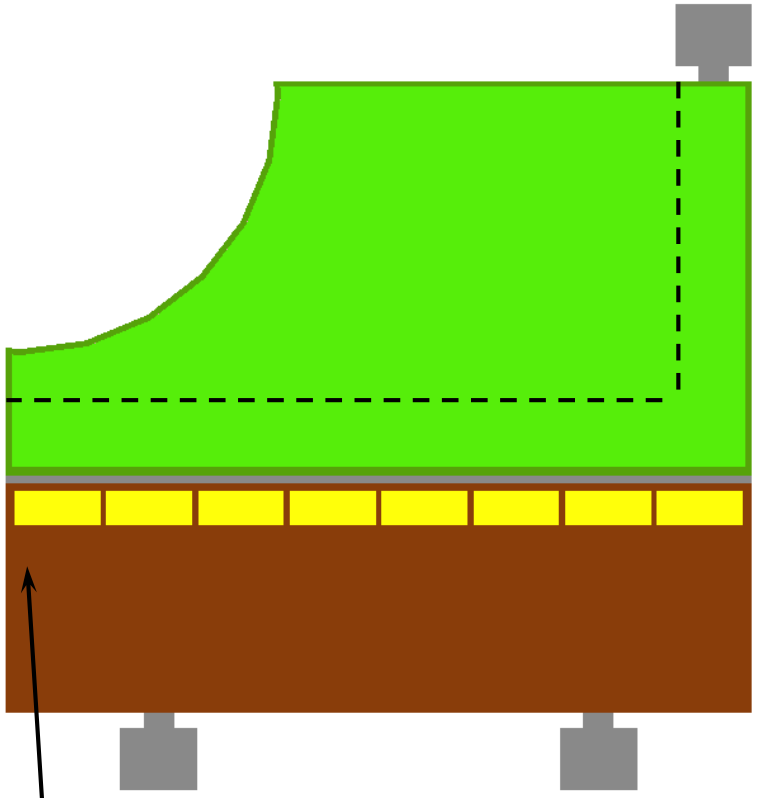
Data rate @ $L=2\times10^{33}$ $cm^{-2}s^{-1}$



- All active e-ports per ASIC together form one lane.
- When event size is not big enough to fill the whole lane, an idle packet(s) is added.

Highest e-port occupancy ~84% @ $L=2\times10^{33}$ $cm^{-2}s^{-1}$

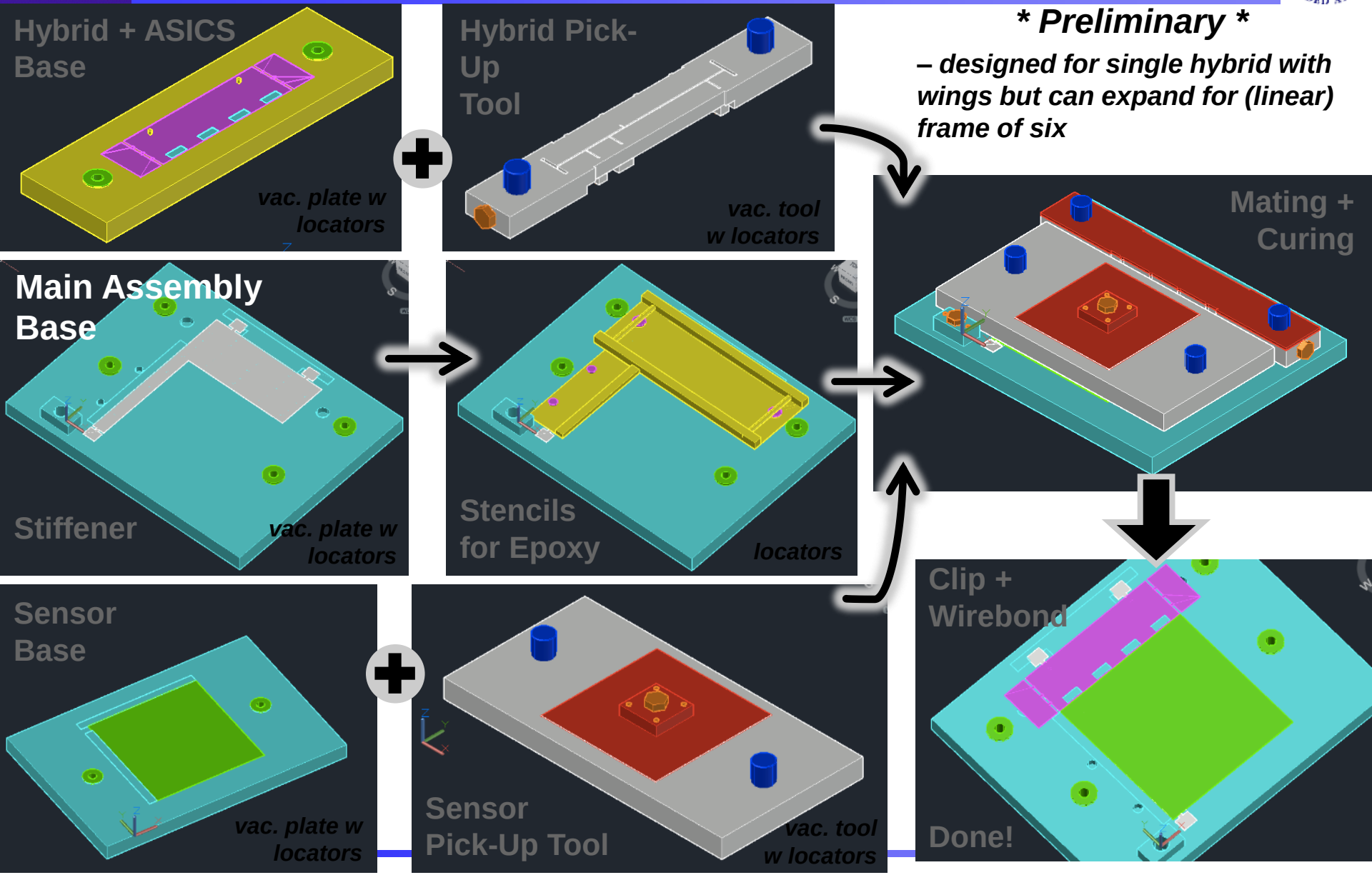
Inter-ASIC Gaps



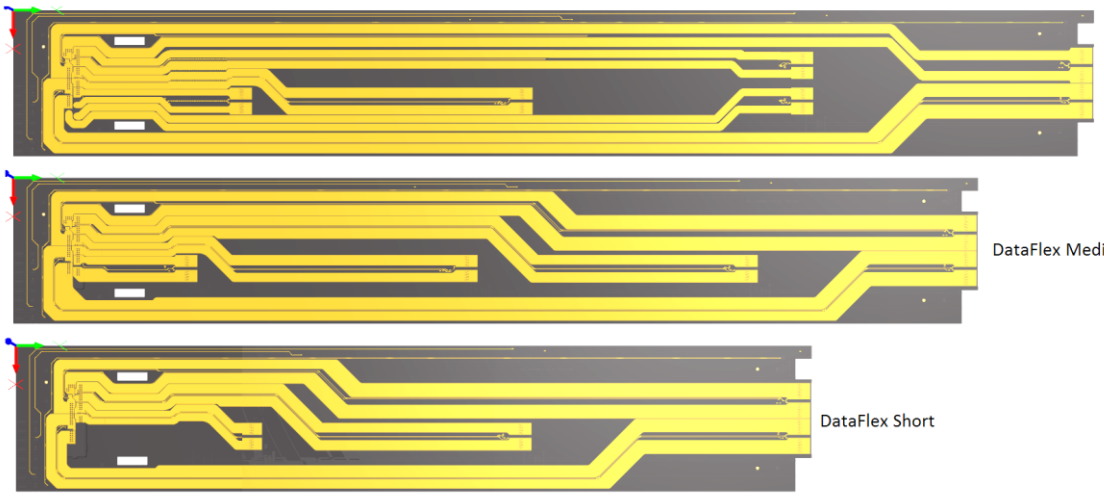
HV filter & connection
on the left side

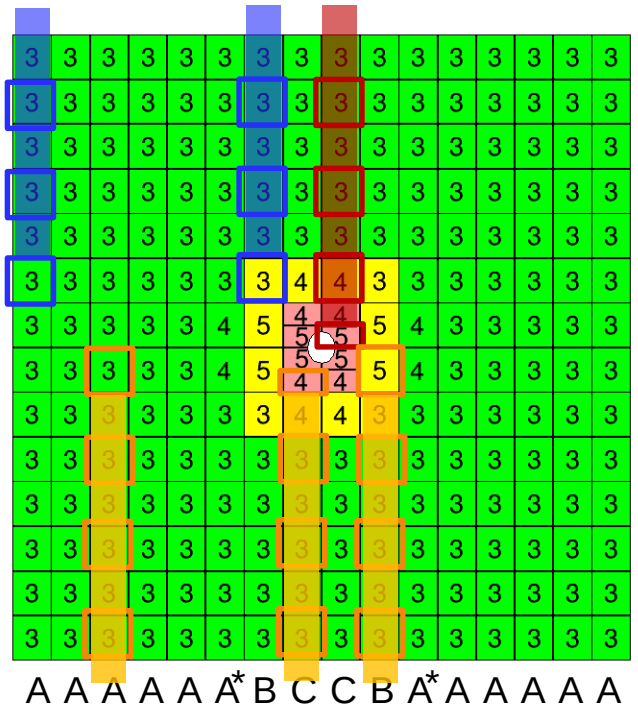
- Chip dimension: 11.2 mm × 4.395 mm
  - Design 10900 μm × 4095 μm
  - Seal ring: 200 μm
  - Dicing: ~100 μm
- Sensor size: 97.5 mm × 99.5 mm
  - Strips (1024): 95.9 mm × 97.9 mm
  - Guard ring: 1.6 mm (2 × 800 μm)
- In a simple design, each ASIC needs to central aligned with a group of 128 strips.
- Inter-ASIC gap = 95.9 / 8 – 11.2 = 0.79 mm.
- Side space = 0.8 mm + 0.79/2 =1.19 mm.
- How much wider can the hybrid flex be? Does it need to be symmetric?
- Which side should the HV connection be?

Module Assembly Procedure



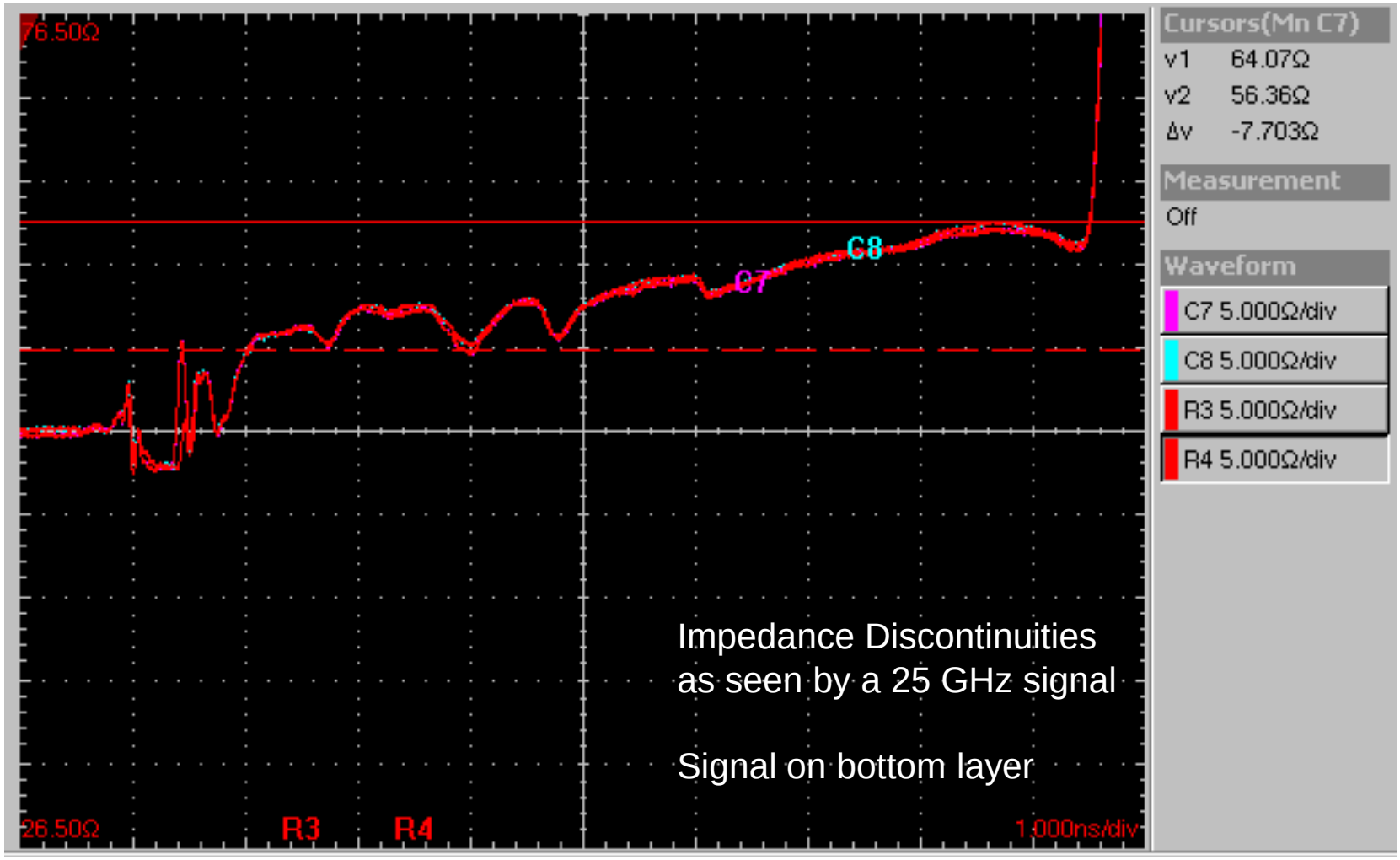
Three Different Designs





- Three different lengths, thus 3 different design minimally:
- Total 272 cables to be mounted: long (16), medium(136), short (120).

G3 Flex Cable Time Domain Reflectometer



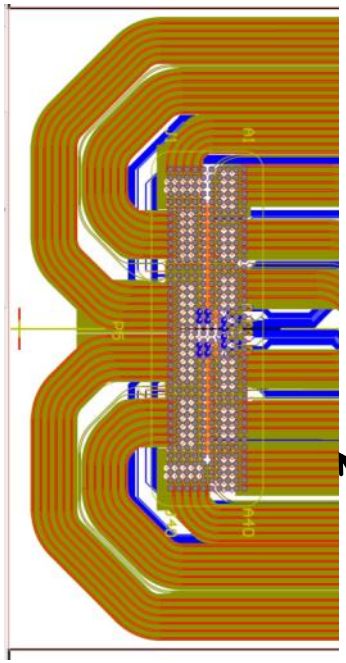
Flex Cable Production

- **No conceptual flaws in the design**
  - Traces size is uniform on the cable, overall, measured with optical inspection
- **Stack-up and trace organization discussed at length and accepted by UT**
- **Some parameters still need to be tuned/measured**
  - Impedance target (100 Ω +/- 10 %) has been almost achieved but we are on the upper limit (~110-112 Ω)
    - → In discussion with manufacturer, a controlled increase of the trace width to reduce Z and resistance of the traces is being done
    - → Mechanical stability/dimensions of sample to sample is being checked
- Prototypes have been made with commercial firms
  - Two potential vendors identified
    - One completely qualified, the second being qualified
    - Prices are different. This large variation not really understood so far
  - CERN shop could act as a backup solution, if necessary

Manufacturer	LOT unit	NRE Tooling Costs	Unitary cost	Delivery time	Accepted quantity	Production capacity
Company 1	7 pieces	$ 600	$ 900	10 wdays	100 %	Max 25/week
Company 2	5 pieces	$ 850	$ 2080	18 wdays	Not yet available	Max 30/week
CERN	10 pieces	N.A>	~ 1200 Euro	~ 10-14 Weeks	80 %	Not known

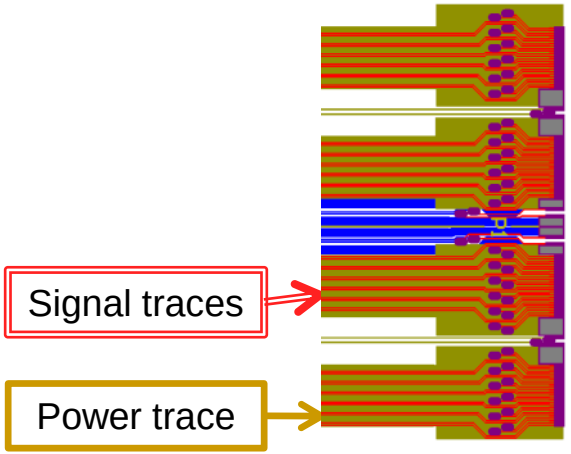
Flex Cables – 2nd Iteration

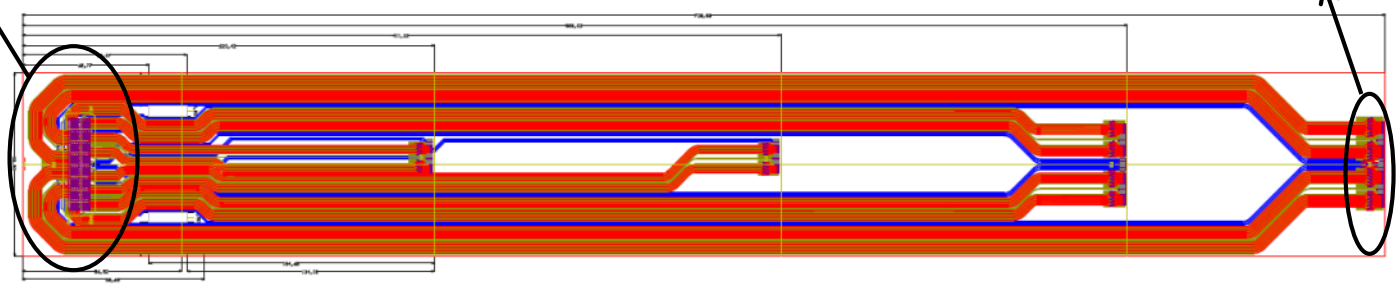
- The 2nd generation design is submitted and will be produced at CERN.
- 4 conductive layers: 2 for signals, 1 for LV power, 1 for test purpose.
- Signal traces run on top of power traces all the way for better impedance uniformity.



Board Stack Report

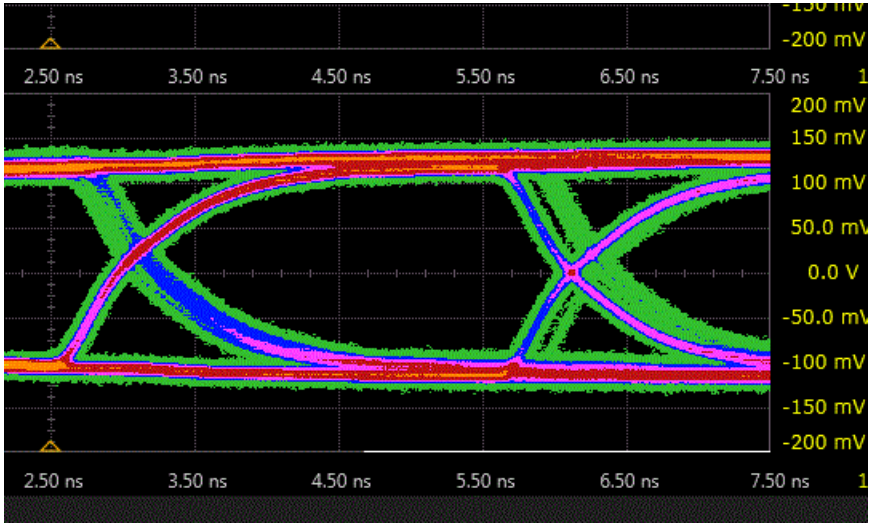
Stack Up			Layer Stack			
Layer	RIGID STACK	FLEX STACKUP	Name	Material	Thickness	Constant
1			Top Paste			
2			Top Overlay			
3			Top Solder	Solder Resist	0,010mm	4,8
4			Top Layer	Copper	0,017mm	
5			Dielectric1	Poliammide	0,100mm	3,4
6			Inner-1	Copper	0,017mm	
7			Dielectric2	Poliammide	0,100mm	3,4
8			Inner-2	Copper	0,017mm	
9			Dielectric3	Poliammide	0,100mm	3,4
10			Bottom Layer	Copper	0,017mm	
11			Bottom Solder	Solder Resist	0,010mm	4,8
12			Bottom Paste			
	Height : 1.6mm	Height : 0,388mm				



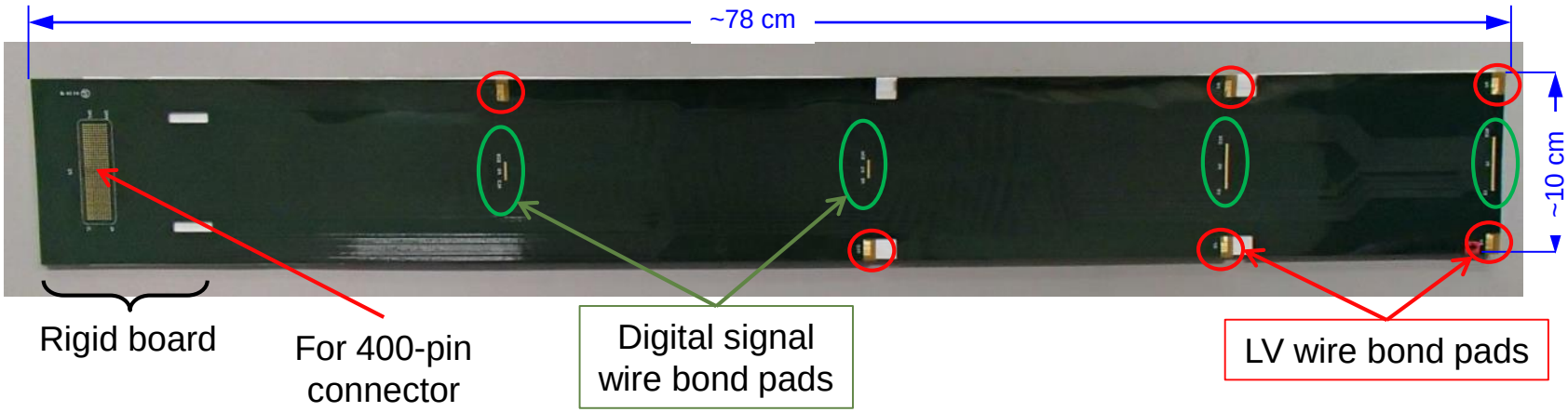


Flex Cables

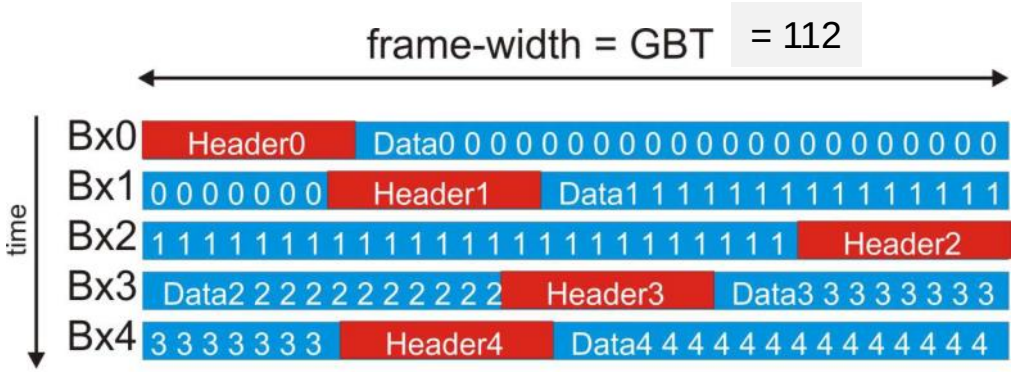
- 4 flex cables per stave for digital signals (up to ~240/cable), LV & HV powers.
- Requirements:
  - Signal integrity.
  - Low material budget.
  - LV round trip drop < 0.5 V (for ~2.5A).
- 1st iteration cables made, single pair signal quality OK, low yield in production.
- 2nd generation design is submitted and will be produced at CERN.



1st iteration cable

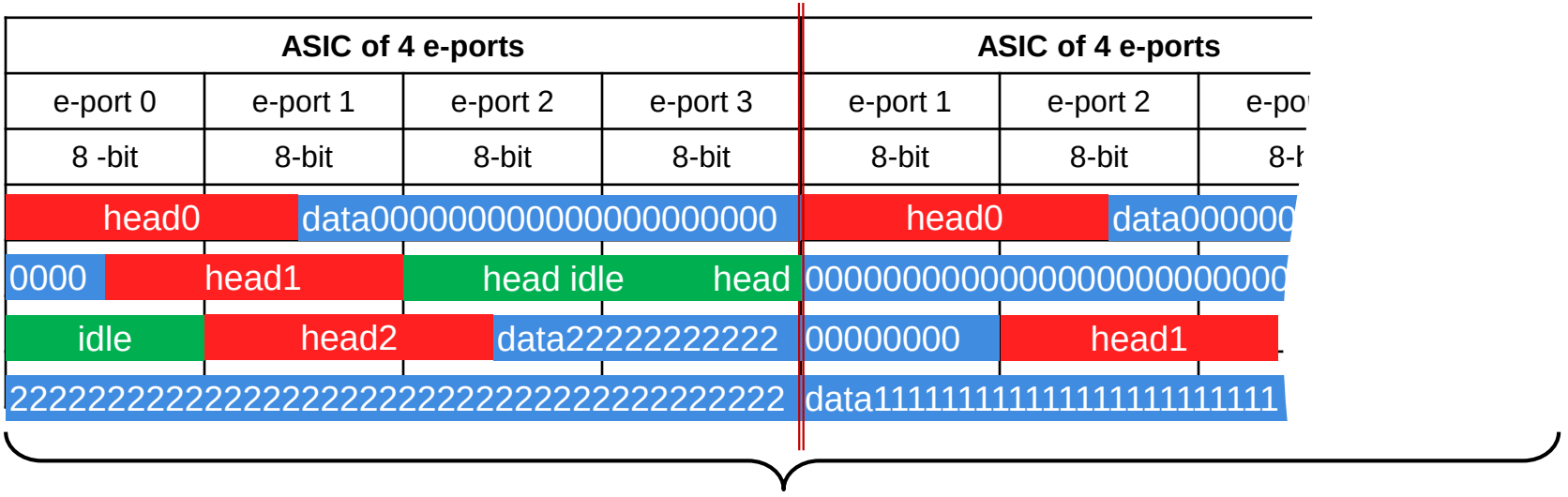


UT GBT Sub-Frame Format



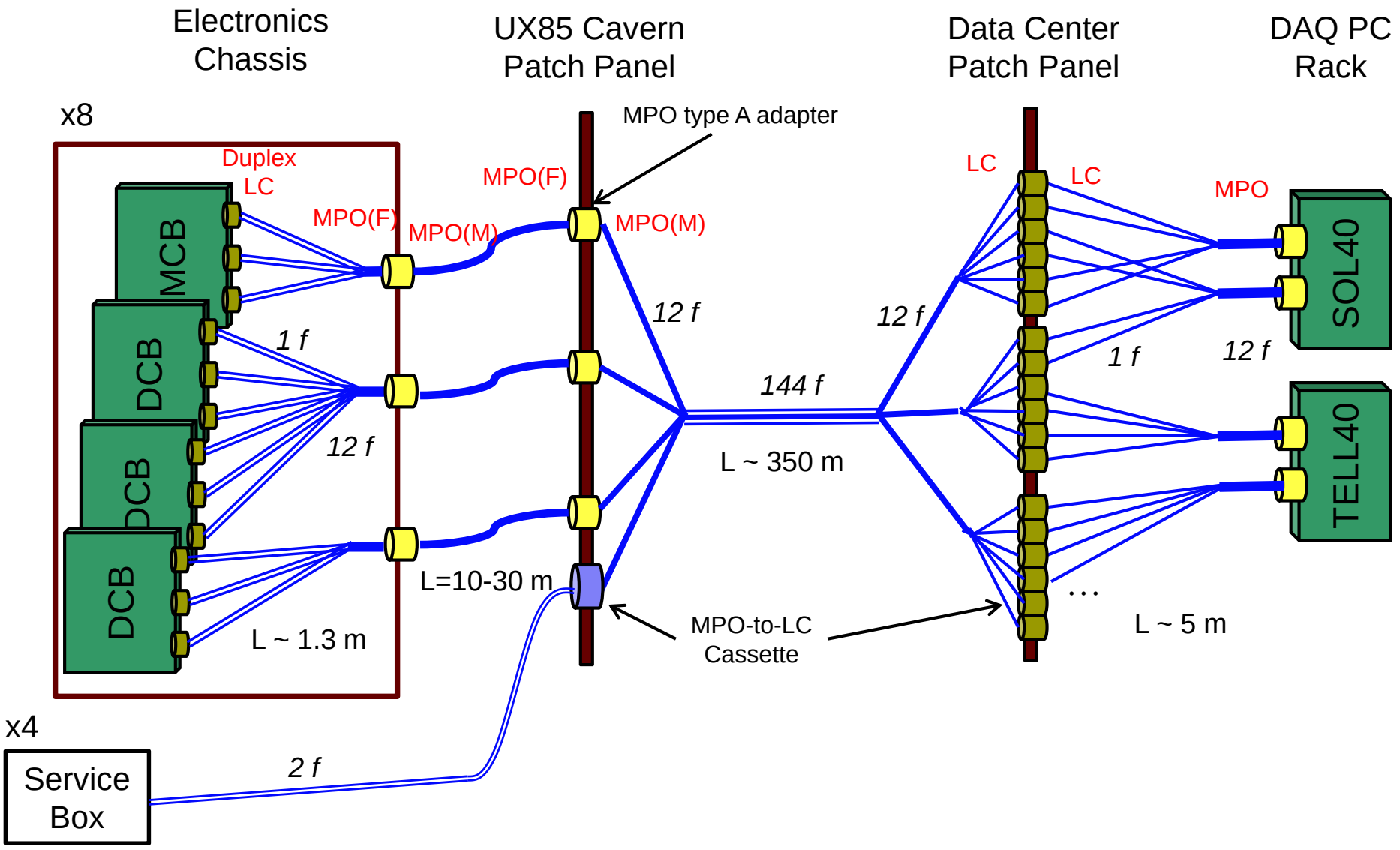
From "Electronics Architecture of the LHCb Upgrade" http://cds.cern.ch/record/1340939

UT ASICs are independent. E-ports within an ASIC send data coherently. Each ASIC data form its own GBT sub-frame.

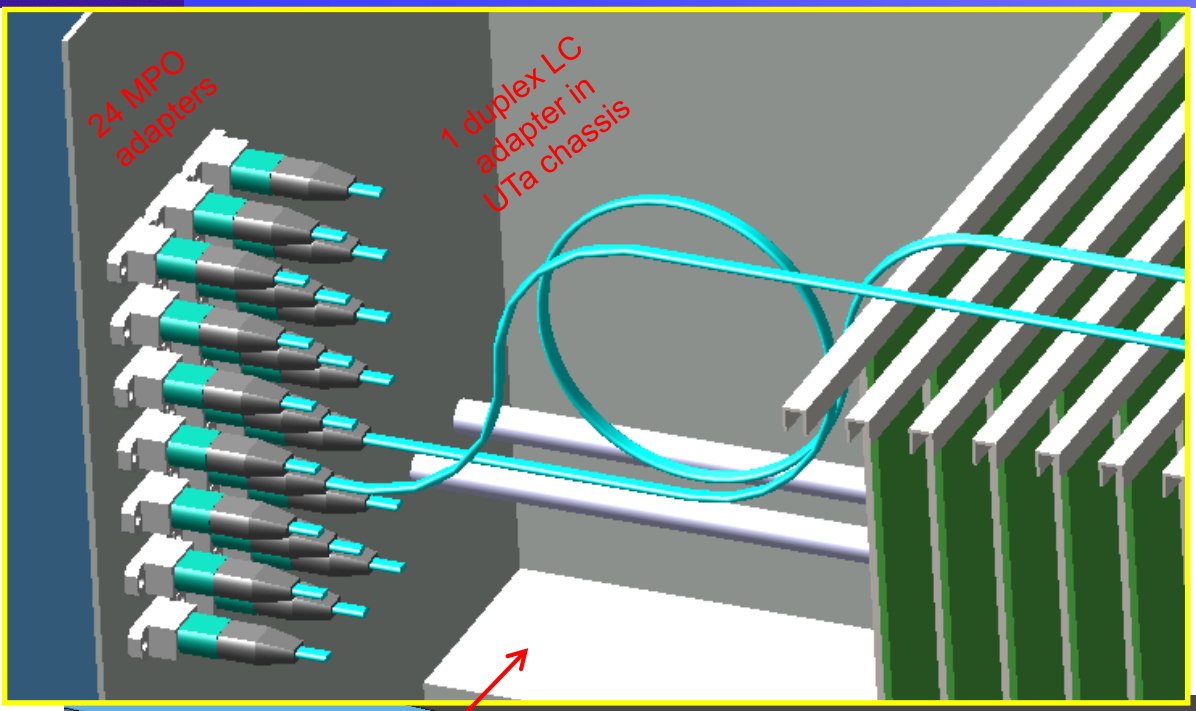


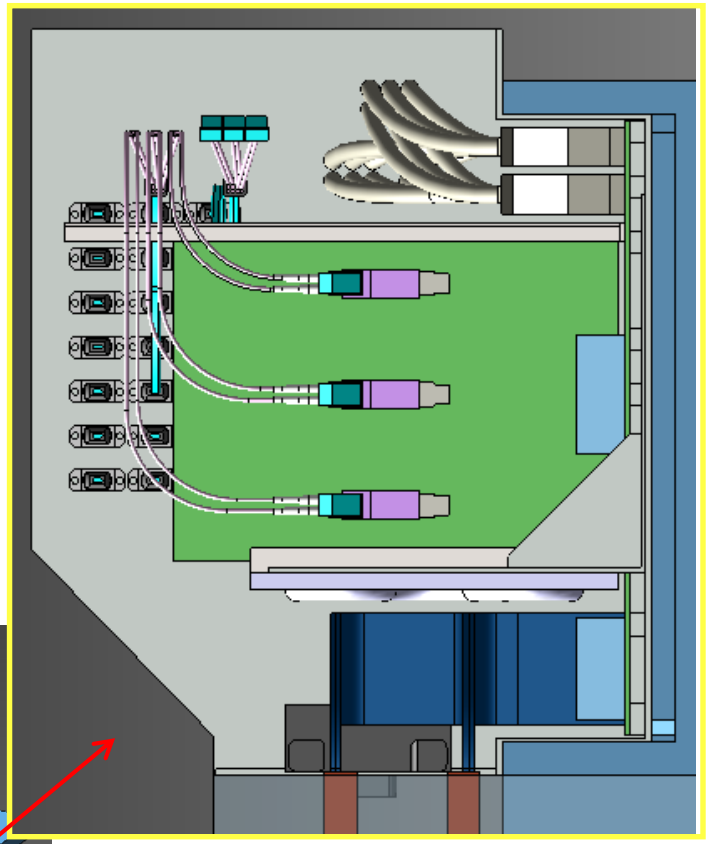
Up to 14 e-ports per GBTx

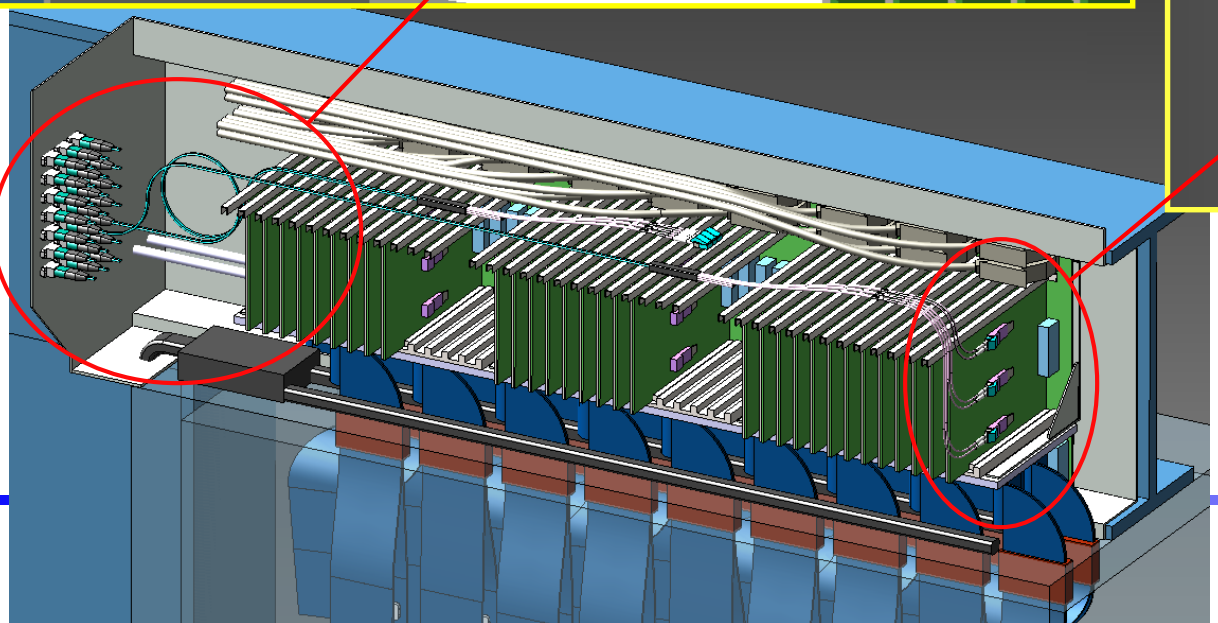
UT Optical Connection



Optical Connections In PEPI Chassis

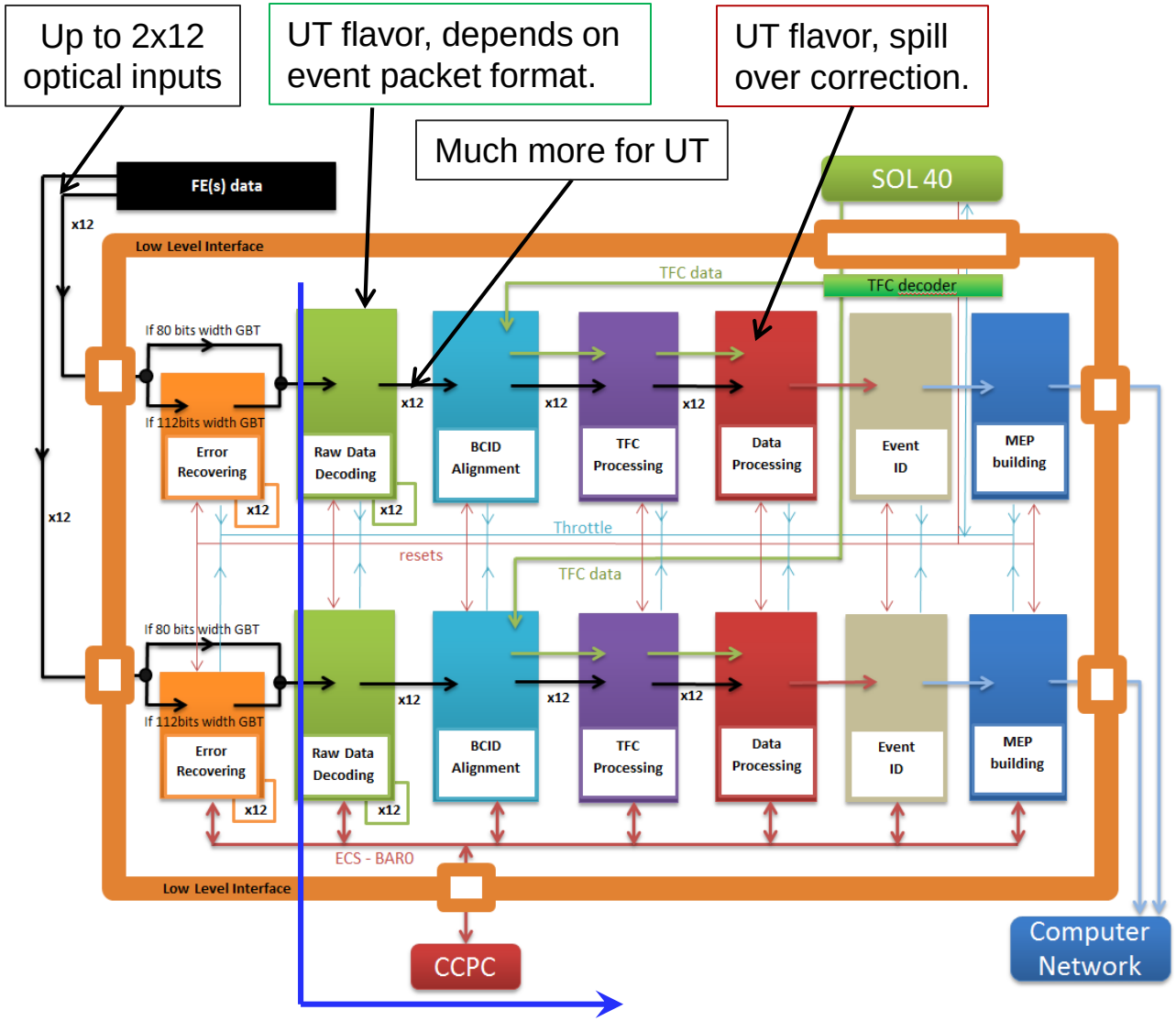






Drawing by Jason

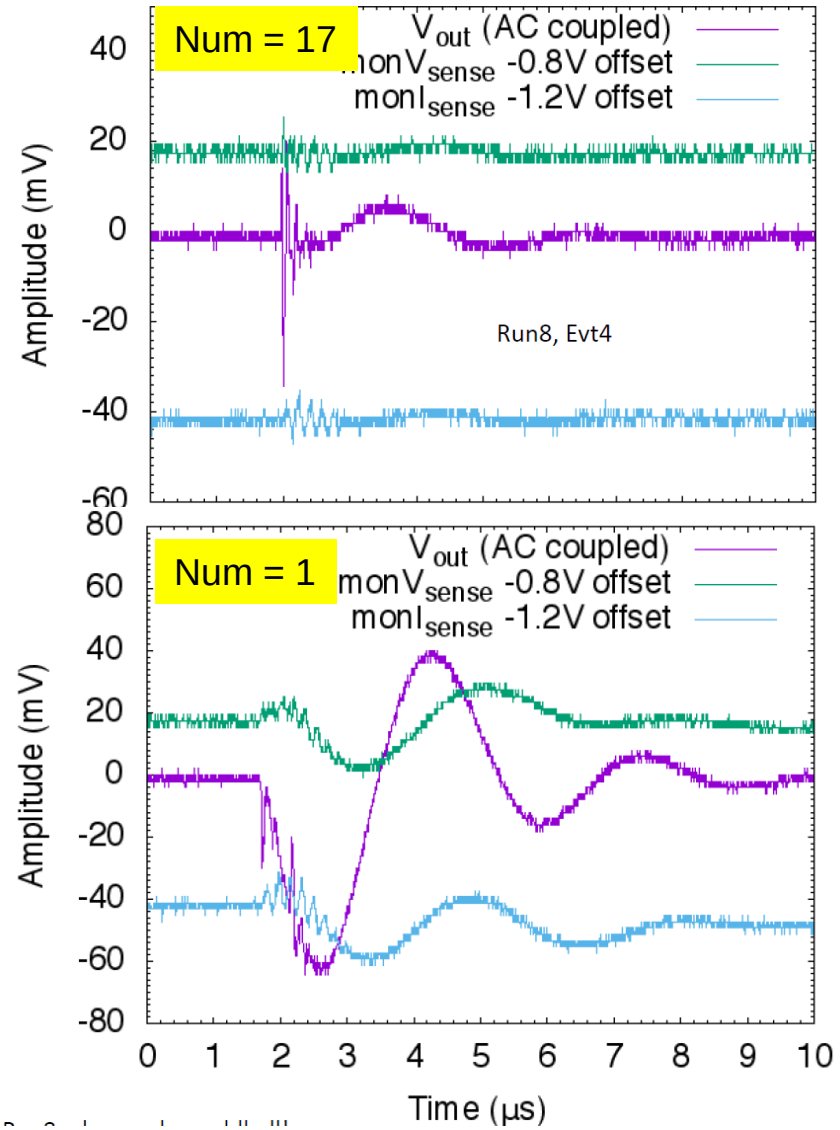
TELL40 Firmware Blocks



Depends on number of sub-frames (ASICs)

- Less than 24 GBT frames × sub-frames inputs due to limited resource in FPGA.
- An early study indicates that resource consumed in LLI & error correction is relatively small. One TELL40 can handle 18 optical inputs.
- Since the number of ASICs is unchanged, ~13% increase of GBTx does not change much the number of TELL40 boards.

SET Test of LV Regulator Board

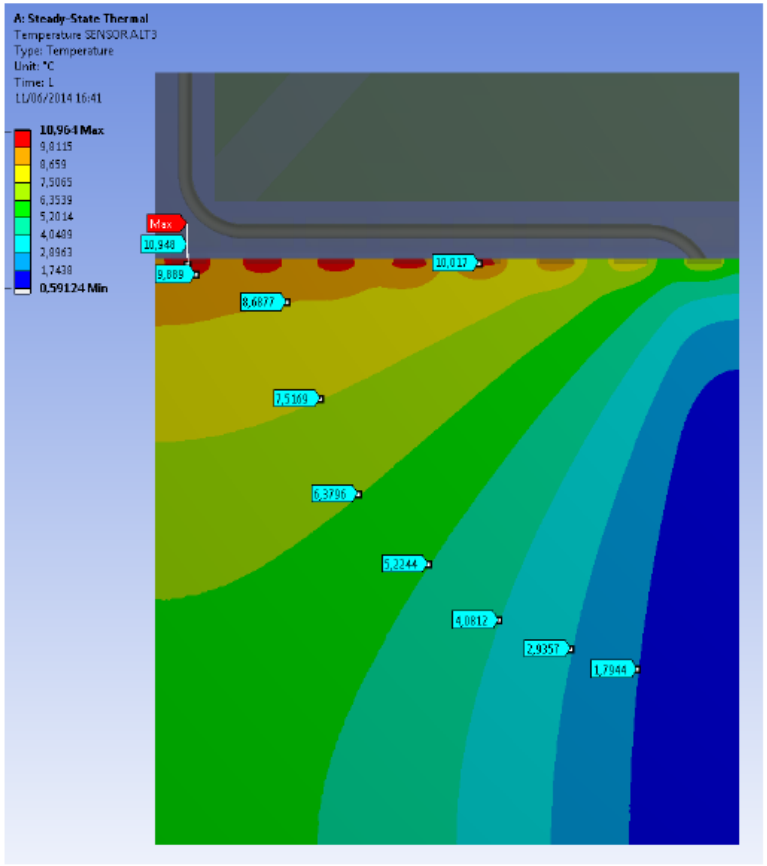


Extracted from slides by Brian Hamilton

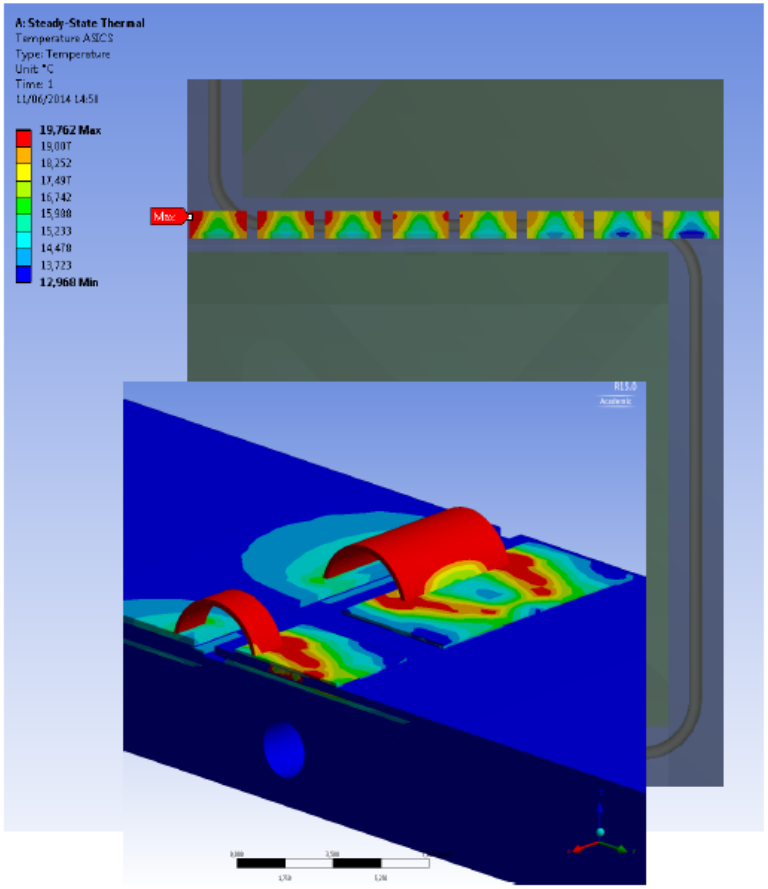
- Successfully tested in a proton beam at MGH, with radiation level varying from LHCb level to much higher, total dose ~ 20 kRad.
- Monitoring voltages at a few key points, and trigger on SET signature.
- Expect more SETs from OpAmps than rad-tolerant LHC4913 LV regulator.
- Observed much less SET (#=1) from OpAmps than from LHC4913 (#=17).
- Overall SET rate is very low. And the amplitude is small.
- Ready to move forward with a next iteration LV regulator board.

Thermal Simulation

sensor temperature



ASICs temperature



Stave Deformation After Cooling Down

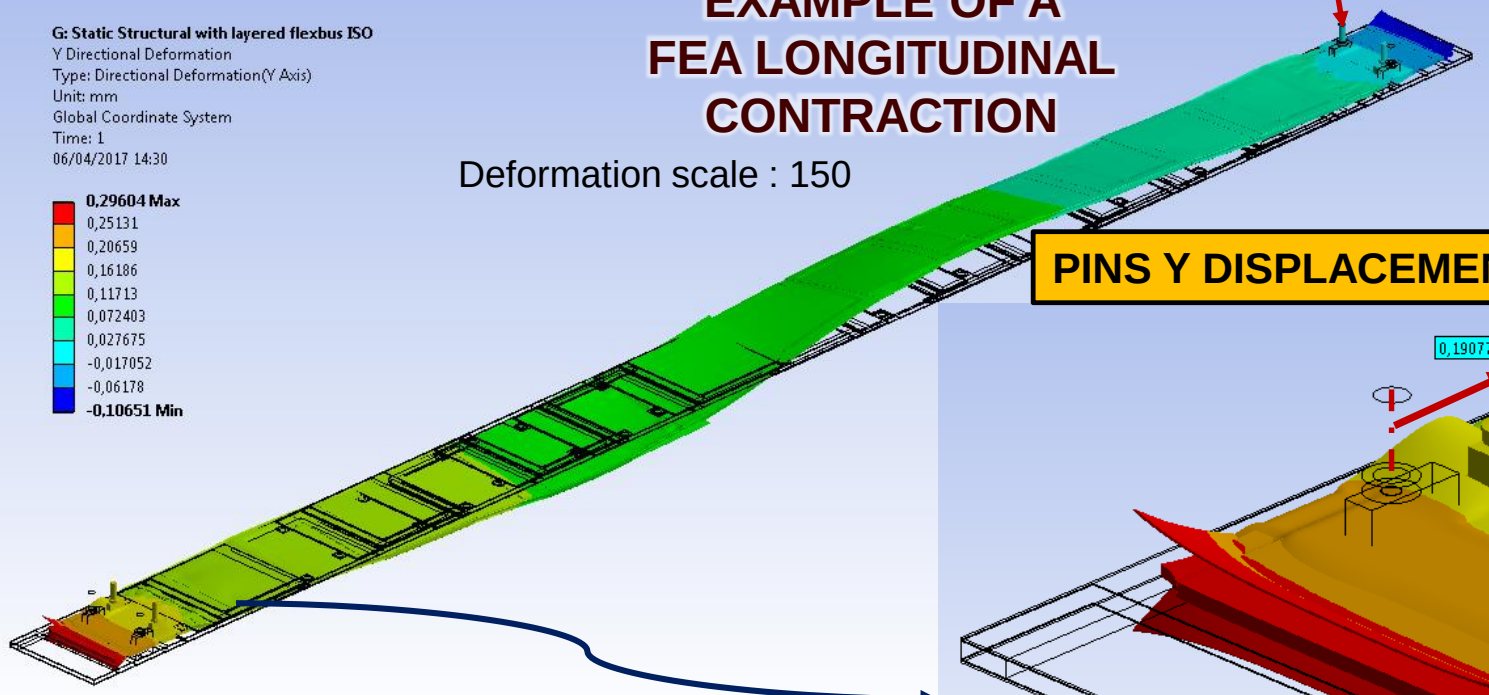
THERMAL LOAD IN THIS EXAMPLE
ΔT = - 45 °C, from +20 °C to – 25 °C
Not the designed ΔT

REFERENCE PIN

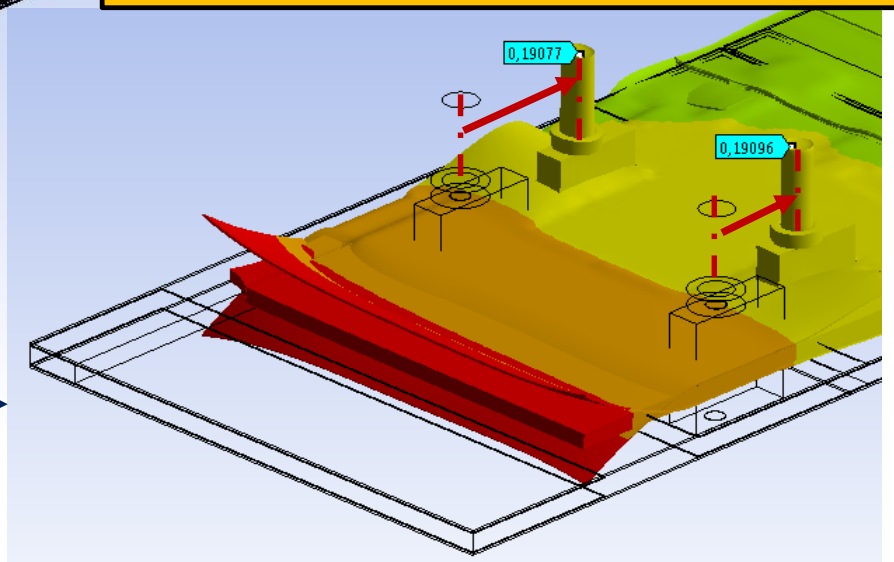
THERMAL CONTRACTION
ΔL = L * CTE * ΔT

EXAMPLE OF A FEA LONGITUDINAL CONTRACTION

Deformation scale : 150



PINS Y DISPLACEMENT: UY = 190 µm



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