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DRX-II chip for the optical links upgrade of the ATLAS Pixel Detector

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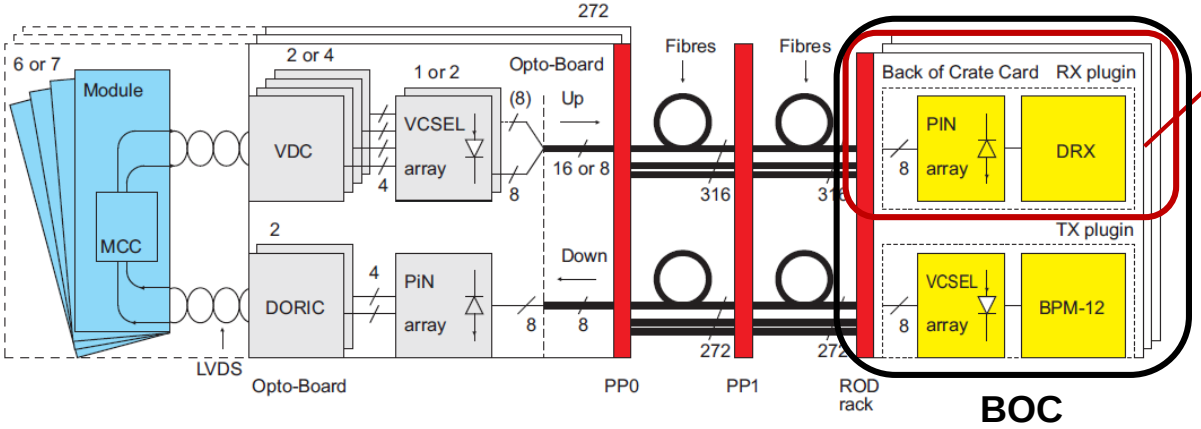
ATLAS Pixel Detector optical links

Elements and path of the optical link from the MCC to the Pixel DAQ



Rx plugin (optical receiver)

→ To convert the attenuated (due to fiber loss) and distorted (owing to the channel dispersion) light signal into digital data

- Optical readout of the L1/L2 will suffer from bandwidth limitation after LS1
- A wider range of threshold setting will help operations
- Option is to use new BOC for pixel operation
- Commercial optical receivers can NOT cope with NRZ (Non Return to Zero) signal
- Old Rx design has different connector, and old DRX chip is NOT available anymore

New Rx plugins needed

Link occupancy at 75 kHz L1 Trigger					
	μ	B-Layer	Layer 1	Layer 2	Disks
50 ns	37	39%	34%	52%	30%
25 ns; 13 TeV	25	35%	31%	48%	27%
	51	53%	59%	66%	39%
	76	71%	73%	111%	64%

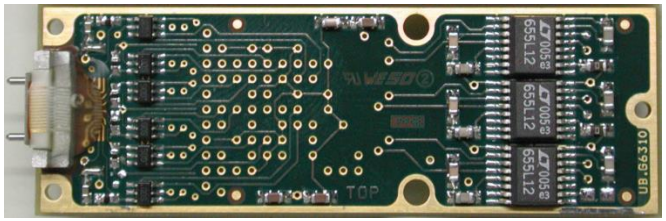
Link occupancy at 100 kHz L1 Trigger					
	μ	B-Layer	Layer 1	Layer 2	Disks
50 ns	37	51%	45%	69%	40%
25 ns; 13 TeV	25	47%	42%	65%	37%
	51	71%	67%	88%	52%
	76	95%	97%	148%	75%

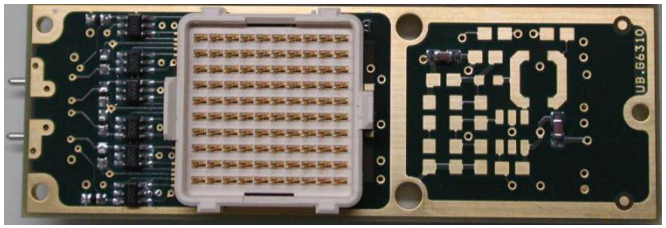
Project requirements

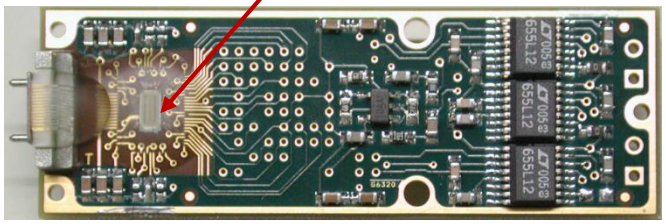
- Should operate with NRZ signals (as in Pixel operations) at 80Mbps
- Have stable operation over a wide range of light power received/input current: from 10 μA up to few mA
- Have independent thresholds for all 12 channels
- Have a BER (Bit error rate) < 10^{-11} after aging
- Should be able to perform a measurement of the input current/light power in order to monitor the stability of the on-detector VCSELS

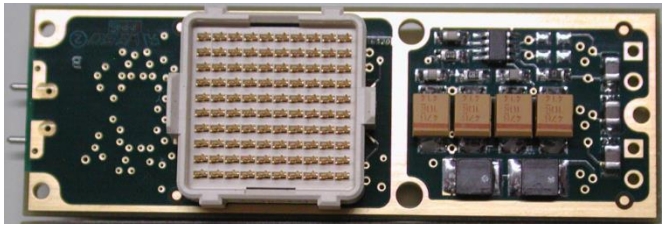
Rx plugin designs

- **Two alternative designs developed: sharing the same optical package, mechanical package and dimensions, but with different data receiver solutions**
- **Discrete solution (P. Lutz, BERN)**
  - **Commercial discrete components**
  - **Using a pull-up resistor and a discriminator**
  - **No amplification applied**
- **ASIC solution (Y. ZHANG, IHEP)**
  - **Full custom design integrated circuit**
  - **Two amplification chains**
  - **Optimized at 80 MHz**

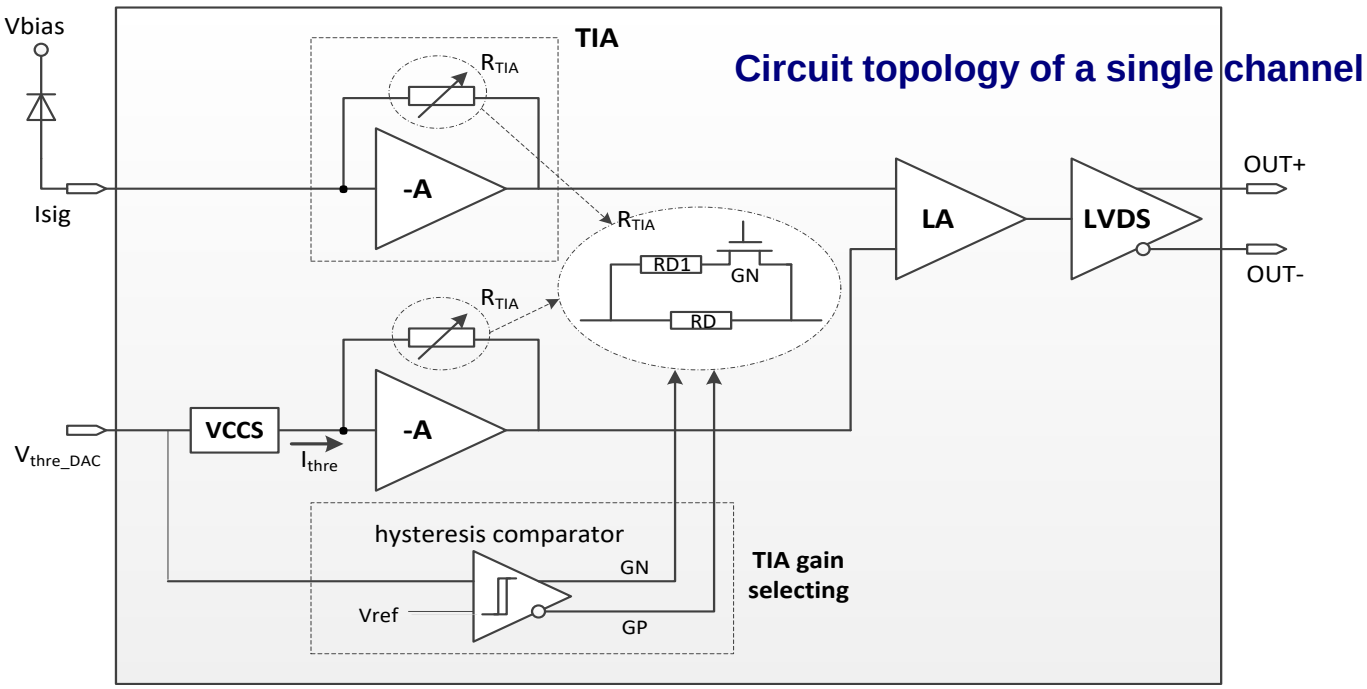








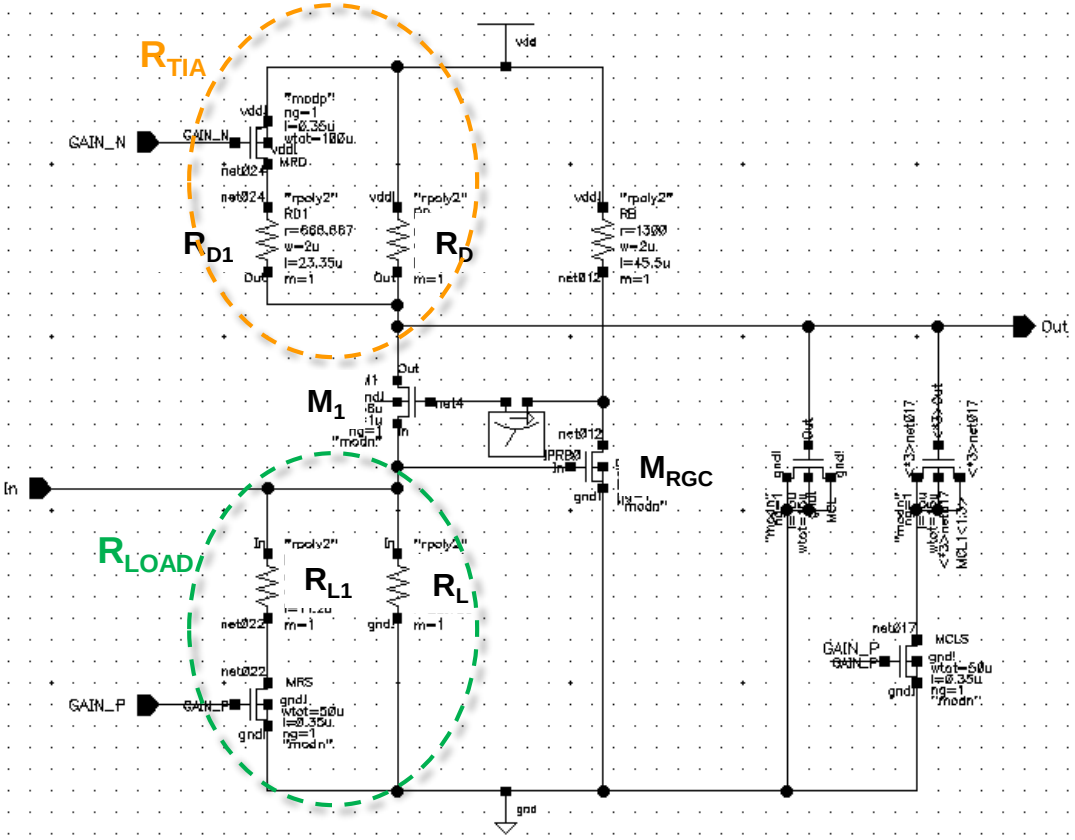
DRX-II chip design (1)

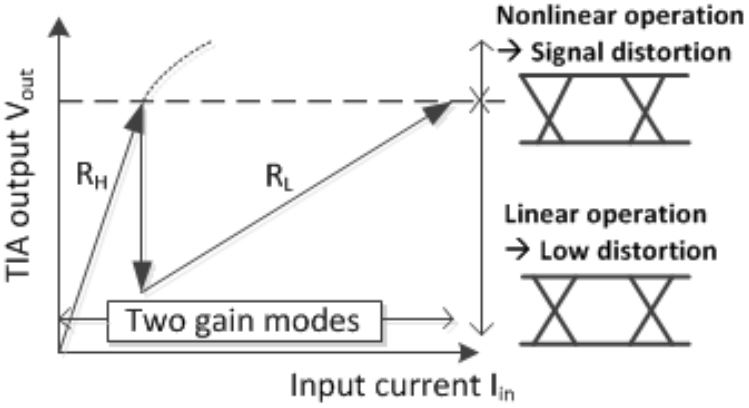


- A single channel consists of two transimpedance amplifiers (TIAs), a voltage-control-currents block (VCCS), a comparator, a limiting amplifier (LA), and an LVDS output driver.
- A two-gain TIA is proposed to extend the effective dynamic range → good linearity over the complete input current range of 10 μA to 2.4 mA
- Designed and fabricated in AMS 0.35 μm CMOS process

DRX-II chip design (2)

- **TIA with two gain modes**
  - **TIA core: RGC (Regulated-Cascode) topology, featuring low input impedance**
  - **Two alternative transimpedance gain controlled by switched**





High gain $R_H = R_D$

Low gain $R_L = R_D \parallel R_{D1}$

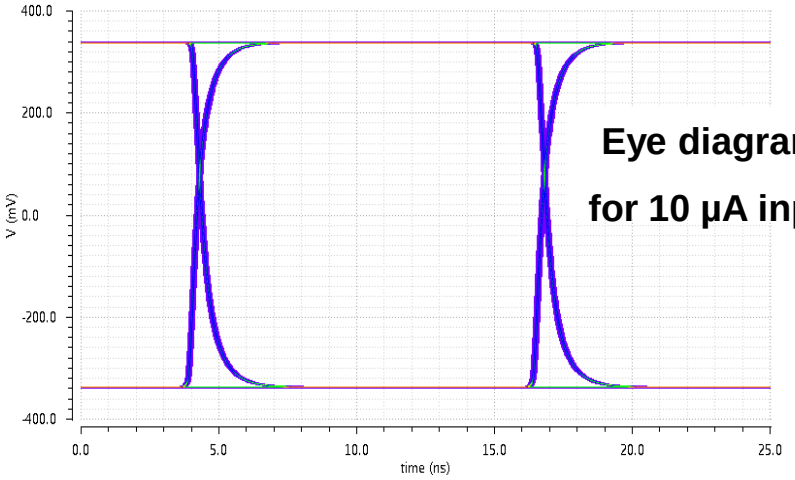
For stable operation in each gain mode, the load resistance linked with the transimpedance gain is also changed.

High gain $R_{LOAD} = R_L$

Low gain $R_{LOAD} = R_L \parallel R_{L1}$

DRX-II chip design (3)

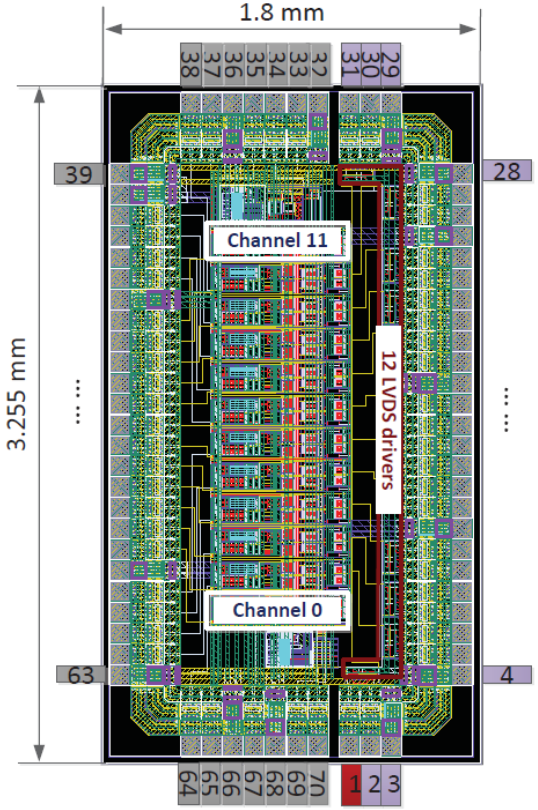
- **Simulated performance of a single channel:**



Eye diagram @ 80Mbps

for 10 μA input with noise

Symbol	Parameters	Typical value	Unit
VDDA/VDD	Power supply	3.3 ± 10%	V
I_p	Supply current	154 to 178	mA/Chip
R_{LOAD}	Output loading	50	Ω
V_{thr}	Individual threshold voltage	0 to 2.5	V
V_GS	TIA gain transition reference voltage	0.45	V
R_T	TIA transimpedance gain	2.5/0.5	kΩ
I_{in}	Linear dynamic input range	10 to 2400	μA
	Data rate	80	Mbps
J_p	Output jitter peak-to-peak	340	ps



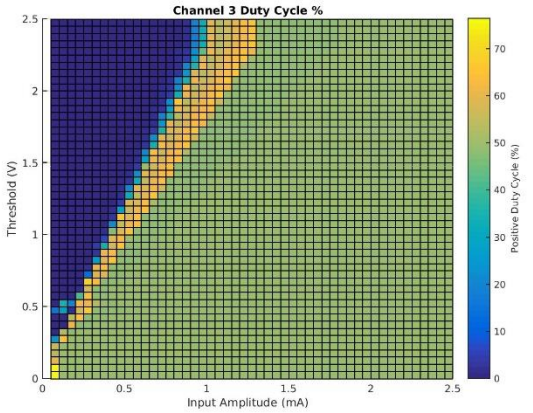
Designed in 2014, using the AMS 0.35 μm CMOS process

DRX-II chip test

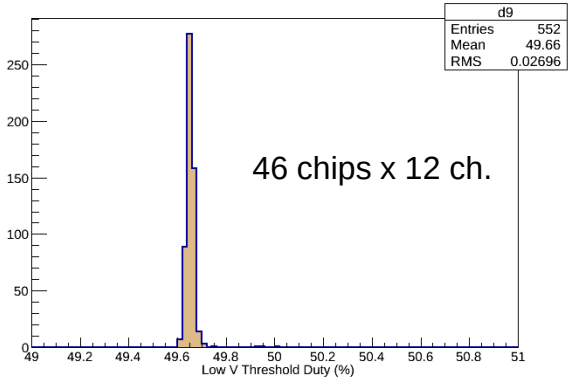
- **All DRX-II chips tested through a custom probe card, stable performance stable among different chips**

Work done by Ohio State University

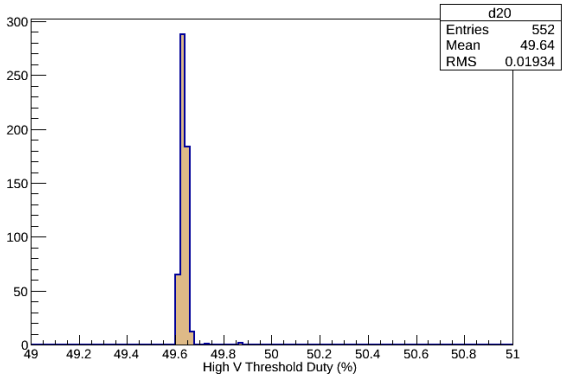
- Pulse generator input
- Test one channel at a time, with the high/low gain mode; measure supply current, LVDS levels and duty cycles
- Repeat test for all 12 ch.



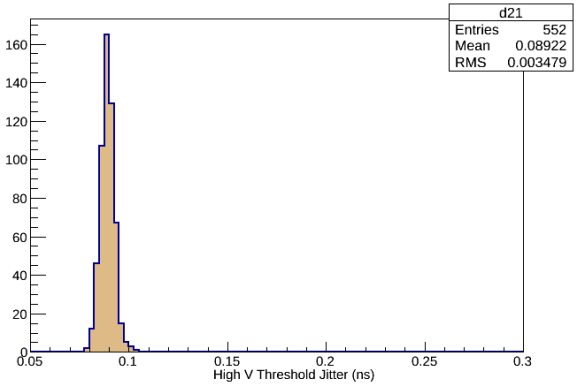
Duty cycle @ low gain



Duty cycle @ high gain



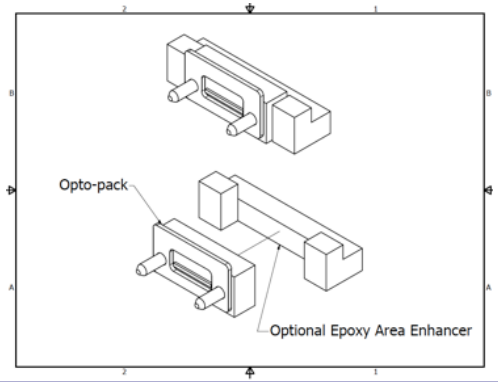
Jitter @ high gain

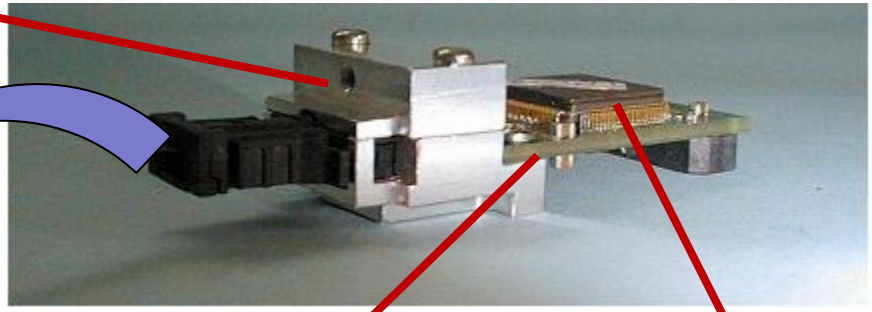


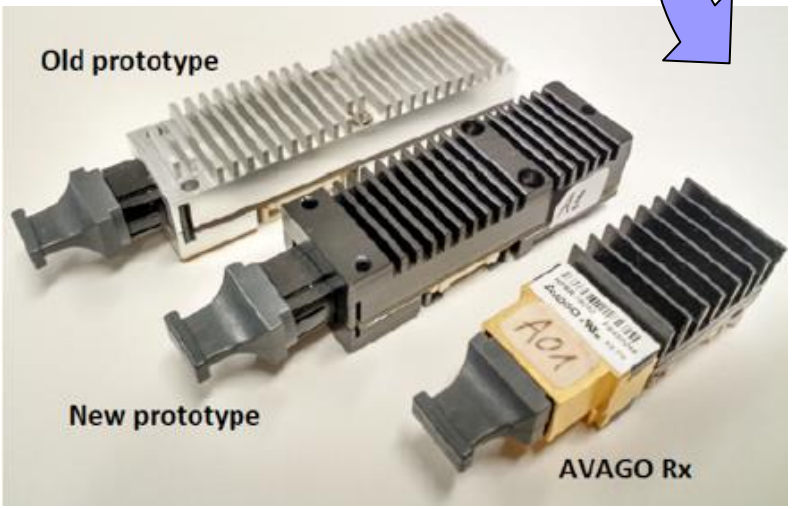
Rx plugin prototype

Optopackage:

provided by OSU







PCB + connector

Designed, loaded, and tested in Bern

Readout electronics:

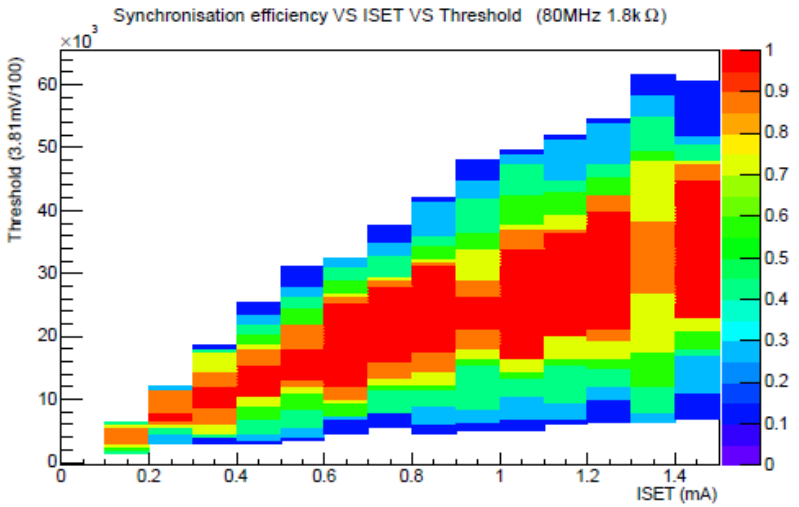
DRX-II chip (IHEP) or

Discrete components (BERN)

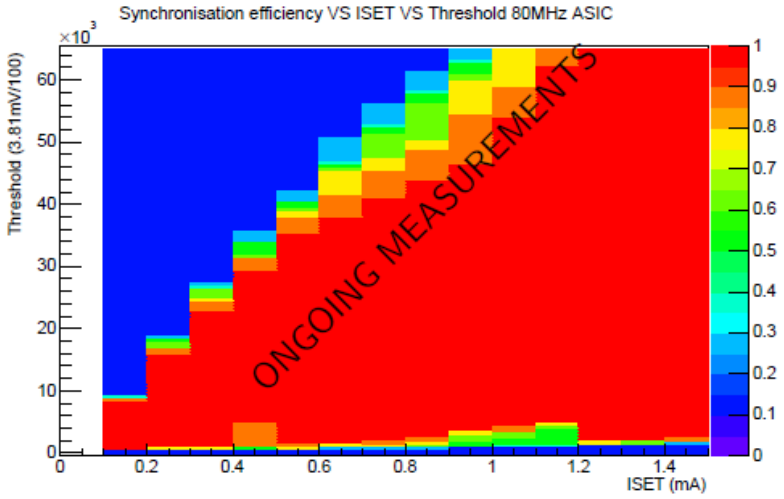
Rx plugin test (1)

- **Synchronization test: the BOC over samples the received signals in order to be able to synch its clock with the incoming signal**
- **Keep on sending an idle word and trying to synchronize on it, scanning thresholds of the prototype and the optical power of the optoboard**
- **synchronization efficiency = No. of synchronized channel/No. of total ch.**

Discrete



ASIC Synch



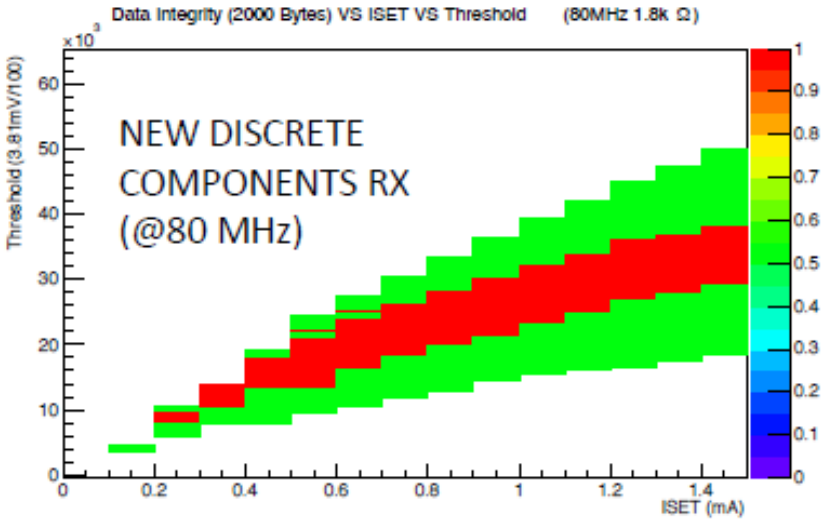
Range of the ASIC significantly broader than the discrete design

Work done by Bern U. & IHEP

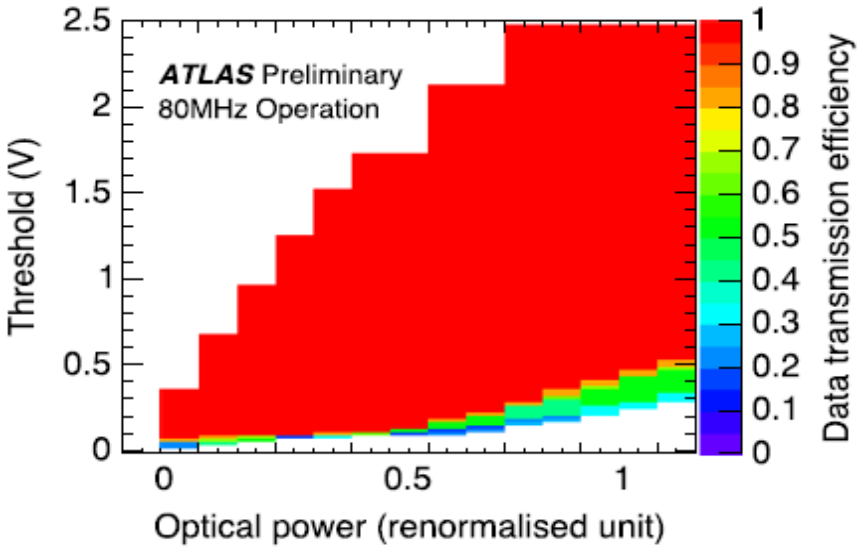
Rx plugin test (2)

- **Data integrity test: in the region where the BOC synchronized, scan sending 10 bytes 8b/10b encoded, including start and end of frame words, 200 times for a total of 2000 bytes**
- **Data integrity efficiency = No. of working channel/No. of total ch.**

Discrete



ASIC



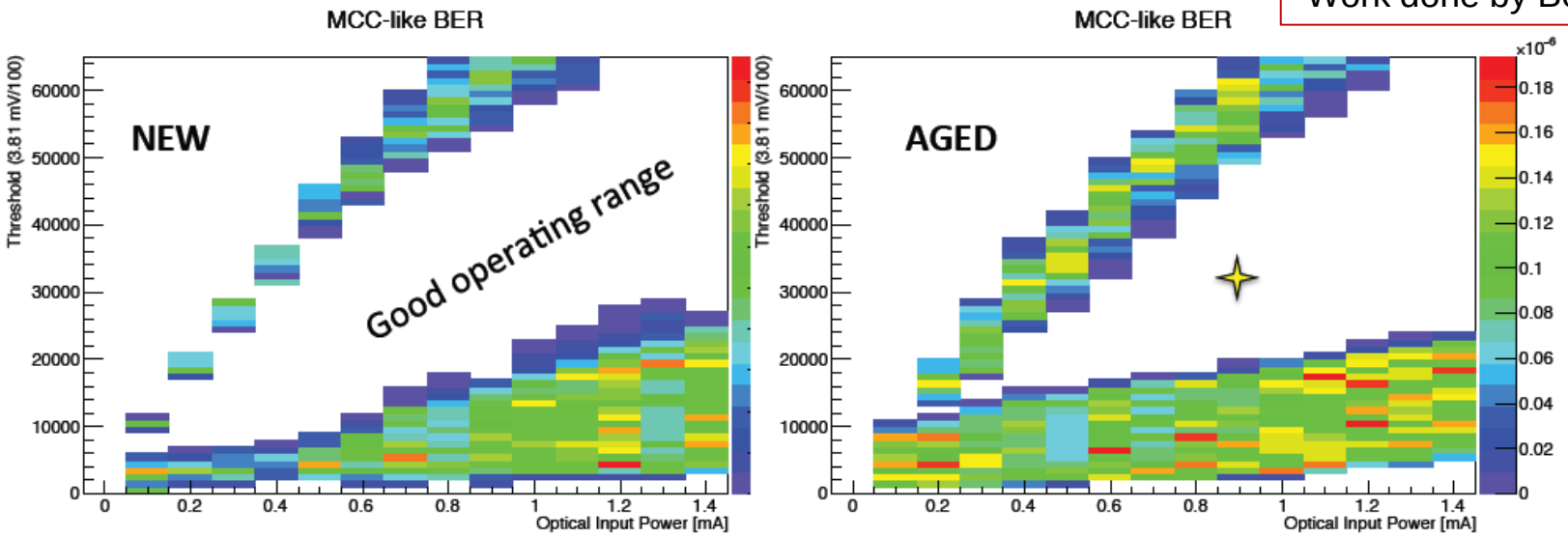
Range of the ASIC significantly broader than the discrete design

Work done by Bern U. & IHEP

Rx plugin test (3)

- **DRX-II chip has been selected as the baseline design for the L1/L2 upgrade, more functional tests performed during pre-production**

Work done by Bern U.



All the tested RX are still working after the ageing.

- Plots show the RX operating range (plotting BER as a function of ISET and Rx threshold)

Left: reference RX operating range
Right: aged RX operating range

Accelerated aging in climate chamber ~1000 hours@ 80°C 80%rel. humidity

Each aged RX has been tested for one point inside the operating range with a test at 10^{-12}

DRX-II/Rx Installation

- **Based on its better performance, DRX-II chip was selected as the baseline design to make the Rx plugins for the Pixel L1/L2 upgrade.**

Produced and tested a total (L1+L2) of 280 Rx

Installation

- 104 Layer 2 SR1 and installation in Sep-Nov 2015
- 24 Layer 1 SR1 and installation in Sep-Nov 2015
- 128 Layer 1 SR1 in November 2016, pit before Xmas 2016

- More Rx plugins for the coming pixel B-layers & Disk upgrade

Table 2: New readout hardware items already installed and still to be installed as of August 2016

	Installed		Still to be installed			
	IBL	Pixel (Ly2+10% Ly1)	Ly1 (90%)	B-Layer	Disk (Disk2 doubled)	Total to be installed (Pit)
ROD	15	32	32	22	16	70
BOC	15	32	32	22	16	70
RX	60	128	128	88	64	280
TX (all pinouts)	30	116	64	44	48	156
QSFP	30	64	64	44	32	140

Summary

- **IHEP designed an ASIC chip (DRX-II) for the optical links upgrade of the ATLAS Pixel Detector (L1/L2).**

- **DRX-II has met all the required specifications, and offers better performance than the alternative solution based on discrete components.**

- **DRX-II chip has been used in the new Rx plugins, which have been installed in the Pixel Detector upgraded readout during 2015 to 2016;** *more to be installed for the coming Pixel B-layer & Disk upgrade.*