

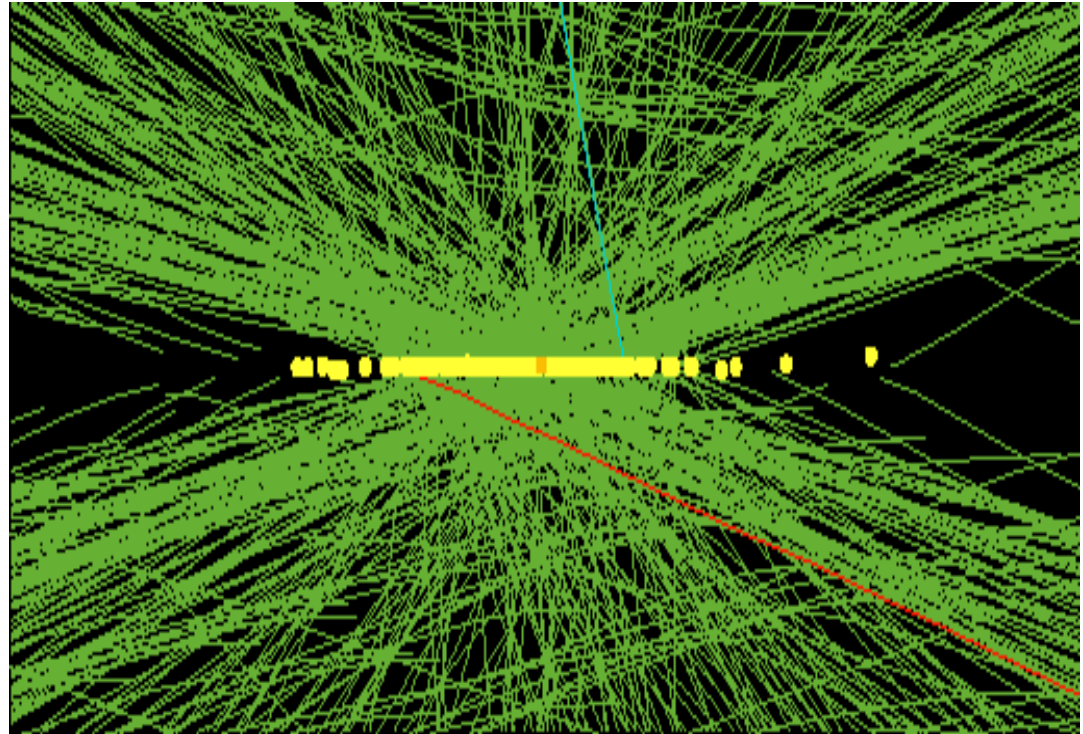
# **Monolithic CMOS Pixel Detectors for Future Track Triggers**

Jike Wang and  
André Schöning, Nigel HESSY, Tamasi Kar

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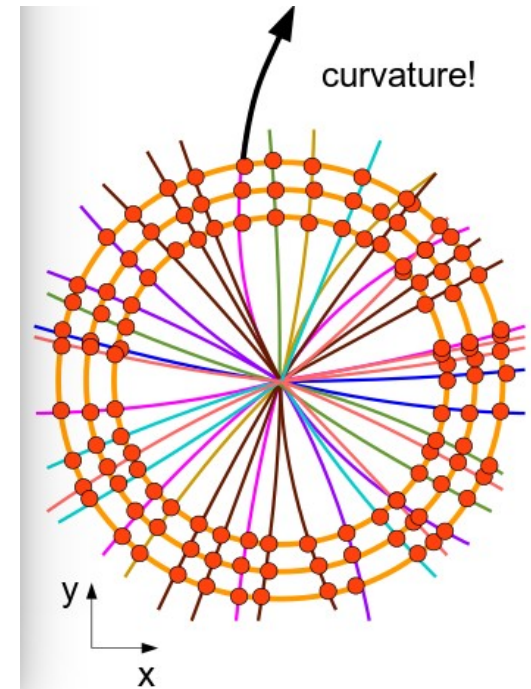
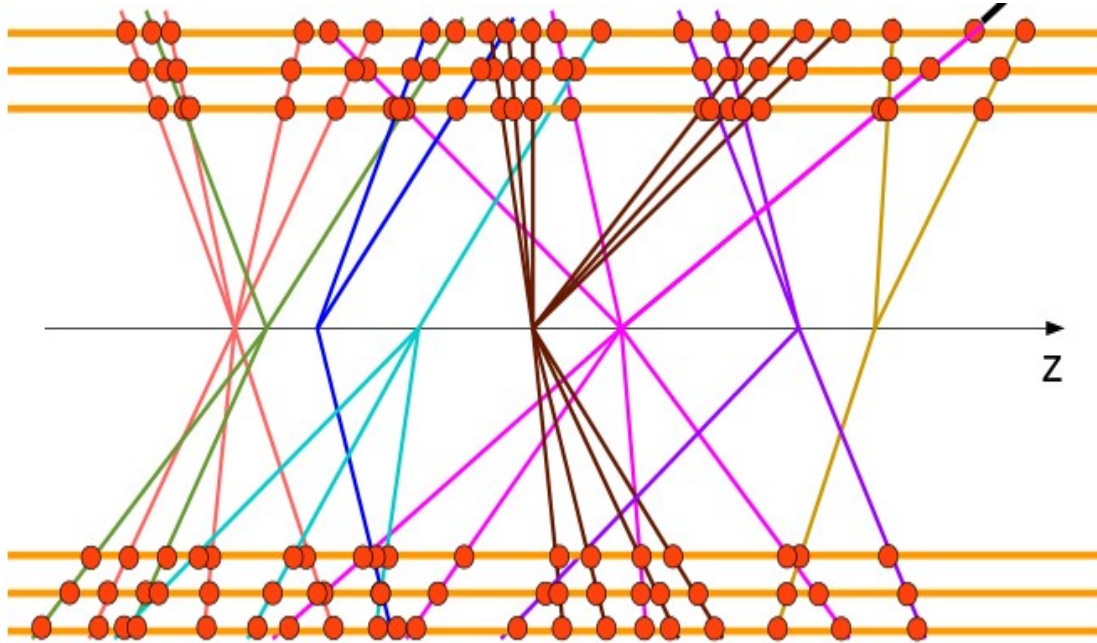
# The overall picture

- There will be very large pileup for HL-LHC
- The current planned L0 triggers are based on Calo and Muon
  - the FTK++ and L1TT could only readout 10% tracks



- Is it possible that we read out all the tracks ?
  - this can gain very much to physics. e.g.  $hh \rightarrow bbbb$
- We propose a new hardware track trigger at L0

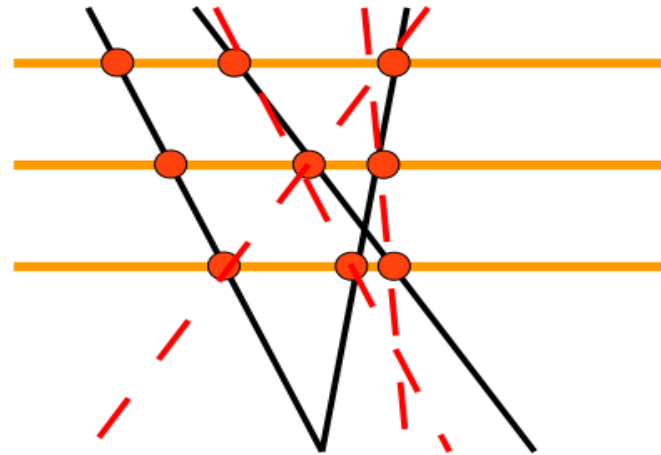
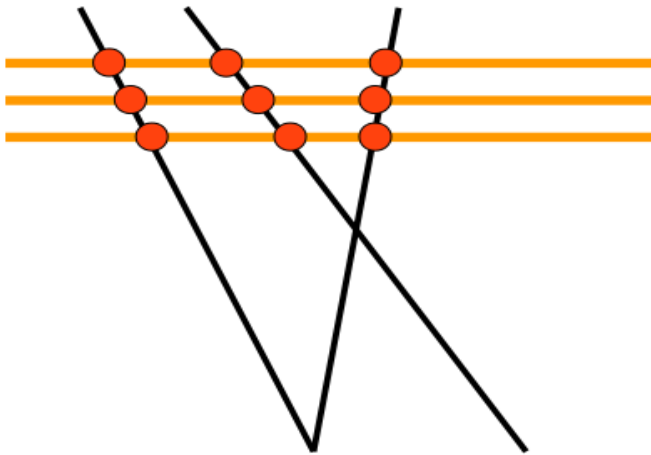
# The key idea



- Put in a new Triplets layer into the Strip
- Consisting of three separated layers  $\Rightarrow$  minimal number to decide a track

# Why three layers close ?

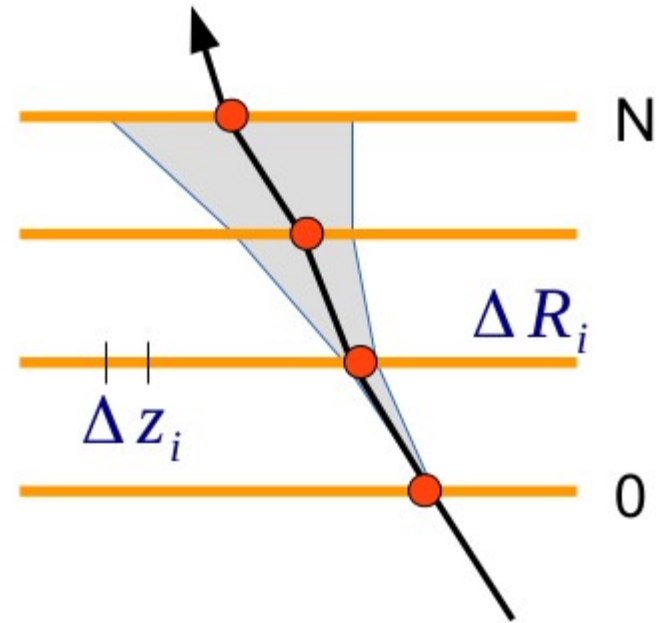
- For fast track triggers there is just no time performing complex operations:
  - **local processing** preferred over global processing
  - linearisations instead of non-linear problem solving
  - too far  $\Rightarrow$  the hit confusion problem
  - too close  $\Rightarrow$  momentum resolution worse; hardware constraint



An important parameter to optimize

# Tracking Materials

- Tracks with momenta of  $p < O(10 \text{ GeV})$  are dominated by multiple scattering (MS) at LHC
  - adds additional complexity for track reconstruction
  - increases significantly phase space of allowed patterns
- relevant for all track reconstruction methods (Kalman filter, lookup techniques, etc)

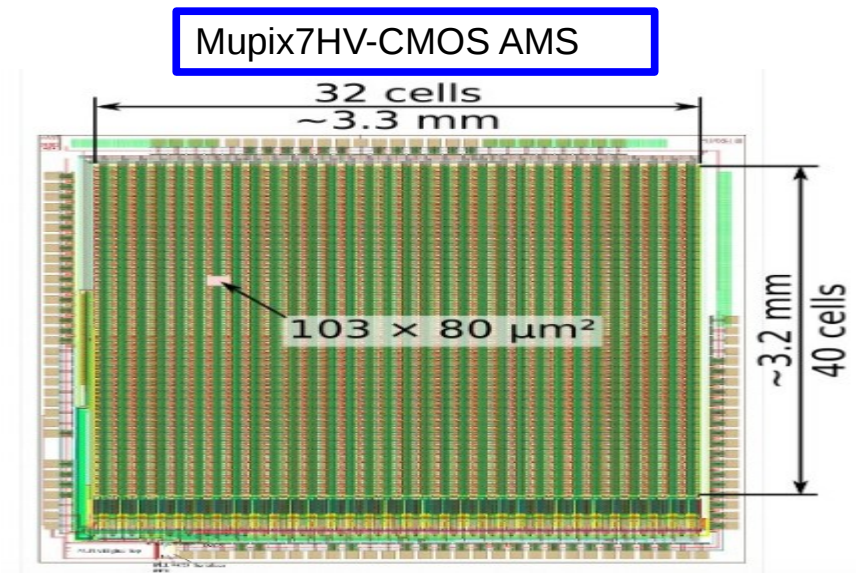
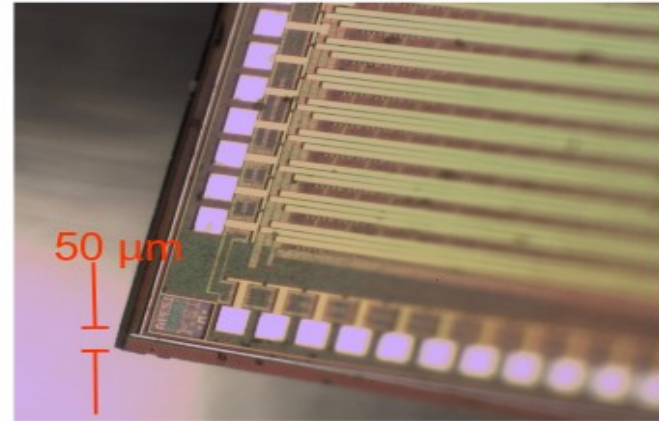


Material also increases the probability for non-interesting physics:

- nuclear interactions
- secondary particles ...

# So a good hardware trigger should satisfy:

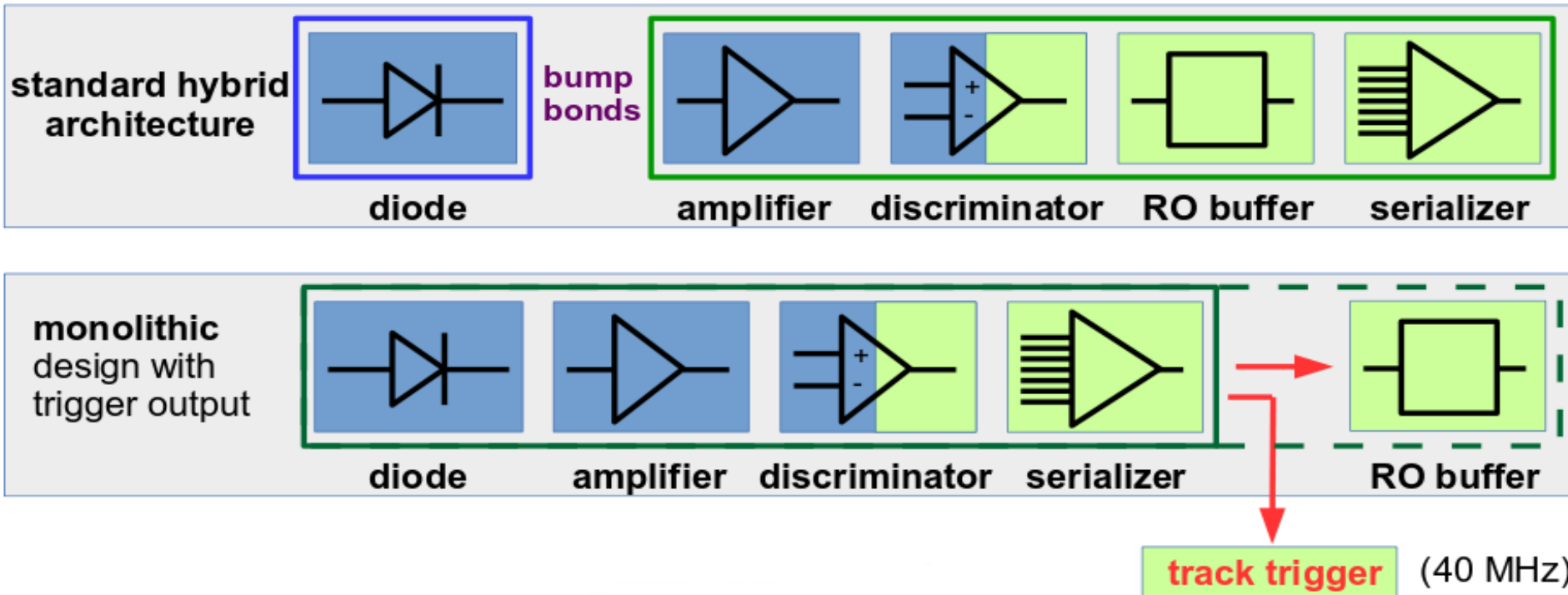
- High granularity and high resolution
  - Pixel
  - reducing ambiguities
- Little material
  - reduce ambiguities
  - Monolithic idea
- Fast readout capabilities
  - high track rates
- Radiation hardness
  - future very high pile-up
- Cheap
  - large sensitive areas



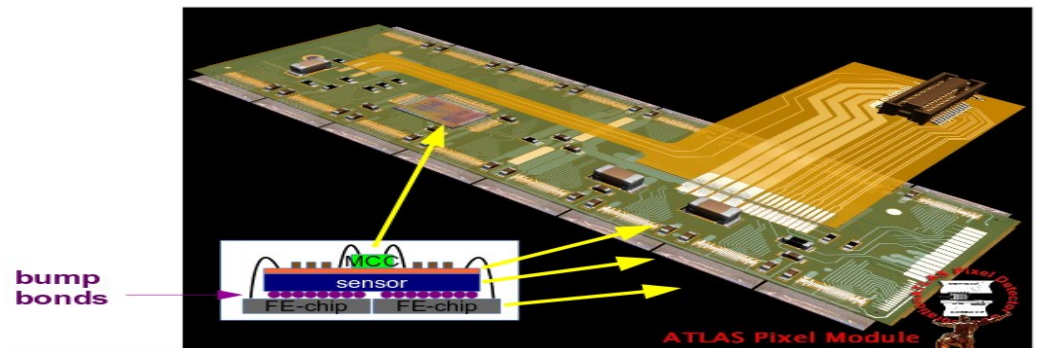
# Monolithic Conception

sensor

RO-chip



- No bump bonds
- All the readouts are integrated into the sensor

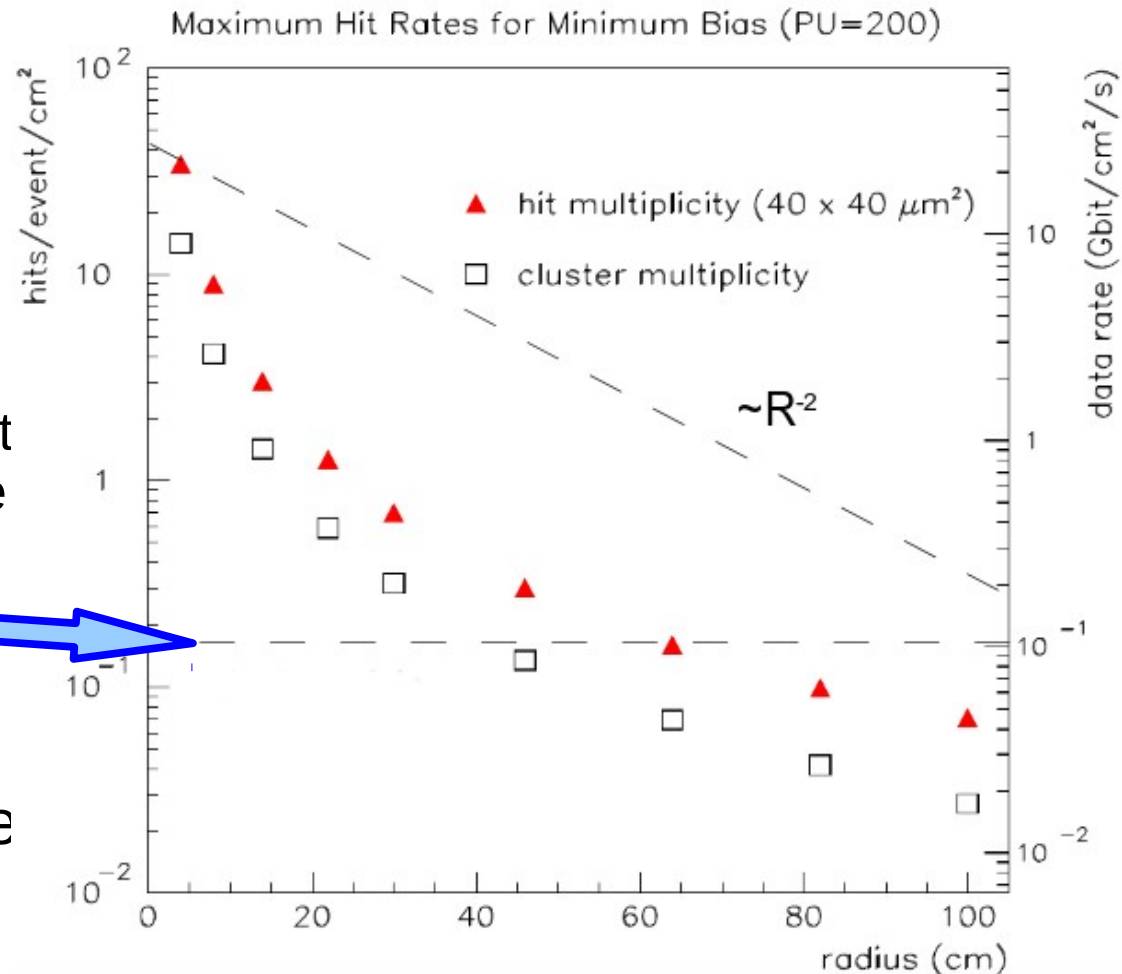


# Studies for implementation into ATLAS ITk

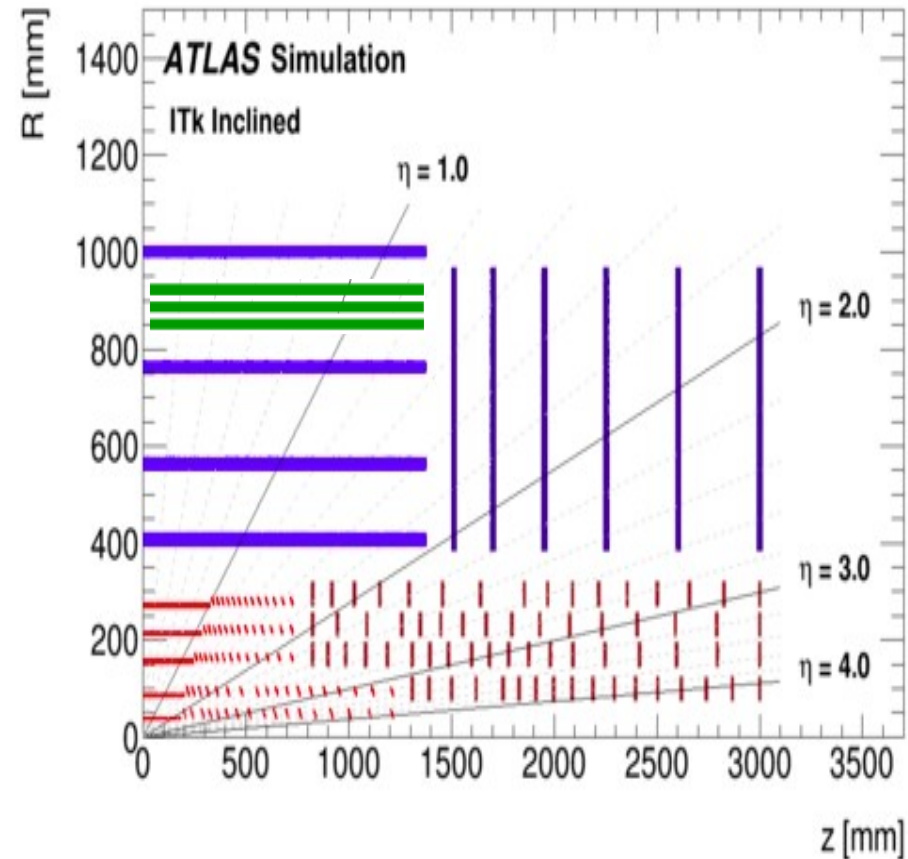
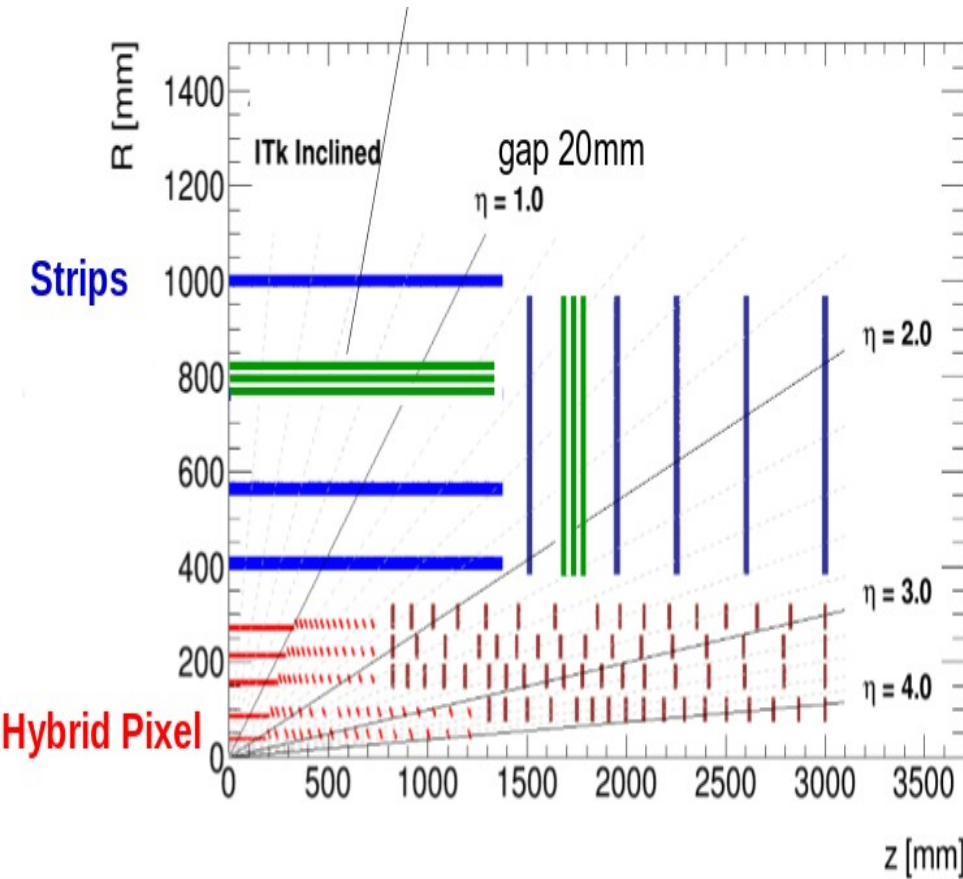
- A new layout design proposal
- Geometry consideration/display
- Hardware consideration
- Analysis results

# Bandwidth

- Bunch crossing  $\Rightarrow$  40 MHz readout
- Assume 100cm<sup>2</sup> for a module, the corresponding data rate  $\sim$ 10Gbit/s.
  - This rate can be realized with 1 or 2 optical links per module
  - So hardware supports:  
**100Mbit/s/cm<sup>2</sup>**
- So readout of all hits for every bunch only feasible at large radii

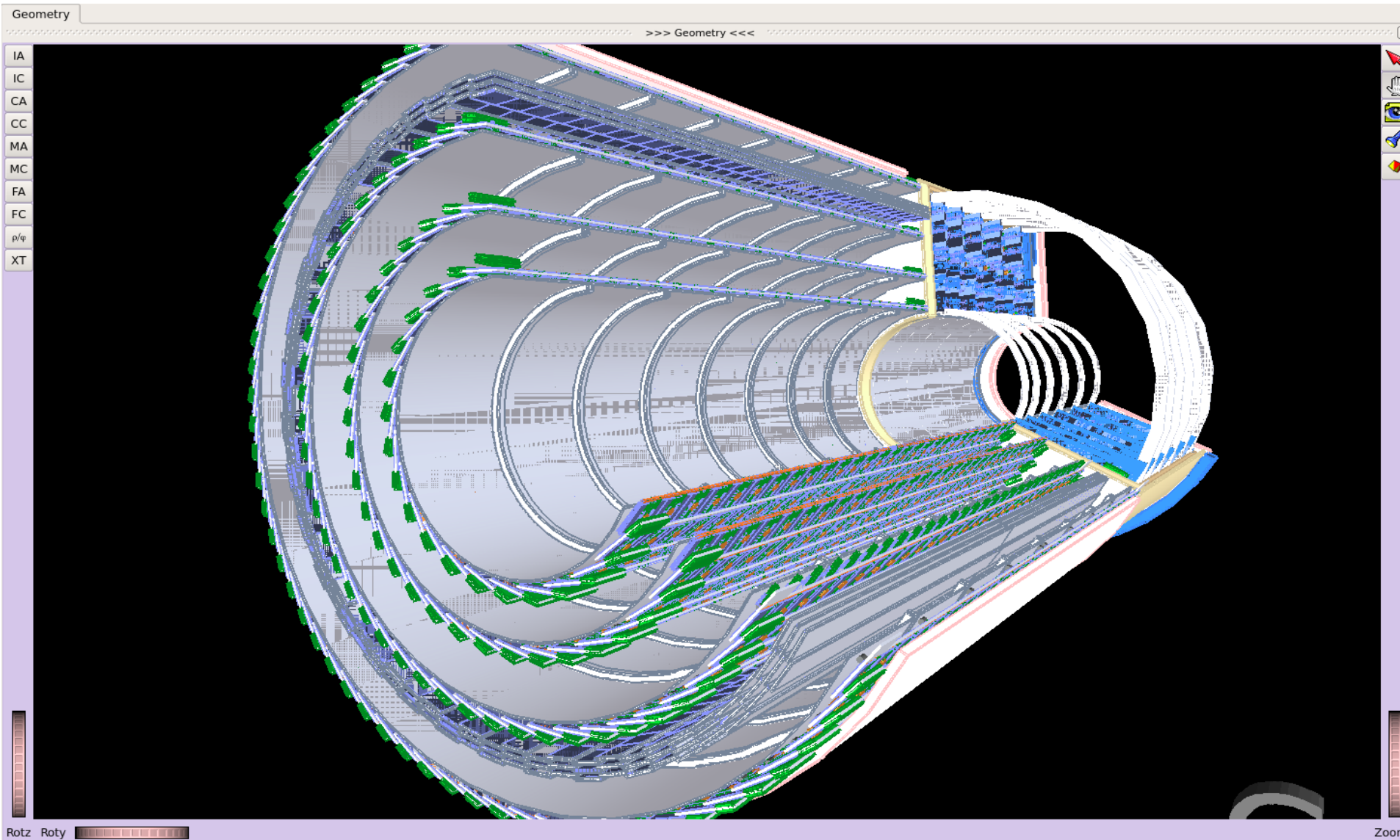


# Possible layouts

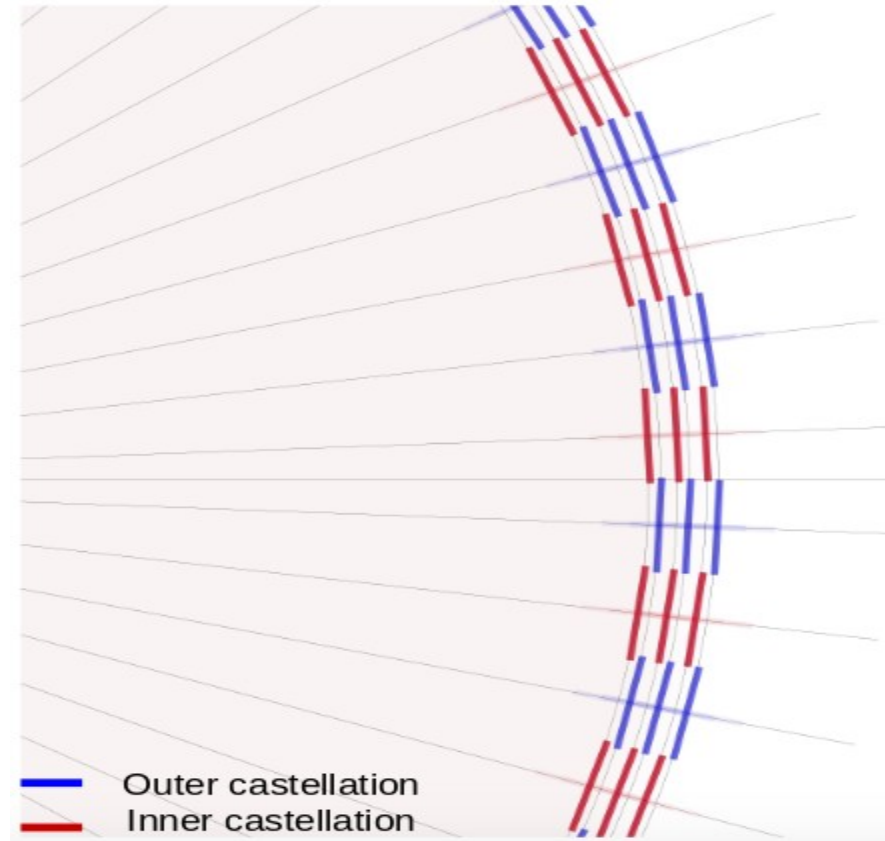
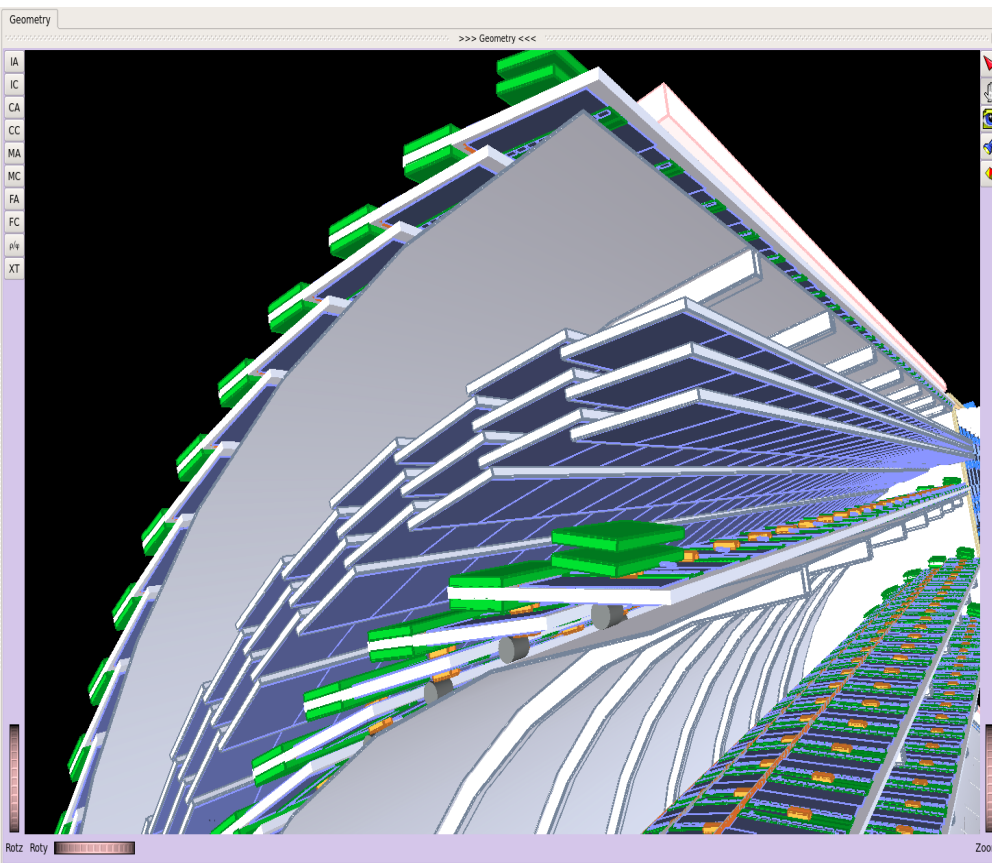


- Replace or insert

# Insert into between 3<sup>rd</sup> and 4<sup>rd</sup> layers

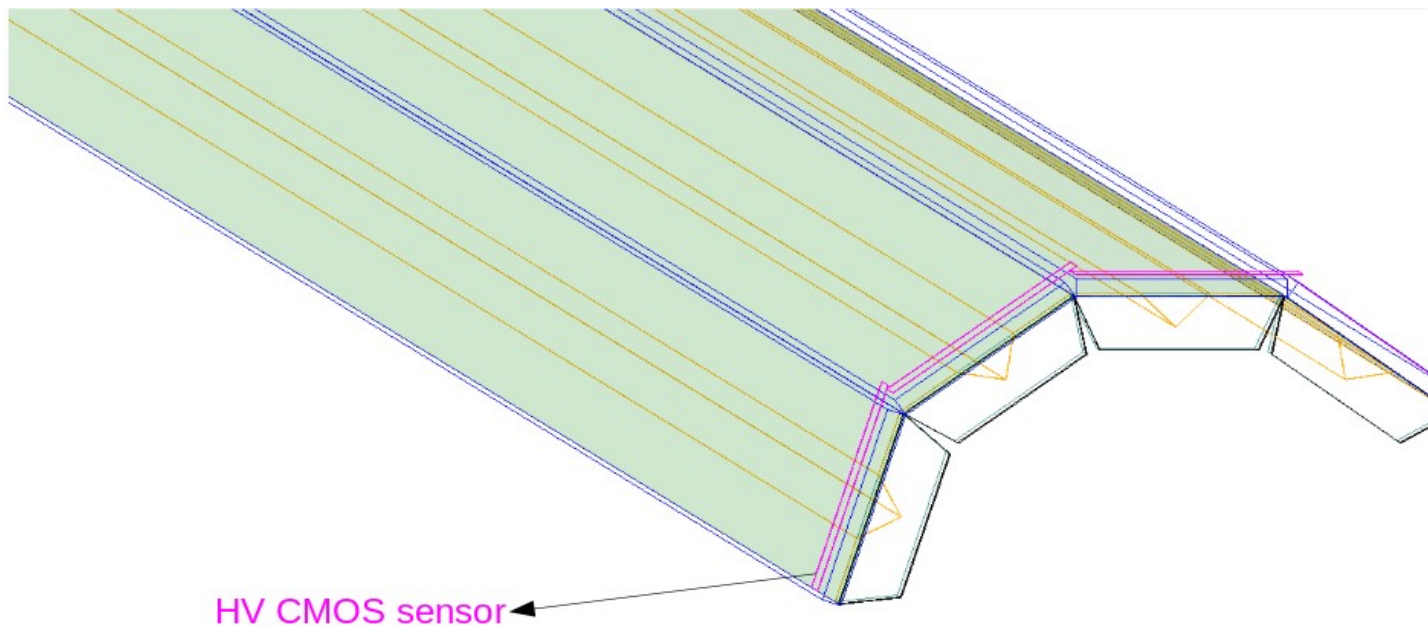
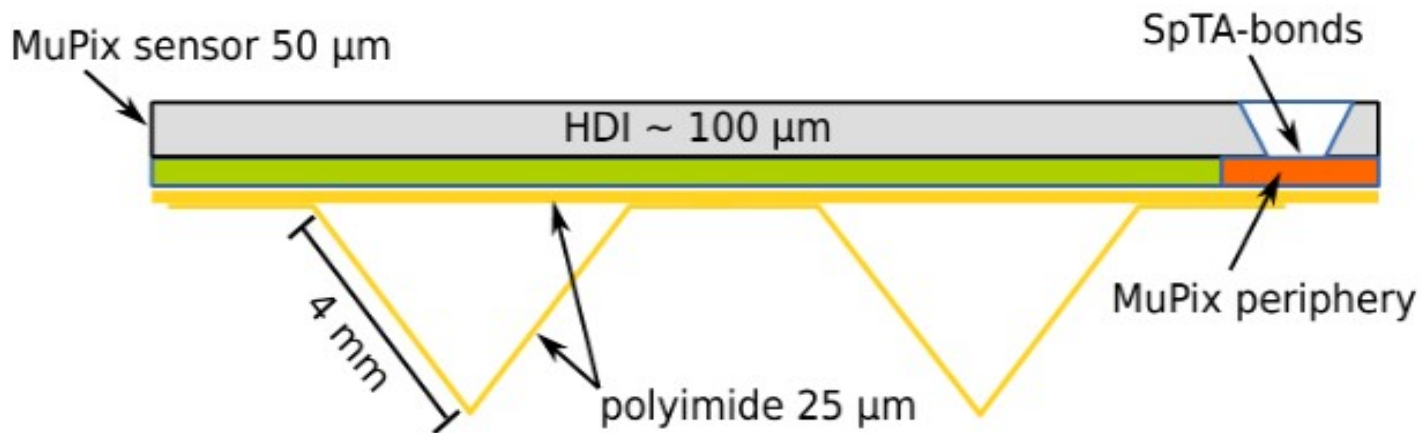


# Castellated



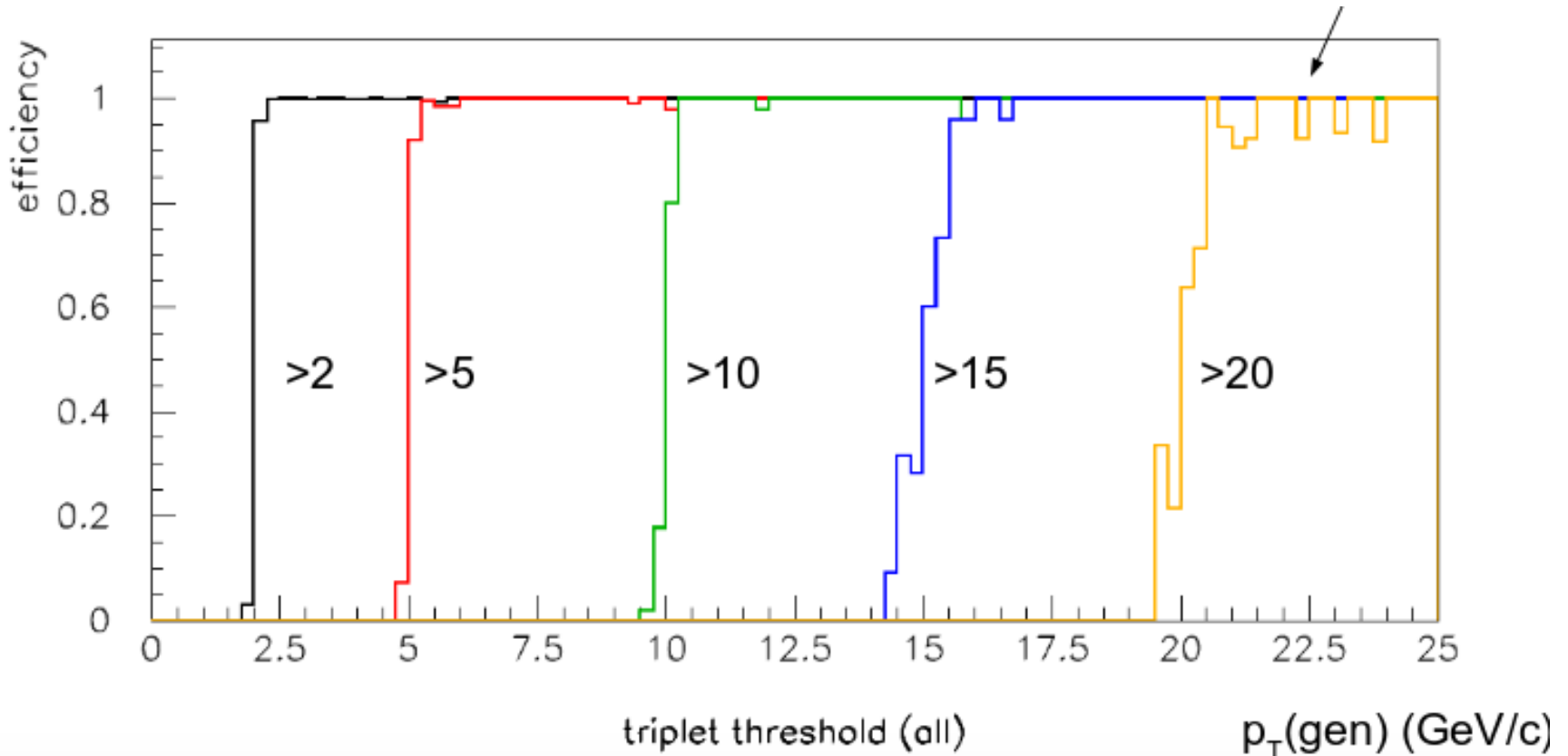
- Always same number of sensors at different radii (only connect the 3 hits within the same sector + IP  $\Rightarrow$  reduce tracking complexity )
- Overlaps  $\Rightarrow$  full coverage

# Stave design



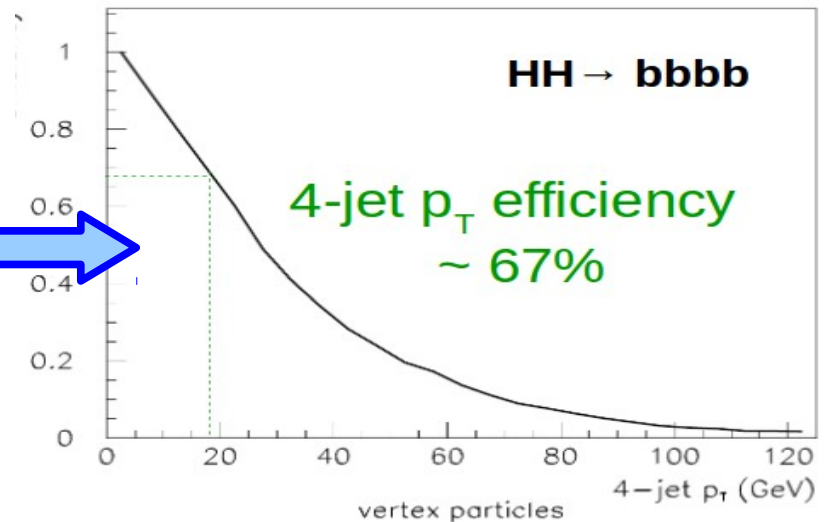
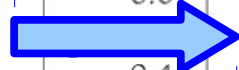
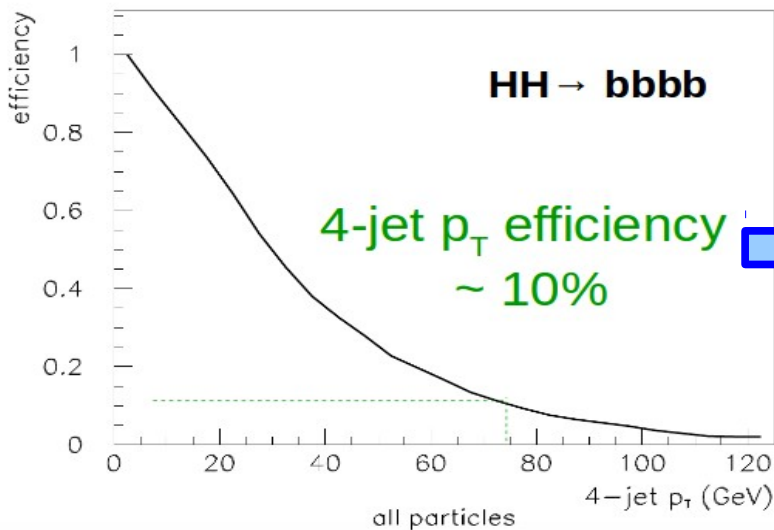
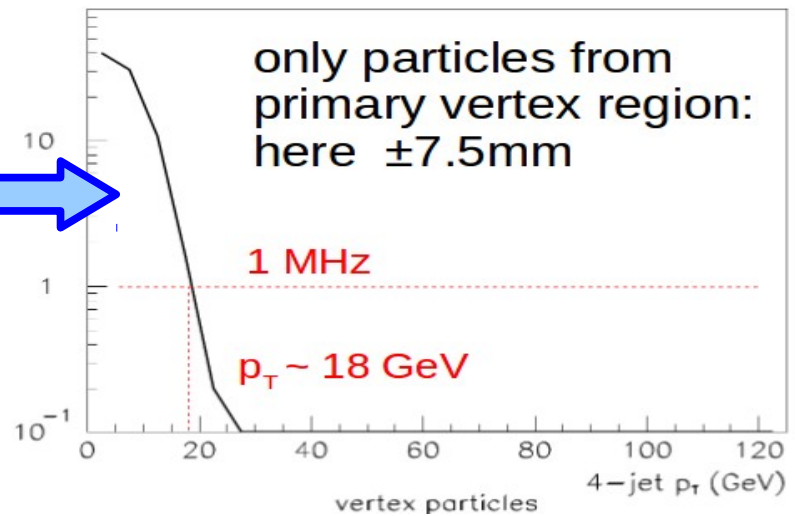
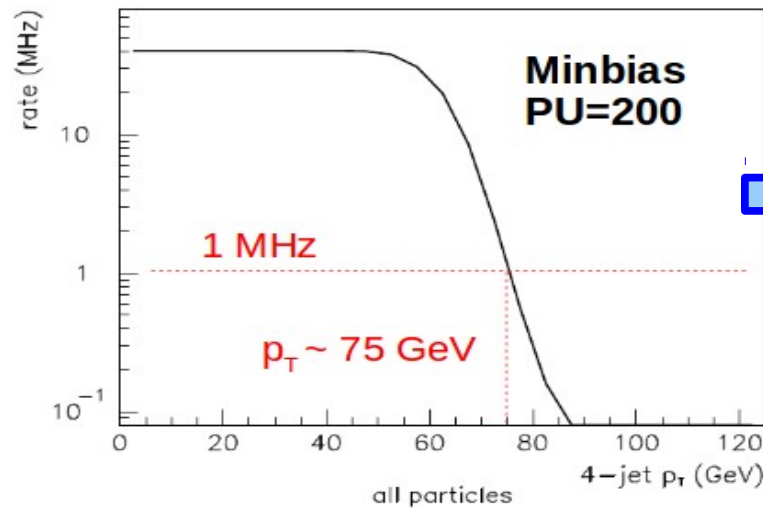
# Track efficiency

- Single track efficiency for different pT threshold



- Reconstruction efficiency  $\sim 100\%$  (also purity  $\sim 100\%$ )

# Physics results



# Summary

- Reconstruction of all tracks for HL-LHC seems possible with high efficiency and purity using a special tracker design
- Hardware preparation is ongoing. Chip demonstrator, stave prototype etc.