LHCb Upgrade: Recent Development of a Large Scintillating Fibre Tracker

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SciFi readout electronics (FE)

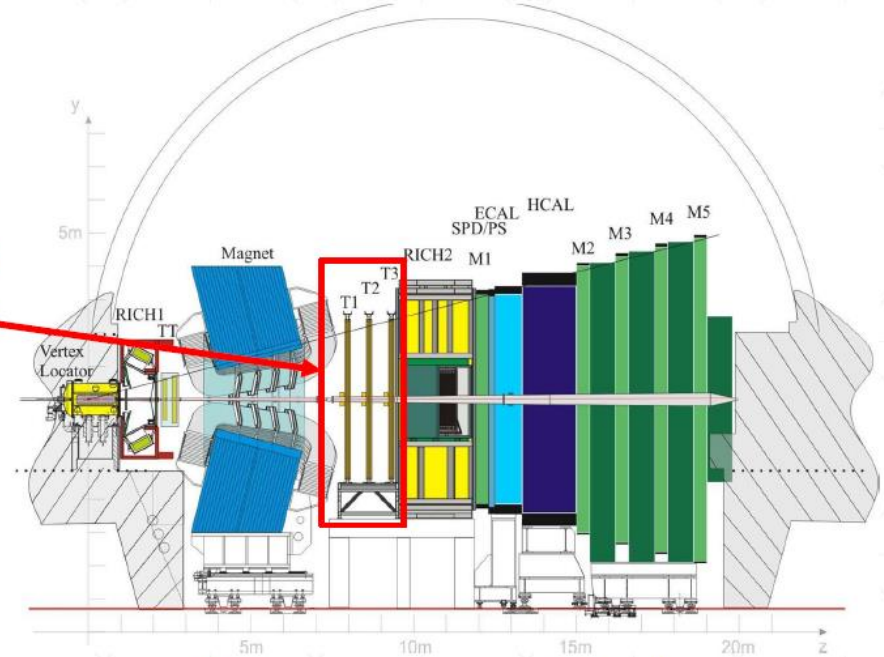
LHCb Upgrade

Goal: increase statistics by more than ×10

- operate at 2×10^{33} cm^{-2} s^{-1} → 50 fb^{-1}
- triggerless 40 MHz readout

the current Tracking Stations
(Gas Straw Tube Tracker + Silicon Tracker)
replaced by
Scintillating Fibre (SciFi) Tracker

- ✓ fast, high efficiency (~99%)
- ✓ high granularity (250μm)
- ✓ high resolution (<100μm)
- ✓ low mass (<1% X_0 /layer)
- ✓ radiation hardness (up to 35 kGy)

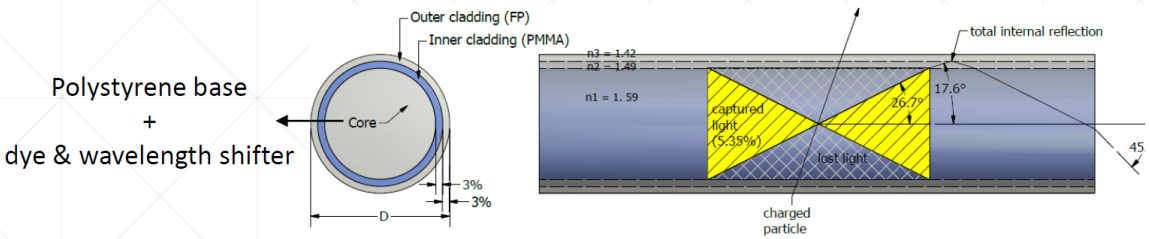


Schematic view of the current LHCb detector

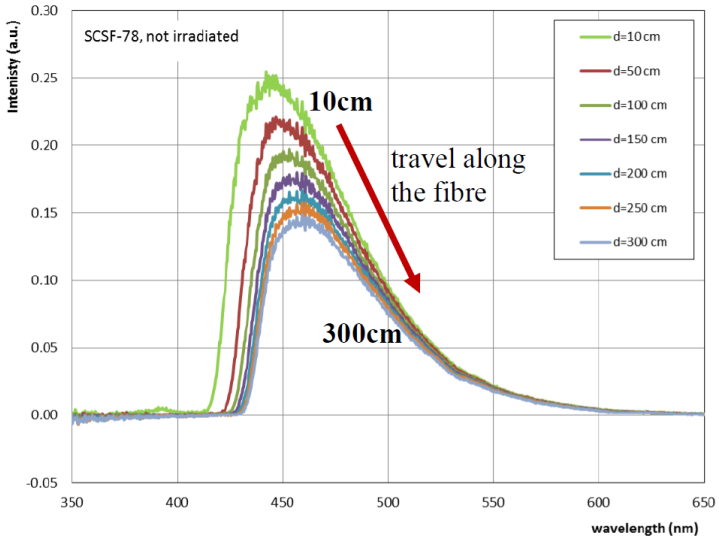
SciFi readout electronics (FE)

- 250μm double-clad plastic scintillating fibre
- emission spectra : peak @ ~ 460nm
- attenuation length : ~3.5m

~300 photons/MIP, only 2× 5% captured



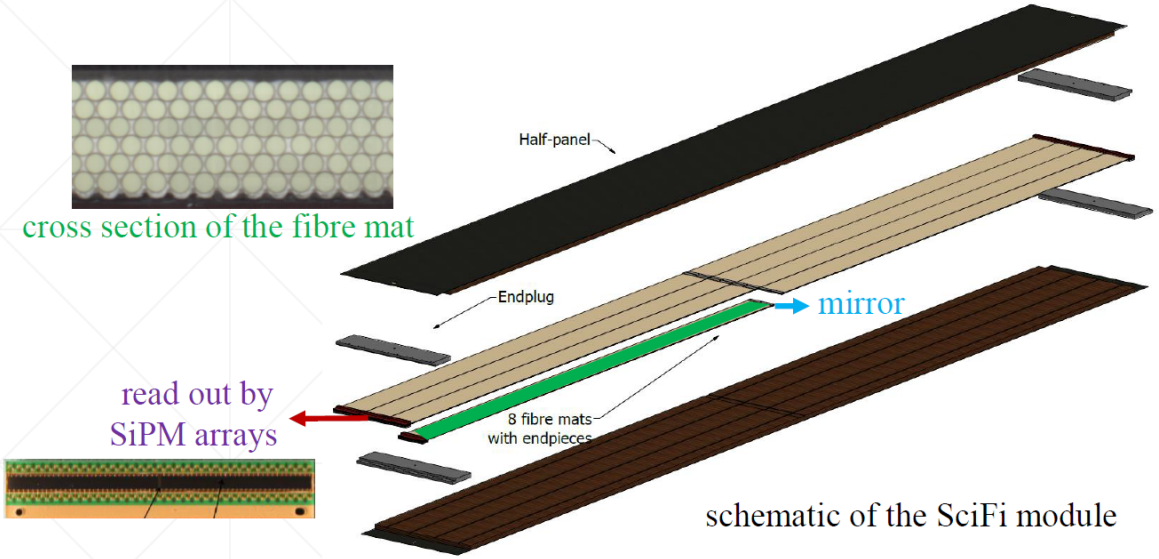
(a) end view (b) side view



measured emission spectra of the scintillating fibre

SciFi readout electronics (FE)

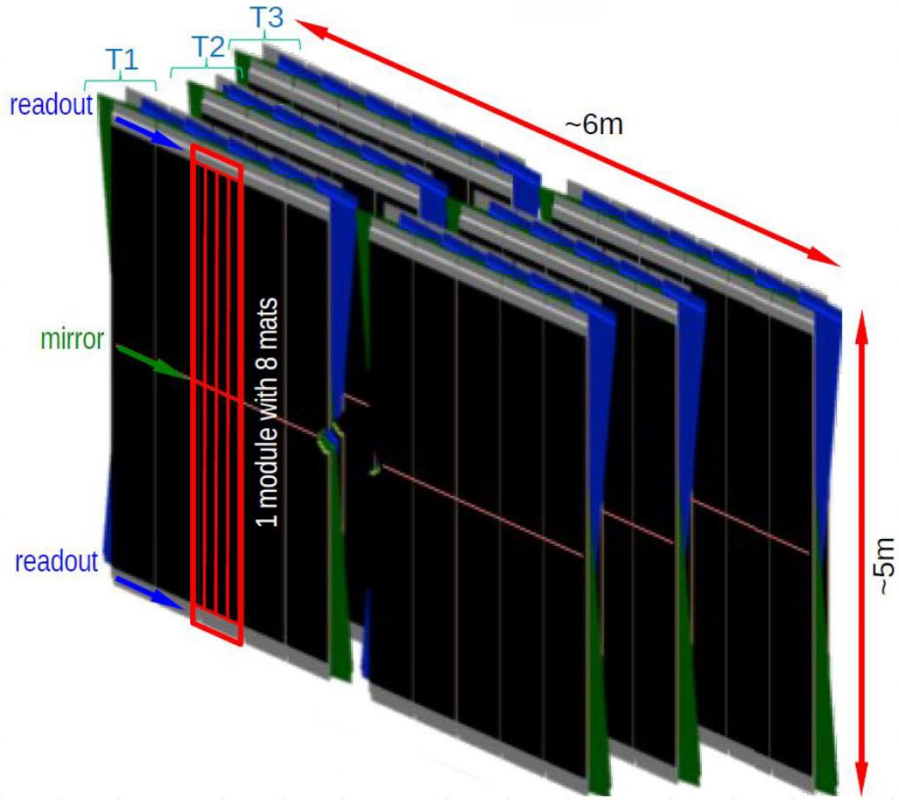
- 250μm diameter scintillating fibre wound into a 6-layer 2.4m-long fibre mat
  - ✓ one end equipped with a mirror
  - ✓ read out by 4× SiPM arrays
- 8 × fibre mat + honeycomb = sandwich-structure 0.5m × 5m module



SciFi readout electronics (FE)

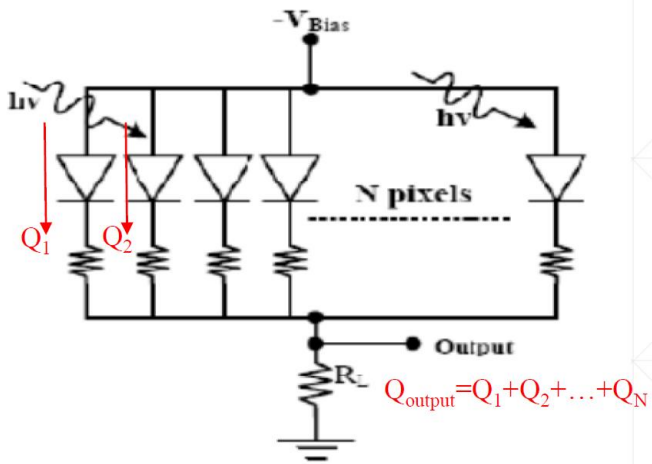
- 128 × modules
- 12 × detector layers (X-U-V-X, 5°)
- 3 × Tracking Stations

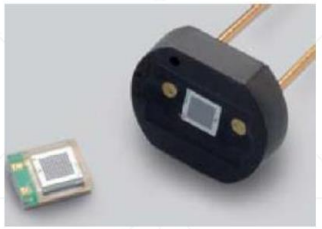
- 11,000 km of fibres
- 524k SiPM channels
- ~340m^2 total active surface



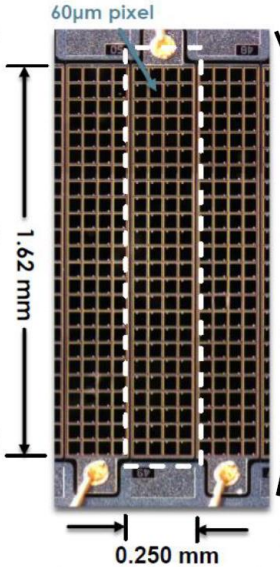
SciFi readout electronics (FE)

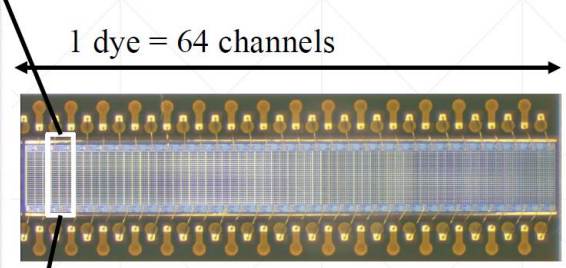
- different names by different producers: MPPC, MAPD, SSPM, DAPD, PPD, MRS APD …
- one pixel = an APD [working in Geiger mode] + a quenching resistor
- one channel = many pixels connected in parallel





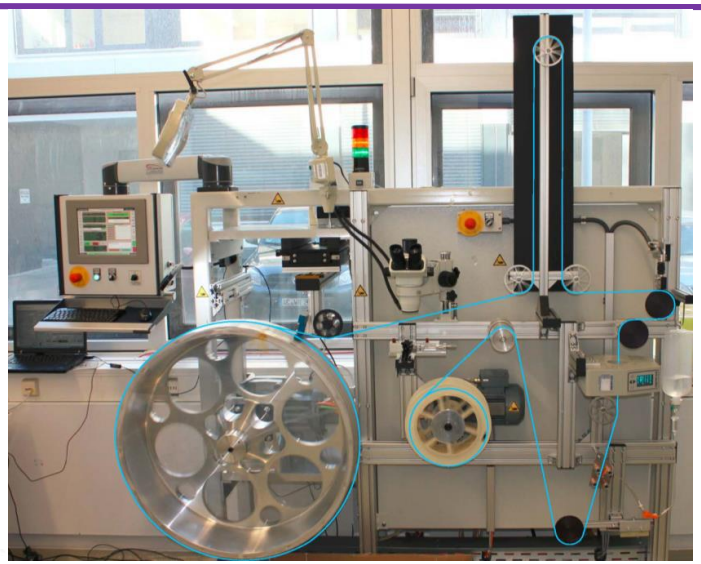
single channel SiPMs

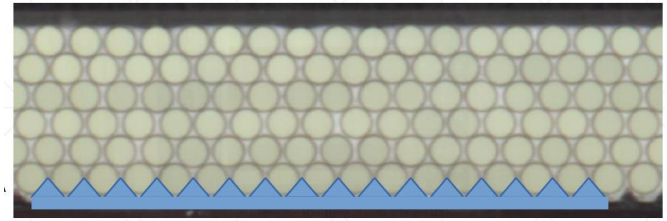




SciFi custom SiPM array

SciFi readout electronics (FE)

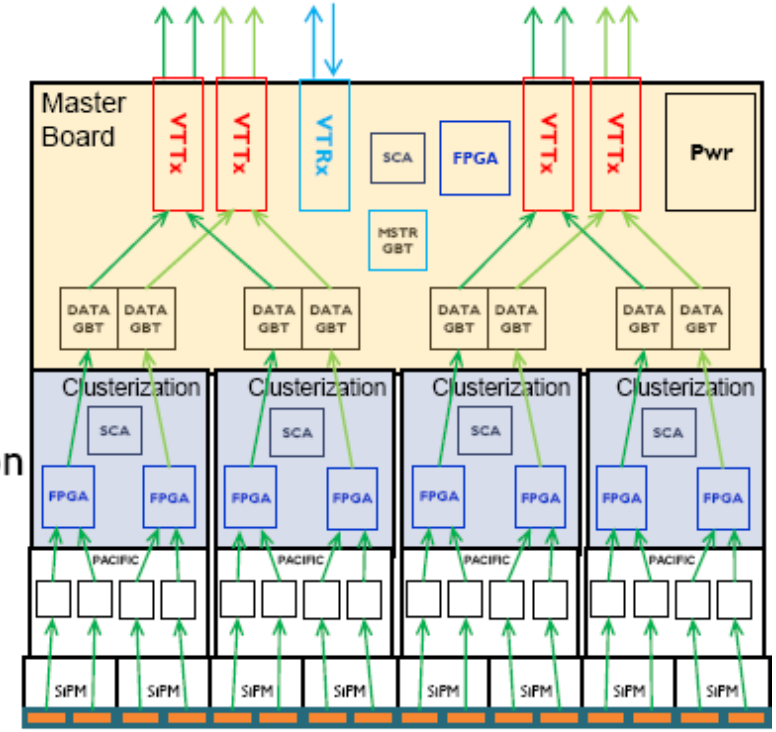




SciFi readout electronics (FE)

½ ROB electronics

- Master Board
  - Master GBT → TFC/ ECS distribution
  - Data GBTs → Data serialisation
  - Power supplies
  - Versatile link optical components
- Clusterization board
  - FPGA based Clustering algoithm
  - SCA for slow controls → Clusterization FPGAs and PACIFIC ASICs
- PACIFIC Board
  - Amplifier, shaper, integrator and ADCs, 2b/channel output based on three threshold values
- SiPM: Silicon Photo Multiplier modules
  - 2 arrays of 64 channel avalanche photodiodes



LHCb Tsinghua Group in SciFi R&D

- SciFi Detector Performance Evaluation Electronics
- SciFi Detector Performance Study
- SciFi Track Reconstruction Software Package Development
- SciFi Readout ASIC (PACIFIC) Quality Assurance System
- SciFi Readout ASIC Board Mass Production and Test (2018)

LHCb Tsinghua Group

Professors： Yuanning GAO， Zhenwei YANG，
Ming ZENG， Guanghua GONG

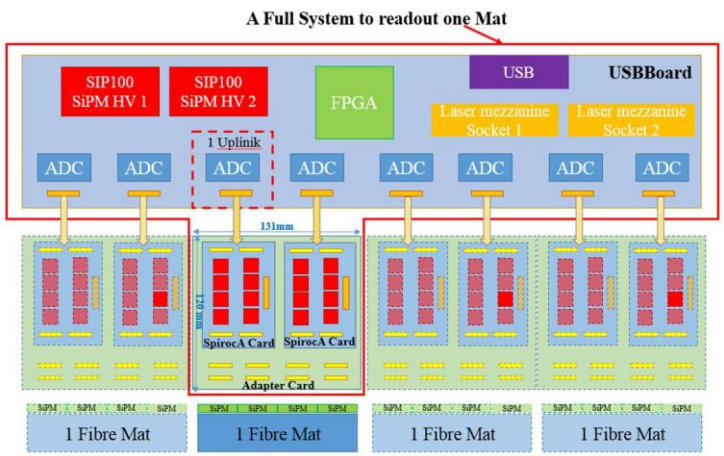
Postdoc： Adam Davis (Scifi Testbeam Simulation)
Biplab Dey (CCNU， SciFi Track Reconstruction)

Ph.D. Students： Yuyan Huang (PACIFIC Quality Assurance System)
Jirong Cang (SciFi Detector Performance Study)
Yuyue Gan (PACIFIC Quality Assurance System)
Mengzhen Wang (SciFi simulation and track reconstruction)
Liupan An (SciFi simulation and track reconstruction)

SciFi Detector Performance Evaluation Electronics

- For SciFi detector module performance study and Test beam experiment.
- Designed by Tsinghua, RWTH and Heidelberg, more than 20 systems offered to SciFi
- Read out up to 2048 SiPMchannels @ ~2kHz = one side of a full module

	瑞士洛桑联邦理工	德国多特蒙德大学	德国亚琛大学	俄罗斯库尔恰托夫研究院	德国海德堡大学	欧洲核子中心
用途	光纤衬垫质控	光纤衬垫质控	光纤衬垫质控	光纤衬垫质控	光纤模组质控	光纤模组束流测试
数量	2	2	2	2	4	4



USB Board

SPIROC Card

SciFi Detector Performance Study

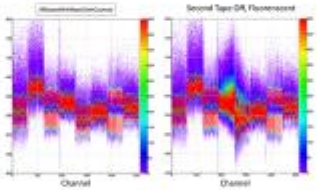
- Based on the Performance Evaluation Electronics, with NIKHEF and Heidelberg. (Several Ph.D. Students)
- Light tightness, cooling, spatial resolution…

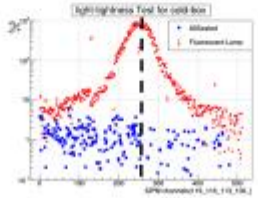
Light tightness test of cold-box

- QUAROS system
  - 2 SPIROCA Cards
  - USBBOARD for data transfer
  - Read 4 SiPMs at once (4 × 128 channels)

All sealed

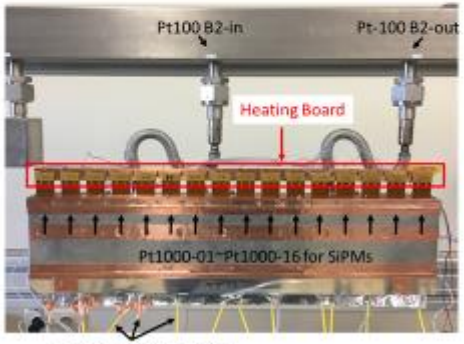
Room light



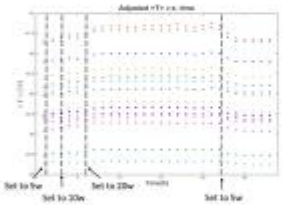


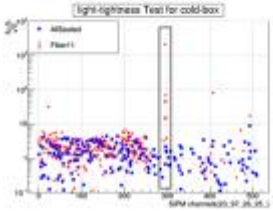
Cooling test

- Cool the SiPMs down to −40°C (working condition)
- Emulate thermal impact of FE Electronics on SiPM temperatures
- Mechanical deformations due to temp. cycles (few channels illuminated by light injection)



Fibers for Light Injection



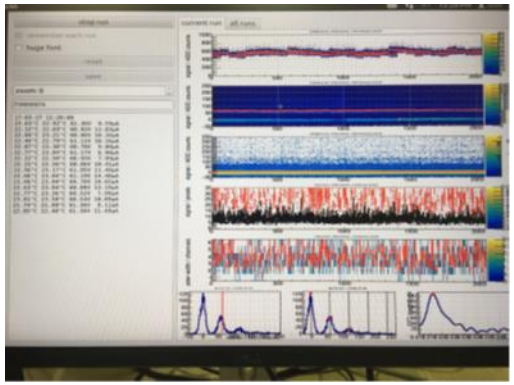


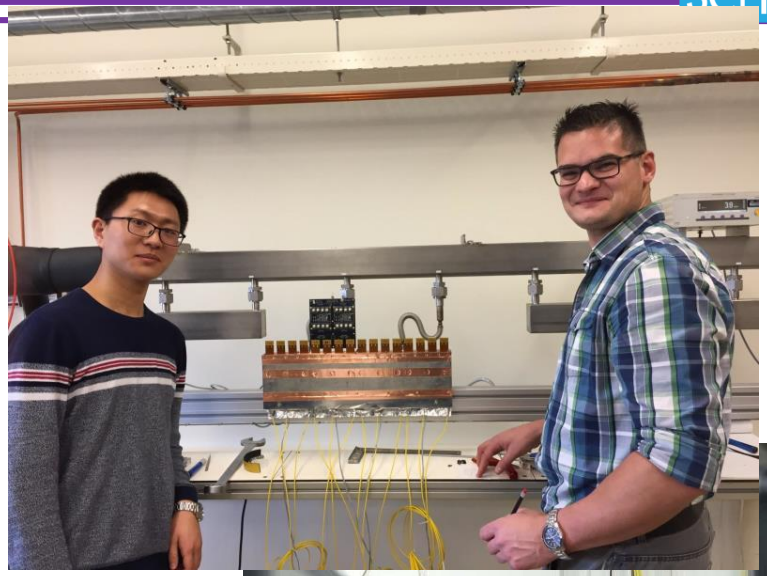
SciFi Detector Performance Study

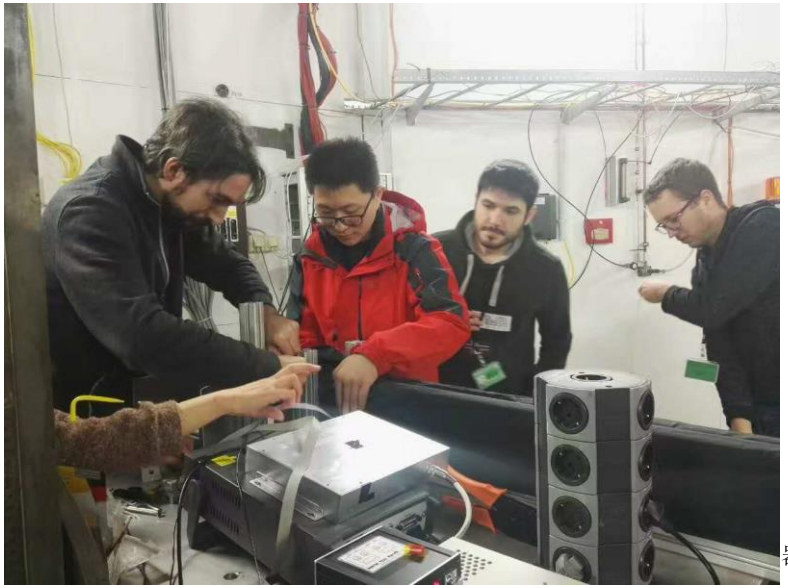
- Mats pre-gluing test:
  - ✓QA method: developed at Heidelberg
  - ✓QA hardware: USB readout + SPIROC + trigger available

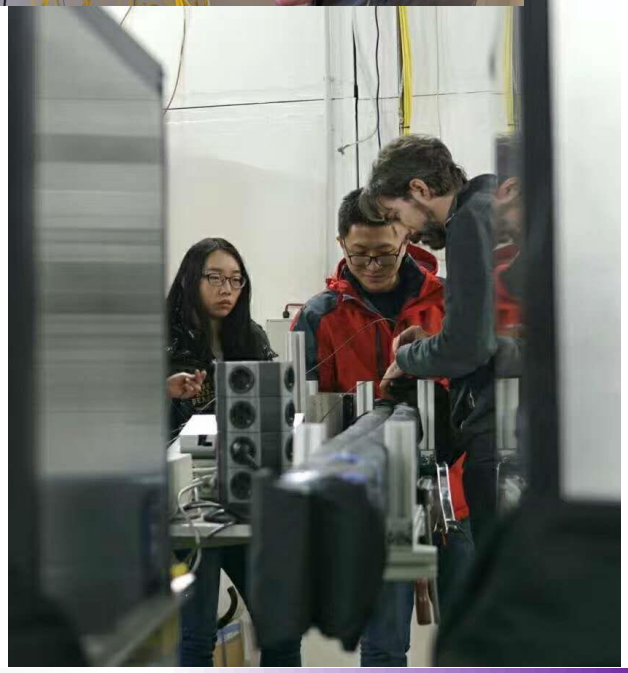
- Module pin-alignment test:
  - QA method: developing system similar to Heidelberg
  - QA hardware: laser + PSD ready, develop mechanics

- Module end-item test:
  - ✓QA method: developed at Heidelberg
  - ✓QA hardware: USB readout + SPIROC + trigger available









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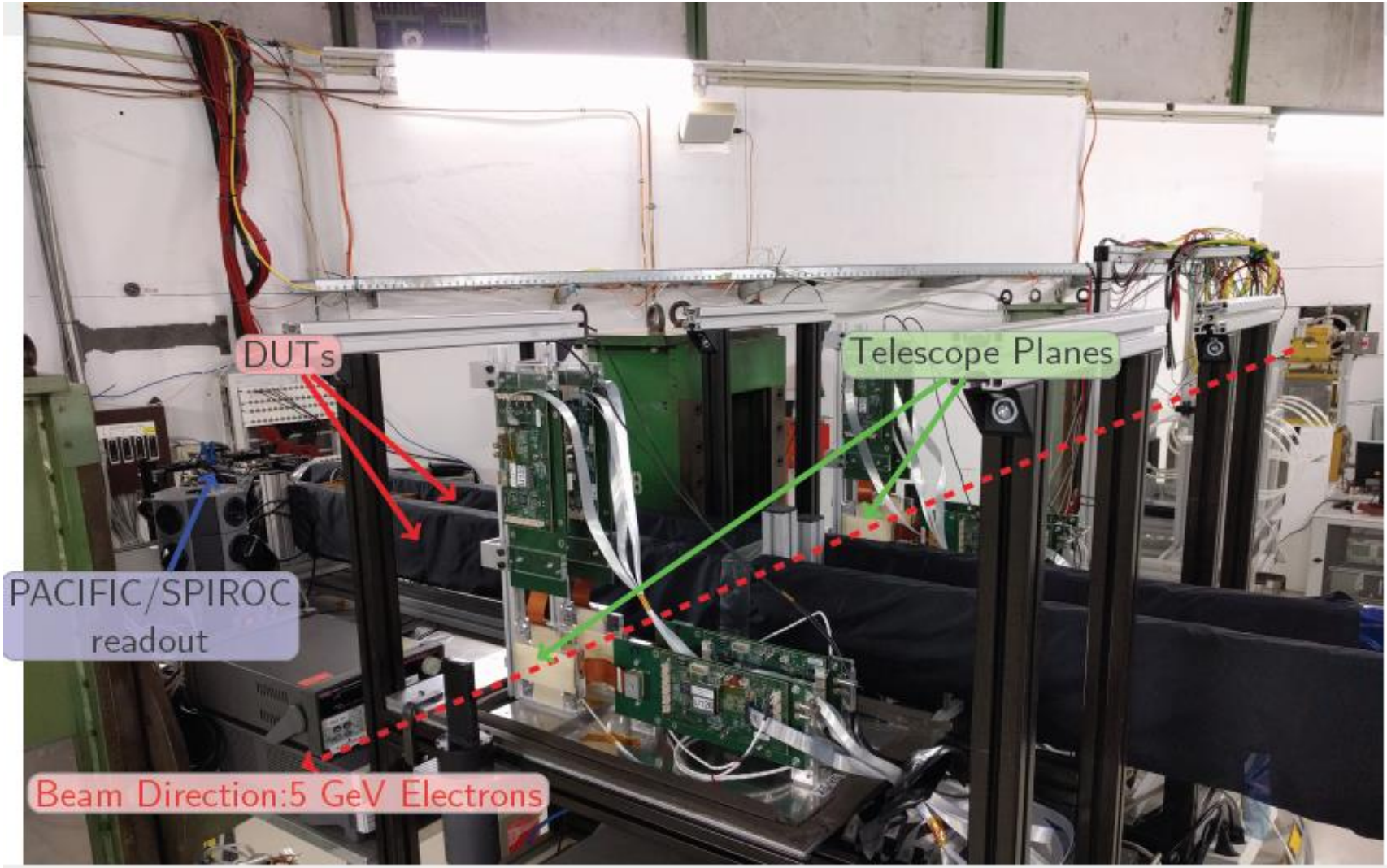
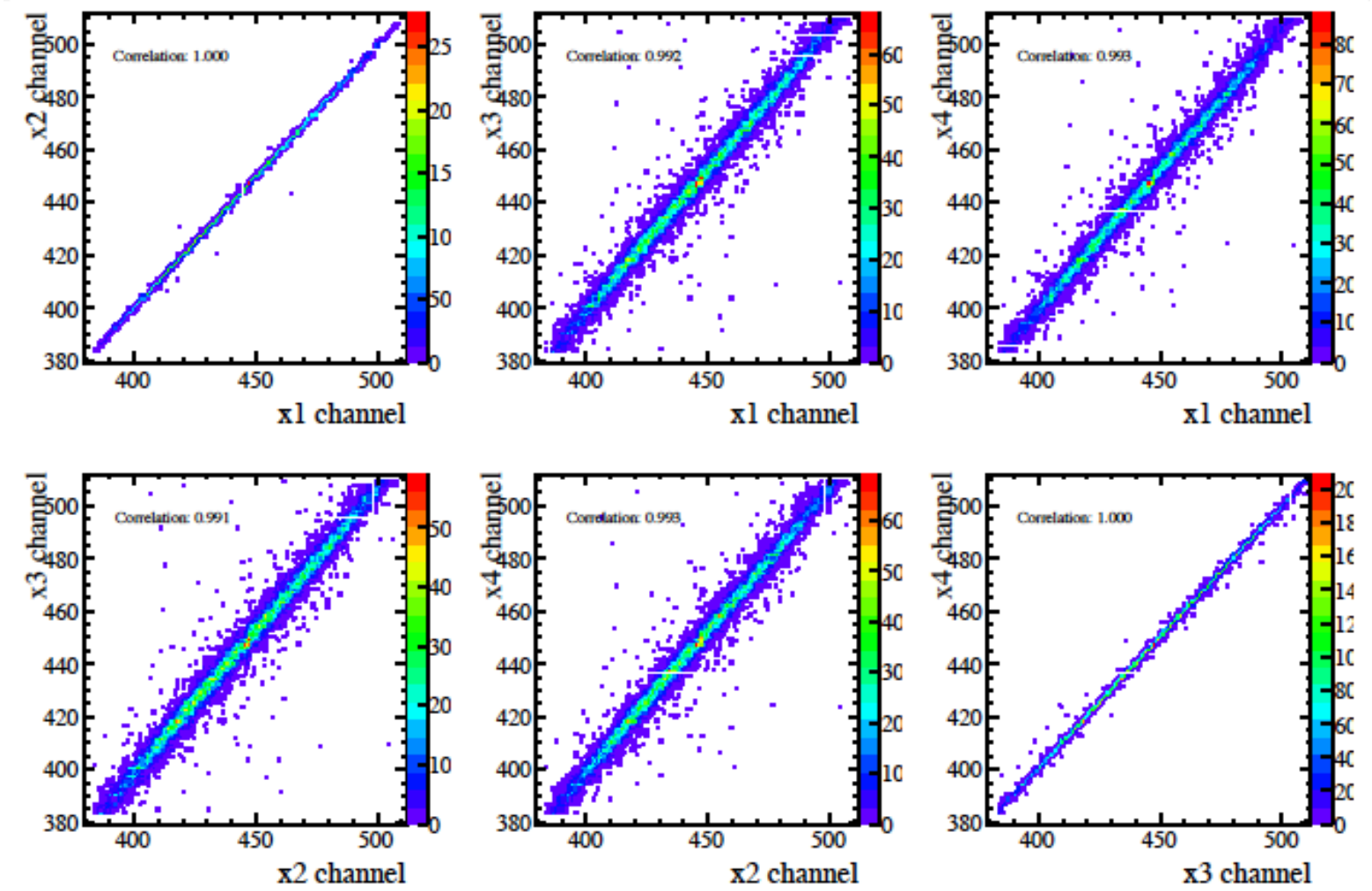
SciFi Track Reconstruction Software Package Development



SciFi Track Reconstruction Software Package Development

Correlation plots of testbeam data from framework: Telescope x



SciFi Track Reconstruction Software Package Development

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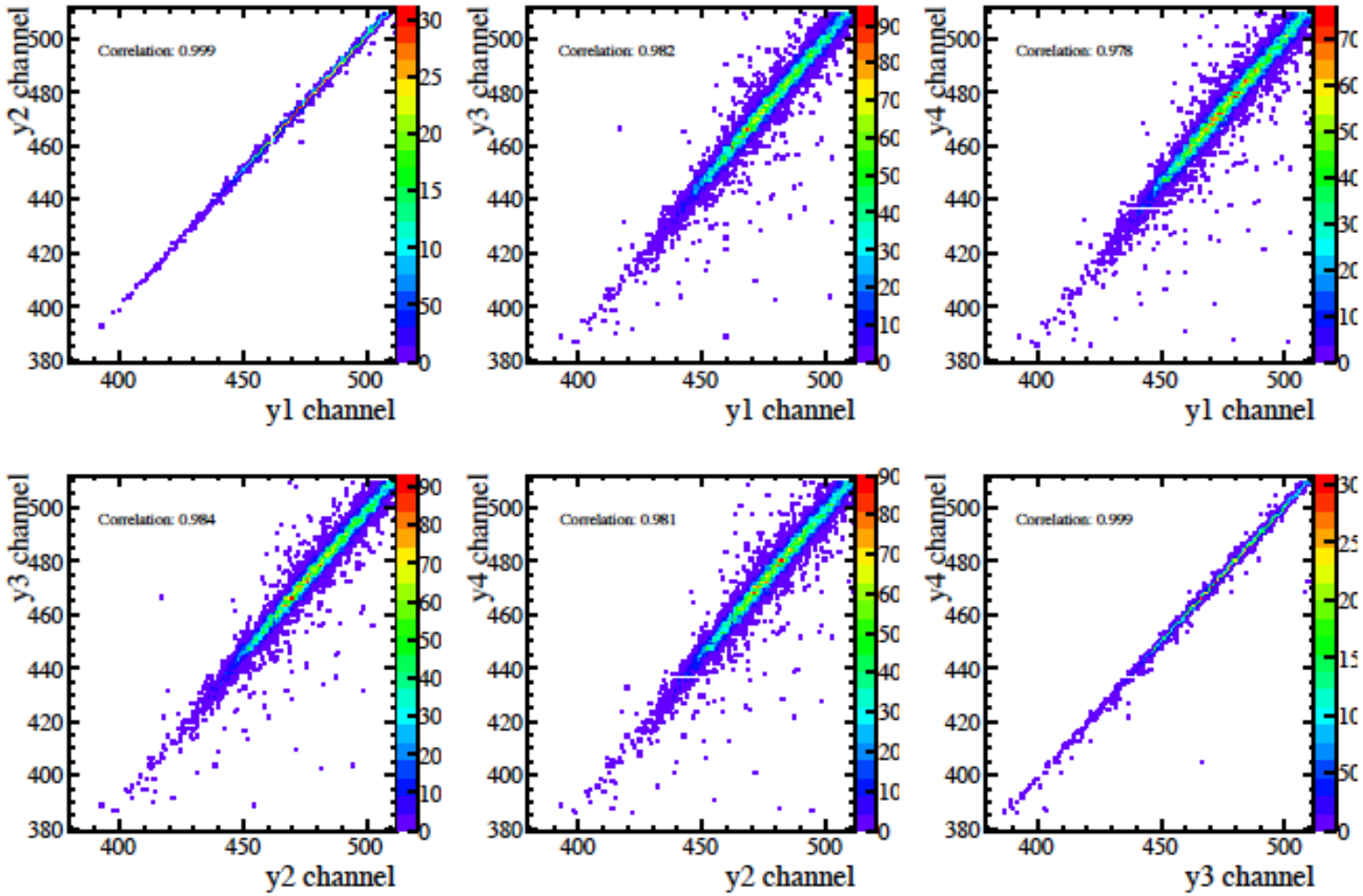

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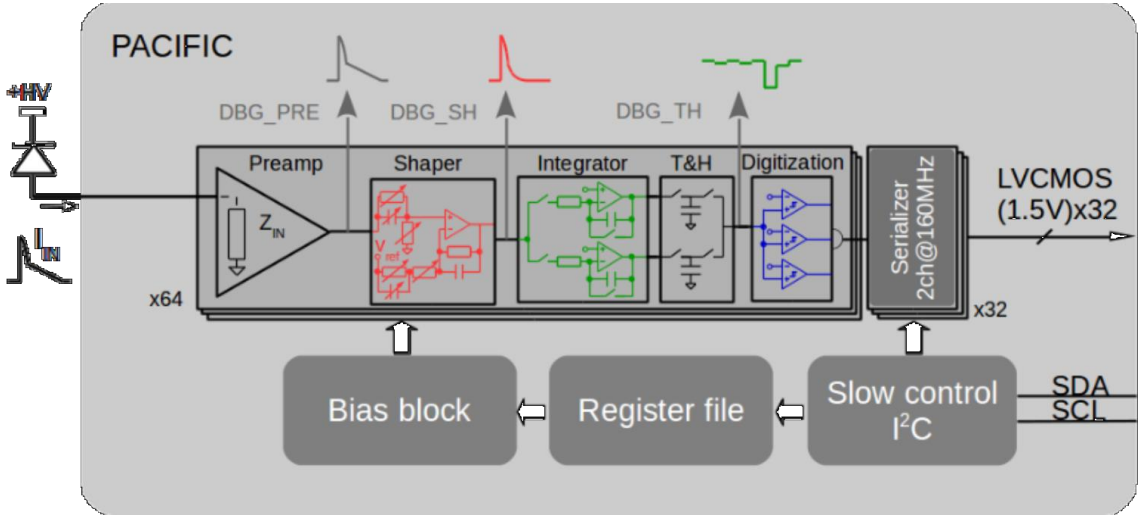
PACIFIC ASIC

PACIFIC a low Power Asic for the sCIntillating FIbre traCker

- 64-channel current mode input
- configurable fast shaper : minimize spillover
- interleaved gated-integrators per channel: minimize dead time
- 2-bit non-linear digitisation per channel : minimum data for sufficient tracking information
- adjustable input anode DC voltage (4-bit DAC, 50mV/LSB)

power consumption <10mW/channel

CMOS 130nm Technology



V5 PACIFIC:
320MHz SLVS differential output

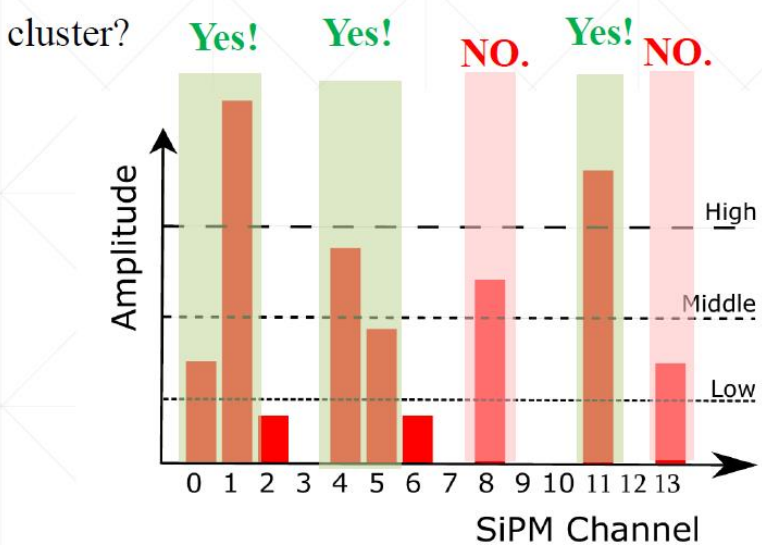
MORE THAN

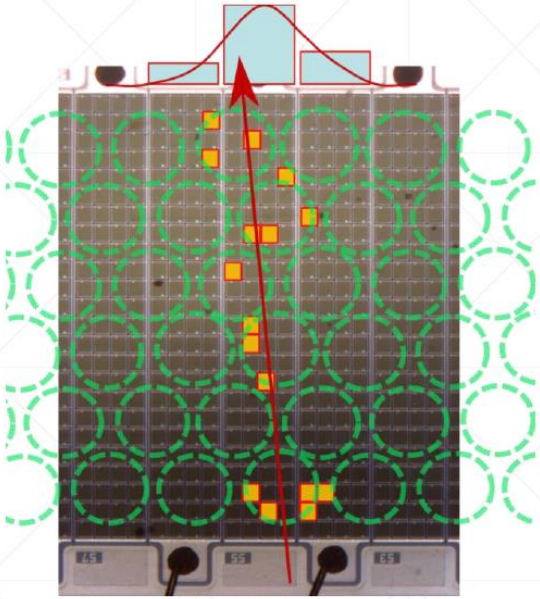
10K CHIPS NEEDED

PACIFIC ASIC

Digitisation & Clustering

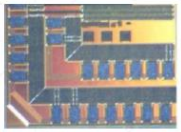
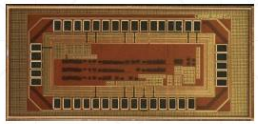
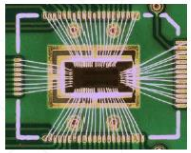
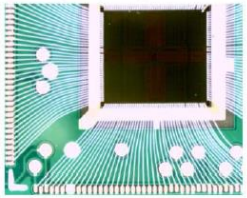
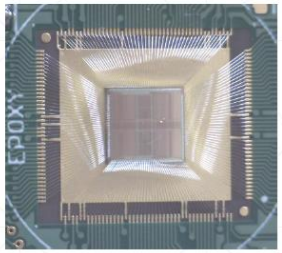
- analog signal digitized by three threshold-tunable comparators per channel
- three thresholds based on the cluster algorithm
  - ✓ **low** threshold: noise suppression
  - ✓ **middle** threshold: cluster candidate
  - ✓ **high** threshold: single channel clusters



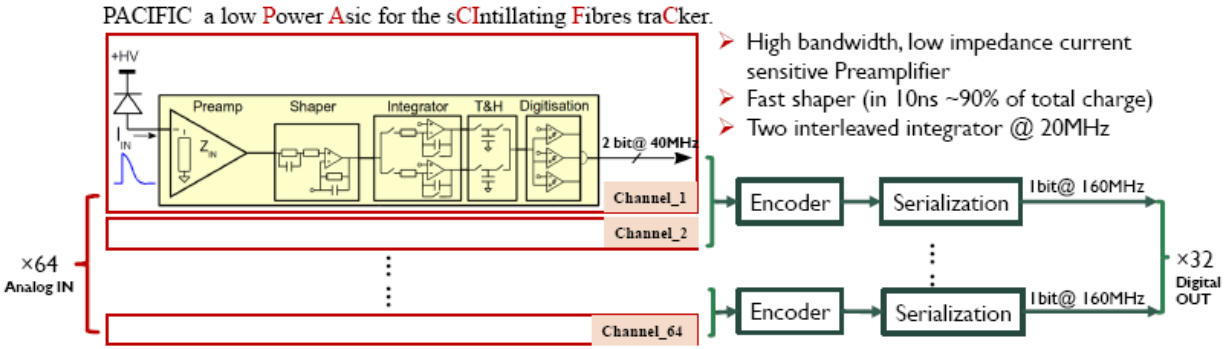


sketch of a typical cluster produced when particles passing through the SciFi detector

PACIFIC ASIC

2013.05	2013.11	2014.08	2015.08	2016.09	2017.03	2018 - 2019
PACIFICr0	PACIFICr1	PACIFICr2	PACIFICr3	PACIFICr4	PACIFICr5	
preamplifier only	single channel full analog chain	8-channel full analog chain	8-channel single-ended output full design	**64-channel single-ended output full design**	64-channel differential output full design	mass production & detector installation
					expected back in May	

SciFi Readout ASIC (PACIFIC) Quality Assurance System



To readout 1 PACIFIC chip means 5.12Gbps raw data rate

- production quantity: 12,000 × PACIFIC ASICs
  2500 × PACIFIC Carrier Boards
- minimum test speed: 1,000 × ASICs / institute / month
  500 × Carrier Boards / institute / month
- Requirement for the QA : <5 mins/ASIC (change ASICs manually)
  <13 mins/ Carrier Boards

- All the ASICs and Carrier Boards should be sperately test.
- Mass production will be done between 04/2018 ~ 05/2018.
- A automatical Quality Assurance system is needed!

PACIFIC ASIC

PACIFIC related schedule

[06/17] : PACIFIC5 back from foundary
[end 07/17] : PACIFIC5 finishes packaging
[beg 08/17] : DESY test beam with PACIFIC5
[end 08/17 ~ mid 09/17] : first 10×PACIFIC5 Carrier Board available
[09/17~10/17] : optimize QA setup with PACIFIC5, prepare for PRR

[10/17] : Electronics PRR
2 month [end 10/17 ~ end 11/17] : PACIFIC5p submission
2 month [end 12/17 ~ end 01/18] : PACIFIC5p back from foundary
1 month [end 02/18 ~ end 03/18] : PACIFIC5p finishes packaging
1 month [end 03/18 ~ end 04/18] : complete tests of the first 1,000×ASICs in HD
2 weeks [end 04/18 ~ end 05/18] : complete production of first 250×PACIFIC5p Carrier Board
[mid 05/18 ~ end 06/18] : complete tests of the 250 carrier boards ready for the first module integration

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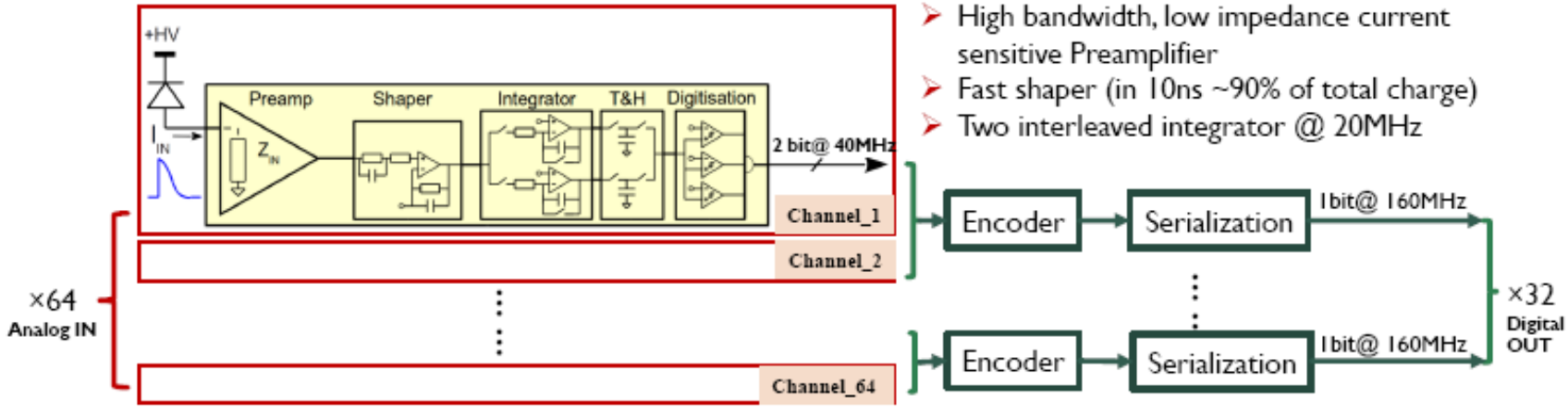
PACIFIC ASIC Test

PACIFIC a low Power Asic for the sCIntillating Fibres traCker.



- High bandwidth, low impedance current sensitive Preamplifier
- Fast shaper (in 10ns ~90% of total charge)
- Two interleaved integrator @ 20MHz

To readout 1 PACIFIC chip means 5.12Gbps raw data rate

PACIFIC ASIC test criteria

basic tests	▪ power consumption measurement ▪ I²C communication ▪ digital output connections ▪ input connections ▪ determine the unique operating parameters for the ASIC ✓ $V_{ref} = +0.5V$ ✓ $V_{refDCFB} = +0.7V$
classify tests	▪ linearity & dynamic range tests of the common/local thresholds ▪ DC baseline variations across all channels ▪ linearity & dynamic range tests of the trim DACs ▪ [optional] internal ADC calibration ▪ [optional] internal temperature sensor calibration
parameter optimization	▪ determine trim-DAC values for each channel to equalize DC baselines across two integrators ▪ save configuration file into data base

PACIFIC ASIC test	PACIFIC Carrier Board test
4× ASIC socket board - 4 × ASIC sockets - 4 × INA219B current sensors - 4 × ADC_in analogue output routed to TEMP_0~3 pins on the FMC connector - External power supply for on-board ICs	FMC connector intermedia board simple pin-to-pin adapter PCBs to avoid broken FMC connectors on the DAQ side due to too many times plug-in and out
test DAQ : PACIFICROB	
PC : process and save test results	
DC power supply (with output 5V/3A at least)	
-	charge injection board
-	(arbitrary) waveform generator

SciFi Readout ASIC (PACIFIC) Quality Assurance System

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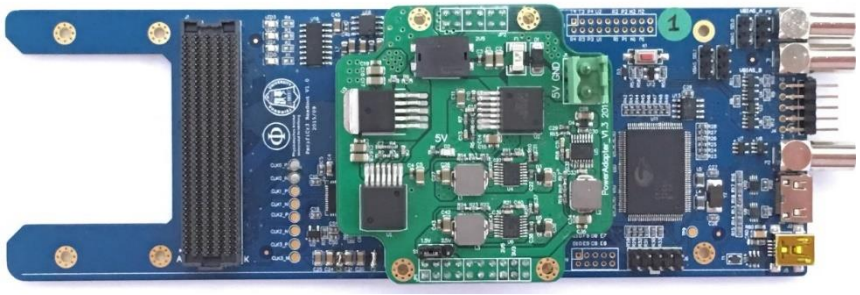
basic tests	▪ power consumption measurement ▪ I²C communication ▪ digital output connections ▪ input connections ▪ determine the unique operating parameters for the ASIC ✓ V_{ref} = +0.5V ✓ $V_{refDCFB}$ = +0.7V
classify tests	▪ linearity & dynamic range tests of the common/local thresholds ▪ DC baseline variations across all channels ▪ linearity & dynamic range tests of the trim DACs ▪ [optional] internal ADC calibration ▪ [optional] internal temperature sensor calibration
parameter optimization	▪ determine trim-DAC values for each channel to equalize DC baselines across two integrators ▪ save configuration file into data base



Single-ended version for PACIFIC v4

- **Two versions have been designed, produced and tested, by Tsinghua and Heidelberg**

SLVS differential version for PACIFIC v5

- key components:
  - ✓ Altera Cyclone FPGA
  - ✓ precision clock conditioner
  - ✓ (LVDS-SLVS convertor)
  - ✓ 8-channel, 12-bit ADC
  - ✓ USB interface to PC

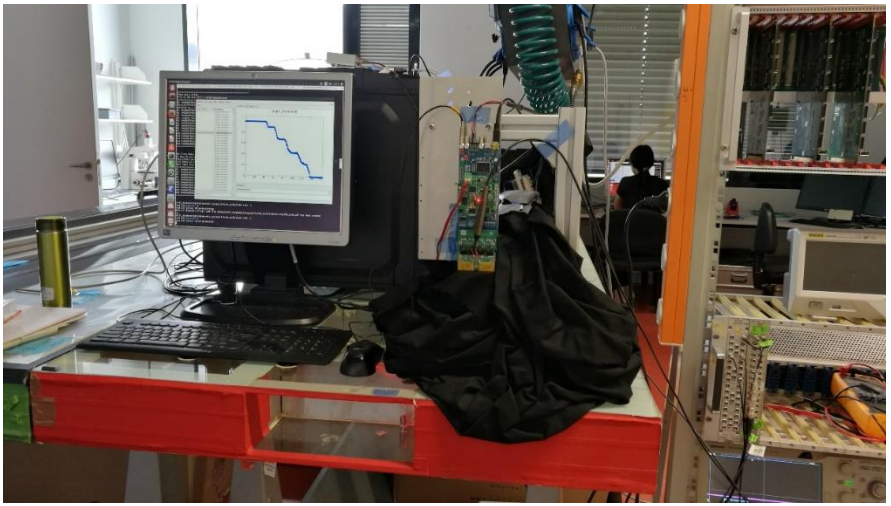
Firmware implementations for QA testbench

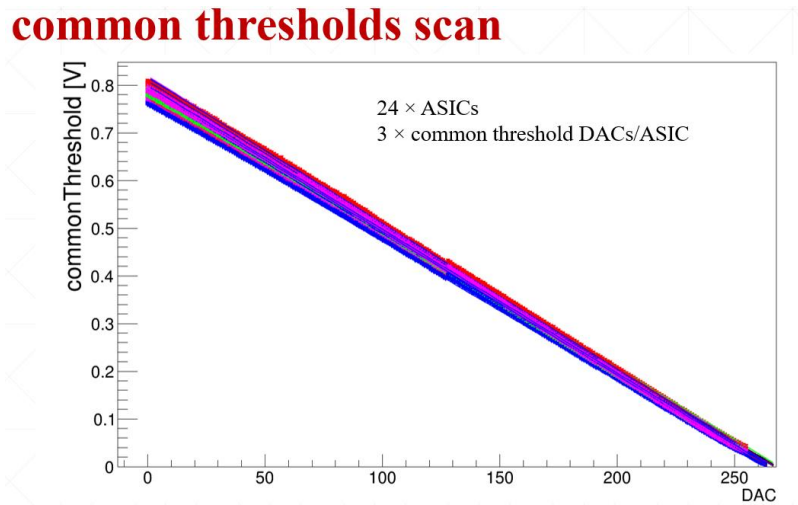
Prototype implementation has been designed and tested with PACIFICr4 by our exchange student Yuyan Huang (Tsinghua)

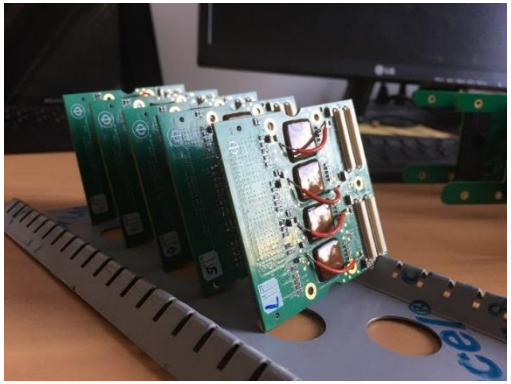
current sensors (INA219B) controlled by I2C	[not yet]	
write then read back one PACIFIC slow control register	[YES]	**<500µs**/ASIC
variant pattern injection test (aim for data error rate 0%)	[YES]	**<ms**/ASIC
resistor ladder circuit readout by external ADCs	[not yet]	
voltage scans using PACIFIC calibration output readout by external ADCs	[YES]	**~50ms**/scan/ASIC for V_{ref}/$V_{refDCFB}$ **~40s**/ASIC for all 195 comparators
threshold scans : s-Curve analysis	[YES]	**<5s**/scan/ASIC with ~600kHz trigger rate

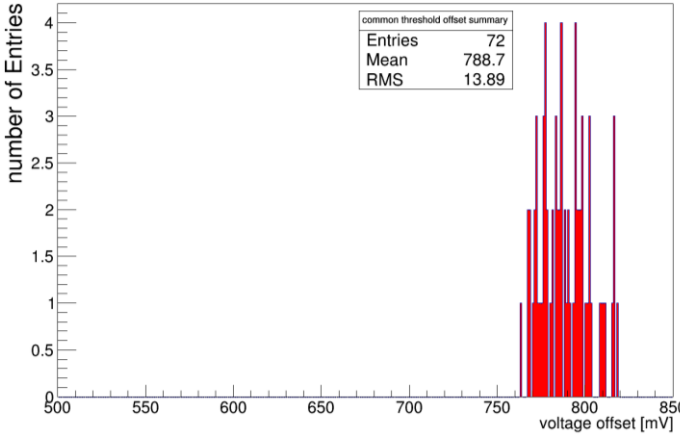
Goal : ***<5min/ASIC***, ***<13mins/carrier board*** during the mass production tests

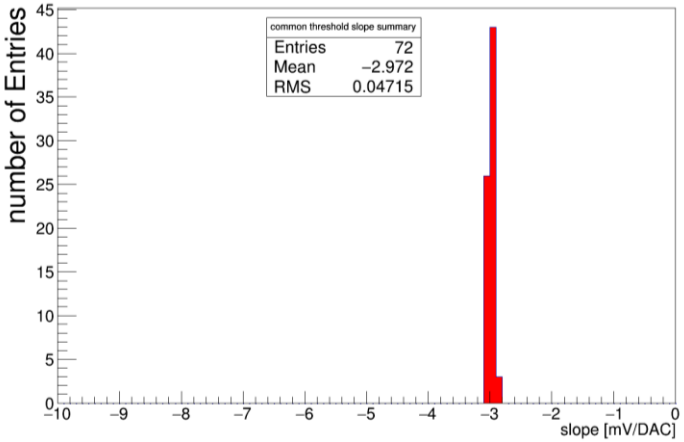
SciFi Readout ASIC (PACIFIC) Quality Assurance System (v4)



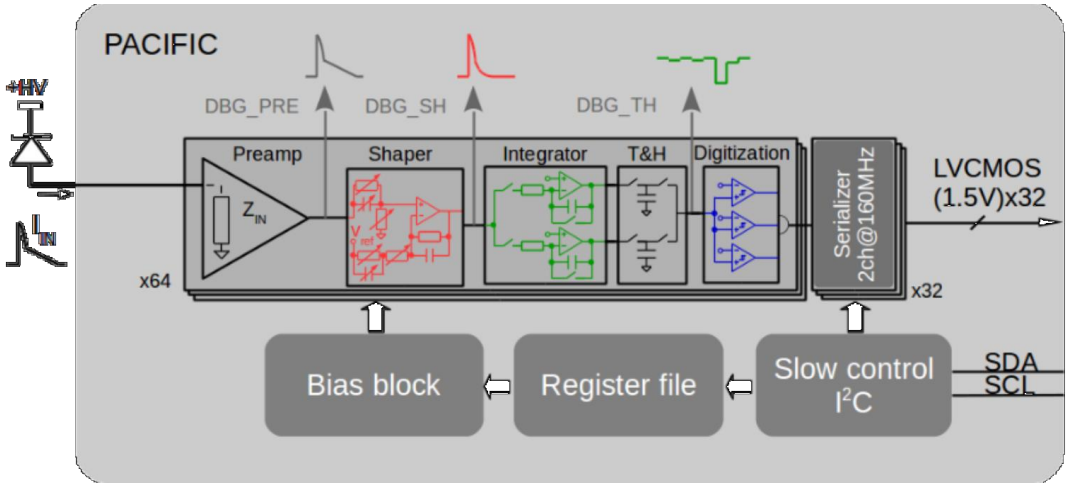




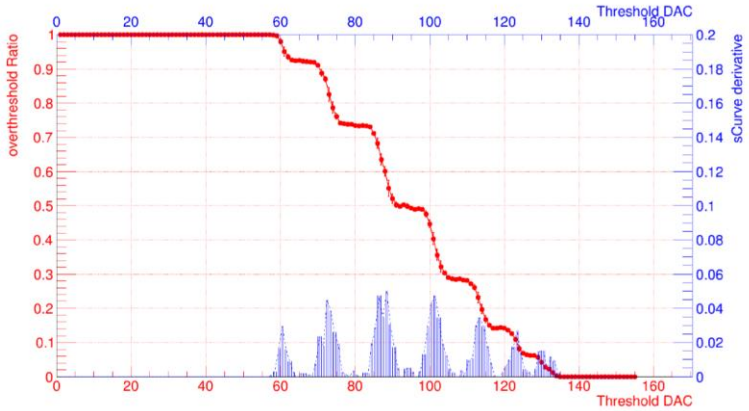




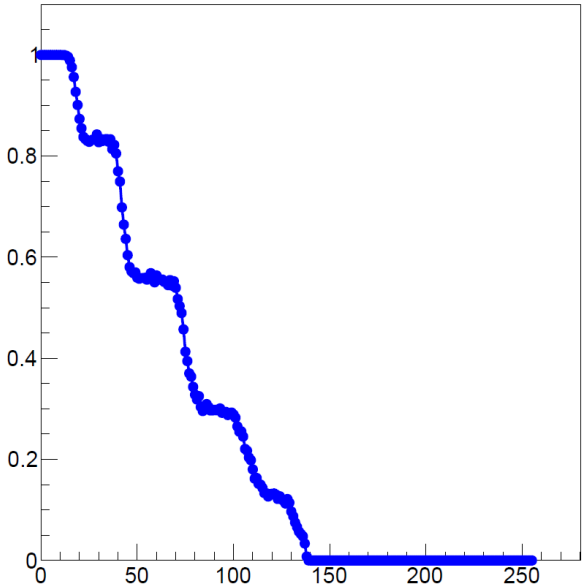
SciFi Readout ASIC (PACIFIC) Quality Assurance System (v4)



- 5ns-width light pulse generated by vertical-cavity surface-emitting lasers (VCSEL)
- using SciFi custom SiPM arrays

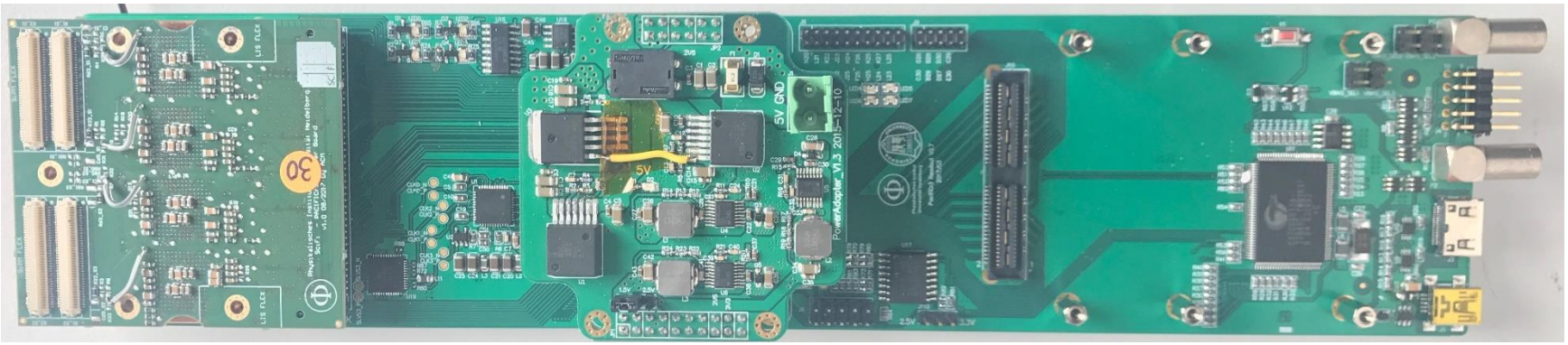


PACIFIC threshold scan result : clear photo-peak steps

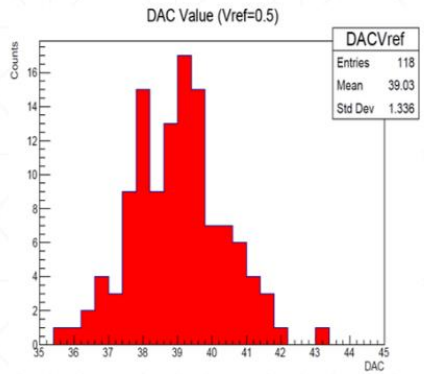


SciFi Readout ASIC (PACIFIC) Quality Assurance System & Mass Production in 2018

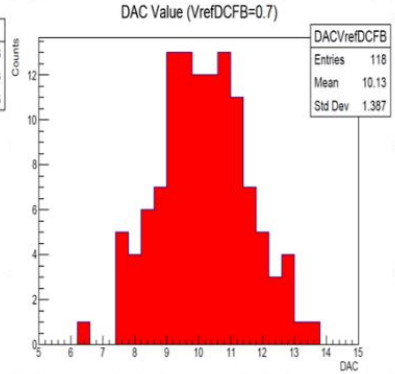
First 128 PACIFIC v5 ASICs have been tested by using the Quality Assurance System



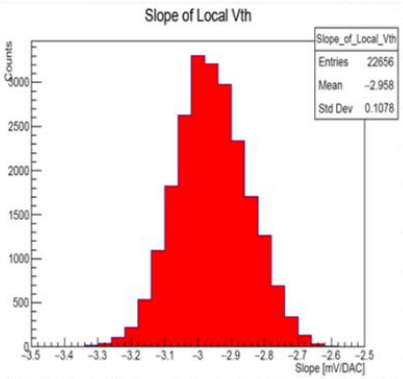
SciFi Readout ASIC (PACIFIC) Quality Assurance System & Mass Production in 2018



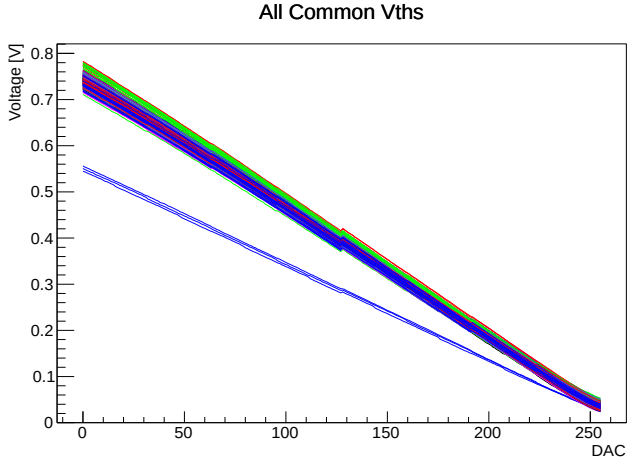
distribution of the V_{ref} = 0.5V setting point



distribution of the $V_{refDCFB}$ = 0.7V setting point



distribution of the resolution of local threshold DACs



ASIC Test Result = 123/128 ≈ 96.1%

ASIC ID	63	143	210	280	301
I2C read & write	×	normal	×	normal	×
common/local Vth DAC result	×	×	×	×	×
V_{ref} DAC result	×	normal	×	×	×
$V_{refDCFB}$ DAC result	×	normal	×	×	×

In 2018, 2500 PACIFIC frontend boards will be produced and test in China !

LHCb Tsinghua Group in SciFi R&D

- SciFi Detector Performance Evaluation Electronics
- SciFi Detector Performance Study
- SciFi Track Reconstruction Software Package Development
- SciFi Readout ASIC (PACIFIC) Quality Assurance System
- SciFi Readout ASIC Board Mass Production and Test (2018)