ATLAS Phase-I upgrade Muon sTGC Front-End Electronics

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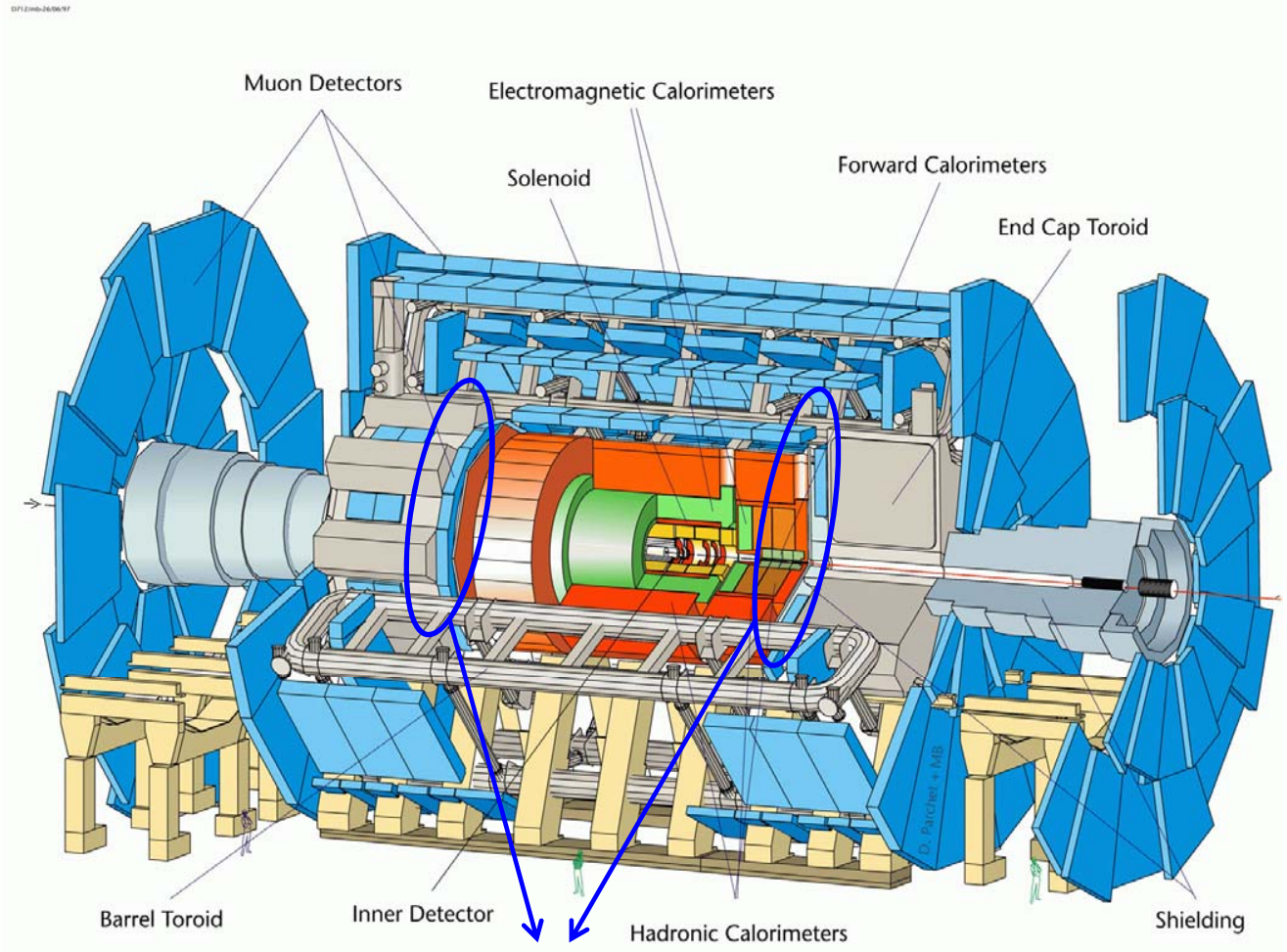
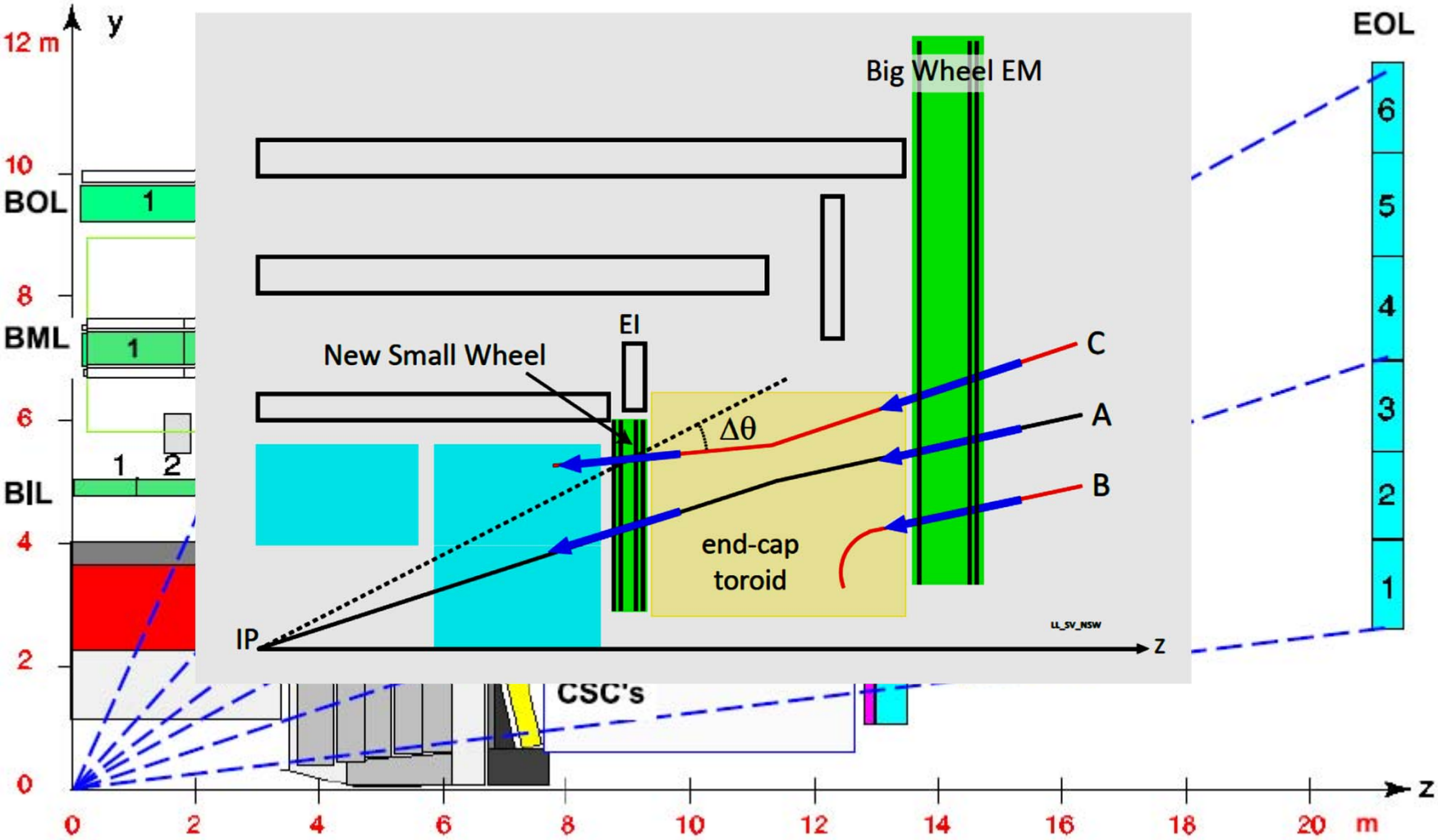
Introduction



SW (Small Wheel)

- **LHC will be upgraded to 14TeV proton-proton collision**
- **ATLAS: Current SW has fake event up to 98%**
- **Build a completely New Small Wheel (NSW)**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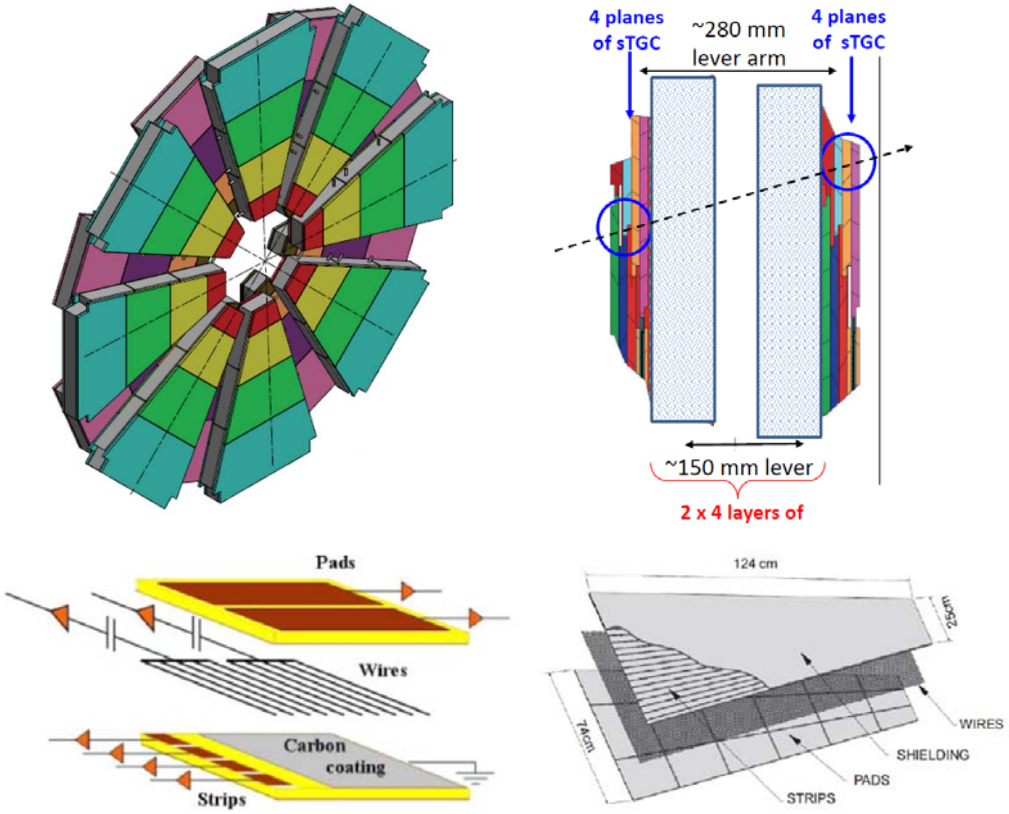
NSW Detector

- sTGC: online trigger detector
- MicroMegas : offline tracking detector
- 768 sTGC modules
- sFEB to handle 512 Strip signals
- pFEB to handle pad/Wire signals for each moudle

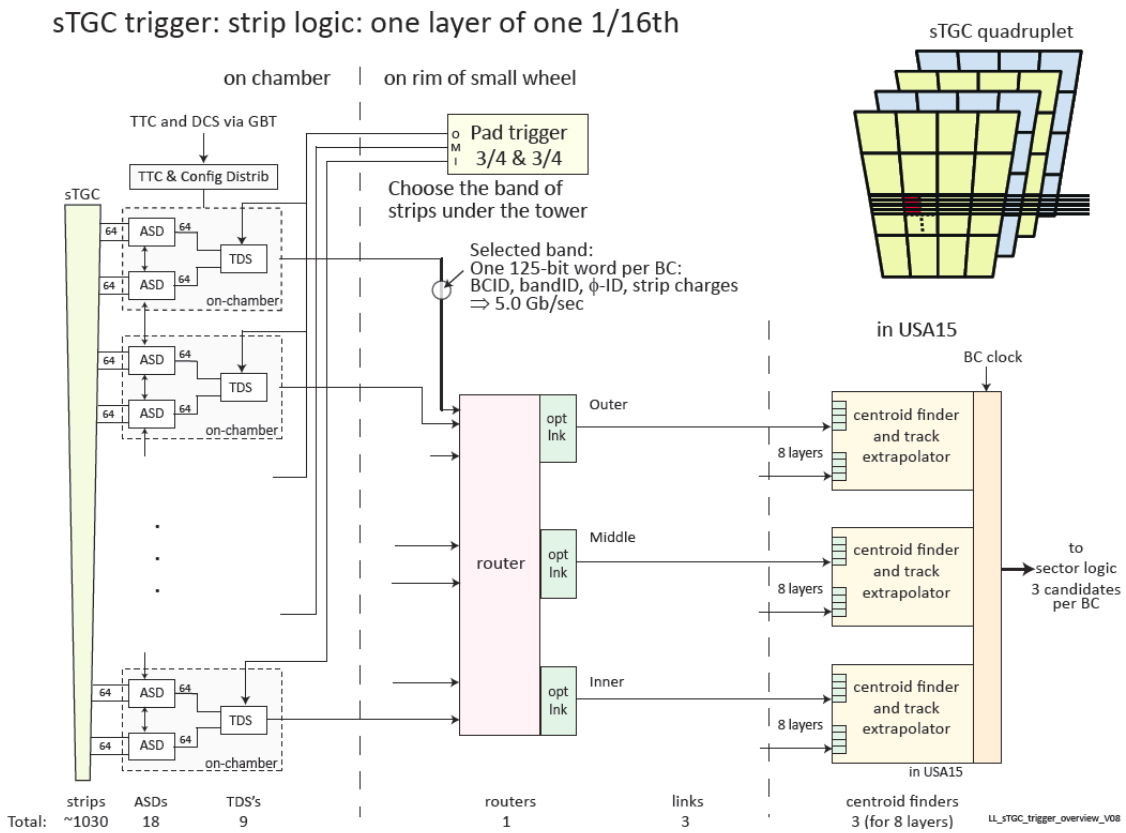


(a) a (b) b

Table 12.1: Some sTGC and MM parameters

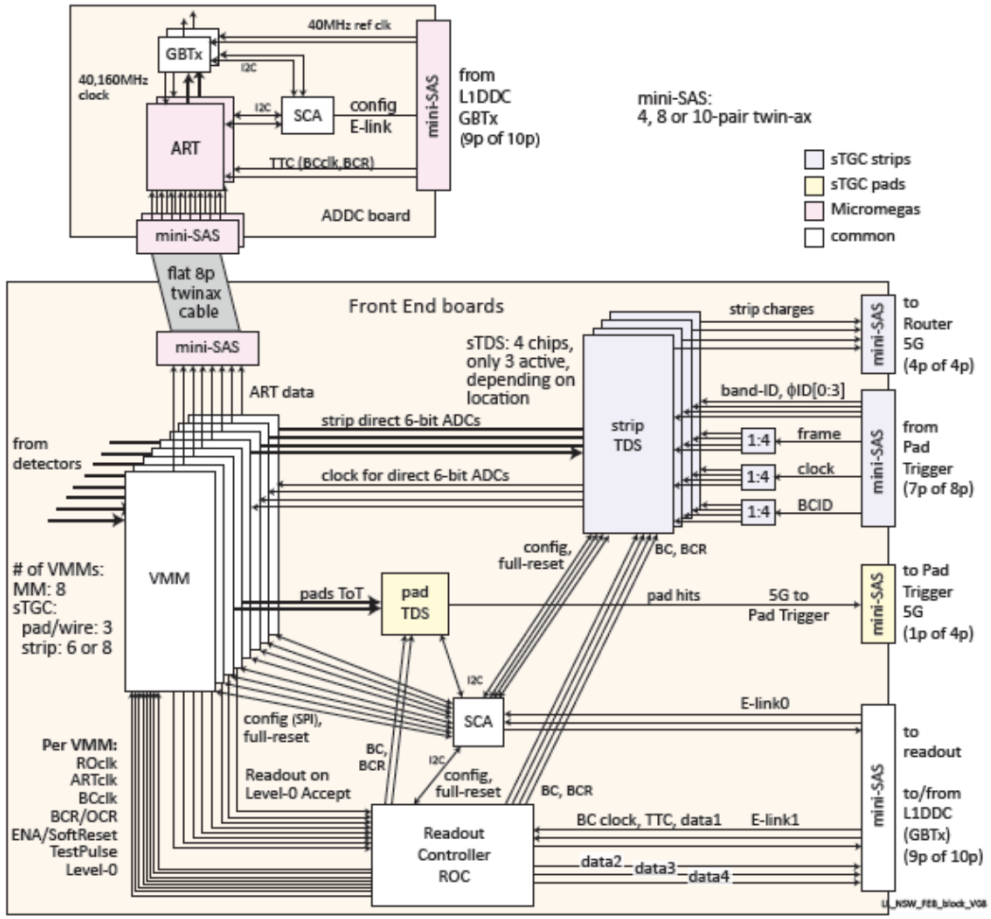
	sTGC	MM
strip width	3.2mm	0.5mm
strips/layer	~1050	8,192
strips/octant	17,260	131,072
triggering pads/octant at $\|\eta\|$ <2.4	2,362	–
All pads/octant	2,738	–
wires/octant	736	–
channels/octant	20,734	131,072
channels/two end-caps	331,744	2,097,152
VMM chips/octant	382	2,048
MM trigger elements	–	32,768

1/16 sTGC trigger diagram



- **768 sTGC module：**
  - **768 Pad/Wire Front end boards(192 channels) in size 16.5*6cm**
  - **768 StripFront end Boards(512 channels) in size 27*6cm**
- **More than 330,000 channels**

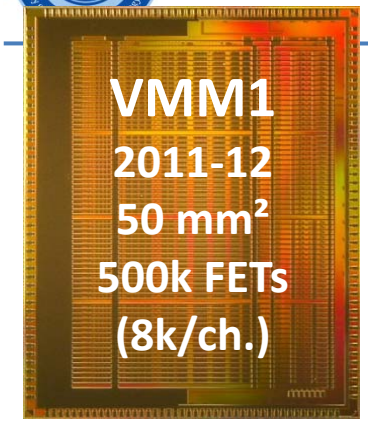
pFEB/sFEB specification



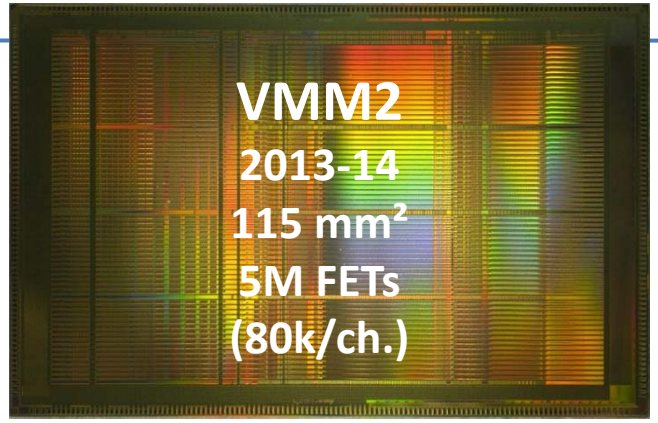
- Read strip and pad/wire signals to VMM on sFEB and pFEB;
- 6B trigger of 2×VMM sent to TDS; 10B data of each VMM to ROC
- pTDS → Pad Trigger, decision sent to sTDS; sTDS → Router
- Configurations and 40MHz clock L1DDC → ROC/SCA
- Components: VMM, TDS, SCA, ROC; FEAST; miniSAS; GFZ

- FEB design: strict PCB size limitation; short traces for analog and high speed data transmission; analogue/digital signals and grounds well separated; etc.

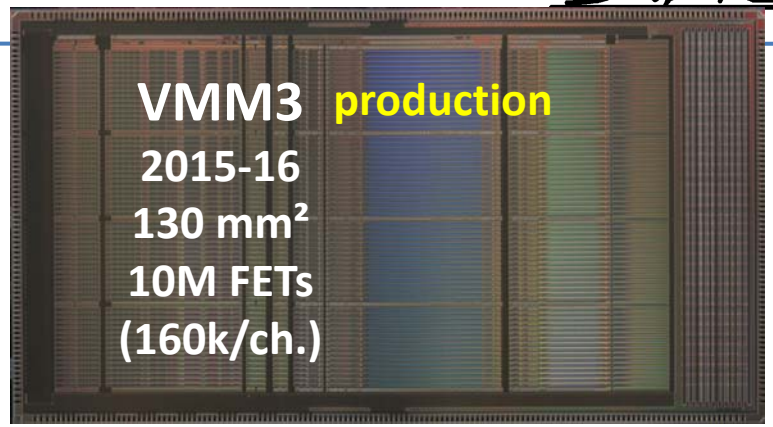
Path Towards VMM



- mixed-signal
- 2-phase readout
- peak and timing
- neighboring
- sub-hysteresis
- few timing outputs



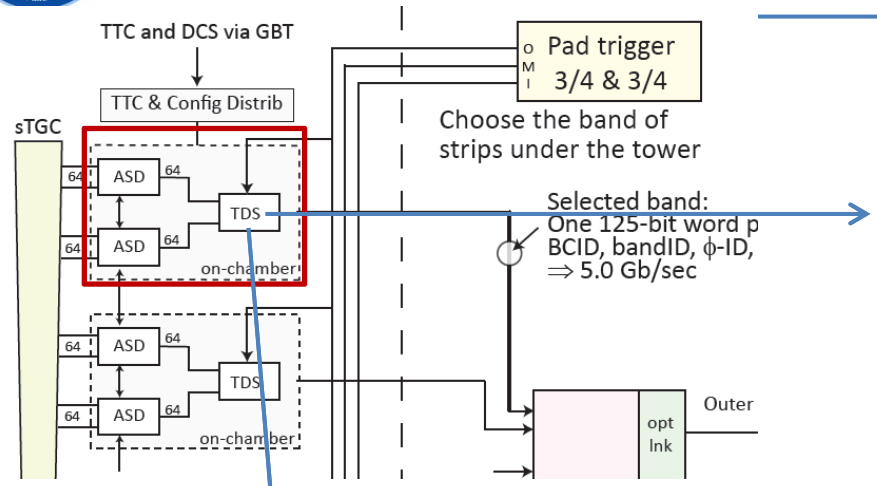
- mixed signal
- continuous fully-digital readout
- current-output peak detector
- increased range of gains
- three ADCs per channel
- FIFOs, serialized data with DDR
- serialized ART with DDR
- additional timing modes
- 64 timing outputs
- ITAR
- additional functions and fixes



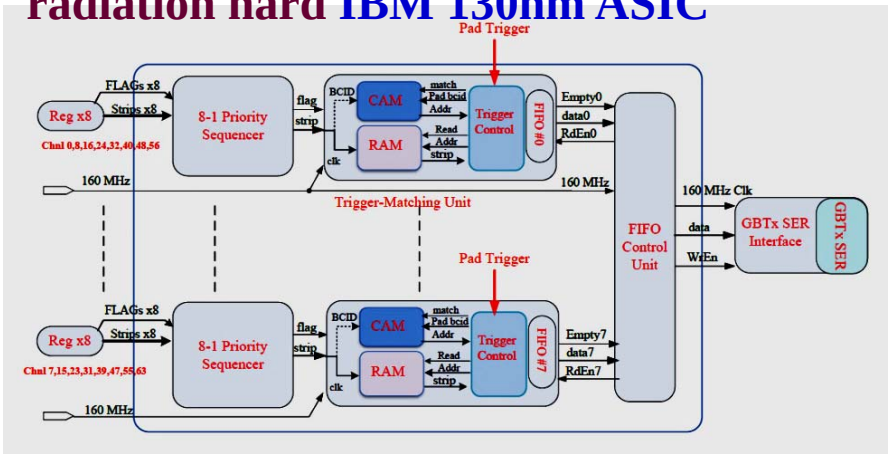
- mixed signal + digital
- continuous simultaneous readout
- SEU-tolerant logic
- deeply revised front-end for TGC (2nF, 50pC, fast recovery, ...)
- L0 handling digital core
- SLVS and new config. interface
- new reset control and fast reset
- timing at threshold
- timing ramp optimization
- pulser range extension
- ART synchronization
- 32-channel skip
- additional functions and fixes

Designed at BNL

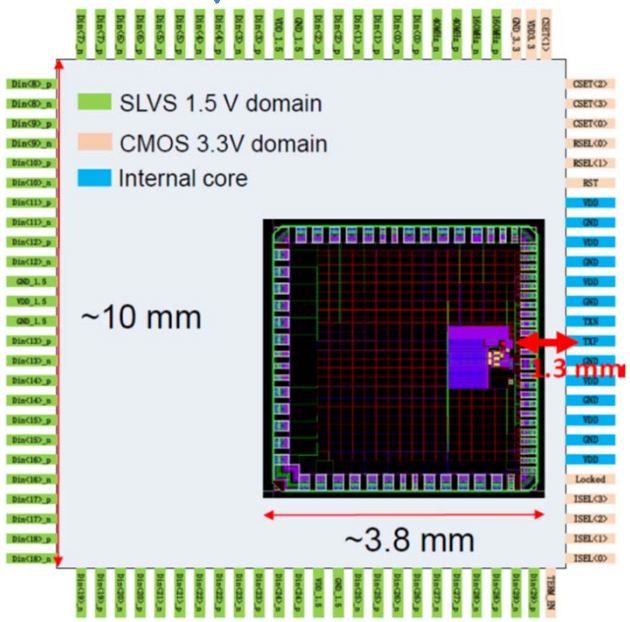
Trig Data Serializer: TDS



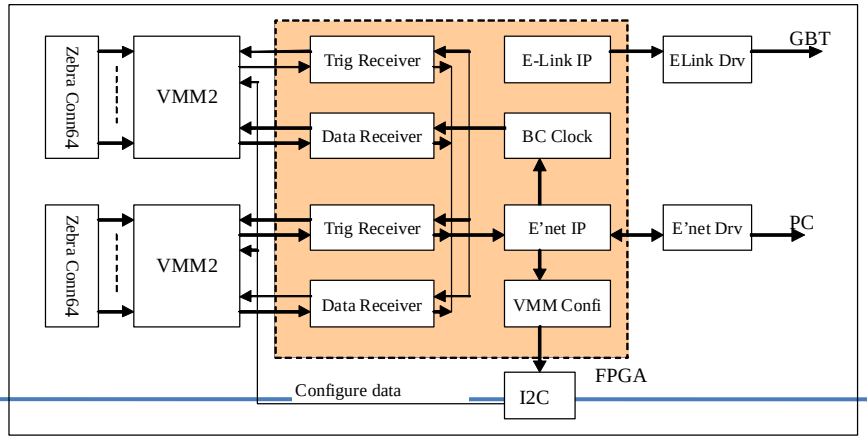
radiation hard IBM 130nm ASIC



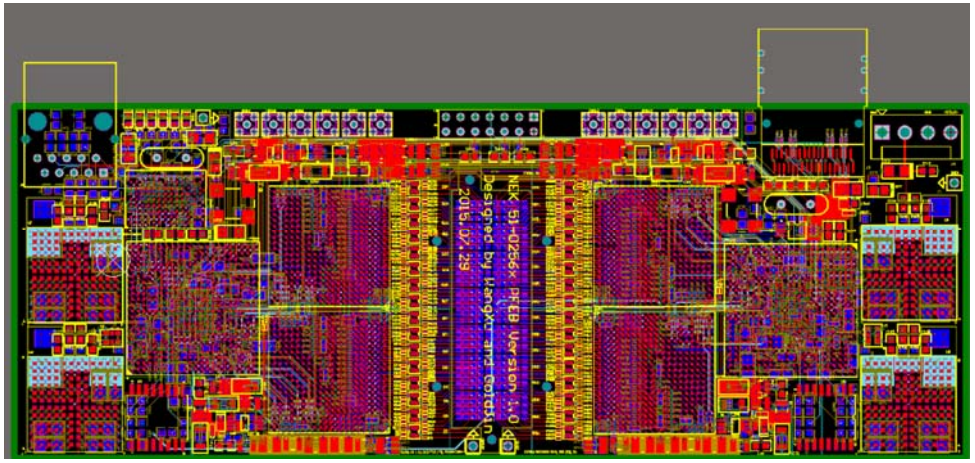
- **Pad/Strip trig data preprocessing**
- **Output: 128b@25ns, 5.1Gbps**

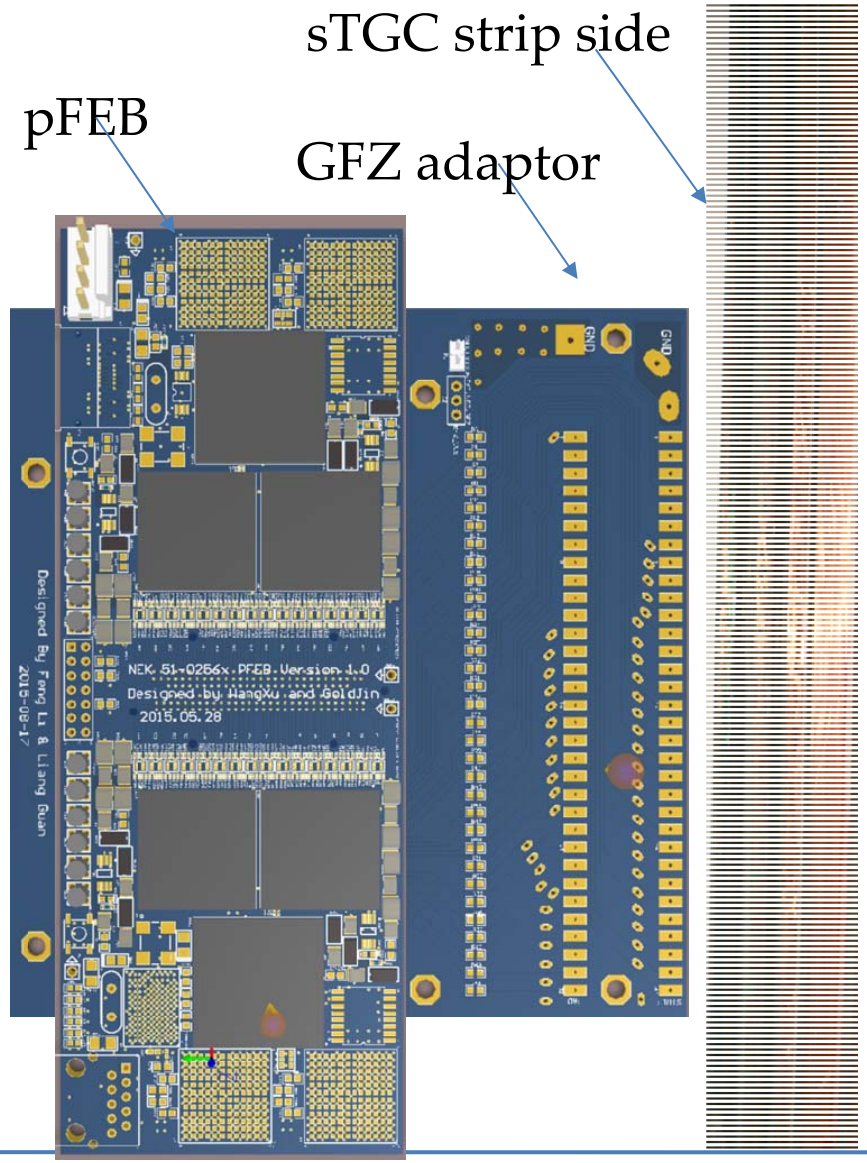


Designed at UM



pFEB v1.0 based on VMM2



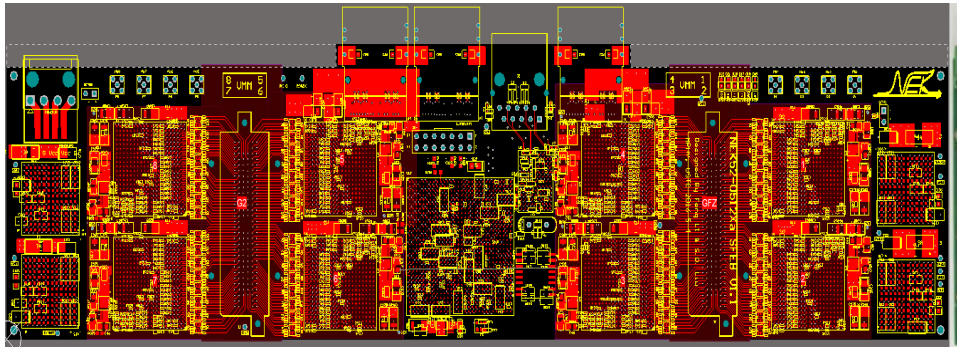


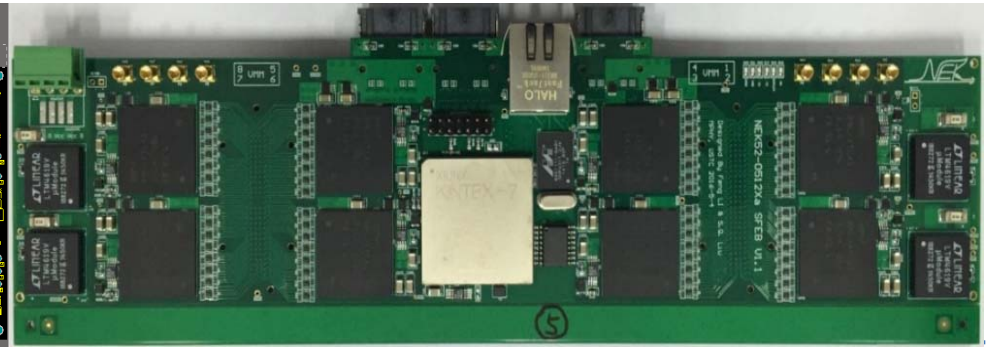
Integration test with mini-sTGC at UM

sFEB v1.0/1.1 based on VMM2

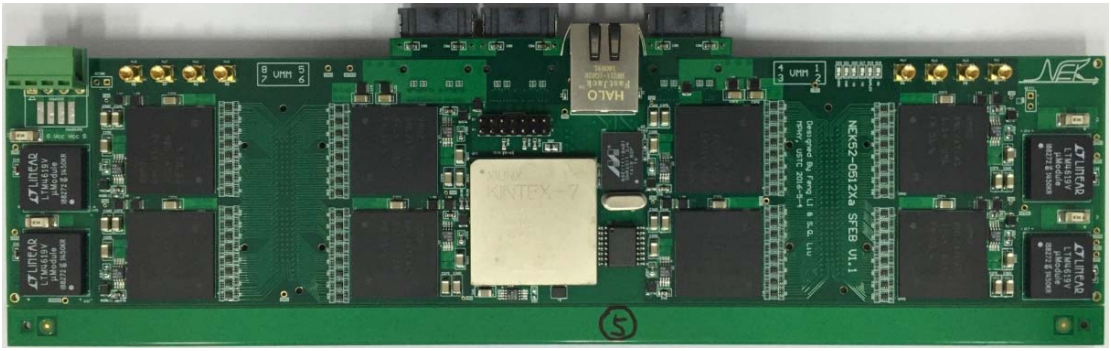
- **VMM configuration and raw data read out**

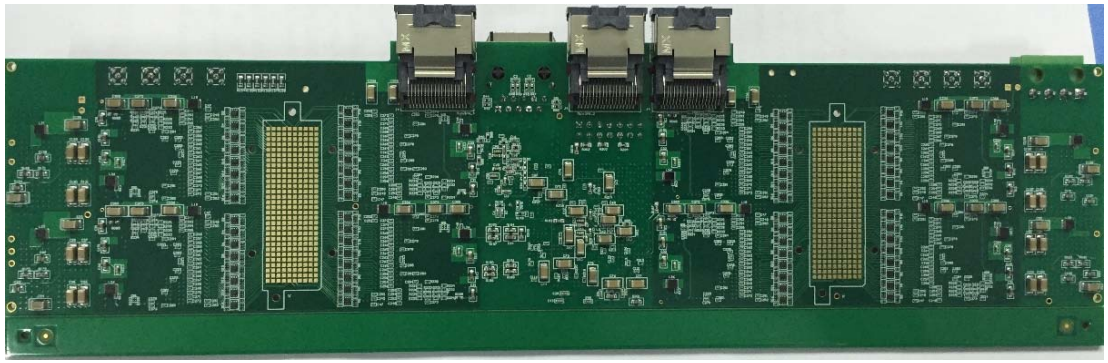
- **MiniSAS connectors added on sFEB v1.1 for data communication**





sFEB v1.1 and pFEB v1.2



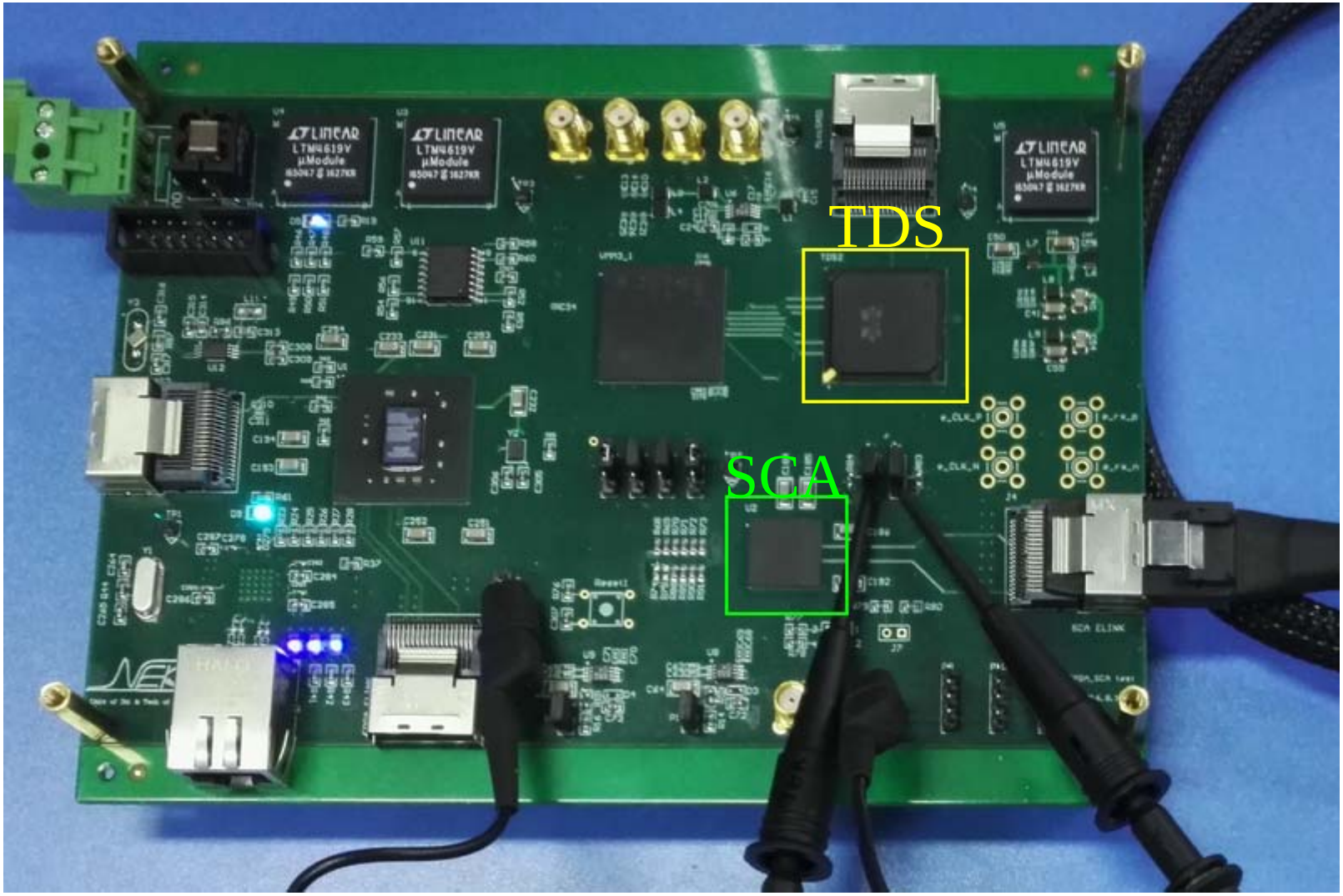


SFEB v1.1

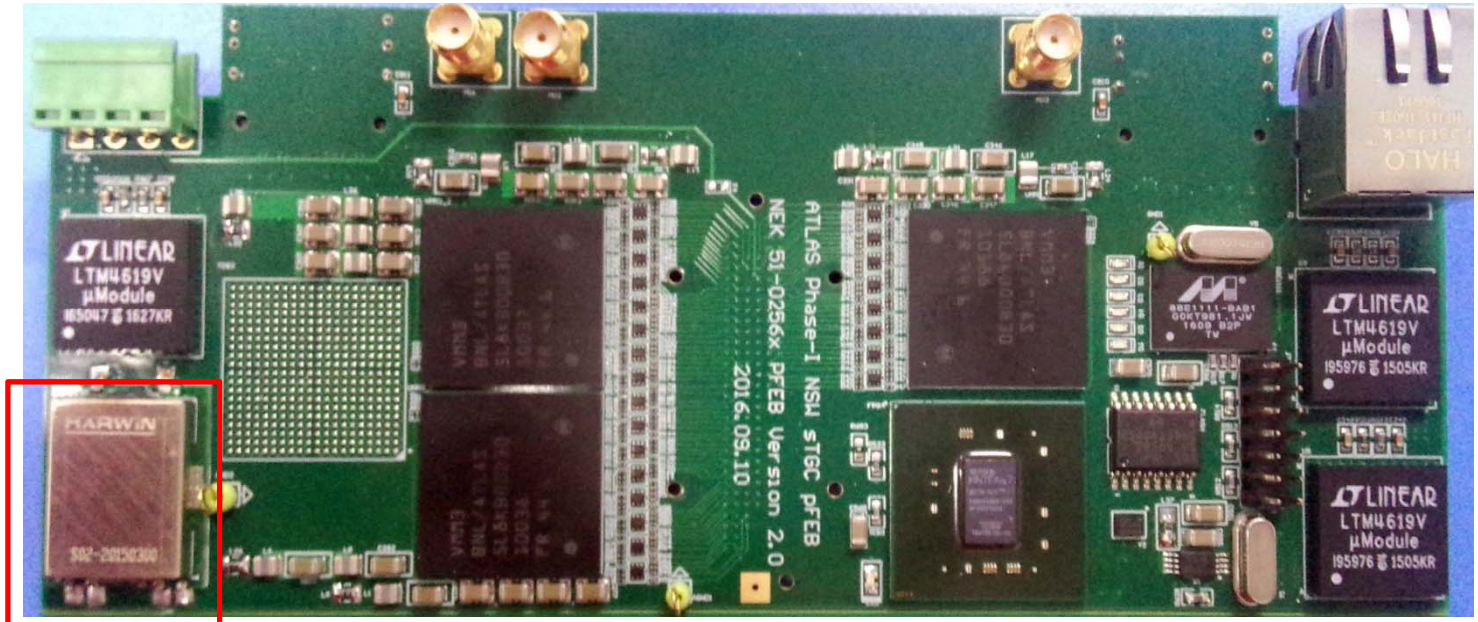
pFEB v1.2

- **NSW upgrade Committee visited USTC for site review in June 2016.**

SCA Board



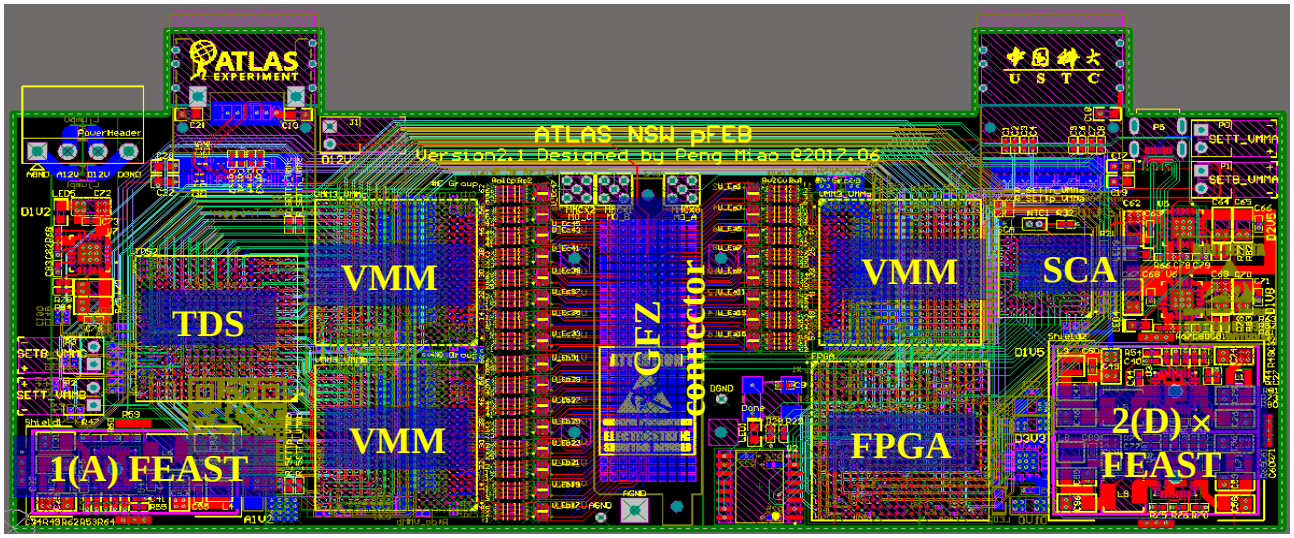
pFEB 2.0 board based on VMM3



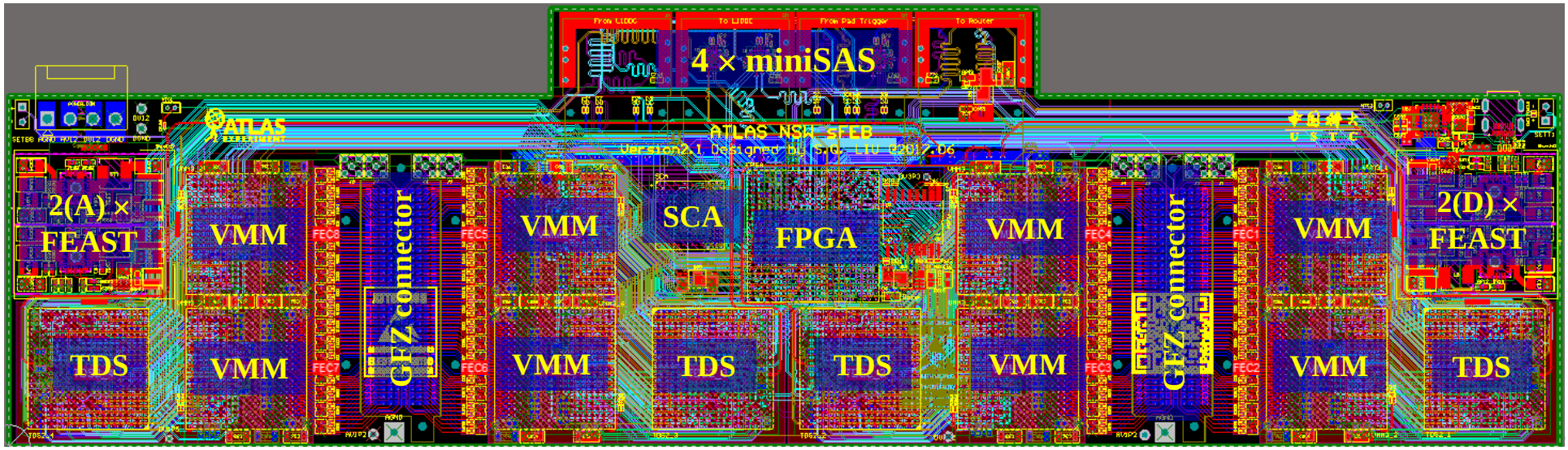
pFEB 2.0

One FEAST module is used as analog power supply

pFEB/sFEB v2.1



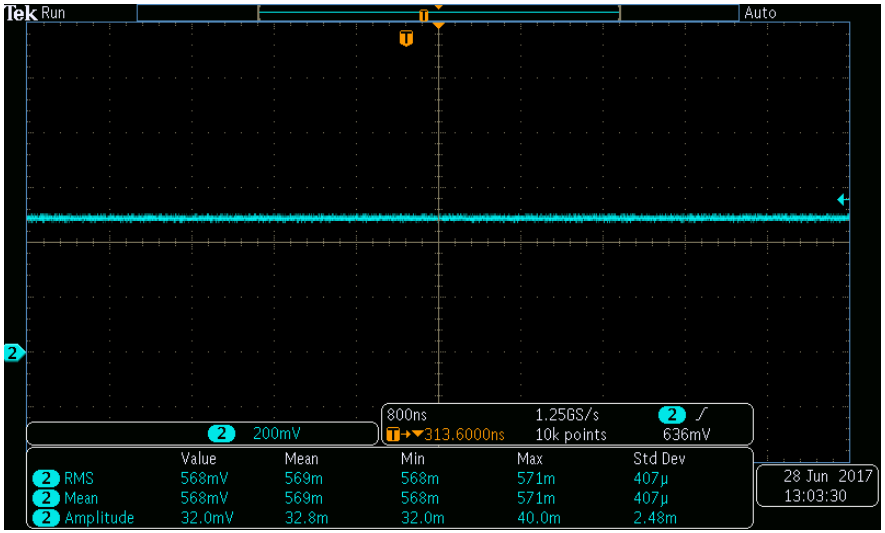
- Based on VMM3
- pFEB: 16.5 × 6cm, 12 layers, 192 Channels;
- sFEB: 27 × 6cm, 14 layers, 512 channels;
- Used at WZ/CERN/McGill /SDU for chamber test



Electronics tests of pFEB v2.1

- Noise of pad signal on pFEB:

Gain (mV/fC)	RMS (mV)	Amplitude (mV)
0.5	0.41	2.5
1	0.50	3.0
3	0.44	4.9
4.5	0.50	5.3

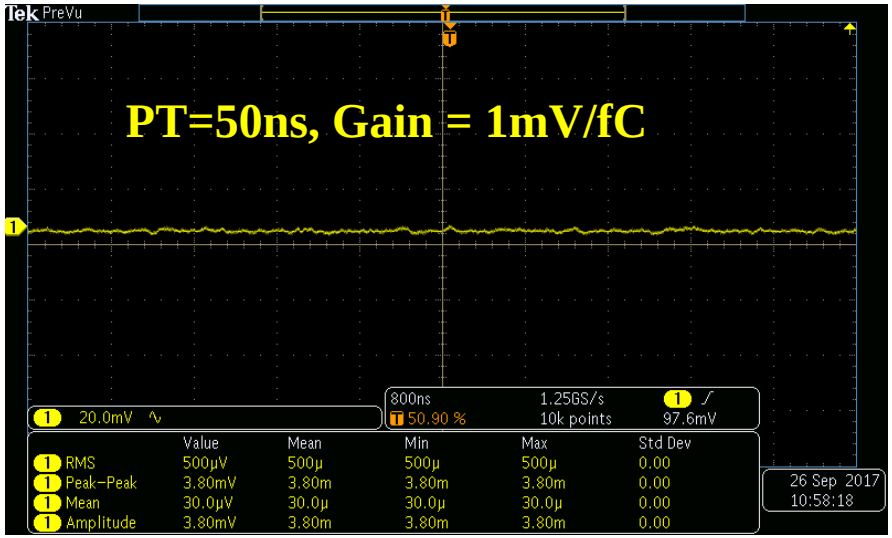


The typical intrinsic noise of pFEB is < 0.5mV for all gains

Electronics tests of sFEB v2.1

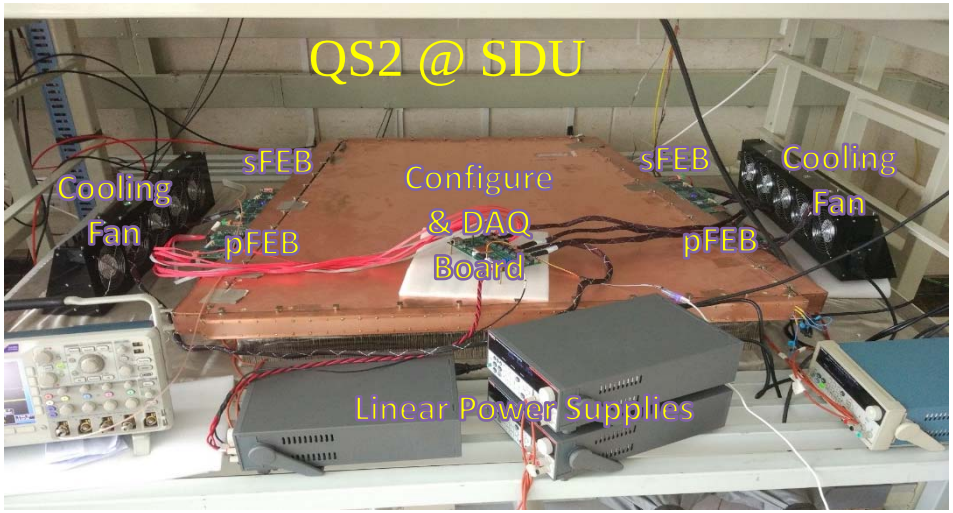
- Noise of strip signal on sFEB:

Gain (mV/fC)	RMS (mV)	Amplitude (mV)
0.5	0.42	3.2
1	0.50	3.8
3	0.52	4.0
4.5	0.54	4.2



The typical intrinsic noise of sFEB is ~ 0.5mV for all gains

FEB v2.1 sTGC test @ SDU & WZ



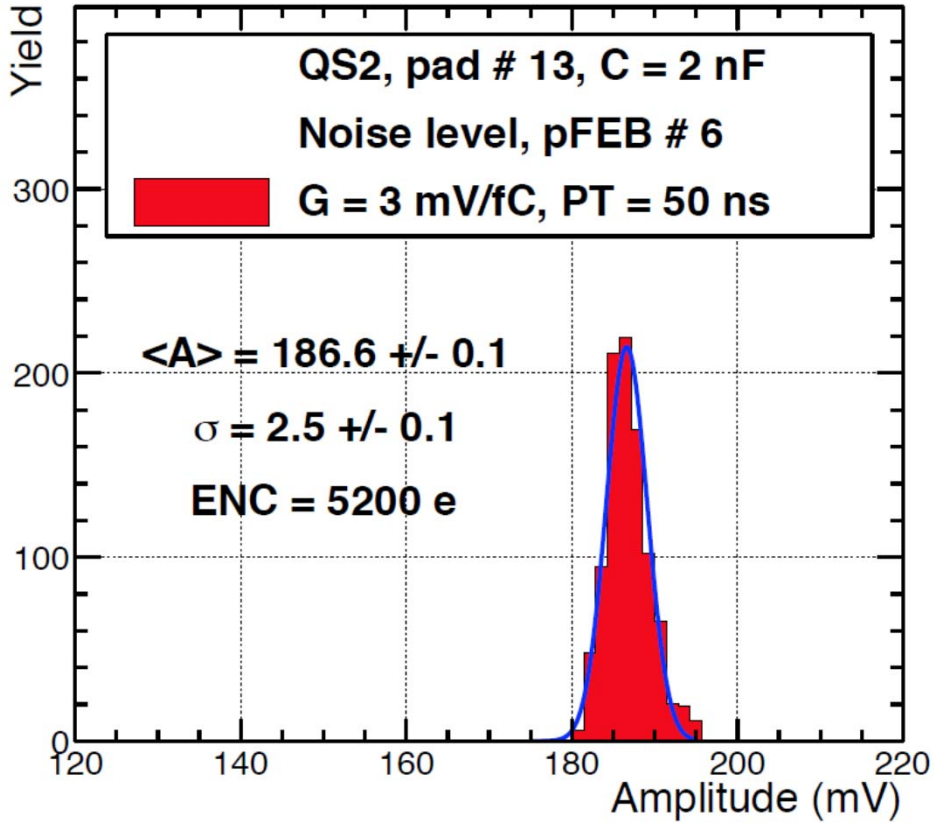
- Full size QS2 with soldered adapter board and sFEB/pFEB
- External trigger by scintillator cosmic coincidence
- Configure and readout via a simple DAQ board
- Good detector grounding and efficient chip cooling are vital

FEB v2.1 sTGC test @ SDU & WZ

- pFEB noise on sTGC @ WZ:

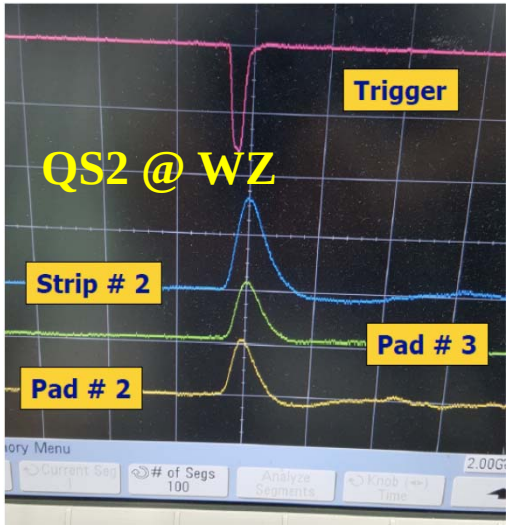
  - Intrinsic noise of pFEB w/o sTGC is reported as 700-800e of ENC

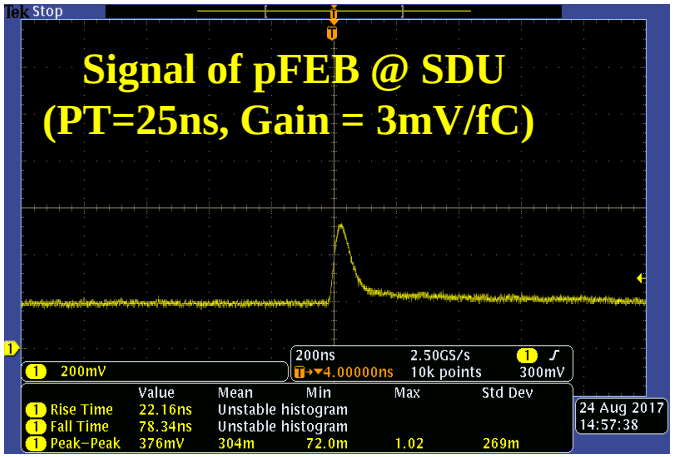
  - When connected to a particular sTGC pad of ~ 2nF and powered up to 3.2kV, the level of noise is ~ 5200e ENC

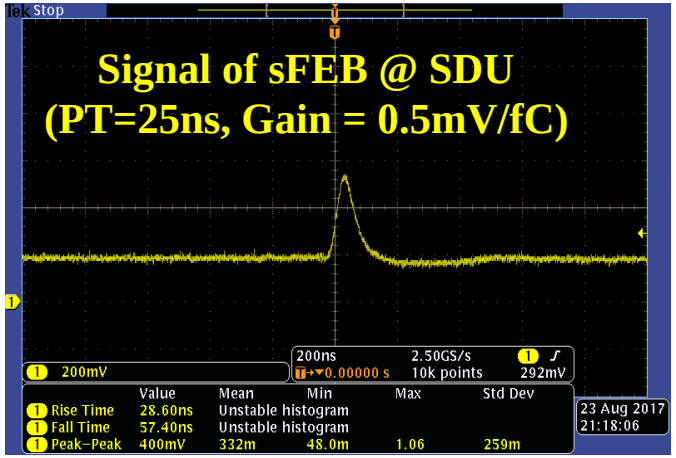


FEB v2.1 sTGC test @ SDU & WZ

- Cosmic signals:



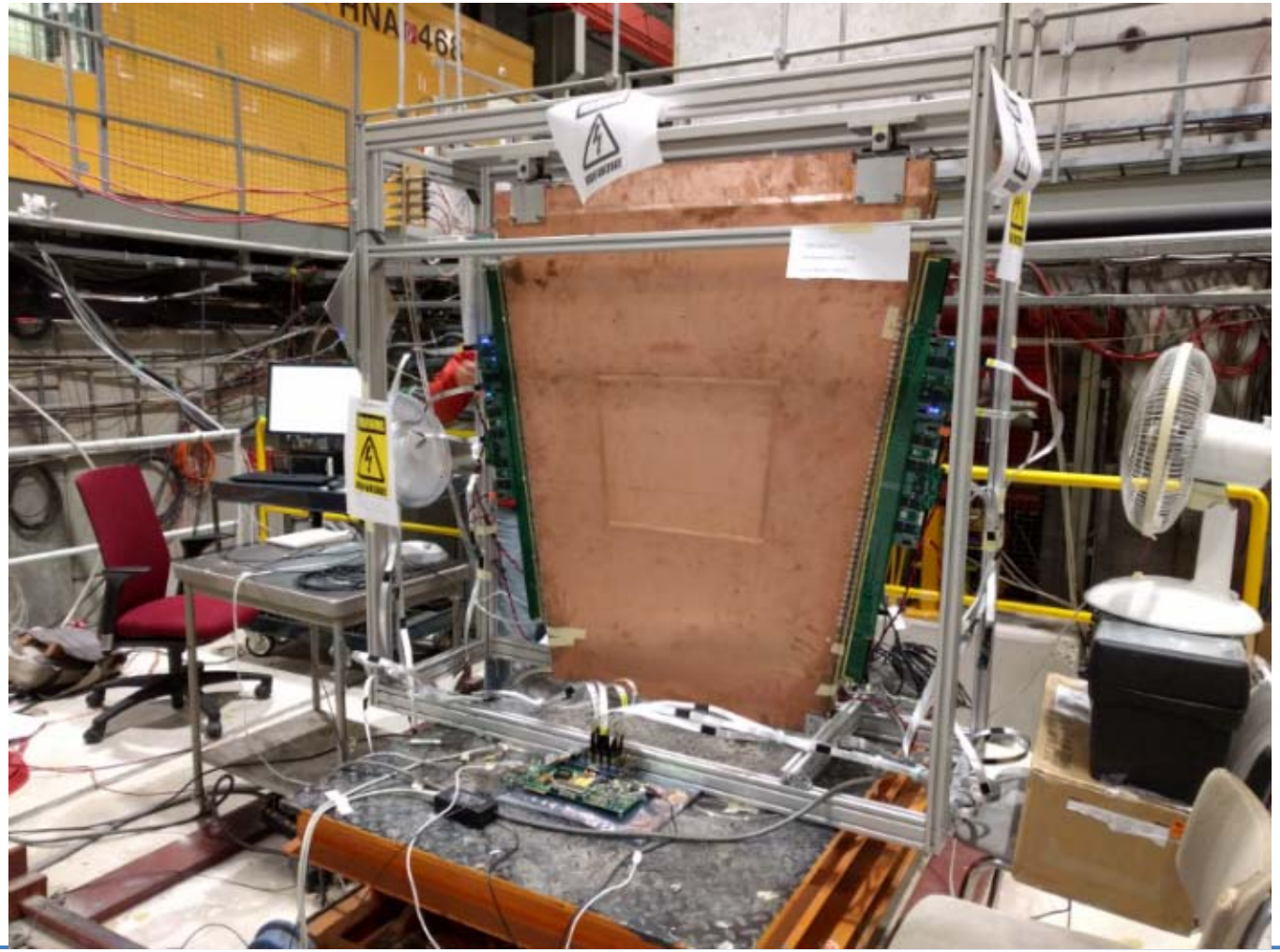




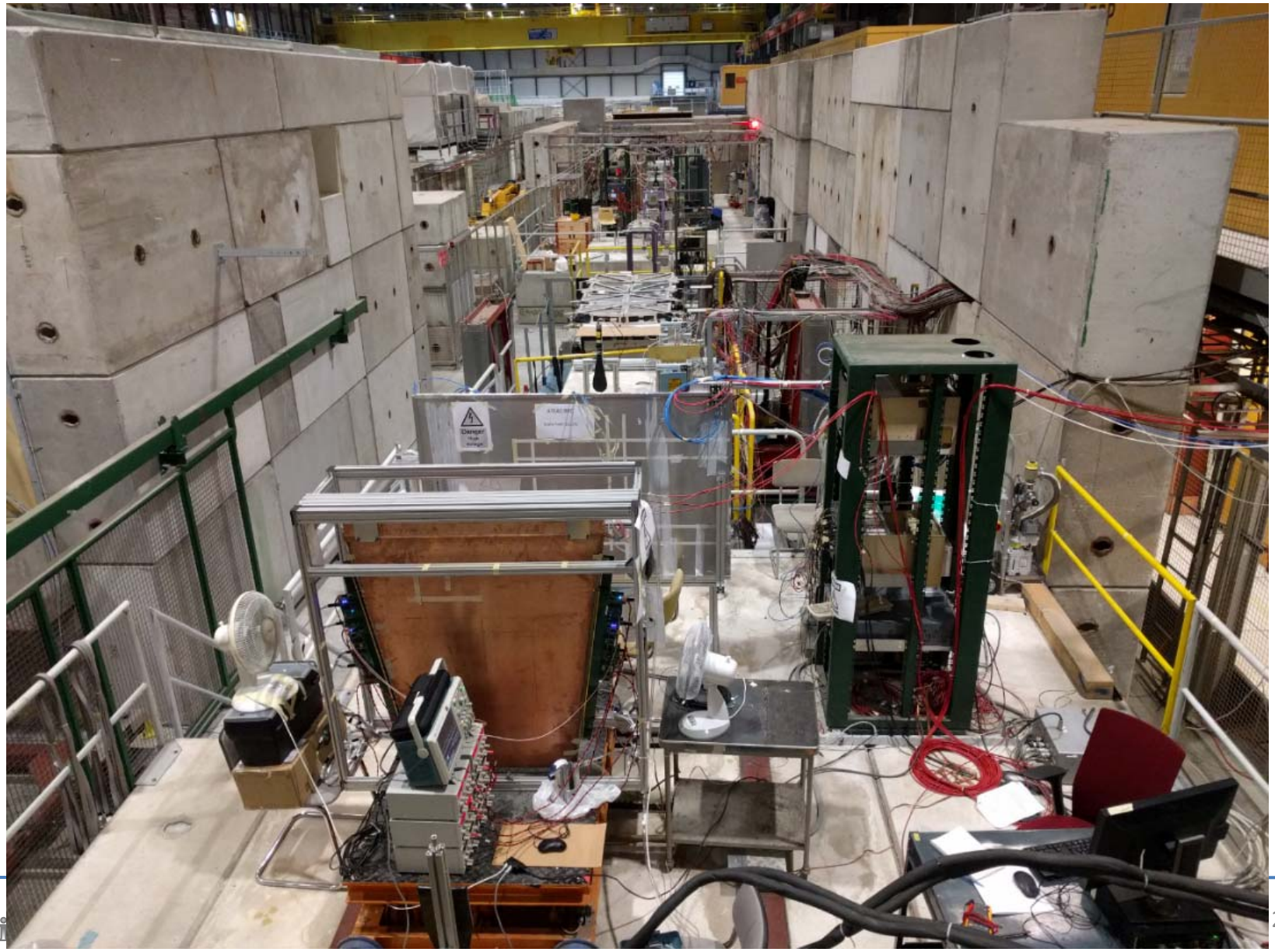
➢ Clean and good analog signals of both sFEB and pFEB can be observed.

Beam Test at CERN, October 5,2017

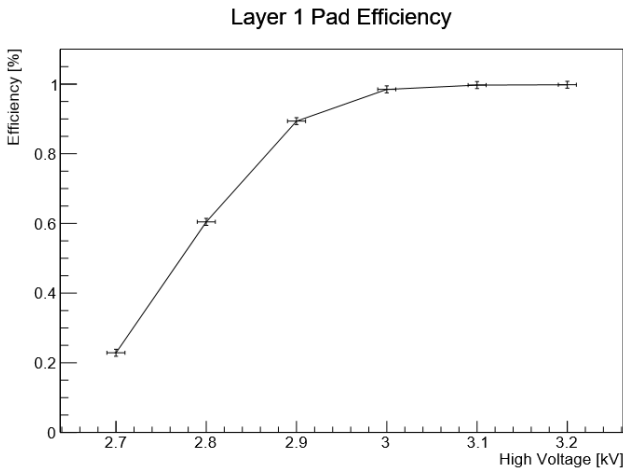
Full setup with pFEB and sFEB installed
(reduced TTC, L1DATA to 80 Mbps; changed the firmware to support VMM daisy chain cfg.)

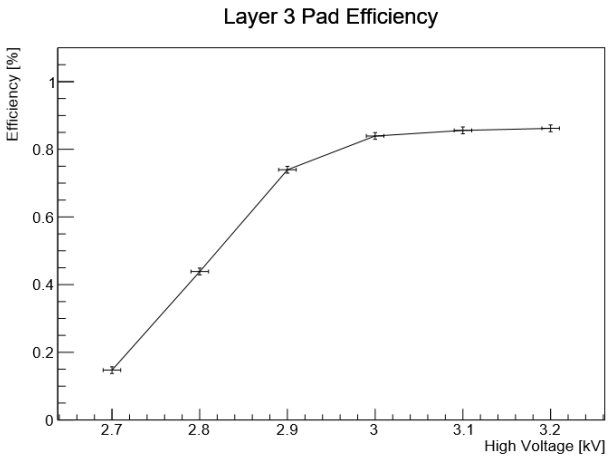


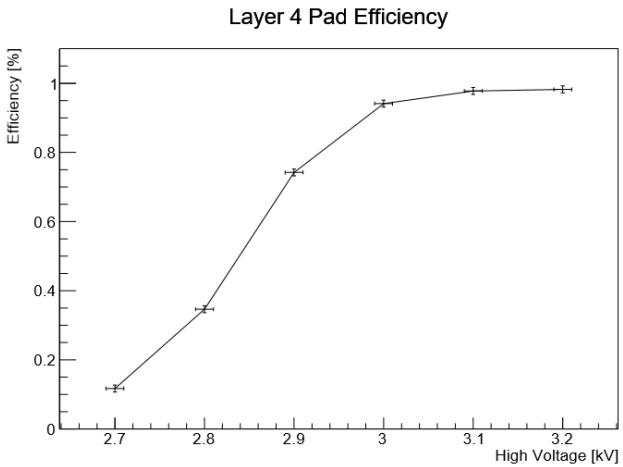
5th Oct.: Full setup (view from top)



sTGC Pad Efficiency







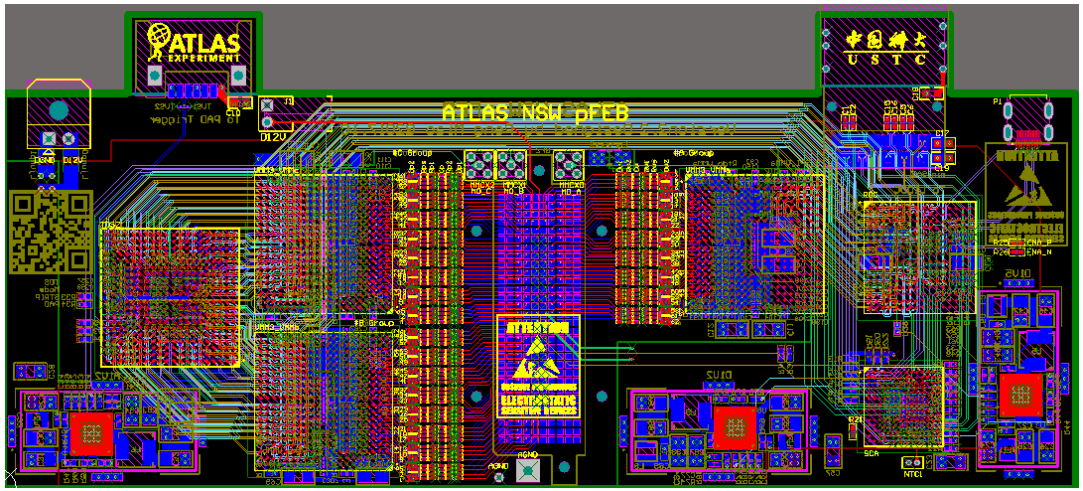
- 3 layers of sTGC measured for Pad efficiency
- Efficiency almost 100% when HV at 3kV

- NSW committee placed an order for 38 p/sFEB v2.1 for chamber production sites and CERN wedge test.
- Cost estimation for FEB
  - pFEB v2.1: 1945 CHF/board
  - sFEB v2.1: 2505 CHF/board
- Overall cost: 169,100 CHF
- Can cover the cost of FEAST/SCA ASICs and MiniSAS/POWER connectors we shall pay.

FEB versions

Version	Descriptions	Tests
v1.2 (2016.06)	VMM2; FPGA to configure/read VMM2 via Ethernet	Site review; TGC test @ SDU
v2.0 (2017.01)	VMM3 + TDS + 1FEAST; FPGA to configure/read VMM3; Separate SCA test board	VS2017.03
v2.1 (2017.06)	VMM3 + TDS + FEAST + SCA; ROC-like FPGA; miniSAS, no ethernet	VS2017.07; SDU & WZ
v2.2 (2017.12)	All-chip prototype	VS2018.01

p/sFEB v2.2



FEAST: POWER ASIC

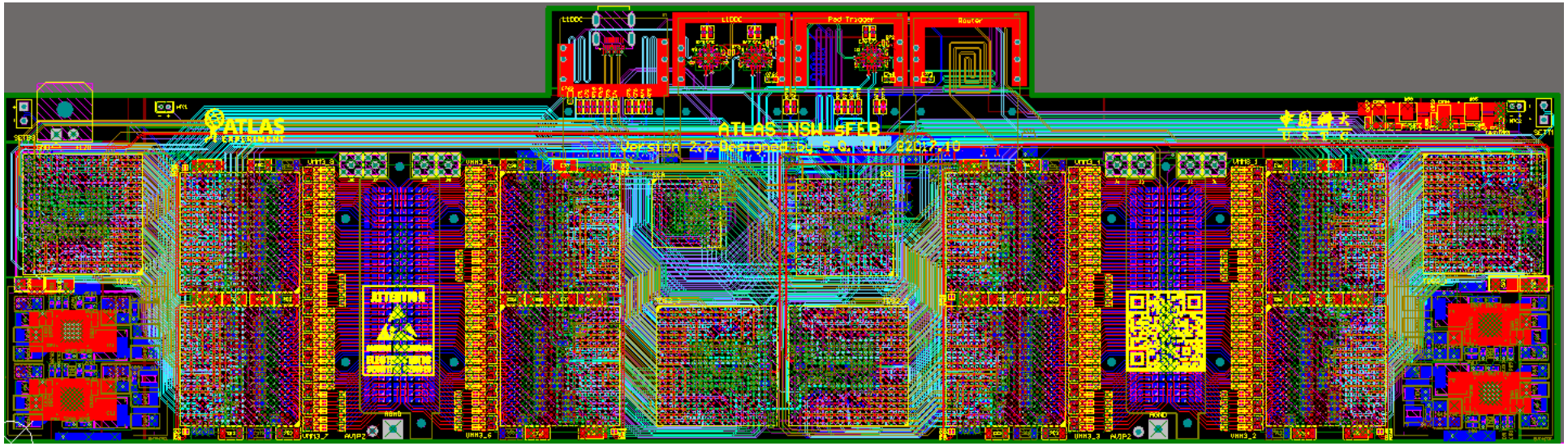
VMM3: Front-end ASIC

TDS2: Trigger Data Serializer

GBT-SCA: Giga Bit Transceiver-Slow Control Adapter ASIC

ROC: Read Out Controller for raw data

Layout completed on November 2017. Have been sent out for production and soldering.



Summary

p/sFEB v2.1:

- All ASICs on FEB can be configured by the full chain.
- The pFEB/sFEB noise level has been measured w/o and w/ full size sTGC detector. The intrinsic electronic noise RMS is ~ 0.5mV, and is less than 2.5mV when connected with powered sTGC.
- Clean analog signals of cosmic have been seen, and digital readout of VMM3 have been tested at chamber sites.
- No dead channel observed at chamber sites.

NEXT:

- Latest p/sFEB v2.2 will join the 5th VS in January 2018.
- ASIC chips for engineering and pre-production run will arrive in May 2018. The production of p/sFEB boards will start April 2018.
- Final production run will start in October 2018.
- Test and commissioning in 2018/2019.

THANKS !